

[54] SCALE CONVERSION APPARATUS

[72] Inventors: Alexander Turnbull Shepherd, Craigleith Crescent; Laurence Philip Smith, Penicuik; Lockhart Taylor, Hailes Gardens, all of Scotland

[73] Assignee: Ferranti, Limited, Hollinwood, Lancashire, England

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[58] Field of Search 235/92, 156; 328/43, 44, 34

[56]

References Cited

UNITED STATES PATENTS

2,566,085	8/1951	Green	235/156
3,404,343	10/1968	Strand	235/92 PL
3,209,130	9/1965	Schmidt	235/92 PL
3,549,870	12/1970	Lay	235/92 PL

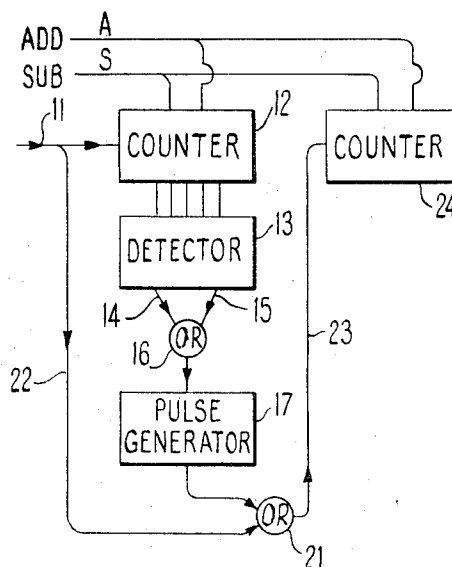
Primary Examiner—Maynard R. Wilbur
Assistant Examiner—Joseph M. Thesz, Jr.
Attorney—Cameron, Kerkam & Sutton

[57]

ABSTRACT

A linear scale converter for converting an input train of electrical pulses each of which represents a required elemental movement (e.g., of a machine tool) of fixed length expressed in a particular scale, such as the Imperial scale, to an output train of pulses each of which represents such movement but expressed in another scale, such as the Metric scale, where the output/input scale ratio is D/N, includes apparatus for defining each input group of N pulses and adding algebraically to it (D-N) pulses at locations spaced approximately evenly over the group, thereby providing an output group of D pulses.

5 Claims, 18 Drawing Figures



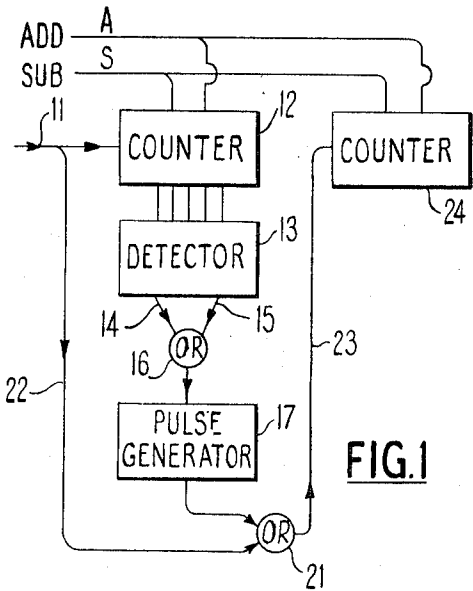


FIG. 1

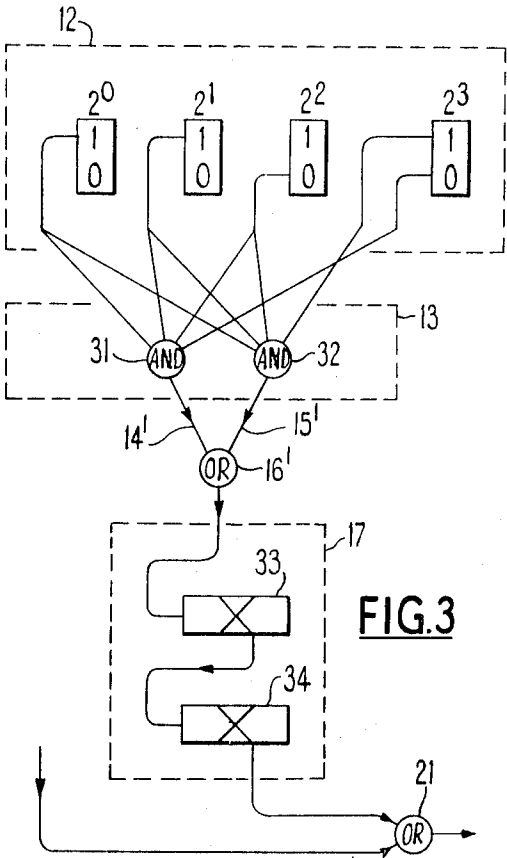


FIG. 3

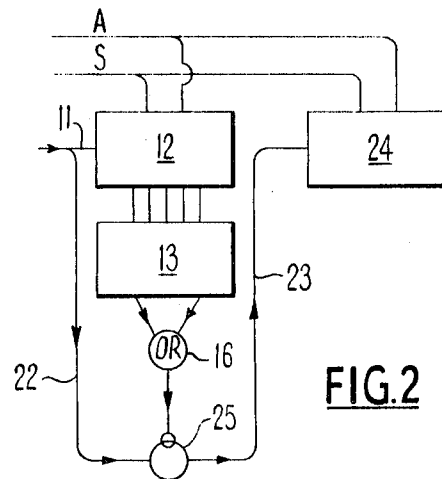


FIG. 2

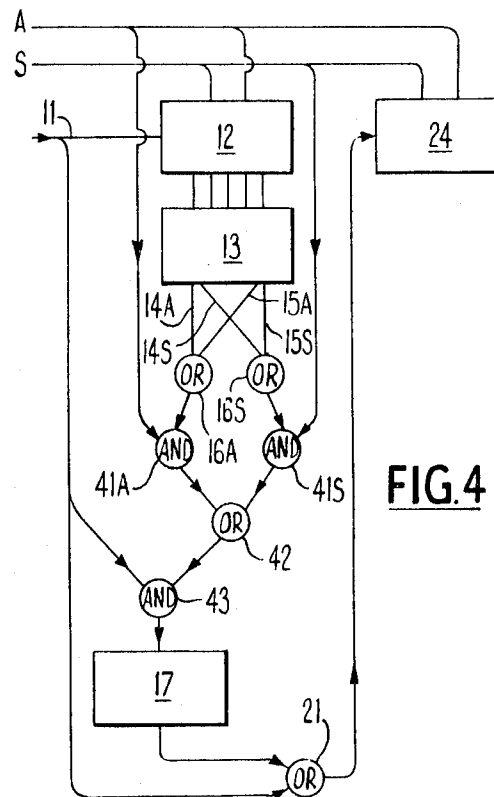


FIG. 4

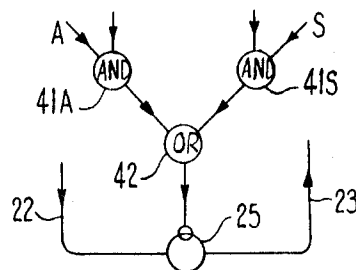


FIG. 5

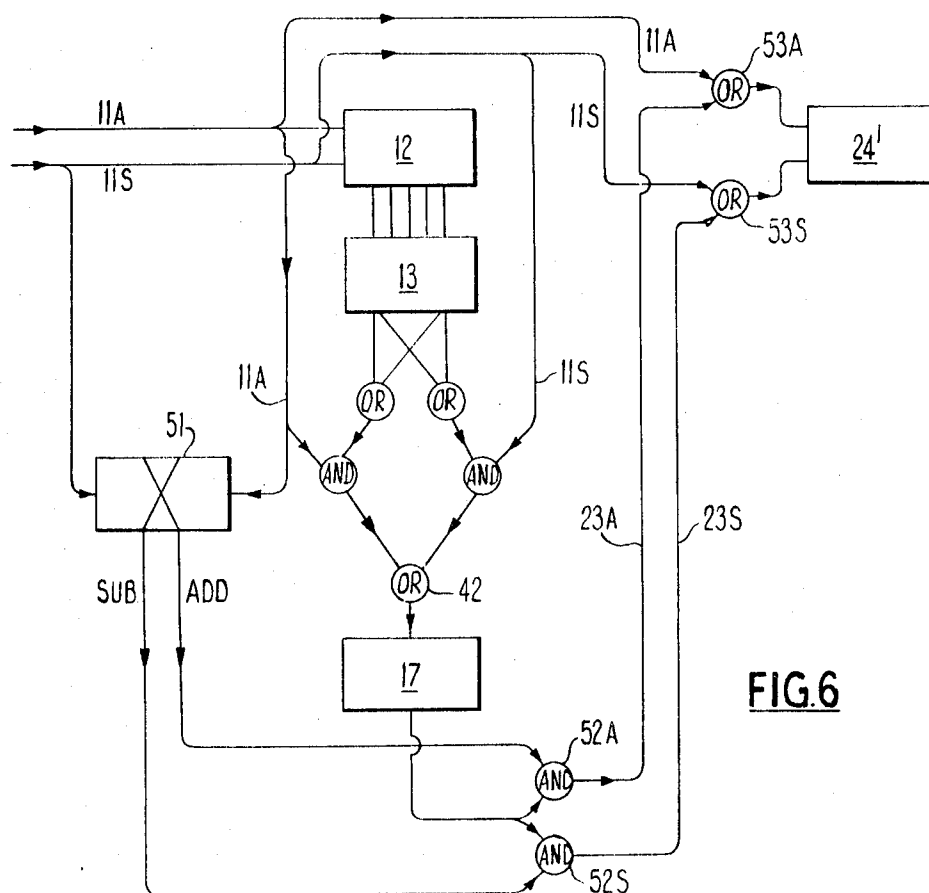


FIG. 6

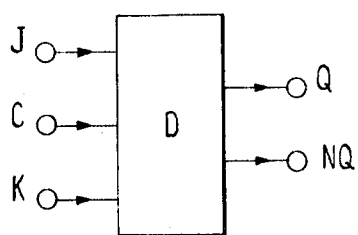
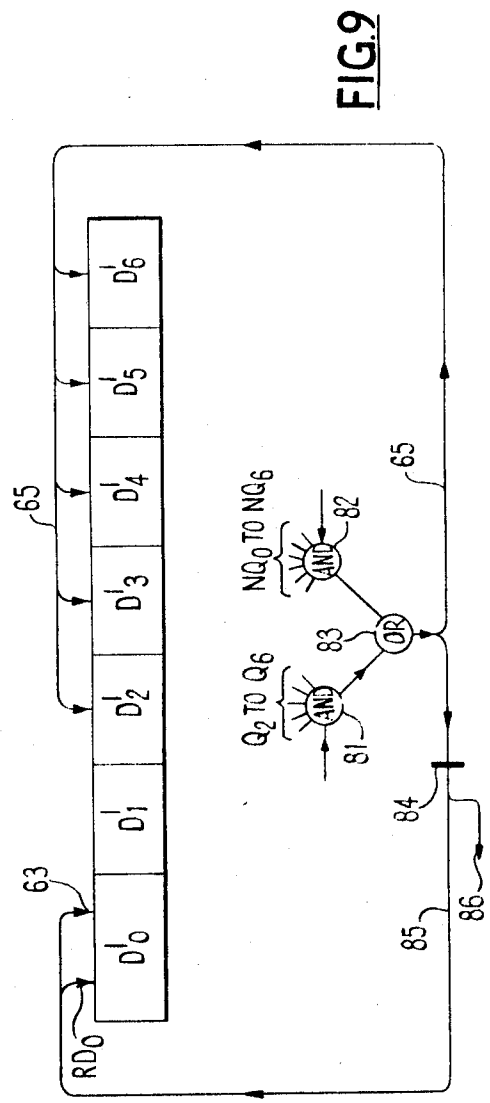
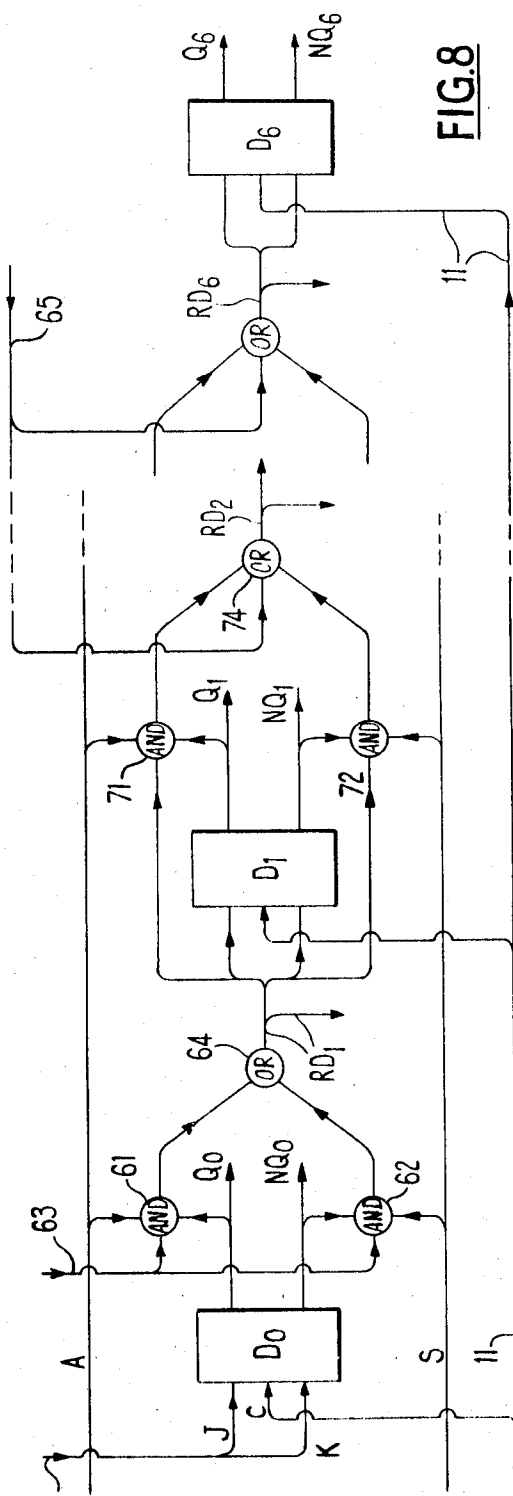


FIG. 7



Inventor

By

Attorney

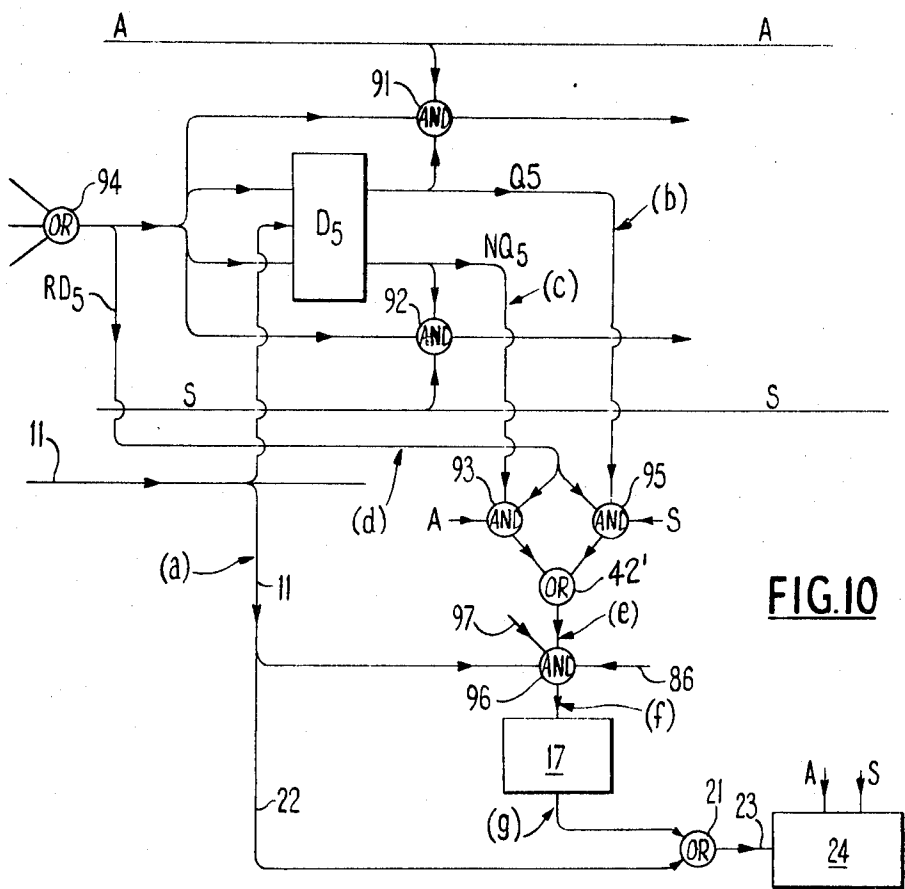


FIG. 10

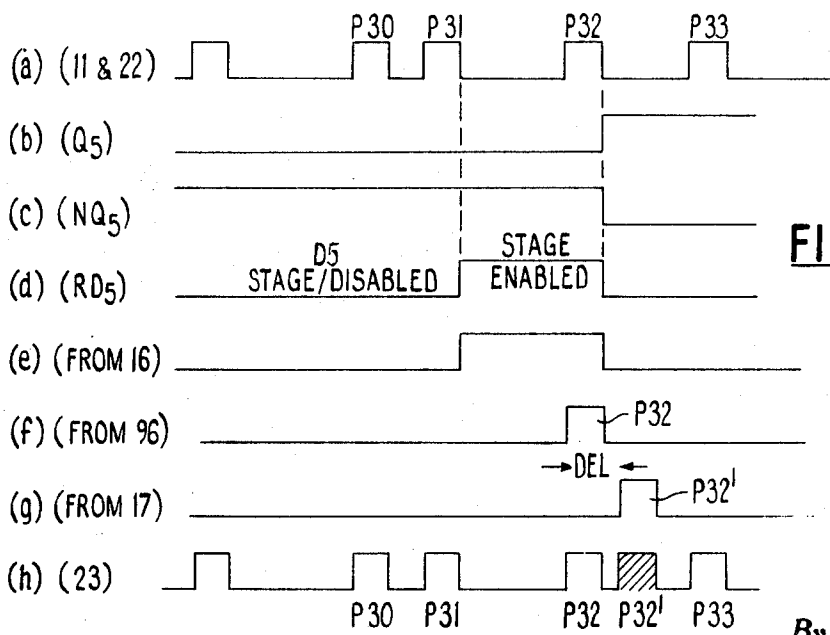
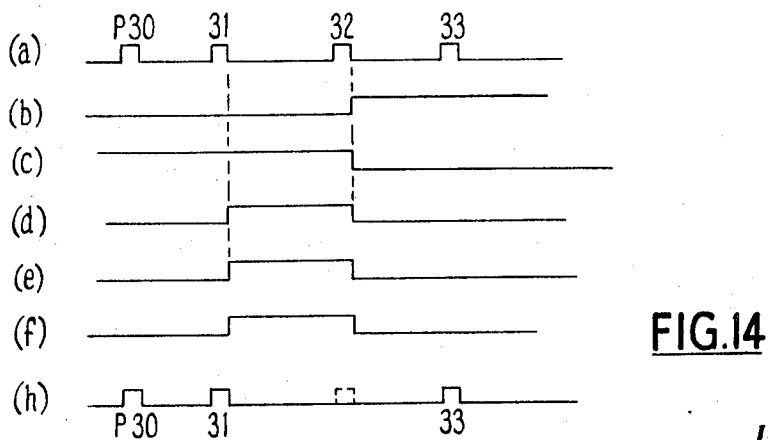
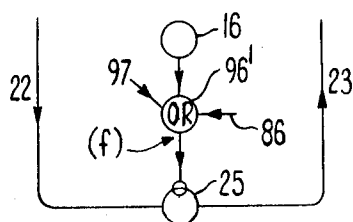
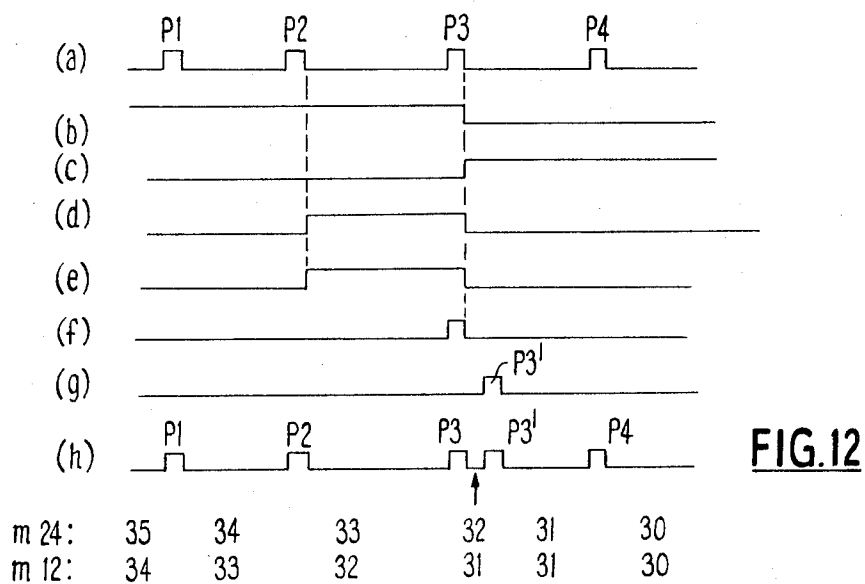


FIG. 11

Inventor

By

Attorney



Inventor

By

Attorney

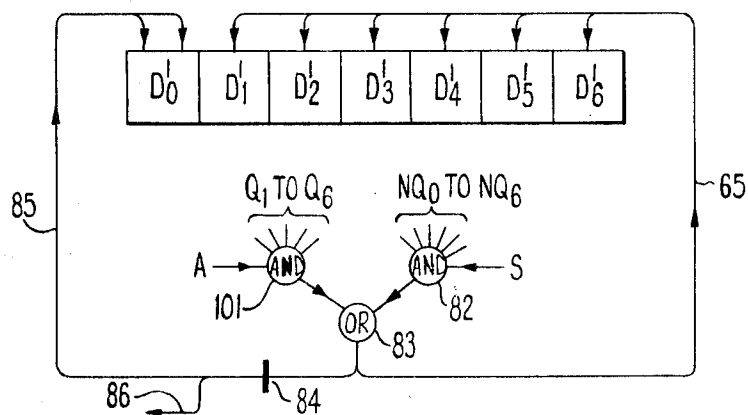
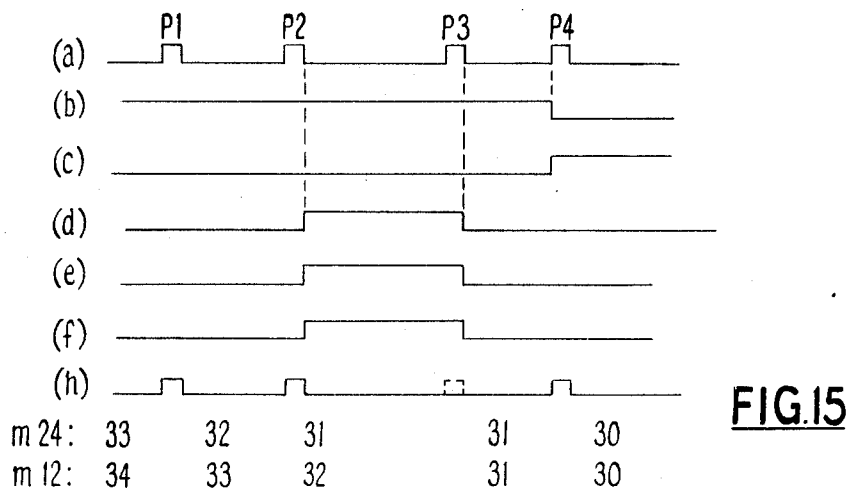


FIG.16

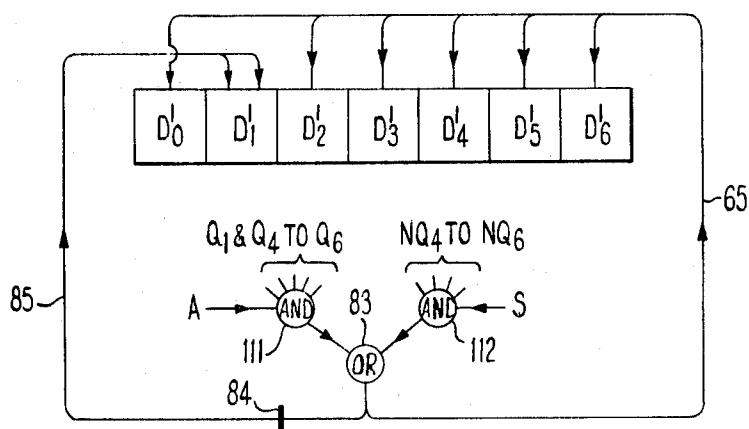


FIG.17

Inventor

By

Attorney

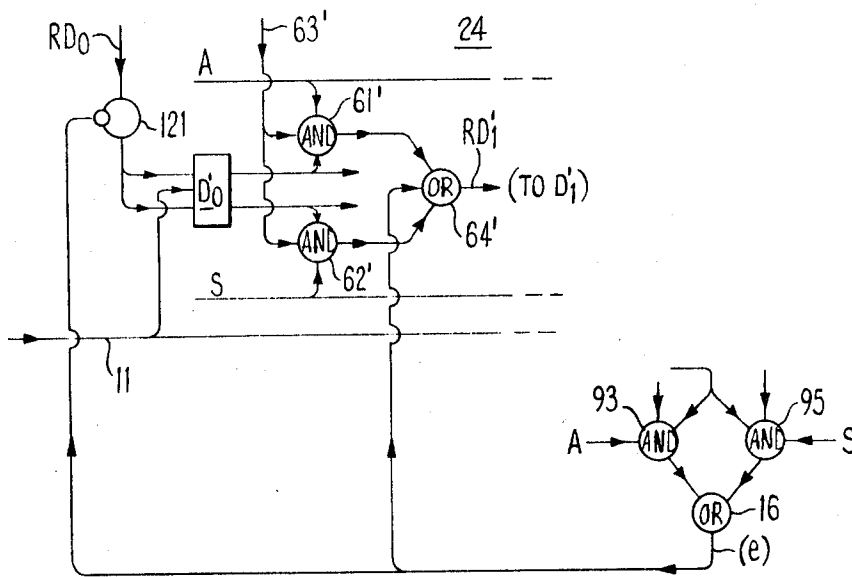


FIG. 18

Inventor

By

Attorney

SCALE CONVERSION APPARATUS

This invention relates to scale conversion apparatus for converting an input series sequence of electrical pulses of either sign significance, representing equal incremental quantities expressed in a particular measurement scale, to an output series sequence of pulses expressed in another scale.

The invention has especial application where the scales are the imperial and metric linear scales. The invention will accordingly be described in that connection; it should however be understood that the invention is not confined to that particular use but is applicable where the quantity concerned is other than a linear measurement and where the scales compared are other than the imperial and the metric.

An object of the invention is to provide scale conversion apparatus for the purpose stated.

In accordance with the present invention, scale conversion apparatus for the purpose stated where the output/input scale ratio is D/N includes conversion means for effectively adding algebraically to each group of input pulses totaling N algebraically $(D-N)$ single pulses of sense dependence on the sign of $(D-N)$ at locations spaced from one another within the group and from the nearest corresponding single pulses of the immediately adjacent group(s) at intervals of approximately $N/(D-N)$ pulses of the input sequence, the sign of $(D-N)$ being here ignored, thereby deriving as said output sequence and output group totaling D pulses algebraically for each of said input groups. When reference is made to $(D-N)$, it should be apparent that the expression means D minus N and not D to N or D through N .

The expression "effectively" adding algebraically should be understood to include not only the case where $(D-N)$ is negative and the said single pulses are inserted negatively in the input group but also the case where $(D-N)$ is negative and no pulses of either sense are actually inserted in the group but instead the corresponding number of pulses are eliminated from the input group, and the case where $(D-N)$ is positive and instead of each of said single pulses being inserted in the input group, a pulse of the input group is given the weight or effect of two pulses.

Where the invention is employed for conversion either way between the imperial and metric linear scales, use is made of the fact that one inch equals 2.54 centimeters exactly. Such a ratio cannot readily be used where the measurement to be converted is in the form of a series sequence of electrical pulses each of which represents a distance or movement (of, say, a machine tool or measuring probe) of fixed value, since fractions of pulses are impracticable units. But a more convenient ratio occurs where each input pulse represents 0.001 inches and each output pulse is to represent 25 microns; for as 0.001 inches is equal to 25.4 microns, the conversion ratio becomes 25.4/25, or 127/125. This ratio is a particular example of the ratio D/N above referred to.

Imperial/metric (I/M) conversion can thus be achieved by replacing each group of 125 imperial pulses by 127 metric pulses. As the term $(D-N)$ is positive, being equal to +2, the conversion merely necessitates the addition of two pulses to each input group.

For M/I conversion, on the other hand, $(D-N)=-2$, with the pulses now of negative sense; here the algebraic addition to each input group means the subtraction of two pulses from it.

In order to make the conversion as smooth as practicable the two pulses are added, or subtracted, singly, at locations which in the output pulse sequence are as evenly spaced with respect to one another as the numerical values allow.

Thus in I/M conversion the two pulses are spaced apart at $125/(127-125)$, or about 62, pulses of the input sequence. Convenient locations are after 31 and 93 pulses of each group. This gives spacing of alternately 62 and 63 pulses along the output train of contiguous groups.

Similarly for M/I conversion. Here the approximate spacings are $127/(125-127)$, or about 63 pulses, ignoring the negative sign of the denominator. Thus the spacings are about

the same as before, with the difference that each single pulse is subtracted from the input sequence rather than added to it.

Other conversion ratios, some of which are referred to later, may also be used.

Thus, very broadly, the conversion means according to the invention for I/M conversion in the ratio 127/125 includes: (a) some sort of a counter, conveniently of the ring kind, to count each input pulse and identify each group of 125; (b) a detector stage so connected to the various digit stages of the counter as to identify—that is, to respond by generating a control signal—each location in the input group where a pulse is to be added; and (c) operative means arranged to be controlled by the control signals to perform the effective algebraic addition of the single pulses to each input group at the locations defined by the detector stage. In the present instance the operative means includes a pulse generator which in response to each signal generates a single pulse and somehow adds it to the input group of pulses without causing pulse loss by overlapping. To ensure that such loss is prevented, a delay stage may be necessary to retain the single pulse until a space between the input pulses is available for it.

Similar arrangements are made for M/I conversion, except that as the "added" pulses are now of negative sense the generator of the operative means is replaced by an inhibit or other form of logical gate between the input and the output channels; when operated by the control signal effects the algebraic addition by causing a pulse of the input sequence to be eliminated at each appropriate location.

The pulses of the input sequence are not required to be regularly spaced in time. This is particularly so with machine tool applications, where each sequence controls the backward and forward movement of a tool or workpiece in one of two or three orthogonal directions.

Embodiments of the invention will now be described by way of example in more detail, with reference to the accompanying drawings in which

FIG. 1 is a schematic diagram of an embodiment of the invention arranged for I/M conversion,

FIG. 2 is a similar diagram to FIG. 1 but in respect of M/I conversion,

FIG. 3 shows suitable circuit details for stages shown generally in FIG. 1,

FIG. 4 is a schematic diagram of a modified form of the arrangement of FIG. 1,

FIG. 5 shows the arrangement of FIG. 4 modified for M/I conversion, and

FIG. 6 shows the arrangement of FIG. 4 modified for a different kind of counter,

FIG. 7 shows in block form part of a stage of a further kind of counter,

FIG. 8 is a schematic diagram of a part of a counter made up of stages as shown in FIG. 7,

FIG. 9 is a schematic diagram of a further part of the counter of FIG. 8,

FIG. 10 is a schematic diagram of an embodiment of the invention for conversion in the I/M direction which makes use of the counter of FIGS. 7 to 9,

FIGS. 11 and 12 show waveforms to illustrate the operation of the embodiment of FIG. 10,

FIG. 13 shows part of the embodiment of FIG. 10 but modified for conversion in the M/I direction,

FIGS. 14 and 15 show waveforms to illustrate the operation of the embodiment of FIG. 13,

FIGS. 16 and 17 show modifications of the apparatus of FIG. 9 to suit other conversion ratios,

and FIG. 18 shows in block form a further embodiment.

The invention will first be described by way of example with reference to FIG. 1 as used for converting in the I/M direction.

The input pulses arrive over a channel 11 and are applied to pulse-counting means in the form of a bidirectional binary ring counter 12 of 125-pulse capacity. The counter is of the kind which has a single input and is conditioned to add or subtract by the biases applied to Add and Subtract leads A and S common to all stages.

Associated with the counter is a detector stage 13 arranged to identify the respective pulse locations by detecting the pulse contents of the counter which precede those locations, and in response supply a control signal over a lead 14 when the counter holds 31 pulses and over a lead 15 when the counter holds 93 pulses. A diode decoding network of a conventional kind connected to each digit stage of the counter may serve for this purpose.

Leads 14 and 15 provide the inputs for an OR-gate 16 the output from which is applied to a combined delay stage and amplifier 17.

Each pulse generated by stage 17 after the delay built into it is applied as one input to an OR-gate 21 having as another input the input signals, delivered from channel 11 by a lead 22. The output lead 23 from gate 21 may be considered the output channel of the apparatus. In this embodiment it is applied as input to a bidirectional counter 24, which is similar to counter 12 (and like it controlled over leads A and S) but of considerably greater capacity.

In operation, the input pulses, each of which represents a tool movement of 1/125th, or 0.001, inches in one or other direction according to the sign represented by the pulse, as prescribed by the bias on leads A and S, arrive in an irregularly spaced manner over the input channel 11. In response, counter 12 adds them algebraically, according to the sign of each, identifying each group totaling 125 by cycling through its contents from 0 back to 0. At the same time the input pulses are applied by way of OR-gate 21 to counter 24, to be added or subtracted there according to the bias on leads A and S.

Each time the count reaches the total 31, appropriate to a pulse location, detector 13 responds by supplying a control signal by way of lead 14 and OR-gate 16 to stage 17, to generate a single pulse after a slight delay. This pulse is fed by way of OR-gate 21 and output channel 23 to the counter 24, the delay in stage 17 being such as to ensure that the pulse is interpolated between successive pulses of the original input pulse sequence without risk of pulse loss due to pulse overlap or coincidence. A single pulse is similarly interpolated each time the counter reaches the number 93.

Where a pulse has been added as described in the preceding paragraph—when the counter reaches the total 31, say—and the input pulses become negative, as prescribed by the bias on leads A and S, with the result that both counters begin to count down, the return of counter 12 to the total 31 again results in the generation and interpolation of a single pulse, but as it is of opposite sign to the single pulse interpolated during the upward count, this further single pulse has the desired effect of cancelling out the earlier one.

Thus each successive input group has its algebraic total of 125 pulses delivered over the output channel with two pulses interpolated to bring the total to 127. The required conversion has thus been carried out.

FIG. 2 shows the modification required for conversion in the M/I direction—that is, where each input group of 127 pulses has to be converted to 125. As the two single pulses have now to be subtracted instead of added, stage 17 is dispensed with, and OR-gate 21 replaced by an Inhibit gate 25 arranged to be so controlled by the control signal from stage 13 as to block a pulse of the input group each time the counter reaches the totals 31 and 92.

Both the above-described arrangements may be modified to suit the kind of counter which in place of the Add and Subtract controls of counters 12 and 24 is provided with Add and Subtract input rails, the sign of each input pulse being indicated by the rail it arrives on. Where the conversion requires pulses to be added, as in the arrangement of FIG. 1, it is necessary to generate each of such supplementary pulses so as to have the sign of the input pulse (32 or 93, in the particular example quoted) which caused its generation. As described below with reference to the corresponding arrangement of FIG. 6, this is conveniently arranged by causing each input pulse to control the setting of a bistable stage to a state representing the sign of that pulse, and applying the output

from the stage to cause the supplementary pulse (if any) to be directed to the appropriate rail of the output counter.

Where the conversion requires pulses to be subtracted, the control signal is applied in parallel to two inhibit gates, one in each of the channels between the input channel and the A and S rails of the output counter.

FIG. 3 shows a suitable decoder circuit for detector stage 13 in the arrangement of FIG. 1. For convenience of illustration it is assumed that the counter is a four-stage binary counter and that the pulse-location numbers to be detected are 3 and 11.

The stage includes two four-entry AND-gates 31 and 32. Gate 31 is designed to detect the number 3, or binary 1100 (most significant digit on the right); hence its four inputs are from the digit 0 outputs from stages 2² and 2³ and the digit 1 outputs from stages 2⁰ and 2¹. Thus the gate passes a signal when the counter holds 3 pulses.

Similarly gate 32, to detect binary 1101, has one input from the digit 0 output of stage 2² and the remaining inputs from the digit 1 outputs of the other stages. The outputs from these gates are respectively applied over leads 14¹ and 15¹ to an OR-gate 16¹—the equivalent of leads 14 and 15 and gate 16 of FIG. 1.

A similar form of detector may also be used in the arrangement of FIG. 2.

FIG. 3 also shows suitable apparatus for stage 17 of FIG. 1. This includes two cascaded monostable stages 33 and 34. Stage 33 is arranged to be triggered ("set") by the control signal from detector 13 and itself to trigger stage 34 on resetting. The output from stage 34 is applied to OR-gate 21. Thus the two monostable stages define by the durations of their respective unstable states the extent of the delay period (between the initiation of the control signal and the initiation of a pulse to be added to the train) and the width of the added pulse.

Some delay will necessarily occur between the initiation of a control signal and its effect in adding or subtracting a pulse. If during this delay period the sense of the input pulses should reverse, a pulse may be wrongly added or wrongly subtracted. For example, if the control signal is initiated to delete a pulse during a forward count, and the input train reverses during the delay period, the control signal will only become effective after reversal, and by subtracting a pulse from the then negative train will make the deletion have the incorrect effect of an addition.

One way to prevent such misoperation is to arrange for stage 13 to detect two adjacent numbers—for example, 32 and 33, 93 and 94—and employ a simple gating network responsive to the sign of the input pulses and to the input pulses themselves to ensure that the control signal is generated at each lower number—32 and 93—on an upward count but at each higher number—94 and 33—on a downward count and to delay the control signal and hence the effective addition of a pulse until the arrival of the next input pulse.

This may be arranged as in FIG. 4, which shows the circuit of FIG. 1 suitably modified.

To simplify the explanation of this embodiment of the invention and those to be described later, the convention will be adopted of referring to leads and output points as energized when representing digit 1 and unenergized or at zero output when representing digit 0; whereas in practice the reverse may be the case, or the energization may be uninterrupted and the respective digits represented by different extents or senses of energization.

Similarly as regards the Add/Subtract bias leads: only the lead A is energized when addition is required, and only the lead S for subtraction.

An And gate will be referred to as "open" when all its inputs are energized, "closed" if at least one input is not, and "alerted" if all its inputs except one are energized.

OR-gate 16 of FIG. 1 is now in two parts 16A and 16S. Gate 16A receives as inputs from detector 13 control signals over leads 14A and 15A which are energized when counter 12 holds the numbers 32 and 93. The output from this gate is ap-

plied as one of the inputs to a two-entry AND-gate 41A. The other input to gate 41A is derived from the Add bias lead A, and its output is applied to an OR-gate 42.

Gate 16S similarly combines the control signals on leads 14S and 15S, responsive when the counter holds the numbers 33 and 94, and applies them to OR-gate 42 by way of an AND-gate 41S, controlled from bias lead S.

The output from OR-gate 42 is applied as one input to an AND-gate 43 having as a second input a connection from the input lead 11. The output from gate 42 is applied to the combined delay and pulse generator stage 17.

In operation, when the number 32 is reached on an upward count, the resulting control signal generated by detector 13 finds gate 41A already alerted by the Add bias on lead A. But as the initiating pulse (the 32nd) has now ceased, the control signal is blocked at the next AND-gate 43 until the next pulse (the 33rd) arrives.

If therefore the direction of count should reverse between those input pulses, no harm would be done, for the reverse of the bias on leads A and S would close gate 41A before the control signal could become effective, with the result that the next input pulse is blocked at gate 43.

If on the other hand reversal should take place after the 33rd pulse had arrived, the control signal initiated by the preceding pulse would have been effective in adding a pulse. But the reversal would allow the control signal in respect of the 33rd pulse to become effective too, by way of gate 41S, and being of the opposite sense to the one just added, would cause it to be cancelled. In other words, the pulse added at the forward count would be eliminated by subtraction at the reverse count.

Where conversion is in the M/I direction, where pulses are to be subtracted rather than added, the arrangement of FIG. 4 may be as shown in FIG. 5. The output from gate 42 is applied direct to the control point of inhibit gate 25 of FIG. 2. As no pulses are to be added, a gate corresponding to gate 43 of FIG. 4 to allow the next input pulse to release the control signal, is unnecessary.

Where the counter is of the kind having only two inputs for pulses to be added or subtracted respectively, the arrangement of FIG. 4 may be modified as shown in FIG. 6.

As there are now no bias lines to determine in advance the sign of the input pulses and hence the sign of the added pulses, each input pulse arriving over the Add line 11A or the Subtract line 11S is applied to control the setting of a bistable stage 51. In one of its states—the "Set" state, say—stage 51 represents Add, and in its reset state Subtract. The stage thus statifies the sign of the last input pulse.

The output from OR-gate 42 (FIG. 4) is applied to stage 17 direct. In this arrangement gate 43 of FIG. 4 is not needed, for the input pulses now arrive over leads 11A or 11S at gates 41A or 41S. The output from stage 17 is applied as one of the inputs to each of two-entry AND-gates 52A and 52S, to the other entries of which are applied those outputs from stage 51 that are energized to represent its Add (Set) and subtract (Reset) states. The outputs from gates 52A and 52S are applied to the Add and Subtract rails of the output counter 24¹ by way of OR-gates 53A and 53S having leads 11A and 11S as the other inputs.

Little description of the operation is necessary. At the end of each input pulse, stage 51 remains representing the sign of that pulse and hence the sign of the pulse to be added, if any. By alerting the appropriate one of gates 52A and 52S, the output from stage 51 causes the additional pulse to be directed to the appropriate rail of the output counter 24¹.

A decoder 12 of the type described with reference to FIG. 3, requiring as it does two output leads from each digit stage of the counter, may be undesirably complex where the counter has more than a few digit stages—e.g., where for a count of 125 seven digit stages are needed. A somewhat neater and simpler decoder may be designed in reliance on the known property of binary counters that in an upward count only one stage changes from 0 to 1 at each input pulse though several

stages may simultaneously change from 1 to 0, and only one stage changes from 1 to 0 on a downward count.

Further, in the *m*th stage of an *n*-stage binary counter the number of such changes during a cycle of the counter is 2^{n-m} and in each stage the change points from 0 to 1 or 1 to 0 are uniformly distributed over the cycle. It is thus possible to select, for the purpose of identifying locations in the pulse sequence for adding or subtracting pulses as described above, any number of change points in the cycle by detecting the changes from 0 to 1 during addition, or 1 to 0 during subtraction, in any one stage or combination of stages.

Taking the numerical example already used, the 32nd (i.e., 2⁵th) pulse may be detected by detecting the change from 0 to 1 in the sixth digital stage; this may be done by differentiating the output from that stage and selecting the positive-going spike of the two which result.

The 93rd pulse is less easy to detect; but by choosing instead the 96th (i.e., 2^7+2^6), identification may be obtained from the sixth and seventh stages by AND-gating the positive pulse from the leading edge of the sixth stage output with output from the seventh stage.

A further simplification results if the binary counter 12 used is of the synchronous type in which each signal pulse is applied to all the digit stages simultaneously and only those respond by changing state which are "enabled" (that is, alerted or primed) by signals derived from the states of earlier stages before the pulse arrived.

Such a counter may be of the kind which uses for each digit stage the particular form of bistable stage known as a JK flip-flop.

Such a digit stage D (FIG. 7) includes control input points J and K, a "clock" input point C, and two output points Q and NQ ("not Q"). For the purpose of the invention the J and K are commoned, the control signal is applied to both, and the circuit has the following properties:

a. The two stable states are: (i) Q energized but NQ unenergized, the stage as a whole holding digit 1; (ii) the reverse of state (i), the stage now holding digit 0. These will be referred to as the Set and Reset states respectively.

b. When the control signal is 0, the common input JK is unenergized; any input "clock" pulse arriving at point C is ineffective, leaving the outputs in the Set or Reset state they happened to be in when the pulse arrived. The stage may be said to be "disabled"—that is, unresponsive to an input pulse at point C—by the control signal at JK.

c. When the control signal is 1, the common input JK is energized; an input pulse arriving at C causes the stage to reverse its state. The control signal is thus maintaining the stage "enabled"—ready to respond to the next input pulse.

Digit stages D₀, D₁, and D₆ of a counter made up of seven such JK stages are shown in FIG. 8.

The JK flip-flop D₀ for the units stage has the common input points J and K supplied over a control lead RD₀. A connection is made to the C input point from the pulse input lead 11, which is common to all seven stages. The output is supplied over leads Q₀ and NQ₀.

Lead Q₀ is connected as one input to a three-entry AND-gate 61 the other entries to which are supplied by the Add bias line A and a lead 63.

Similarly lead NQ₀ is connected as an input to an AND-gate 62 having further inputs from Subtract lead S and lead 63.

The outputs from gates 61 and 62 are applied as inputs to an OR-gate 64.

The output from gate 64 is applied over a control lead RD₁ as the combined JK control input to stage D₁. Except for deriving its control JK input from stage D₀ and the third inputs to its AND-gates 71 and 72 from lead RD₁, instead of from lead 63, stage D₁ is similar to stage D₀, and supplies a control signal to stage D₂ by way of gates 71 and 72, an OR-gate 74, and lead RD₂.

Stages D₂ to D₅ (not shown) are exactly similar to stage D₁, except that each OR-gate corresponding to gate 64 has a third entry from a lead 65. Stage D₆ is also similar, except that, as it

is the last stage, two AND gates corresponding to gates 71 and 72 of stage D_1 are not required. Each of these remaining stages includes an input from lead 65 to an OR gate corresponding to gates 64 and 74.

The operation will now be described for the particular case of an upward count from zero to 125, or binary 1011111 (Note: the binary numbers quoted in this specification have the least significant digit on the left.).

Until that total is reached, as described below with reference to FIG. 9, leads RD_0 and 63 are steadily energized, whereas lead 65 is unenergized. This energization of lead RD_0 holds stage D_0 in its enabled condition throughout the count.

In the quiescent stage of the counter, holding the number zero, each stage is in its Reset stage. As already mentioned, stage D_0 is enabled. On the other hand stage D_1 is disabled because (a) gate 61 is closed since lead Q_0 is unenergized; and (b) gate 62 is closed because bias lead S is unenergized. Thus neither of the inputs to gate 64 nor its output lead RD_1 is energized. As at this stage lead 65 is also unenergized, all the higher stages are similarly disabled, each holding digit 0.

The first pulse to arrive is applied by lead 11 to the C inputs of all seven stages but finds only stage D_0 enabled. The pulse therefore reverses the stage, leaving it still enabled but in its Set stage and so energizing lead Q_0 rather than NQ_0 . With gate 61 thereby opened, stage D_1 is enabled, though as yet remaining in its Reset state, ready to respond to the next pulse. The remaining stages stay disabled.

The second pulse, finding stage D_0 still enabled, switches it back to its Reset state, closing gate 61. As stage D_1 is also enabled, the pulse, acting by way of the direct connection from lead 11, switches it to Set. In this condition stage D_1 is no longer enabled, because gate 61 is now closed. The overall condition is that stage D_0 is enabled (as always, until the end of the count) but is now in its Reset state holding digit 0; stage D_1 is disabled but Set, so holding digit 1 and energizing lead Q_1 , and all the other stages are disabled and Reset. Thus the count reads 0100000.

The third pulse merely switches D_0 to Set, reopening gate 61 and reenabling stage D_1 , leaving it still holding digit 1. With output lead Q_1 still energized by stage D_1 , a path is completed through the reopened gate 61 and gates 64, 71, and 74 to enable stage D_2 (not shown). Both stages D_0 and D_1 now hold digit 1, with the counter reading 1100000.

The fourth pulse finds each of stages D_0 to D_2 enabled and so reverses each of them, bringing D_0 and D_1 to Reset but D_2 to Set, and leaving only D_0 enabled: 0010000.

Suppose now that a pulse arrives to be subtracted—that is, with lead S energized rather than lead A. The effect of this reversal of the Add/Subtract bias is to enable both stages D_1 and D_2 : D_1 by way of gate 62 (now open, since leads NQ_0 and S are energized as well as lead 63) and 64, and D_2 by way of gates 62, 64, and 72. As all three stages are enabled before the pulse arrives, the effect of it is to reverse each of them, and so change the number held from 0010000 to 1100000. So long as the counter remains conditioned for subtraction, only stage D_0 is enabled, the higher stages being blocked by gates 61 and 62 because of the unenergized condition of leads A and NQ_0 respectively. The next pulse would then change the number to 0100000. If the Add/Subtract bias should be changed to Add while the counter held the number 1100000 all three stages would be enabled, and the next pulse would be added as the fourth pulse was as described in the preceding paragraph.

It will therefore be seen that a stage is disabled on an upward count until each lower stage holds digit 1; and on a downward count until each holds digit 0.

The operation is similar in response to further pulses of either sign.

As the counter has to have an effective total of 125 pulses rather than its natural total of 127, arrangements have to be made to force its Reset to zero on receipt of the 125th pulse in an upward count, and to revert from 0 to 125 on receipt of the first pulse after zero has been reached on a downward count. This is the function of leads RD_0 , 63, and 65, and their sources

of energization, in the arrangement just described. They act by detecting the arrival of the 124th pulse on an upward count and in response to the next pulse switch to their Reset state all stages that are in their Set state when the pulse arrives. As 124 corresponds to the binary number 0011111, the task amounts to the resetting of each of stages D_2 to D_6 when the total 125 is reached. Similarly the task when zero is reached on a downward count is to switch those stages to their Set state when the next pulse arrives. Suitable apparatus for doing this is shown in FIG. 9.

Block D'_0 represents digit stage D_0 of FIG. 8 together with its output AND-gates 61 and 62. Block D'_1 represents stage D_1 , together with its input OR-gate 64 and output AND-gates 71 and 72. The remaining blocks are similar to block D'_1 except that block D'_6 has no output AND-gates.

A six-entry AND-gate 81 has one input from lead A (Add) and one each from output leads Q_2 to Q_6 . An eight-entry AND-gate 82 has one input from lead S (subtract) and one each from output leads NQ_0 to NQ_6 . The outputs from these gates are combined at an OR-gate 83. The output from gate 83 is connected to lead 65 and, by way of a negater stage 84 and lead 85, to leads RD_0 and 63. A further output from negater 84 is supplied over a lead 86 to apparatus which is described below with reference to FIG. 10.

In operation, when the counter holds zero with the Add bias line energized, gate 81 is closed because none of the output leads Q_2 to Q_6 is energized. Gate 82 is also closed, because although leads NQ_1 to NQ_6 are all energized, lead S is not. Thus the output from gate 83 is unenergized. This condition is reversed by negater 85 to supply an energizing signal over lead 85 to the control lead RD_0 and to lead 63, to maintain stage D_0 enabled and gate 61 alerted throughout the count as above described.

During a subsequent upward count, gate 82 remains closed. Gate 81 also remains closed—until the total 124 is represented by the energization of each of leads Q_2 to Q_6 . The resulting output from gate 83, reversed by stage 84, removes the signal from each of leads RD_0 and 63. On the other hand the energization of lead 65, acting by way of OR-gate 74 and the corresponding gates of the higher stages, switches each of stages D_2 to D_6 from digit 1 to digit 0 - i.e., to its Reset state. All stages now hold zero.

The operation is similar when zero is reached on a downward count; this time it is gate 81 that remains closed, and gate 82 opens when each of stages NQ_0 to NQ_6 holds zero. Lead 65 is also energized as before, but this time the switching action which it exerts on stage D_2 to D_6 is to reverse them from digit 0 to digit 1, leaving stages D_0 and D_1 holding zero. Thus the counter holds the binary number 0011111 or decimal 124.

The modification necessary to the circuit of FIG. 1 where the counter 12 is of the JK kind described above with reference to FIGS. 7 to 9 is shown in FIG. 10, using the same reference numerals for components corresponding to those of FIG. 1 and assuming again that conversion is in the direction I/M with 125 pulses in each input group.

As the pulses that are to be detected are the 32nd and 96th of each group, the digit stage which the detector has to respond to is stage D_5 . The control signal for the stage is derived over a lead RD_5 , which here acts the part of detector 13, from an OR-gate 94 corresponding to gates 64 and 74 of stages D_1 and D_2 , see FIG. 8. The outputs over leads Q_5 and NQ_5 assist in controlling output AND-gates 91 and 92 corresponding to gates 71 and 72 of stage D_1 .

Corresponding to gates 41A and 41S of FIG. 4 are two three-entry AND-gates 93 and 95. Gate 93 has inputs from leads A, NQ_5 , and RD_5 , whereas gate 95 has inputs from leads S, Q_5 , and RD_5 . The outputs are combined at an OR-gate 42', corresponding to gate 42 of FIG. 4, and applied as one of the inputs to a four-entry AND-gate 96. The remaining inputs to the gate include a connection from lead 11, thereby rendering the gate the equivalent of gate 43 of FIG. 4, lead 86 (FIG. 9) and a lead 97 the energization of which is manually controlled. The output from gate 96 is applied to pulse generator 17,

which may take the form described with reference to FIG. 3. The delayed pulse thereby derived is applied as one of the inputs to OR-gate 21 having the pulses on lead 22 (FIG. 1) as the other input and applying its output over channel 23 to counter 24, all as described with reference to FIG. 1.

The remaining six stages D_0 to D_4 and D_6 may be as described above with reference to FIG. 8, except that the Q and NQ outputs are only used to control the local AND-gates and the switching stages 81 and 82 of FIG. 9.

The operation of this equipment will be described with reference to the signal waveforms of FIG. 11. These show at (a) the input pulses arriving over leads 11 and 22 at random, with the 31st and 32nd pulses labeled P31 and P32. Waves (b), (c), and (d) represent the signals on leads Q_5 , NQ_5 , and RD_5 ; waves (e) and (f) show the outputs from gates 42' and 96 both waves representing the control signal; wave (g) shows the pulse generated by stage 17, and wave (h) shows the train of pulses delivered by gate 21 to the output channel 23.

It is assumed that the Add/Subtract bias leads A and S are in their Add condition—that is, with only lead A energized.

Before the arrival of pulse P31, stage D_5 is holding digit 0 and so is energizing its output lead NQ_5 rather than Q_5 —see waves (b) and (c). The stage is disabled by a zero signal on lead RD_5 —wave (d)—because one at least of the five lower stages is not holding digit 1. Thus gates 93 and 95 are both closed, the outputs from gate 42', gate 96, and pulse generator 17 are also zero—waves (e) to (g)—and the incoming pulses are passing uninterruptedly through gate 21 to channel 23 and counter 24—wave (h). As regards gate 96, the input to it over lead 86 is energized from OR-gate 83 and negater 84 in the absence of outputs from gates 81 and 82 as explained with reference to FIG. 9; lead 97 is also energized, under manual control; and signals are awaited from gate 42' and lead 11 before the gate can open.

With the arrival of the 31st pulse the number held by the counter as a whole is 1111100. Hence each of the five stages below stage D_5 holds digit 1. In consequence stage D_5 is enabled by the signal on lead RD_5 initiated in synchronism with trailing edge of pulse P31—wave (d), but as yet remains holding digit 0.

Each of the three entries to AND-gate 93 (including lead NQ_5) is thus energized and the gate transmits through gate 42' a control signal of waveform (e). This however is blocked by gate 96 which is closed in the absence of a signal on lead 11 since by this time the signal P31, which initiated by its trailing edge this control signal from gate 42', has itself ended. The stage is thus ready for pulse P32, with gate 96 fully alerted.

When that pulse arrives, to switch stage D_5 to digit 1, its leading edge completes the entries to gate 96 and so passes as waveform (f) to stage 17, which it triggers to generate a pulse P32'—wave (g)—after a delay DEL to follow pulse P32 in the output train—wave (h)—delivered over the output channel 23 to counter 24. This operation of stage 17 is exactly as described above with reference to FIG. 3. The delay is long enough to separate pulse P32' from pulse P32 without any overlap but short enough to ensure that pulse P32' is added in advance of the next pulse P33 at the least possible pulse spacing of the input pulse sequence.

It will be seen that the control signal derived from detector 13—that is, over lead RD_5 —is held up at gate 96 until the arrival of the next input pulse, just as in the arrangement of FIG. 4 the control signal is held up at gate 43, thereby similarly preventing misoperation due to a reversal of pulse sense.

A further result of pulse P32 is to Reset each of the five lower stages, the number being now 0000010. Stage D_5 is thus disabled by the return to zero of the signal on lead RD_5 —wave (d)—and remains with its output lead Q_5 energized to represent digit 1.

Stage D_5 remains in that condition until the 63rd pulse reenables it, ready to cause the 64th pulse to switch on the last stage D_6 . This time, however, no supplementary pulse is generated because the signal on lead RD_5 is unable to open either gate 93 (as lead NQ_5 is unenergized) or gate 95, since lead S is unenergized.

For the next 31 pulses stage D_5 remains disabled and holding digit 0 exactly as it did during the first 31. The 95th pulse reenables the stage exactly as did the 31st, and the 96th pulse results in the generation of a supplementary pulse exactly as did the 32nd.

Thus supplementary pulses are generated and inserted at intervals of $(96-32)=64$, and $(125-96+32)=61$ pulse intervals.

The effect of the signal on lead 86 is to close gate 96 during each of the special counter switching conditions represented by the opening of gate 81 or 82 in the circumstances described with reference to FIG. 9 and so prevent the accidental addition of a pulse during one of the forced resets of counter 12 above described.

The effect of the signal on lead 97 under manual control is to allow the gate to be closed continuously at will whenever it is desired to arrest the conversion and instead transmit the input pulse sequence to the output channel unmodified.

The operation of the circuit in counting down is as follows.

The waveforms of FIG. 11 are modified as shown in FIG. 12, with (h) the pulses proceeding to counter 24 for subtraction. It is assumed that some 34 pulses have previously arrived for addition, and been passed into counter 24, together with a supplementary pulse added after the 32nd pulse as above described. Thus counter 24 holds 35 pulses whereas counter 12 holds 34, or binary 0100010.

Lead S is now energized instead of lead A.

The next pulses to arrive are therefore for subtraction. They are labelled P1, P2, P3, etc., in FIG. 12 in the order of their arrival. At the foot of the diagram are inserted the numbers left in the respective counters after each pulse has been absorbed.

Pulse P1 drops the counters to 34 and 33; pulse P2 drops them to 33 and 32. With counter 12 thus holding binary 0000010, stage D_5 is enabled—wave (d)—holding digit 1, with lead Q_5 energized.

Reverting now to FIG. 10, the leads Q_5 and S are energized as well as lead RD_5 , causing gate 95 to pass a signal—wave (e)—through gate 16 to fully alert gate 96 in readiness for the next pulse P3. That pulse, which itself on arrival reduces the counts to 32 and 31, results in the generation of a supplementary pulse P3' which, being also for subtraction, reduces the number in counter 24 to 31 while counter 12 remains holding 31. The supplementary pulse added an upward count has thus been cancelled on the downward count, and further subtractive pulses step the counters downwards in numerical correspondence.

If the counting direction is changed from Add to Subtract after the 31st additive pulse P31 had arrived, and accordingly stage D_5 is enabled holding digit 0 and with gate 93 alerted, the deenergization of lead A causes gate 93 to close while gate 95 remains closed because of the zero signal on lead Q_5 . Thus the next pulse to arrive—the first for subtraction—finds gate 96 closed by the zero signals from both gates 93 and 95 and so does not result in the generation of a supplementary pulse.

There is no third condition of sign reversal, for the mere sign change between pulses P32 and P32', or P3 and P3', has no effect until the next pulse arrives; and, as already stated, the delay between a supplementary pulse and the preceding one is too short for a pulse to arrive during that delay interval.

FIG. 13 shows the alterations necessary for the circuit of FIG. 10 where the conversion is in the M/1 direction, so that pulses have to be subtracted rather than added. The changes closely correspond to those between FIG. 1 and FIG. 2. As gating by the input pulses is not required, gate 96 of FIG. 10 is now a three-entry gate 96', with only the inputs on leads 86 and 97 as well as that from gate 42'. The output is applied to control the inhibit gate 25 in the path between leads 22 and 23 as in FIG. 2.

For addition, the corresponding waveforms are shown in FIG. 14. Waves (a) to (e) are the same as in FIG. 11. Being free from control by the input pulses, gate 96' delivers a signal which is coterminous with the enabling signal RD_5 —wave (f). As these signals do not end until the end of pulse P32, the latter is eliminated by the inhibiting signal from gate 96' as shown in wave (h) where the deleted pulse is indicated in broken lines.

FIG. 15 shows the waveforms corresponding to those of FIG. 14 to illustrate the effect of a change from Add to Subtract after the input train had delivered 34 pulses. This time the deletion of a pulse has caused counter 24 to hold one less than counter 12—33 pulses as against 34. By the time pulses P1 and P2 have been absorbed, counter 12 holds 32 and is enabled by a signal on RD₅—wave (d)—with the result that gate 25 is closed in readiness to delete pulse P3. The result of thus deleting a *subtractive* pulse is to *add* a pulse and so counteract the pulse deletion made during the upward count. From pulse P3 downwards, therefore, the two counters are in numerical correspondence.

If reversal should come after the stage has been enabled by pulse 31, both AND-gates 93 and 95 are closed by the zero signals on leads A and Q₅ as in the arrangement of FIG. 10; in consequence the count turns down before a pulse has been subtracted.

The reversal operations are similar in the region of the 96th pulse.

Conversion in the M/I direction also requires some alterations to the arrangements of FIG. 9 so as to force the reset at 127 rather than 125. As shown in FIG. 16, the only material difference is that as the number to be detected during an upward count is binary 0111111, rather than 0011111, the six-entry AND-gate 81 of FIG. 9 is replaced by a seven-entry AND-gate 101 to which the extra input is lead Q₁. Gate 82, having again to detect a total zero, is as before. The only other change is that output lead 65 from OR-gate 83 is now extended to the input OR-gate 64 (FIG. 8) of stage D₁.

Other conversion ratios may be used. Thus where it is desired to convert a series sequence of pulses each of which represents 1/1,000 inches to a sequence of pulses each representing 20 microns, the conversion ratio is 100 to 127, with $(D-N)=27$. A seven-stage binary counter is again needed, though its scope has to be severely curtailed. Rather than force a reset from 100 to zero, it may be preferable to centralize the used range of the counter to the region from 15 to 115, or binary 1111000 to 1100111.

The circuits of FIGS. 9 and 16 are therefore modified as shown in FIG. 17.

A five-entry AND-gate 111 has one input from the Add lead A and further inputs from leads Q₁, Q₄, Q₅, and Q₆. It thus detects the number 114 or binary 0100111. In response, and acting by way of OR-gate 83 and lead 65, it renders all stages except D₁ enabled, so that the 115th pulse switches the counter to binary 1111000 or 15.

To detect 15 on a downward count a four-entry AND-gate 112 has an input from the Subtract lead S and inputs from leads NQ₄, NQ₅, and NQ₆. Its response also acts by way of lead 65 so as to render all stages except D₁ enabled. There is no ambiguity in relying only on the three most significant digit stages for this detection as the counter never operates below binary 1111000.

In this arrangement the output from gate 83 by way of negator 84 and lead 85 is applied to the control and the AND gate inputs of stage D₁ rather than stage D₀ as in the embodiments previously described.

Where $(D-N)$ is positive and the output pulses are applied to a counter, such as counter 24, it is not necessary for each supplementary pulse to be literally added to the input pulses; instead, each may be effectively added by so applying the control signal as to cause the next input pulse to have the effect of two at counter 24.

A suitable modification of the arrangement of FIG. 10 is shown in FIG. 18 wherein counter 24 is assumed to be of the JK flip-flop form as described above for counter 12 with reference to FIG. 8. To simplify the description, therefore, the first stage of counter 24 is depicted similarly to that of counter 12, but with the corresponding references primed.

Stage 17 and gates 21 and 96 are not required; lead 11 is connected to the digit stages of counter 24 direct; and the control signal of waveform (e) (FIG. 11), derived by gate 16, is applied as a third input to OR-gate 64¹ and to the control point of an Inhibit gate 121 inserted in lead RD₁⁰.

In operation, leads RD₁⁰ and 63¹ are positively energized while the counter is in action. The effect of each control signal is to close gate 121, thereby disabling state D₁⁰, and pass by way of gate 64¹ to enable stage D₁¹, instead. Thus the next pulse of the input series arriving over lead 11 actuates stage D₁¹ rather than stage D₁⁰, and so has the weight or effect of two pulses, i.e., it is counted as two.

If when the control signal is derived, stage D₁¹ is already enabled, the signal leaves it enabled, and merely disables stage D₁⁰.

What we claim is:

1. Scale conversion apparatus for converting an input series sequence of electrical pulses of either sign significance, representing equal incremental quantities expressed in a particular measurement scale, to an output series sequence of pulses expressed in another scale, where the output/input scale ratio is D/N , comprising pulse-counting means arranged to count the input pulses and identify each group totalling N algebraically, a detector stage responsive to the state of the counting means to identify in each group the locations for $(D-N)$ single pulses spaced substantially evenly one another within the group and from the nearest corresponding single pulses of immediately adjacent group(s), and develop a control signal with respect to each location, and operative means arranged to be controlled by those control signals so as to effectively add the single pulses algebraically, in dependence on the sign of $(D-N)$, to each input group at the locations identified by the detector stage, thereby deriving as said output sequence an output group totalling D pulses algebraically for each of said input groups of N pulses together with gating means responsive to the sign of the input pulses and to the input pulses themselves, for delaying each such effective addition of a single pulse until the arrival of the next input pulse, thereby preventing such addition if a change of sign should occur after generation of the corresponding control signal but before such addition has taken place.

2. Apparatus as claimed in claim 1 wherein the pulse-counting means includes a bidirectional binary synchronous counter and said detector stage is arranged to develop a said control signal each time a particular one of the digit stages of the counter changes from digit 0 to digit 1 on an upward count or from digit 1 to digit 0 on a downward count, thereby in each case identifying one of said locations.

3. Apparatus as claimed in claim 2 wherein the detector stage includes a gating network arranged to derive a control signal each time a pulse of the input group finds that particular digit stage enabled and holding either digit 0 on an upward count or digit 1 on a downward count.

4. Scale conversion apparatus for converting an input series sequence of electrical pulses of either sign significance, representing equal incremental quantities expressed in a particular measurement scale, to an output series sequence of pulses expressed in another scale, where the output/input scale ratio is D/N and $(D-N)$ is positive, comprising pulse counting means arranged to count the input pulses and identify each group totalling N algebraically, a detector stage responsive to the state of the counting means to identify in each group the locations for $(D-N)$ single pulses spaced substantially evenly from one another within the group and from the nearest corresponding single pulses of immediately adjacent group(s), and develop a control signal with respect to each location, and operative means arranged to be controlled; by those control signals so as to effectively add the single pulses algebraically, in dependence on the sign of $(D-N)$, to each input group at the locations identified by the detector stage, said operative means including means to be operated by said control signal to give the input pulse at each of said locations the effect of two pulses thereby deriving as said output sequence an output group totalling D pulses algebraically for each of said input groups of N pulses.

5. Scale conversion apparatus for converting an input series sequence of electrical pulses of either sign significance, representing equal incremental quantities expressed in a par-

particular measurement scale, to an output series sequence of pulses expressed in another scale, where the output/input scale ratio is D/N , comprising pulse-counting means arranged to count the input pulses and identify each group totalling N algebraically, said pulse-counting means including a bidirectional binary synchronous counter and said detector stage is arranged to develop a said control signal each time a particular one of the digit stages of the counter changes from digit 0 to digit 1 on an upward count or from digit 1 to digit 0 on a downward count, thereby in each case identifying one of said locations, a detector stage responsive to the state of the counting means to identify in each group the locations for $(D-N)$ single pulses spaced substantially evenly from one another within the group and from the nearest corresponding

single pulses of immediately adjacent group(s), and develop a control signal with respect to each location, and operative means arranged to be controlled by those control signals so as to effectively add the single pulses algebraically, in dependence on the sign of $(D-N)$, to each input group at the locations identified by the detector stage, said operative means including connections for causing the control signal to disable the counter stage of least significance and enable the next higher stage (if not already enabled), thereby causing the next input pulse to have the effect of two pulses thereby deriving as said output sequence an output group totalling D pulses algebraically for each of said input groups of N pulses.

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