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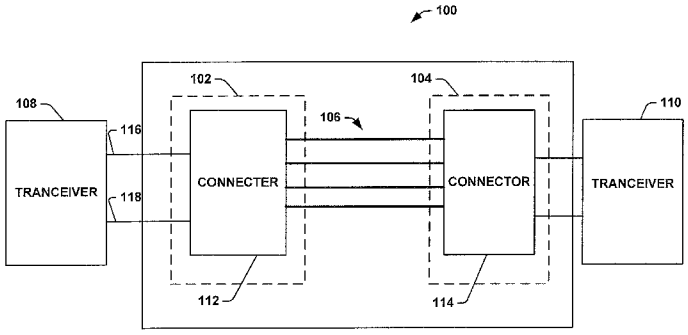

FIG. 1

(57) Abstract: Cable systems and assemblies integrate a reduced number of twin axial copper pairs to transmit and received in a full-duplex transmission signals at transmission speeds greater than or equal to one hundred Giga bytes per second. The reduced number of twin axial copper pairs comprise four or less twin axial copper pairs, in which each pair forms a single twin axial full-duplex cable for passive or active communication of the signals.

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DUPLEX TRANSMISSION OVER REDUCED PAIRS OF TWINAX CABLES

TECHNICAL FIELD

[0001] This disclosure relates generally to full duplex transmissions.

BACKGROUND

[0002] Cables are often utilized as physical media to connect devices that may be networked. Signals can be sent over a physical layer of wires, for example, in which signal coding can used for enhancing the transmission. The cable can include a data link layer for messages sent between a controller (master) and a slave device. The messages could have a set of normal bits for bit synchronization, followed by a frame sync pattern, for example. The frame sync pattern, for example, can be followed by data bit frames, in which each frame could include a start bit, a bit data field, a parity bit and/or a set of fill bits of zero.

[0003] For applications requiring a high data rate with low latency performance, such as in Storage Area Networks and High Performance Computing, the interconnect media selected should have a very high bandwidth capacity, such as with twin axial (twinax) cable, to support the un-modulated baseband signal. To obtain low latency while having low power dissipation, baseband digital communication is typically used instead of a complex modulation scheme requiring sophisticated coding techniques. A drawback is media analog bandwidth. For example, in order to support 10 Gbps (Gigabit/sec) data communication, the media support a certain frequency Hertz of analog bandwidth. In order to achieve these bandwidths, the cable design and coding is refined to address performance parameters in this frequency range.

SUMMARY

[0004] Various embodiments for twin axial transmission over a reduced number of twinax pairs integrated together at respective ends are disclosed herein. An exemplary system comprises a set of duplex twinax pairs configured for communicating a set of signals in different directions. A plug assembly is configured for integrating at least one end of the set of duplex

twinax pairs with a set of interconnects, and connecting the at least one end with an interface port. The plug assembly comprises a transceiver component configured for communicating the set of signals in the different directions to and from the interface port via the set of duplex twinax pairs, and a processor that is operatively coupled to the transceiver component. The processor is configured for digital signal processing of the set of signals for transmission via the set of duplex twinax pairs.

[0005] In another embodiment, a method comprises integrating a reduced set of twinax pairs with a processor and a transceiver of a plug assembly. One or more signals can be received via the plug assembly. At least a part of the one or more signals is encoded with a first communication protocol by the processor. The transceiver transmits the one or more signals via the reduced set of twinax pairs from the processor.

[0006] In another embodiment, a device comprises a memory to store computer-executable instructions, and a first processor, coupled to the memory, that facilitates execution of the computer-executable instructions to perform operations. The operations comprises transmitting a first set of signals via a twin axial copper cable assembly comprising four or less twinax copper pairs to a second device in a first communication protocol at a transmission speed greater than one hundred Gigabytes per second. A second set of signals is received simultaneously in a full-duplex transmission mode from the second device via the four or less copper twinax pairs of the twin axial copper cable assembly.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] **FIG. 1** is a block diagram illustrating an embodiment of a cable assembly system.

[0008] **FIG. 2** is a block diagram illustrating an embodiment of a cable assembly system.

[0009] **FIG. 3** is a block diagram illustrating an embodiment of cable assembly system.

[0010] **FIG. 4** is a block diagram illustrating an embodiment of cable assembly system.

[0011] **FIG. 5** is a block diagram illustrating an embodiment of a transceiver system.

[0012] **FIG. 6** is a block diagram illustrating an embodiment of a transceiver system.

[0013] **FIG. 7** illustrates a flow diagram of an embodiment for a cable assembly system.

[0014] **FIG. 8** illustrates a flow diagram of an embodiment for a cable assembly system.

[0015] **FIG. 9** illustrates a block diagram of an example electronic computing environment.

[0016] **FIG. 10** illustrates a block diagram of an example data communication network.

DETAILED DESCRIPTION

[0017] In consideration of the above-described trends or deficiencies among other things, various embodiments are provided for 100 Gbps transmission rates or greater for full-duplex communications over a reduced number of twinaxial (twinax) pairs. For example, a cable assembly can include a set of twinaxial (or "twinax") cables that can each comprise a full-duplex twinax pair of conductors or a half-duplex twinax pair of conductors. The cable assembly can be configured for communicating one or more signals in two directions simultaneously at transmission speeds of 100 Gigabytes per second or greater, such as processing or transmitting communications at speeds greater than 150 Gigabytes per second or greater than 200 Gigabytes per second. One twin axial cable can comprise, for example, a twin axial conductor pair, or, in other words, two inner conductors. The cable assembly can comprise, for example, four twin axial cables that comprise four twinax pairs of full-duplex twin axial conductors so that each twin axial cable comprises a twin axial pair (pair of conductors) integrated together to form one cable assembly that can communicate between workstations or devices in high speed, full-duplex communications of data signals for further networking of components or processing.

[0018] The twin axial cables can communicate signals according to a full-duplex data transmission, for example, which means that data can be

transmitted in both directions on a signal carrier at the same time or simultaneously, or in a half-duplex mode where one direction is communicated at a time For example, on a local area network with a technology that has full-duplex transmission, one workstation (e.g., device) can be sending data via the cable assembly over at least one conductor of the twinax pair of a twinax cable, while another workstation is receiving data across the same or different twinax pair, or, in other words, over the set of twinax pairs integrated within the cable assembly, in which a "set" as used herein can mean "one or more." Full-duplex transmission implies a bidirectional communication path or line (one that can move data in both directions). Each twinax pair can comprise or constitute a full-duplex twinaxial (twinax) cable. For example, the twinaxial cables can comprise a two-conductor twisted balanced wire, which can have the same or different impedances and a shielding braid that can be wrapped around the two wires or the two conductors. Unlike a simple coaxial cable, twinax wire pairs can include two inner conductors instead of one.

[0019] In one embodiment, the cable assembly can be configured as a passive cable device or as an active cable device, in which either can operate at speeds of at least one hundred Gigabytes per second (100 Gbps) with a reduced number of twinax cable pairs within the cable assembly, such as four or less twinax cable pairs being integrated into the one cable assembly. Processing of communication can also be performed at speeds greater than 150 Gbps and greater than 200 Gbps. The cable assembly can be configured as a passive interconnect cable assembly that does not draw power from within the cable assembly, or as an active assembly that draws power from one or more ends of the twinax pairs into the cable assembly. The passive interconnect cable assembly operates to not consume power and the active cable assembly draws or consumes power at the ends of the cable assembly. The twinax cable pairs can comprise a pair of copper cables, wires or conductors that deliver a high performance option to the interconnections between devices at short and long range distances with increased speed. Although copper conductor, wires, and the like are discussed within various embodiments, cables or twinax pairs with metal conductors other than copper

are also envisioned (e.g., alloys such as but not limited to gold, silver, platinum or the like).

[0020] **FIG. 1** illustrates one embodiment of a cable assembly 100 that is configured as a passive cable device for communicating signals in a full-duplex transmission mode at 100 Gbps via four pairs of conductors or less, eight conductors total or less, four pairs of twinax pairs or less, or, in other words, four twinax cables or less. The cable assembly 100 comprises a plug assembly 102 and a plug assembly104 that can respectively operate as an end housing that integrates and combines interconnects and components for facilitating full-duplex communications between devices or device components along a reduced set of full-duplex twinax wire pairs 106.

[0021] The plug assemblies 102 and 104 can be located at each end of the cable assembly 100 and configured for integrating the respective ends of the set of full-duplex twinax wire pairs 106 with one or more receiving ports or plugs (not shown) of user devices (not shown) for signal communication via the twinax pairs 106. Each twinax pair can comprise a pair of conductors or a single twinax cable within the cable assembly 100.

[0022] The plug assemblies 102 and 104 can respectively comprise a transceiver 108 and a transceiver 110 for receiving and transmitting signals, which can be integrated with a processor as a transceiver microprocessor or controller respectively. The transceivers 108 and 110 can also be located on a circuit board of a user device and operatively coupled to connectors 112 and 114 at each of the twinax cable ends so that the transceivers 108 and 110 are external to the plug assemblies 108 and 110. The transceivers 108 and 110 can comprise traces on a circuit board (not shown), for example, or other conductor interfaces or paths that provide interconnections (e.g., copper interconnects) to the twinax pairs 106 and the transceivers 108 and 110 via the plug assemblies 102 and 104.

[0023] In one example, the transceiver 108 and 110 can be located on a reception or receiving port, jack or sleeve on a respective user device, such as a processor device and other component device connected via the cable assembly 100. The transceivers 108 and 110, for example, can support various communication protocols such as Ethernet, Sonet/SDH, Fibre Channel applications across various switching and routing architectures for

implementation in Local Area Network (LAN), Wide Area Network (WAN), Metropolitan Area Network (MAN), ring networks, storage area networks and the like, as well as for communications between devices that can be connected within these networks for various transmission media. Alternatively or additionally, the transceivers 108 or 110 can operate as a receiver that receives and processes communication transmissions or as a transmitter that transmits and processes communication data for transmission only. The transceiver 108, 110 can include multiple transceivers for receiving or transmitting communications.

[0024] In one embodiment, the transceivers 108 and 110 comprise one transceiver at each end of the cable assembly 100 and that is operatively coupled to the connector 112 and the connector 114 respectively. For example, a receive and a transmit line from the transceiver 108 to the connector 112 enables communication signals to be transmitted and received to the connector 112 and via the twinax cables 106 that each comprise a twinax cable pair of conductors. The receive path 116 and transmit path 118 illustrated can be routed traces, or other interconnects (e.g., copper interconnects), which can operate to receive and/or transmit over the same interconnect.

[0025] The twinax cables 106 operate to transmit and receive data that can be encoded, partitioned or reformatted for transmission via the connectors 112, 114 at 100 Gbps (Gbps) or at greater transmission rates, for example. The connectors 112 and 114 can be different from one another or the same, for example, and further comprise interfaces that can function to automatically terminate the twinaxial cables or twinaxial pairs, integrate the transmissions between different impedances, or convert between signals that can be be balanced or unbalanced. The connectors 112 and 114 can, for example, comprise interfaces that enable signals received or transmitted to comply with a multitude of standards and integrate the twinax pairs to share a common connector for joining to an electronic device. In one example, multiple different standards could be transmitted over the same cable and/or different twinax pairs with various pin connections or trace connections within each connector 112 or 114. Each connector, for example, can comprise a clock (not shown) for re-timing or re-clocking different signals also. The

connectors 112 and 114 can comprise balun connectors for the twinax pairs and/or other interfaces, for example, such as a Medium Dependent Interface (MDI), PMDA, SERDES, etc.

[0026] **FIG. 2** illustrates an embodiment of a cable assembly 200 that comprises a first end section 206 and a second end section 222 for an interconnection of one or more devices (not shown), such as a computer device, mobile processing device, display device personal digital assistant, etc.. The cable assembly 200 is operable as an active twinax cable device for high speed, full-duplex transmissions among devices or device processors with a reduced set of twinax conductor pairs. Additionally, the cable assembly 200 can operate to simultaneously transmit and receive data at a transmission speed of 100 Gbps or greater for one or more different communication protocols. Additionally or alternatively, the cable assembly 200 with four or less twinax pairs can operate to simultaneously transmit and receive data at a transmission speed of 800 Gbps or greater for one or more different communication protocols.

[0027] For example, the cable assembly 200 comprises an interface 210 and an interface 226 at each end that can include a set of interconnects 204, 220 (e.g., copper interconnects or paths) that interface with a receiving port or a plug such as a Quad Small Form-factor Pluggable (QSFP), a Small Form-factor Pluggable, or other pluggable connector. The interface 210 and 226 can be operatively connected to a circuit board 216 and 230 or a surface mount or processor package mount (e.g., a ball grid array or the like) having a processor 208 and 224. The interface 210 and 226 includes a plug portion of the cable assembly 200, which operates as a mate for connection to a plug or port of a device or processing device for communication between one or more other devices. The cable assembly 200 operates as an active cable device that draws or consumes power at one or more ends of the assembly 200, and further processes, encodes and decodes transmissions of one or more communication protocols with low bit error rates and high efficiency.

[0028] The cable assembly 200 comprises a plug assembly 202 and 218 at an end of the cable assembly 200 that comprises the plug portion or the interface 210 that operates as the mate for connection to a plug or port of a device. The plug assembly 202 or 218 can comprise a processor 208 or

224 operatively connected to the circuit board 216 or 230 or a surface mount respectively. The processor 208 or 224 can operate with a transceiver 212, 228 to encode, decode, partition, or process error correction code (ECC) such as Forward Error Correction Code (FEC) according to one or more algorithms that can enable high speed, full-duplex transmissions of data at 100 Gbps or greater Gbps via the twinax pairs 214.

[0029] In one embodiment, the processors 208 or 224 can operate to draw or consume power from an independent power source (not shown) located internally, which can be coupled to the circuit board or processor package 216, 230. In addition, the signals being transmitted can be used to power the cable. For example, a power signal transmission can be utilized to power the processors for transmission, such as by an electromagnetic coupling or other remote power signals. A power source from the device coupled to the cable assembly can also be utilized to power the processors 208, 224, such as from an external power source located on the device.

[0030] The processors 208 and 224 can be integrated as transceiver processors that operate to transmit and receive signals for full-duplex transmissions along the twinax pairs. In addition, the processors 208 and 224 can be coupled to a transmitter, receiver, or transceiver 212, 228 located within the plug assembly 202, 218. For example, a transceiver 212, or 228 can be coupled to the processors on the circuit board 216 or 230 via routed traces or a processor package having connect pads, ball grid array, or other like interconnects mounted on the circuit board 216, 230 (e.g., a printed circuit board) of the cable assembly 200.

[0031] The cable assembly 200 can be similar to the cable assembly 100 discussed above, but instead of having a microprocessor on a device board and a connector to the plurality of twin axial cables 214, a microprocessor 208, 224 can be integrated on the head of the twinax cables 214, in which the connection on the head of the microprocessor through the circuit board is the plug or interface 210 or 226 and/or a receiving port, for example. The cable side of operation can operate to drive the cable assembly 200 with power drawn or consumed with an integrated mount and package on a substrate (e.g., a semiconductor substrate).

[0032] In another embodiment, the cable assembly 200 can include one side having service connections via the board that are coupled to interconnects 204, 220. One transceiver end (e.g., the plug assembly 202) can be coupled to the twinax pairs or twinax cables 214 (e.g., four twinax copper pairs or eight conductors) in which each pair is bi-directional or a full-duplex communication system to receive one communication protocol while another end converts the communication protocol to another communication protocol in order to standardize a diversity of different communication signals into one signal for use by multiple different ports or jacks within devices. At the other end of the cable assembly 200 (e.g., the plug assembly 218) can operate to decode and also convert back to the first communication protocol based on the type of connecting device or connecting interface 210, 226. The plug assembly 202 or 218 can operate to comply with multiple different standards for communication. One end of the cable assembly could process one communication protocol and the other end a different communication protocol, or both ends the same communication protocol depending upon the mode of operation selected by the processor, the device in which the plug assemblies are interfaced with or connected to, a specification provided by the device connected to the cable assembly 200, and/or a selection of one or more of the twinax pair of twinax pairs for communication. For example, the plug assembly 202 or 218 can operate in a first mode for a first communication protocol or in a second mode for a different communication protocol of communication, in which one or more of communication data or signals in the communication protocols can be transmitted over eight or less conductors of four or less pairs of twinax cables at 100 Gbps or a greater transmission rate.

[0033] **FIG. 3** illustrates an embodiment of the cable assembly 300 coupled to a plug 302 and a plug 304, which can comprise a receiving port, for example, which can be a Quad Small Form-factor Pluggable (QSFP), a Small Form-Factor Pluggable (SFP) port, a Small Form Factor SFF casing, or the like receiving port. The cable assembly 300 is similar to the cables assemblies discussed above with similar components for operation.

[0034] The cable assembly 300 includes interfaces 204 and 220 operate with the surface mount components to join interconnects 204, 220

therein with the plug 302 and 304 respectively as a cage and a mate. The plug 302 and 304 can comprise QSFP and/or SFP protocols, which are form factors designed to reduce costs and power consumption, improve reliability and reduce thermal footprint: SFP plus is a small form factor pluggable plus (specified under SFF-8431) and QSFP is quad small form factor pluggable (specified under SFF-8436). Originally intended for an optical form factor, these interfaces can include copper interconnect solutions. The SFP and QSFP form factors are lower power-consuming modules, in which lower power (less heat) increases reliability.

[0035] The board 216 comprises the chip or processor 208 mounted at the head of the cable assembly 202, in which the chip or processor 208 is powered through the QSFP connection of the plug and the plug assembly 210. The chip can operate as a transceiver chip that is connected to the plurality of twinax cables 214. In one embodiment, the plurality of twinax pairs 214 can comprise different cable assembly configurations that communicate at different transmission rates in a single cable assembly 200 with multi-rate communication transmissions. The plurality of twinax pairs 214 can comprise a first twinax pair, a second twinax pair, a third twinax pair, and a fourth twinax pair, in which each twinax pair can comprise a pair of conductors that can respectively communicate at various transmission rates (e.g., 100 Gbps, 40 Gbps and/or 10 Gbps).

[0036] **FIG. 4** illustrates an example of a cable assembly that operates at high speed transmission for transmitting and receiving data back and forth from one or more devices. A cable assembly 400 comprises similar components as discussed above and further includes encoding components and decoding components mounted on a surface mount or circuit board within the plug assemblies 202 and 218.

[0037] The cable assembly 400 is operatively coupled to a first device 402 and a second device 404 via the reduced set of twinax pairs 214 at speeds of 100 Gbps or greater. The first device 402 or the second device 404 can respectively comprise a processor 406, 410 and one or more data stores 408 and 412. The first device 402 or the second device 404 can comprise a processing device such as a personal computer device, a mobile device, an

input/output device, a display, a personal digital assistant, or other similar device operable for communicating via the plug 302 or 304.

[0038] The surface mount or electronic board 216, 230 of the plug assemblies 202 and 218 at opposite ends of the twinax pairs 214 can comprise encoders 414 and 418 and decoders 416 and 420 respectively that are operatively coupled to a processor and/or transceiver architectures on the circuit boards 216, 230 or a mounting assemblies. The encoder 414, for example, can operate to convert at least a part of information of signals from one format, code or communication protocol to another via one or more algorithms based on a selection of a communication protocol. For example, the selection can be predetermined or dynamic based on the type of devices coupled to the cable assembly 400. The communication protocol (e.g., a Universal Serial Bus standard, a Peripheral Component Interconnect Express standard, a Display Port standard, High-Definition Multimedia Interface, S-Video, RCA, etc.), for example, can be based on a specification or a determination by the device of the one or more signals, a communication protocol of the one or more signals, a device communication protocol of the first device or the second device coupled to one or more ends of the reduced set of twinax pairs 214, and/or a selection of a twinax pair of the reduced set of twinax pairs, which can be specified by a processor (e.g., 208, 224 discussed supra) of the cable assembly 400.

[0039] The decoder 416 or 420 can operate to reverse the operation of the encoder in order to convert the information from one format or protocol into the original format or protocol. For example, the decoder 416 or 420 can operate to convert binary information from a number of lines to a unique output lines. For example, in cases where one or more encoders encode data from the first device 402 into one format for high speed transmission, the plug assembly 218 can operate to decode and/or re-code the data based on the second device 404 being a different device operating in a different communication protocol.

[0040] In one embodiment, the twinax pairs 214 comprise only four or less pairs of conductors for communicating over twinax cables at a transmission rate of 100Gbps or greater. In one example, the cable assembly 400 comprises the plurality of twinax cables 214 that operate at multi-rate

transmission speeds. The plurality of twinax pairs can comprise a first twinax pair and a second twinax pair that operate at multi-rate transmissions or at different transmission rates respectively. For example, the first twinax pair can operate within the cable assembly at a forty Gigabytes per second rate and the second twinax pair can operate at a ten Gigabytes per second rate. The cable assembly can operate as an active assembly that draws or consumes power similar to that discussed above.

[0041] The plurality of twinax pairs comprising the first twinax pair and the second twinax pair, for example, can comprise an active copper, in which rather than four pairs both of the twinax pairs (first and second) can be two twinax cables that are operable as full-duplex transmission lines that are two directional with 40 Gbps and 10 Gbps transmission speeds. The cable assembly therefore has twinax pairs that can have two pairs of conductors operating at 40 Gbps, and two 10 Gbps, and/or one 100 Gbps cable assembly.

[0042] **FIG. 5** and **FIG. 6** together illustrate aspects of transceiver architectures for the cable assembly 400 discussed in this disclosure. **FIG. 5** illustrates the plug assembly 202 having a transceiver architecture for transmission of encoded data at high transmission speeds (e.g., 80 Gbps or 100 Gbps, and greater). **FIG. 6** illustrates the plug assembly 202 having a transceiver architecture for receiving of encoded data at high transmission speeds (e.g., 80 Gbps or 100 Gbps, and greater). These illustrations are examples for the sake of explanation and the architectures discussed can be comprised by both plug assemblies 202 and 218, or comprised in opposite plug assemblies 218 and 202 for a communication encoding and decoding in the opposite direction.

[0043] **FIG. 5** illustrates similar components as discussed above with the transceiver component 212 comprising a Forward Error Correction (FEC) encoder 502, a signal processing pipeline 506 and a Digital-to-Analog Converter (DAC) 508. The FEC encoder 502 operates to encoded data received and to transmit most significant bits (msbs) to a signal processing pipeline 506, which can include one or more processing components for processing signals concurrently. The signal processing pipeline 506, for example, can include a mapper that receives signals over a set of bit stream

pathways (e.g., three connections) and assimilates the data to output a set of symbols for transmission across the channel (e.g., the twinax pairs 214). The DAC 508 converts the digital signal to an analog signal for transmission.

[0044] **FIG. 6** illustrates similar components discussed above also with the transceiver component 228 comprising a programmable gain amplifier (PGA) 602, an Analog-to-Digital Converter (ADC) 604, an equalizer component 606, and an FEC Decoder 608. The twinax pairs 214 communicate (transmit and receive) in a full-duplex mode of transmission to and from the transceiver component 228. The signal can be amplified by the PGA 602, converted from analog to digital by the ADC 604, equalized by the equalizer 606 and further decoded by the FEC decoder 608 for 80 Gbps or 100Bbps and greater transmissions.

[0045] An example method 700 for a cable assembly to transmit and receive communication data at high speed transmissions along a reduced set of twinax pairs is illustrated in **FIG. 7**. At 702, the method 700 comprises integrating a reduced set of twinax pairs with a processor and a transceiver of a plug assembly. The twinax pairs are reduced to four or less pairs of twin axial conductors, such as twin axial copper conductors that enable full-duplex communication between different end devices via the twinax pairs. The cable assembly is operable at 80 Gbps or greater, such as at 100 Gbps transmission rates for transmission of signals in full duplex communication modes. At 704, the method comprises receiving one or more signals via the plug assembly.

[0046] At 706, at least a part of the one or more signals is encoded with a first communication protocol by the processor. The encoding can further comprise encoding at least a portion of the one or more signals in a second communication protocol to transmit the one or more signals from the first device and to the second device. The method 700 can also include selecting from the first communication protocol and the second communication protocol which protocol to encode the at least the part of the one or more signals. For example, the selecting can be based on at least one of a specification of the one or more signals, a communication protocol of the one or more signals, a device communication protocol of the first device or the second device coupled to one or more ends of the reduced set of twinax pairs, or a selection

of a twinax pair of the reduced set of twinax pairs. At 708, the transceiver transmits the one or more signals via the reduced set of twinax pairs from the processor via the reduced set of twinax pairs.

[0047] In one embodiment, integrating the reduced set of twinax pairs with the processor and the transceiver of the plug assembly can comprise integrating four or less twin axial cables that respectively comprise a pair of twinax conductors with a microprocessor package assembly having a mounting assembly to a circuit board. Receiving and transmitting the one or more signals can comprise communicating the one or more signals in a full-duplex communication simultaneously in different directions between a first device and a second device.

[0048] **FIG. 8** illustrates a method 800 for a cable assembly operable to communicate data at 100 Gbps or greater over reduced pairs of twinax pairs. For example, four or less cables each having a twinax pair or pair of twin axial conductors, such as copper conductors or conductors of another alloy can operate to transmit and receive signals in a full-duplex communication mode at increased rates of 100 Gigabytes per second or greater.

[0049] At 802, data is communicated from a first device via eight or less conductors (e.g., copper conductors) that form four or less twinax pairs for a full duplex communication mode in a twin axial cable assembly at 100 Gigabytes per second or less.

[0050] At 804, the data is received at a second device via a plug assembly that integrates the eight or less conductors forming four or less twinax pairs in the full duplex communication mode via the plug assembly that integrate the eight or less conductors with a processor and a transceiver.

[0051] As mentioned, the techniques described herein can be applied to any device and/or network where power management is desirable in a multiprocessor system. Handheld, portable and other computing devices and computing objects of all kinds can be used in connection with the various embodiments, i.e., anywhere that a device may wish to implement power management for a multiprocessor system. Accordingly, the below general purpose remote computer described below in **FIG. 9** is one example, and the disclosed subject matter can be implemented with any client having network/bus interoperability and interaction. The disclosed subject matter can

be implemented in an environment of networked hosted services in which very little or minimal client resources are implicated, *e.g.*, a networked environment in which the client device serves merely as an interface to the network/bus, such as an object placed in an appliance.

[0052] **FIG. 9** illustrates an example of a computing system environment 1300 in which some aspects of the disclosed subject matter can be implemented, although as made clear above, the computing system environment 1300 is one example of a computing environment for a device.

[0053] **FIG. 9** is an exemplary device for implementing the disclosed subject matter includes a general-purpose computing device in the form of a computer 910. Components of computer 910 may include a processing unit 920, a system memory 930, and a system bus 921 that couples various system components including the system memory to the processing unit 920. The system bus 921 may be any of several types of bus structures including a memory bus or memory controller, a peripheral bus, and a local bus using any of a variety of bus architectures.

[0054] Computer 910 includes a variety of computer readable media. Computer readable media can be any available media that can be accessed by computer 910. The system memory 930 may include computer storage media in the form of volatile and/or nonvolatile memory such as read only memory (ROM) and/or random access memory (RAM).

[0055] The computer 910 may also include other removable/non-removable, volatile/nonvolatile computer storage media. For example, computer 910 could include a hard disk drive that reads from or writes to non-removable, nonvolatile magnetic media, a magnetic disk drive that reads from or writes to a removable, nonvolatile magnetic disk, and/or an optical disk drive that reads from or writes to a removable, nonvolatile optical disk, such as a CD-ROM or other optical media.

[0056] The computer 910 can operate in a networked or distributed environment using logical connections to one or more other remote computer(s), such as remote computer 970, which can in turn have media capabilities different from device 910. The logical connections depicted in **FIG. 9** include a network 971, such local area network (LAN) or a wide area

network (WAN), but can also include other networks/buses, either wired or wireless.

[0057] **FIG. 10** provides a schematic diagram of an exemplary networked or distributed computing environment. The distributed computing environment comprises computing objects 1010, 1012, etc. and computing objects or devices 1020, 1022, 1024, 1026, 1028, etc., which may include programs, methods, data stores, programmable logic, etc., as represented by applications 1030, 1032, 1034, 1036, 1038 and data store(s) 1040. Each computing object 1010, 1012, etc. and computing objects or devices 1020, 1022, 1024, 1026, 1028, etc. can communicate with one or more other computing objects 1010, 1012, etc. and computing objects or devices 1020, 1022, 1024, 1026, 1028, etc. by way of the communications network 1042, either directly or indirectly. Even though illustrated as a single element in **FIG. 10**, communications network 1042 may comprise other computing objects and computing devices that provide services to the system of **FIG. 10**, and/or may represent multiple interconnected networks, which are not shown.

[0058] In a client/server architecture, a client is usually a computer that accesses shared network resources provided by another computer, e.g., a server. In **FIG. 10**, as an example, computing objects or devices 1020, 1022, 1024, 1026, 1028, etc. can be clients and computing objects 1010, 1012, etc. can be servers where computing objects 1010, 1012, etc., acting as servers provide data services, such as receiving data from client computing objects or devices 1020, 1022, 1024, 1026, 1028, etc., storing of data, processing of data, transmitting data to client computing objects or devices 1020, 1022, 1024, 1026, 1028, etc., although any computer can be considered a client, a server, or both, depending on the circumstances.

[0059] In addition, the disclosed subject matter can be implemented as a method, apparatus, or article of manufacture using typical manufacturing, programming or engineering techniques to produce hardware, firmware, software, or any suitable combination thereof to control an electronic device to implement the disclosed subject matter. Computer-readable media can include hardware media, or software media. In addition, the media can include non-transitory media, or transport media.

CLAIMS

What is claimed is:

1. A system, comprising:

a set of full duplex twinax pairs comprising a set of four twin axial cables or less configured for communicating a set of signals in opposite directions concurrently at a speed of at least one hundred gigabytes per second;

a plug assembly configured for integrating at least one end of the set of full duplex twinax pairs with a set of interconnects, and connecting the at least one end with an interface port, the plug assembly comprising:

a transceiver component configured for communicating the set of signals in the different directions to and from the interface port via the set of full duplex twinax pairs; and

a processor operatively coupled to the transceiver component that is configured for digital signal processing of the set of signals via the set of full duplex twinax pairs.

2. The system of claim 1, wherein the processor is further configured for facilitating a communication of the set of signals via the at least one end of the set of full duplex twinax pairs via a surface mount assembly operatively coupled to the transceiver component, and the set of full duplex twinax pairs comprises a twinaxial pair of two conductors that is configured for a communication of the set of signals in opposite directions simultaneously.

3. The system of claim 1, wherein the set of full duplex twinax pairs is configured for communicating the set of signals directions at the speed of at least 100 Gbps by encoding at least a portion of the set of signals in a communication protocol to transmit the set of signals from a first device and to a second device.

4. The system of claim 1, wherein the plug assembly is operatively connected to the set of full duplex twinax pairs via the set of interconnects, and further configured for consuming power from the at least one end of the set of full duplex twinax pairs, and the plug assembly further comprises an interface that comprises at least one of a quad small form factor pluggable interface or a small form factor pluggable interface.

5. A method comprising:

integrating a reduced set of twinax pairs comprising four or less full duplex twin axial cables with a processor and a transceiver of a plug assembly;

receiving one or more signals via the plug assembly;

encoding at least a part of the one or more signals with a first communication protocol by the processor; and

transmitting by the transceiver the one or more signals via the reduced set of twinax pairs from the processor at a speed of at least one hundred gigabytes per second.

6. The method of claim 5, wherein the transmitting the one or more signals via the reduced set of twinax pairs comprises communicating the one or more signals at a speed of at least one eighty gigabytes per second.

7. The method of claim 5, wherein the integrating the reduced set of twinax pairs with the processor and the transceiver of the plug assembly comprises integrating the four or less twin axial cables comprising a pair of twinax conductors with a microprocessor package assembly having a mounting assembly coupled to a circuit board, and the receiving the one or more signals and the transmitting the one or more signals comprise communicating the one or more signals in a full-duplex communication simultaneously in different directions between a first device and a second device.

8. The method of claim 5, further comprising:

encoding at least a portion of the one or more signals in a second communication protocol to transmit the one or more signals from a first device and to a second device;

selecting from the first communication protocol and the second communication protocol which protocol to encode the at least the part of the one or more signals; and

drawing power via at least one end of the reduced set of twinax pairs from at least one of an independent power source, the one or more signals received from a first device or a second device, or a power source of the first device or the second device.

9. A device comprising:

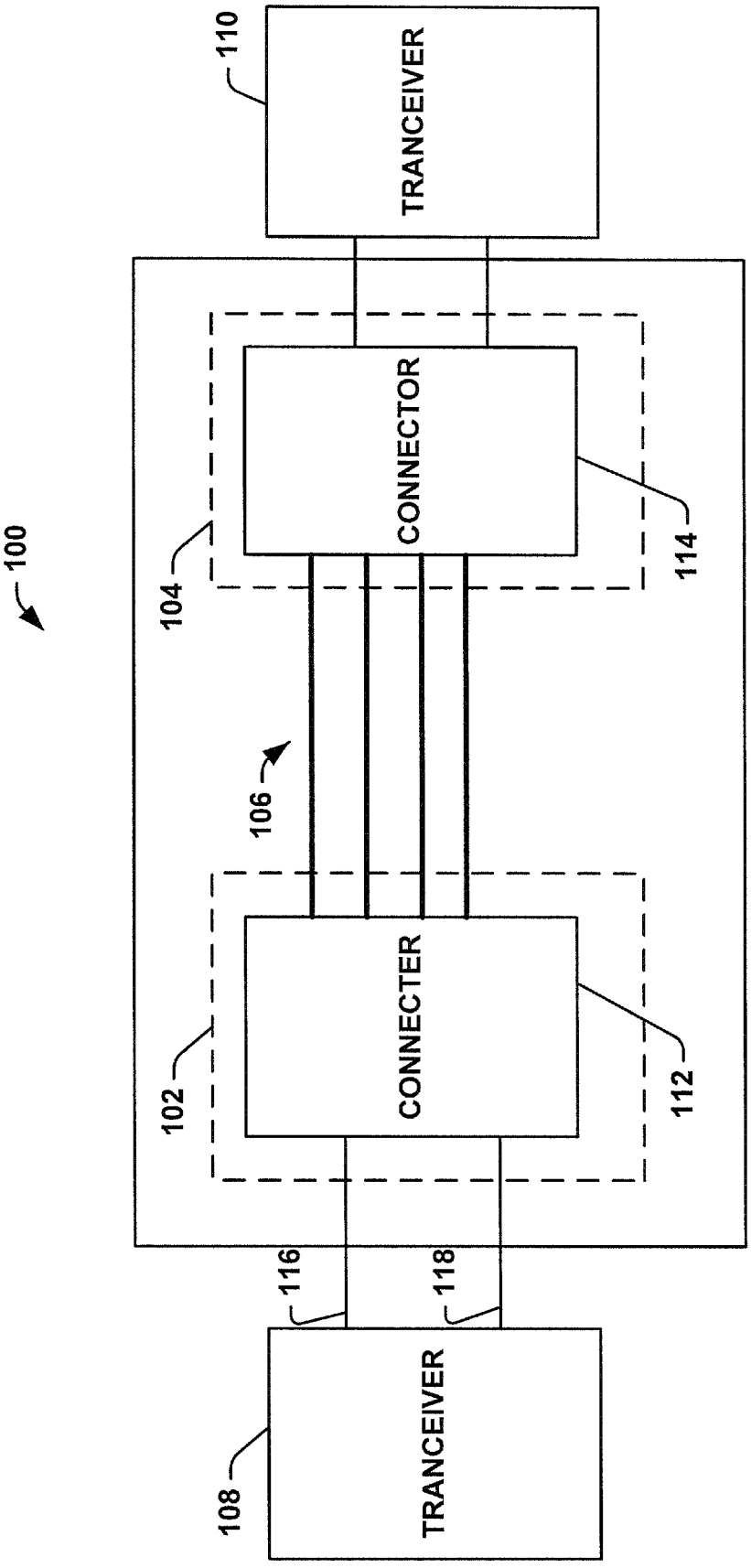
a memory to store computer-executable instructions; and

a first processor, coupled to the memory, that facilitates execution of the computer-executable instructions to perform operations, comprising:

transmitting a first set of signals via a twin axial copper cable assembly comprising four or less twinax copper pairs to a second device in a first communication protocol at a transmission speed of at least one hundred gigabytes per second; and

receiving simultaneously in a full-duplex transmission mode a second set of signals from the second device via the four or less copper twinax pairs of the twin axial copper cable assembly.

10. The device of claim 9, wherein the transmitting comprises encoding, via a second processor, at least a part of the first set of signals in the first communication protocol with the transmission speed comprising eighty gigabytes per second or one hundred gigabytes per second, and the second processor is integrated within a plug assembly configured for integrating the four or less twinax copper pairs on a package mount assembly comprising copper interconnects to the second processor and draws power from at least one of an independent power source within the plug assembly and connected to the package mount assembly, the first set of signals or the second set of signals, or a power source external to the twin axial copper cable assembly that comprises the plug assembly.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TRANCEIVER
104
CONNECTOR
114
106
102
CONNECTER
112
116
118
108
TRANCEIVER

FIG. 1

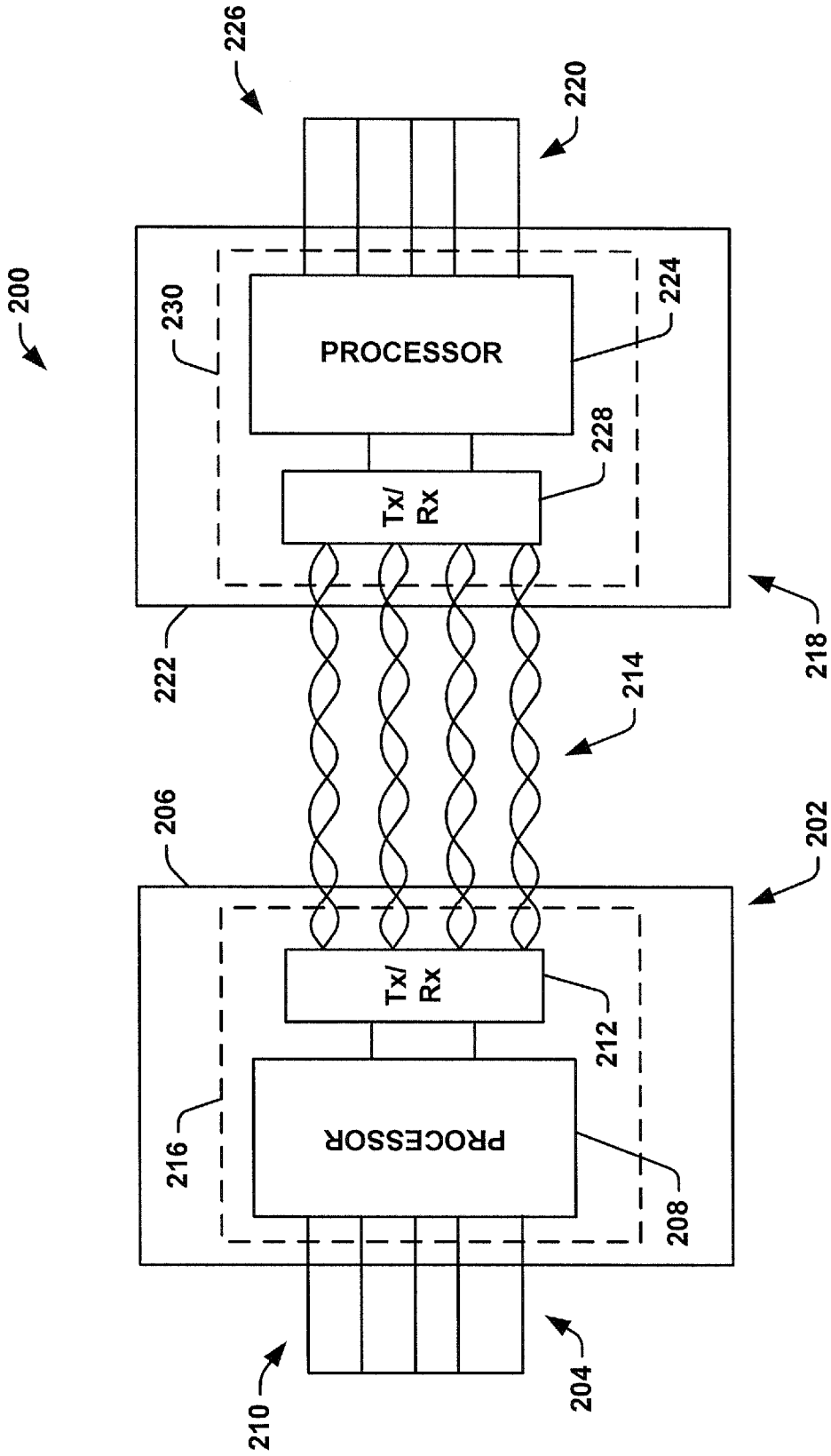
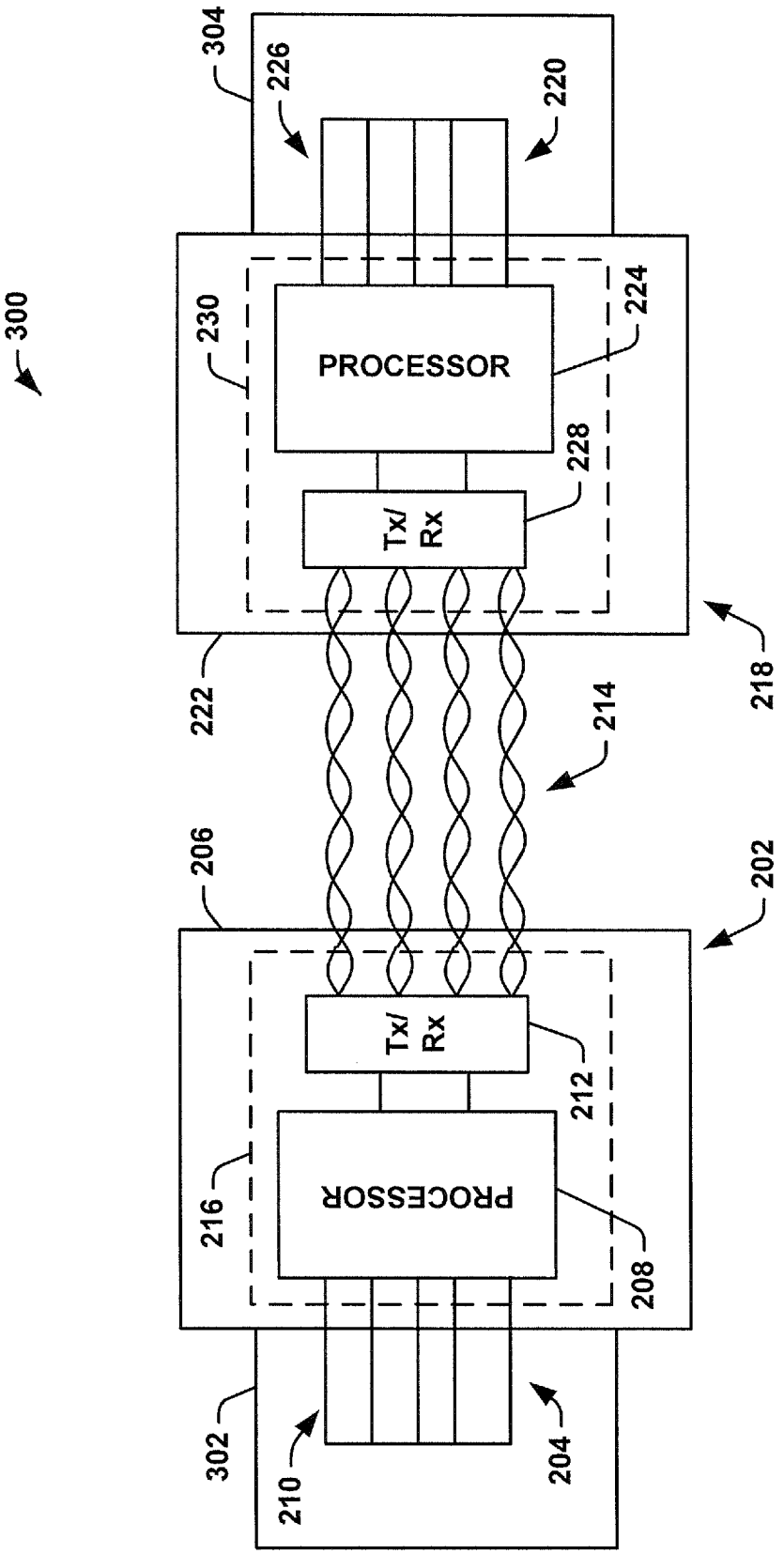

200
226
220
230
PROCESSOR
224
228
Tx/
Rx
222
218
214
206
202
Tx/
Rx
212
216
PROCESSOR
208
210
204

FIG. 2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304
226
220
230
PROCESSOR
224
228
Tx/
Rx
222
218
214
206
202
Tx/
Rx
212
216
PROCESSOR
208
302
210
204

FIG. 3

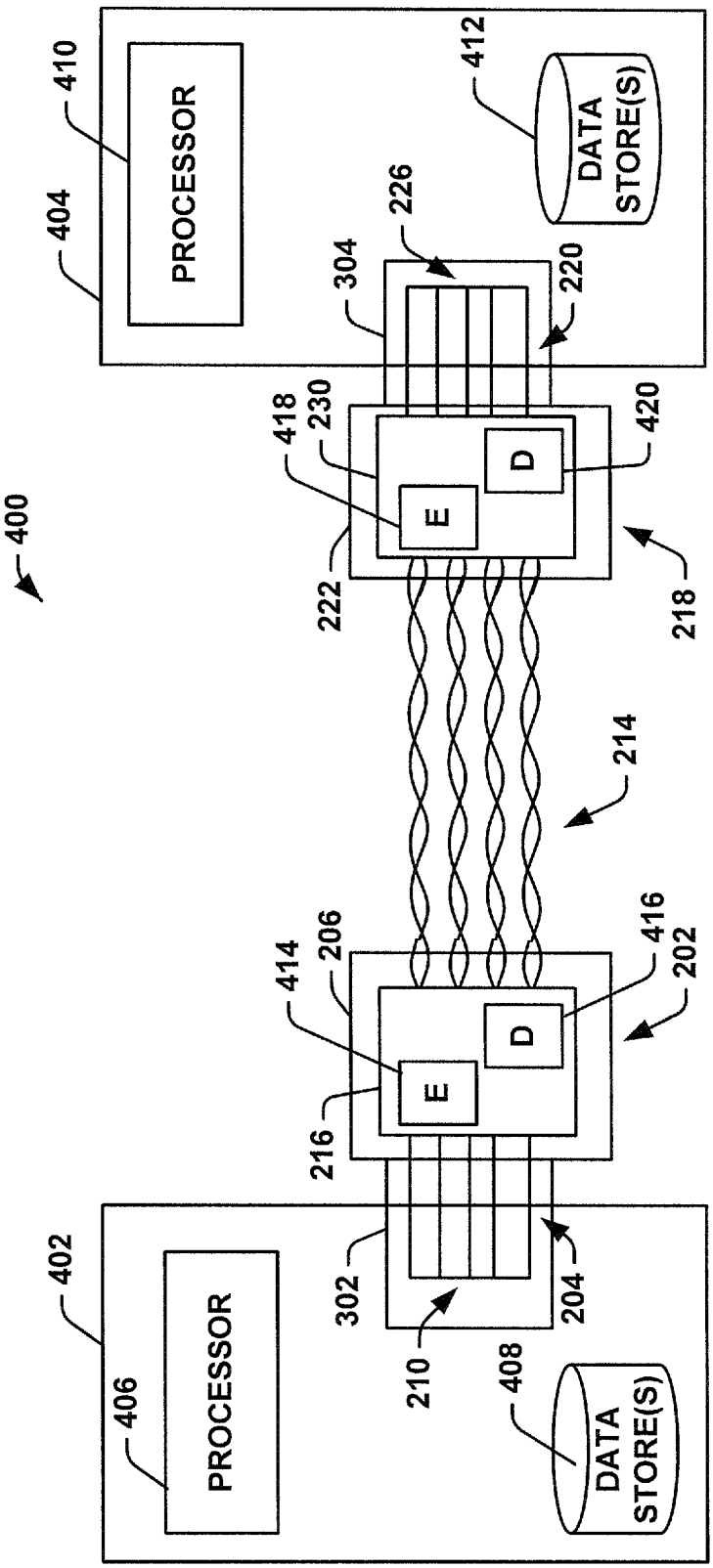
400
402
PROCESSOR
406
404
PROCESSOR
410
DATA STORE(S)
408
DATA STORE(S)
412
202
204
206
210
214
216
218
220
222
226
230
302
304
414
416
418
420
D
E
D
E

FIG. 4

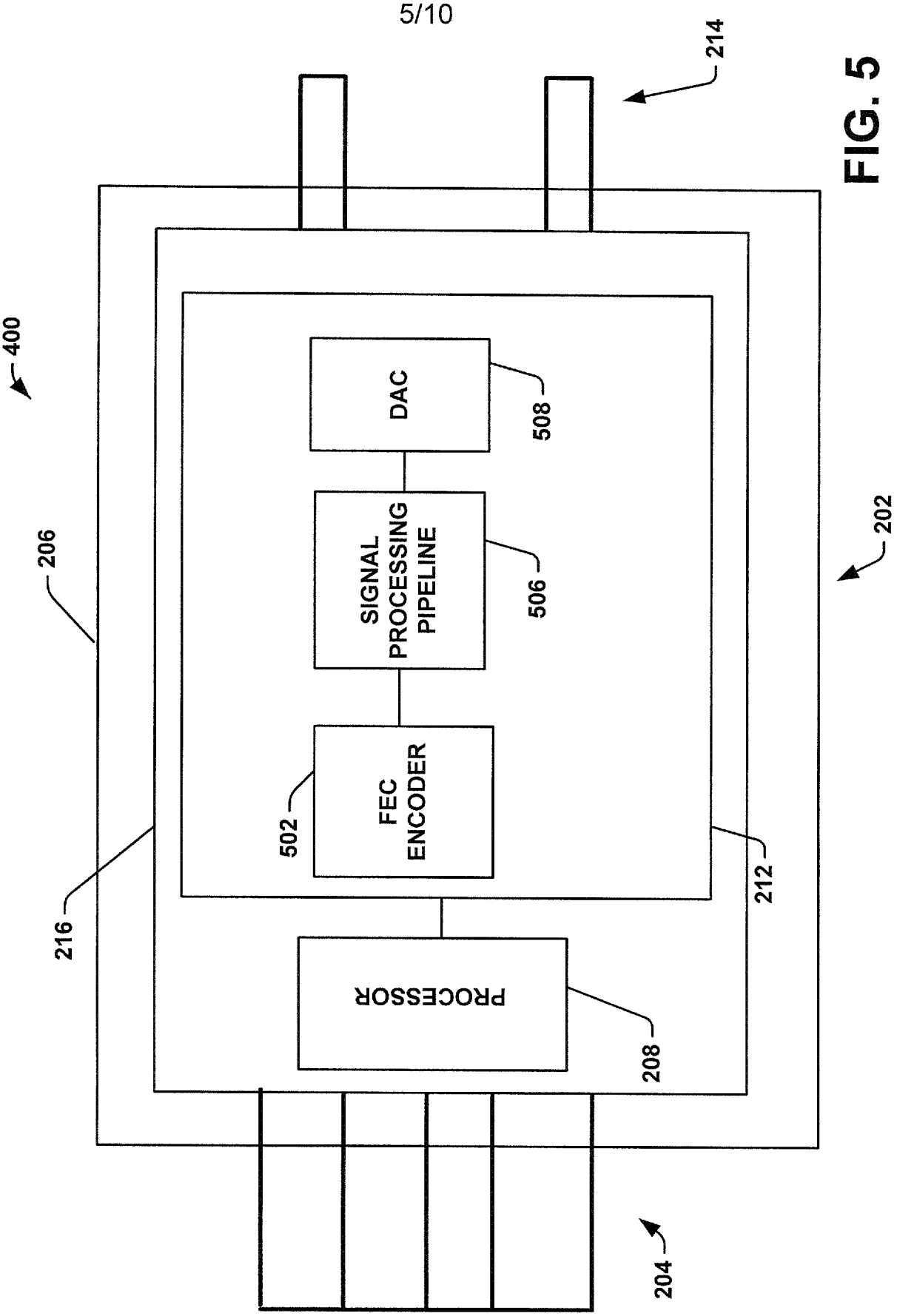
400
214
202
206
216
212
DAC
508
SIGNAL PROCESSING PIPELINE
506
FEC ENCODER
502
PROCESSOR
208
204

FIG. 5

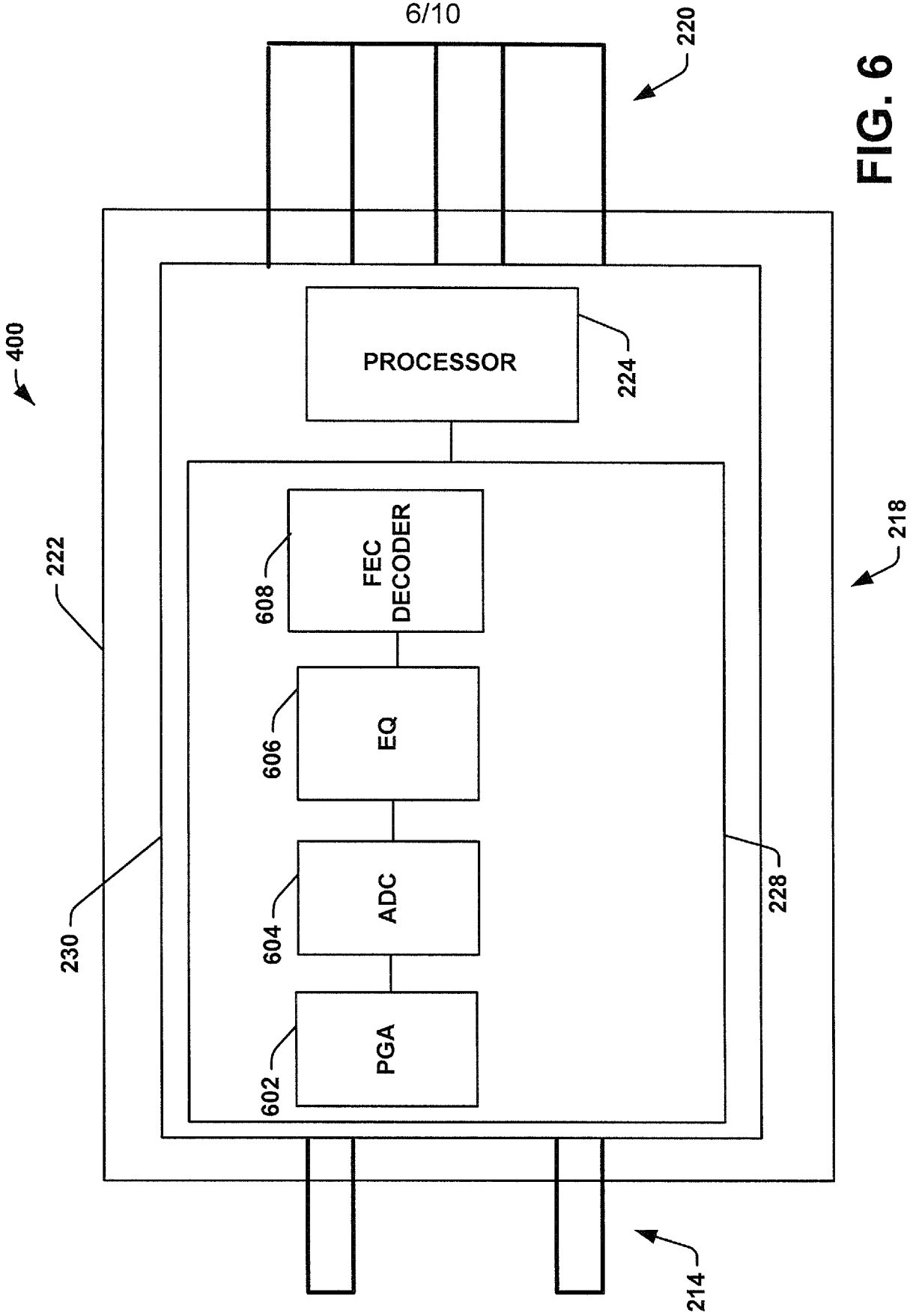
400
220
PROCESSOR
224
222
218
608
FEC DECODER
606
EQ
604
ADC
602
PGA
230
228
214

FIG. 6

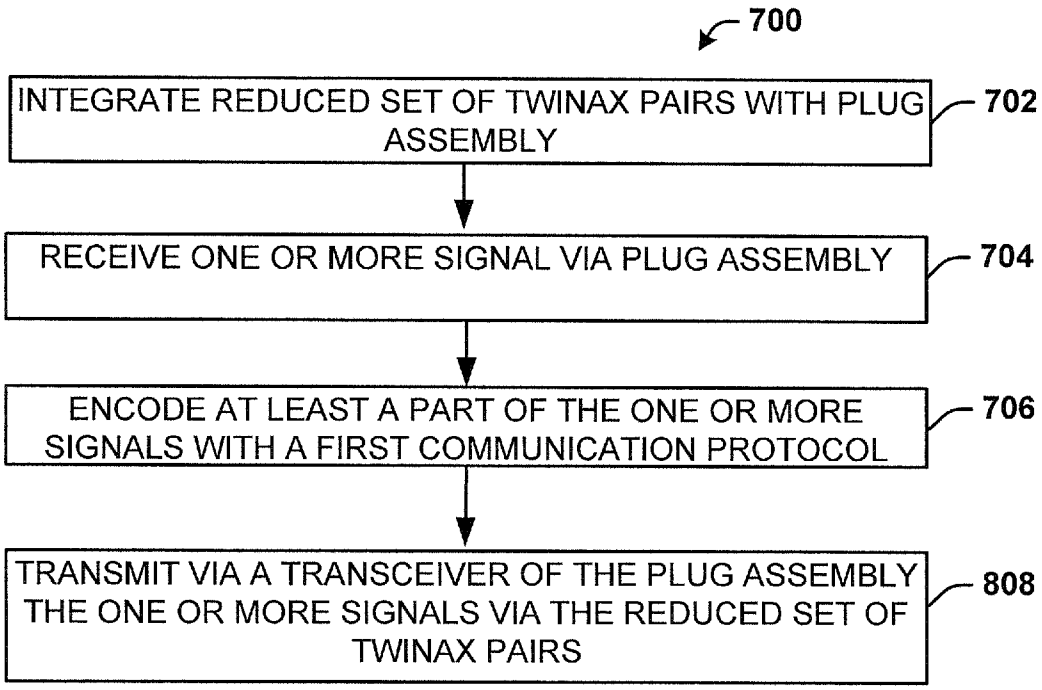
700
INTEGRATE REDUCED SET OF TWINAX PAIRS WITH PLUG ASSEMBLY
702
RECEIVE ONE OR MORE SIGNAL VIA PLUG ASSEMBLY
704
ENCODE AT LEAST A PART OF THE ONE OR MORE SIGNALS WITH A FIRST COMMUNICATION PROTOCOL
706
TRANSMIT VIA A TRANSCEIVER OF THE PLUG ASSEMBLY THE ONE OR MORE SIGNALS VIA THE REDUCED SET OF TWINAX PAIRS
808

FIG. 7

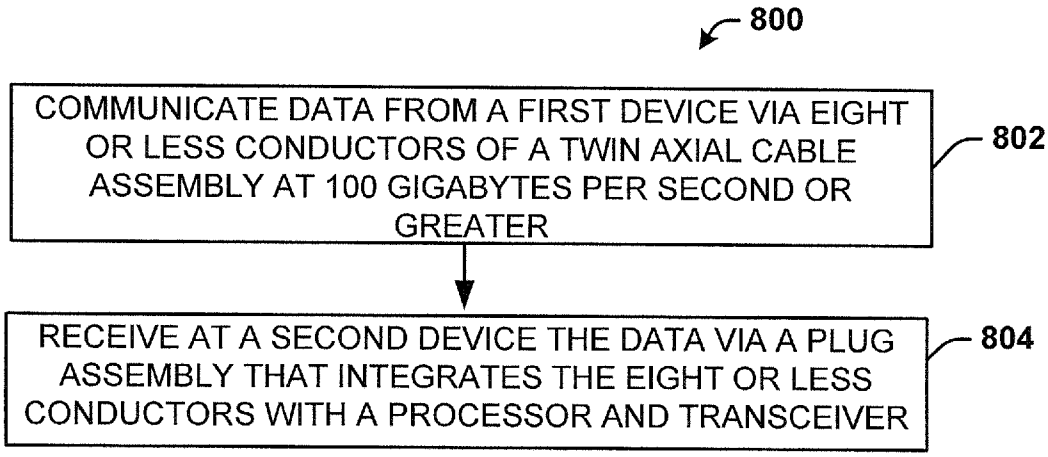
800
COMMUNICATE DATA FROM A FIRST DEVICE VIA EIGHT OR LESS CONDUCTORS OF A TWIN AXIAL CABLE ASSEMBLY AT 100 GIGABYTES PER SECOND OR GREATER
802
RECEIVE AT A SECOND DEVICE THE DATA VIA A PLUG ASSEMBLY THAT INTEGRATES THE EIGHT OR LESS CONDUCTORS WITH A PROCESSOR AND TRANSCEIVER
804

FIG. 8

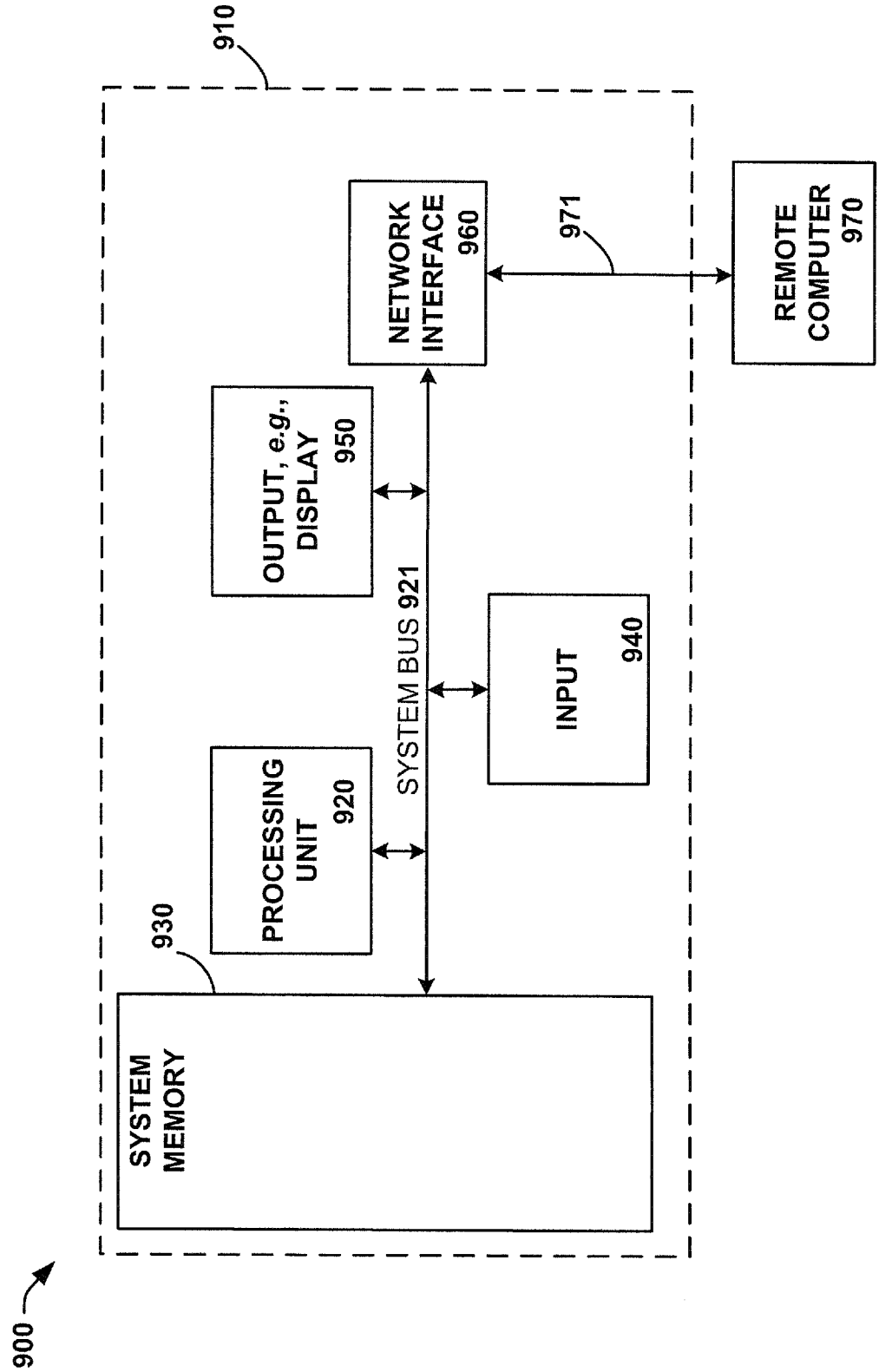
900
910
SYSTEM MEMORY
930
PROCESSING UNIT 920
SYSTEM BUS 921
OUTPUT, e.g., DISPLAY 950
INPUT 940
NETWORK INTERFACE 960
971
REMOTE COMPUTER 970

FIG. 9

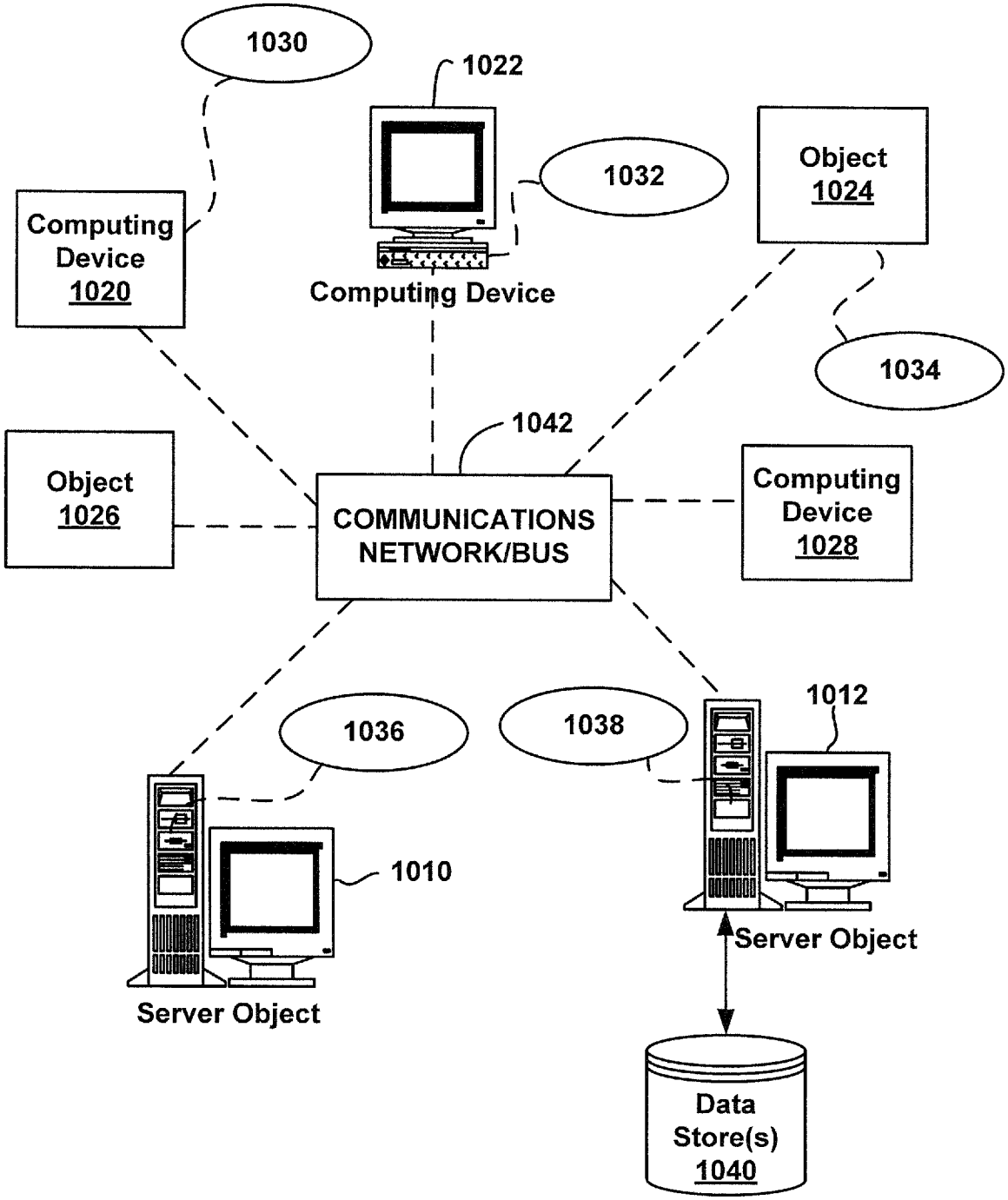
1030
1022
1032
Object
1024
Computing
Device
1020
Computing Device
1034
1042
Object
1026
COMMUNICATIONS
NETWORK/BUS
Computing
Device
1028
1012
1036
1038
1010
Server Object
Server Object
Data
Store(s)
1040

FIG. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/042589

A. CLASSIFICATION OF SUBJECT MATTER

H01B 11/02(2006.01)i, H01B 13/016(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01B 11/02; G06F 11/30; H01B 7/00; H04L 25/00; H04B 10/00; H04B 3/00; H01B 7/34; H04L 5/20; H04B 10/12; H01B 13/016

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: duplex, twinax, cable, transceiver

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 8989283 B1 (APPLIED MICRO CIRCUITS CORPORATION) 24 March 2015 See abstract; column 2, lines 12-15, column 3, lines 36-52, column 4, line 53 - column 5, line 52, column 6, lines 8-9, column 7, lines 37-42; and figures 1-4.	1-10
A	US 2010-0307790 A1 (SATOSHI OKANO) 09 December 2010 See abstract; claims 1-4; and figures 1A-5B.	1-10
A	US 05483020 A (WILLIAM G. HARDIE et al.) 09 January 1996 See abstract; claims 1-11; and figures 1-4.	1-10
A	WO 97-32252 A1 (DATA GENERAL CORPORATION) 04 September 1997 See abstract; claims 1-7; and figures 1-13.	1-10
A	US 2012-0263454 A1 (TOSHIAKI KOIKE-AKINO et al.) 18 October 2012 See abstract; claim 1; and figure 1.	1-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 April 2016 (27.04.2016)	**27 April 2016 (27.04.2016)**

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International Application Division
Korean Intellectual Property Office
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KIM, Yeon Kyung
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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/042589

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		DE 69730593 T2	06/10/2005
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		EP 0883845 B1	08/09/2004
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		JP 2000-509172 A	18/07/2000
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		WO 98-21660 A1	22/05/1998
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		US 8433205 B2	30/04/2013