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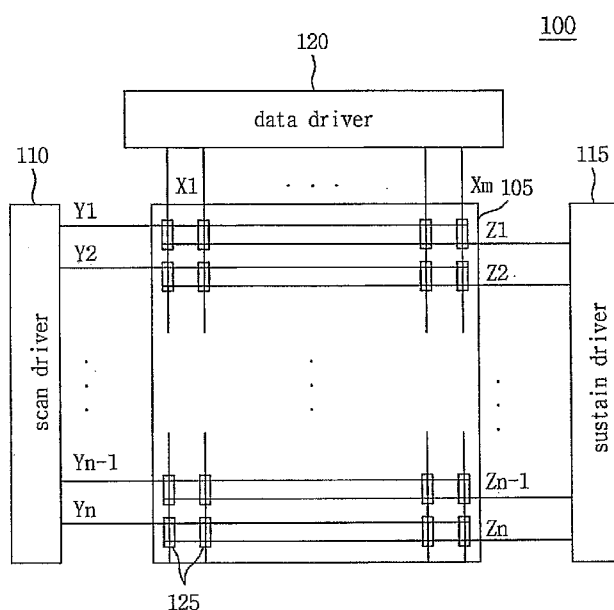
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(54) Title: PLASMA DISPLAY APPARATUS AND METHOD OF DRIVING



(57) Abstract: A plasma display apparatus includes a data driver and a plasma display panel having a first address electrode and a second address electrode. The data driver is configured to initiate a change in a voltage value of a first data signal supplied to the first address electrode at a first initiation time, and to initiate a change in a voltage value of a second data signal supplied to the second address electrode at a second, different initiation time. Each of the data signals gradually changes from a first data voltage to a second data voltage during a respective first period, maintains at the second data voltage during a respective second period, and gradually changes from the second data voltage to a third data voltage during a respective third period.

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Description

PLASMA DISPLAY APPARATUS AND METHOD OF DRIVING

Technical Field

- [1] This document is related to driving a plasma display apparatus.

Background Art

- [2] A plasma display apparatus includes a plasma display panel having electrodes and a driver that supplies driving signals to the electrodes. The plasma display panel includes discharge cells partitioned by a barrier rib. Phosphor is formed within the discharge cells.
- [3] When certain driving signals are supplied to the electrodes of the plasma display panel, a sustain discharge is generated within a discharge cell. As a result of the sustain discharge, discharge gas in the discharge cell generates vacuum ultraviolet rays that cause the phosphor to emit light.
- [4] Before an occurrence of the sustain discharge, a reset discharge initializing wall charges of the discharge cell, and an address discharge selecting a discharge cell where a sustain discharge will occur are generated within the discharge cell.

Disclosure of Invention

Brief Description of the Drawings

- [5] FIG. 1 is a block diagram of a plasma display apparatus;
- [6] FIG. 2 is a perspective view of a plasma display panel of the plasma display apparatus of FIG. 1;
- [7] FIG. 3 is a timing diagram of signals of the plasma display apparatus of FIG. 1;
- [8] FIG. 4 is a graph of driving signals of the plasma display apparatus of FIG. 1;
- [9] FIG. 5 is a graph of a scan signal and a data signal of the plasma display apparatus of FIG. 1;
- [10] FIG. 6 is a graph of data signals of the plasma display apparatus of FIG. 1;
- [11] FIG. 7 is a schematic diagram of electrodes in the plasma display panel of FIG. 2;
- [12] FIG. 8 is a graph of data signals of the plasma display apparatus of FIG. 1;
- [13] FIG. 9 is a circuit diagram of a basic unit of a data driver of the plasma display apparatus of FIG. 1;
- [14] FIG. 10 is a switching timing diagram of the data driver of FIG. 9;
- [15] FIG. 11 and FIG. 12 are images displayed on the plasma display apparatus of FIG. 1; and
- [16] FIGS. 13, 14 and 15 are graphs of data signals.

Mode for the Invention

- [17] FIG. 1 illustrates a plasma display apparatus 100 that includes a plasma display panel

105, a scan driver 110, a sustain driver 115, and a data driver 120.

- [18] The plasma display panel 105 includes discharge cells 125, scan electrodes $Y_1, \dots, Y_n$, sustain electrodes $Z_1, \dots, Z_n$, and address electrodes $X_1, \dots, X_m$, including first and second address electrodes X_1 and X_2 that are adjacent to each other.
- [19] The scan driver 110 supplies, to the scan electrodes $Y_1, \dots, Y_n$, a reset signal initializing the wall charge state of discharge cells, a scan signal selecting discharge cells to emit light, and a sustain signal that causes the emission of light from the selected discharge cells.
- [20] The sustain driver 115 supplies, to the sustain electrodes $Z_1, \dots, Z_n$, a sustain bias signal that helps the selection of the discharge cells and a sustain signal that causes emission of light from the selected discharge cells.
- [21] The data driver 120 supplies data signals to the address electrodes $X_1, \dots, X_m$ at different supply time points. The data signals gradually rise to a data voltage during a first period, are maintained at the data voltage during a second period, and gradually fall from the data voltage during a third period. The address electrodes include a first address electrode and a second address electrode. The data driver 120 supplies a first data signal to the first address electrode, and a second data signal to the second address electrode. The supply start time point of the second data signal, which is the point in time when the first data signal starts to rise in the first period, is different from the supply start time point of the first data signal. The first data signal or the second data signal gradually rises to the data voltage during a first period, is maintained at the data voltage during a second period, and gradually falls from the data voltage during a third period.
- [22] The scan driver 110 supplies a scan signal corresponding to the first data signal and the second data signal.
- [23] FIG. 2 illustrates a perspective view of an exemplary plasma display panel of a plasma display apparatus. As illustrated in FIG. 2, the plasma display panel 105 includes a front panel 200 and a rear panel 210. The front panel 200 includes a front substrate 201 on which a scan electrode 202 and a sustain electrode 203 are formed. The rear panel 210 includes a rear substrate on which address electrodes 213 crossing the scan electrode 202 and the sustain electrode 203 are formed.
- [24] An upper dielectric layer 204 covers the scan electrode 202 and the sustain electrode 203.
- [25] The scan electrode 202 and the sustain electrode 203 may include transparent electrodes 202a and 203a and bus electrodes 202b and 203b. The transparent electrodes 202a and 203a are made of Indium Tin Oxide. The bus electrodes 202b and 203b improve the electric conductivity.
- [26] Alternatively, the scan electrode 202 and the sustain electrode 203 of FIG. 2 may

includes only the bus electrodes 202b and 203b.

- [27] The upper dielectric layer 204 limits a discharge current of the scan electrode 202 and the sustain electrode 203, and insulates the scan electrode 202 and the sustain electrode 203. The upper dielectric layer 204 comprises a glass material including R_2O and metal oxide MO_2 .
- [28] The metal oxide MO_2 includes at least one of MnO_2 , CeO_2 , SnO_2 , or SbO_2 , each of which has 3 or 4 valence. R_2O includes at least one of Li_2O , Na_2O , K_2O , Rb_2O , Cs_2O , Cu_2O , or Ag_2O . MO_2 prevents Ag ions or Cu ions of the scan electrode 202 or the sustain electrode 203 from diffusing throughout the upper dielectric layer 204. Accordingly, a discoloration of the upper dielectric layer 204 is prevented. MO_2 may range from 0.5 wt% to 10 wt% of the total weight of the dielectric layer. When MO_2 ranges from 0.5 wt% to 10 wt% of the total weight of the dielectric layer, R_2O decreases the softening point of a glass, and improves the liquidity of the glass.
- [29] A protective layer 205 is positioned on the upper dielectric layer 204, and improves a discharge condition. The protective layer is formed by the disposition of magnesium oxide MgO .
- [30] The address electrodes 213 supply data signals to discharge cells. A lower dielectric layer 215 covers the address electrodes 213, and insulates the address electrodes 213.
- [31] The lower dielectric layer 215 includes PbO , SiO_2 , B_2O_3 , Al_2O_3 and CuO . CuO may range from 0.2 wt% to 0.4 wt% of the total weight of the lower dielectric layer 215. CuO decreases the viscosity of a dielectric paste. Accordingly, when CuO ranges from 0.2 wt% to 0.4 wt% of the total weight of the lower dielectric layer 215, CuO prevents the generation of bubbles inside the lower dielectric layer 215, and thereby decreases the necessary driving voltage. As a result of the decrease of the driving voltage, noise and electromagnetic interference are reduced.
- [32] A stripe type barrier rib or a well type barrier rib 212 is formed on the lower dielectric layer 215. The barrier rib partitions discharge cells. A discharge gas is filled in the discharge cells. A phosphor 214 is formed within the discharge cells.
- [33] FIG. 3 explains an exemplary method of implementing gray scales in the plasma display apparatus.
- [34] As shown in FIG. 3, in order to implement the gray scale, each image frame is divided into sub-fields SF1 to SF8. Each sub-field is also divided into a reset period for initializing all of the discharge cells, an address period for selecting discharge cells to emit light, and a sustain period for emitting light from the selected discharge cells. The sub-fields have different durations of the sustain periods. The grey scale of each discharge cell is implemented by selecting some sub-fields to emit light with proper durations of the sustain periods. For example, if it is desired to display an image with 256 gray scales, a frame period (16.67ms) corresponding to 1/60 of a second is divided

into eight sub-fields SF1 to SF8.

- [35] The time duration and the number of sustain pulses that are associated with each sustain period increase by the ratio of 2^n (where, $n=0,1,2,3,4,5,6,7$) for each sub-field SF1 to SF8. For example, the duration of the sustain period of sub-field SF2 is twice the duration of the sustain period of sub-field SF1. As such, since the duration of the sustain period varies from one sub-field to the next, the gray scale of a discharge cell is achieved by controlling which sustain periods are to be used to emit light from the discharge cell, i.e., by controlling the number of the sustain discharges that are realized in the discharge cell.
- [36] FIG. 4 illustrates driving signals of the plasma display apparatus.
- [37] The scan driver 110 supplies, to the scan electrode, a rising ramp signal gradually rising to a sum voltage V_s+V_{setup} , which is the summation of a sustain voltage V_s and a setup voltage V_{setup} , during a setup period of a reset period. The sustain voltage V_s is the highest voltage of a sustain signal.
- [38] The rising ramp signal generates a weak dark discharge, i.e., a setup discharge, in the discharge cells. As a result of the setup discharge, wall charges sufficient for the generation of an address discharge are accumulated within the discharge cells. The slope of the rising ramp signal may range between $0.0005V/nsec$ and $0.005V/nsec$.
- [39] The scan driver supplies a falling ramp signal gradually falling from a positive voltage, which is lower than the sum voltage V_s+V_{setup} , during a setdown period. The falling ramp signal generates a weak erase discharge, i.e., a setdown discharge, within the discharge cells. As a result of the setdown discharge, some of the wall charges accumulated within the discharge cells are erased. The slope of the falling ramp signal may range between $-0.0005V/nsec$ and $-0.005V/nsec$.
- [40] The scan driver 110 supplies to the scan electrode a scan signal which falls from a scan reference voltage V_{sc} to a scan voltage $-V_y$, is maintained at the scan voltage $-V_y$, and rises to the scan reference voltage V_{sc} .
- [41] The data driver 120 supplies a first data signal and a second data signal, which correspond to the scan signal, to the first address electrode and the second address electrode respectively. The first and second address electrodes are adjacent to each other. The first data signal and the second data signal are supplied at different supply time points t_1, t_2 . The first data signal or the second data signal gradually rises to a data voltage V_d during a first period, is maintained at the data voltage V_d during a second period, and gradually falls from the data voltage V_d during a third period.
- [42] The durations of the first and the third periods may be between 5% and 20% of the duration of the second period. The durations of the first and the third periods may be between 50nsec and 200nsec. The slope of the data signal during the first period may range between $0.1V/nsec$ and $1V/nsec$. The slope of the data signal during

the third period may range between -0.1 V/nsec and -1 V/sec .

- [43] When the first data signal or the second data signal as above is supplied, noise and Electro Magnetic Interference due to a voltage variation are reduced because the voltage on the first address electrode and the second address electrode varies gradually.
- [44] Also, the supply of the first and second data signals at different supply start time points t_1 and t_2 reduces noise. When the data signals are supplied at the same supply start time point, the voltage difference between the data signals and the scan signal increases noise. On the other hand, when the data signals are supplied at the different supply start time points t_1 and t_2 , noises generated by the voltage difference of the data signals and the scan signal are spread in time, and the whole noise is reduced.
- [45] When the difference Δt between the supply start time points t_1 and t_2 of the data signals may range from 0.2 times to 1 times the duration of the first period, the noise and the electro magnetic interference are effectively reduced.
- [46] When the difference Δt between the supply start time points t_1 and t_2 of the data signals ranges from 0.4 times to 0.8 times the duration of the first period, the scan signal and the data signals sufficiently overlap for a stable address discharge, and at the same time, the noise and the electro magnetic interference are reduced.
- [47] When the difference Δt between the supply start time points t_1 and t_2 ranges from 10 ns to 300 ns, the noise and the electro magnetic interference are reduced, while preventing an excessive increase of the address period.
- [48] The supply start time points t_1 and t_2 of the data signals may be different from the supply start time point t_3 of the scan signal. Then, the noise generated between the scan electrode and the first address electrode or the second electrode is reduced.
- [49] The sustain driver 115 supplies a sustain bias voltage V_{zb} to the sustain electrode during the address period. The sustain bias voltage V_{zb} prevents the occurrence of an erroneous discharge generated by the interference between the sustain electrode and the scan electrode during the address period.
- [50] The scan driver 110 and the sustain driver 115 supply sustain signals to the scan electrode and the sustain electrode during the sustain period. As a result of the supply of the sustain signals, the discharge cells selected during the address period emit light. In another implementation, the scan driver 110 may supply a sustain signal swinging from a positive sustain voltage to a negative sustain voltage to the scan electrode and the sustain driver 115 may supply a ground level voltage to the sustain electrode during the sustain period.
- [51] FIG. 5 illustrates exemplary waveforms of the scan signal and the data signal. As illustrated in FIG. 5, the scan signal may gradually fall from the scan reference voltage V_{sc} to the scan voltage $-V_y$ during a fourth period. The slope of the data signal during the first period may be different from that of the scan signal during the fourth period.

- [52] When the voltage on the scan electrode and the voltage on the address electrode change gradually and the slope of the scan signal during the fourth period is different from the slope of the data signal during the first period, noise is reduced.
- [53] FIG. 6 illustrates supply start time points of data signals supplied to address electrodes. As illustrated in FIG. 6, data signals are applied to address electrodes X1, X2, X3 and X4 at different supply start time points t_0 , t_1 , t_2 and t_3 , respectively. As a result, the noise is reduced.
- [54] The plasma display panel of the plasma display apparatus may include address electrodes which are divided into address electrode groups. Data signals are supplied simultaneously to address electrodes in the same address electrode group. However, data signals are supplied at different times to address electrodes in different address electrode groups. FIG. 7 illustrates an exemplary grouping of address electrodes. The plasma display panel of FIG. 7 includes 4 address electrode groups AEG1 to AEG4. The number of address electrodes in each address electrode group may be same or different.
- [55] FIG. 8 illustrates first and second data signals. As illustrated in FIG. 8, a first data signal is supplied to address electrodes of address electrode group AEG1 at a supply start time point t_1 , and a second data signal is supplied to address electrodes of address electrode group AEG2 at a supply start time point t_2 . By supplying the data signals at different times to address electrodes of different address electrode groups, the noise generated between the scan electrodes and the address electrodes is reduced.
- [56] FIG. 9 illustrates an exemplary structure of the basic unit 500 of the data driver of the plasma display apparatus and FIG. 10 illustrates a switching timing diagram of the data driver of FIG. 9. The data driver includes basic units for each address electrode.
- [57] As illustrated in FIG. 9, the basic unit 500 of the data driver of the plasma display apparatus includes a data drive integrated circuit 530 connected to the first address electrode or the second address electrode, a data voltage supply unit 510 for supplying a data voltage V_d to the first address electrode or the second address electrode through the data drive integrated circuit 530, and an energy recovery unit 520 for gradually increasing a voltage of the first address electrode or the second address electrode to the data voltage V_d or decreasing the voltage of the first address electrode or the second address electrode from the data voltage V_d .
- [58] The operation of the data driver basic unit 500 in FIG. 9 to generate a data signal is explained below with reference to FIG. 10. As illustrated in FIG. 10, when a switch Q2 and a switch Qt are turned on during the first period, an energy stored at a capacitor C is supplied to the first address electrode or the second address electrode through the switch Q2, an inductor L and the switch Qt. The inductor L forms a resonance, and the voltage on the first address electrode or the second address electrode gradually rises

from a ground level voltage GND to a data voltage Vd.

- [59] When a switch Q1 and the switch Qt are turned on and the other switches are turned off during the second period, the data voltage Vd is supplied to the first address electrode or the second address electrode. A voltage on the first address electrode or the second address electrode is maintained at the data voltage Vd.
- [60] When a switch Q3 and the switch Qt are turned on and the other switches are turned off during the third period, the capacitor C recovers the energy from the first address electrode or the second address electrode through the switch Qt, the inductor L, and the switch Q3. The inductor L forms a resonance, and the voltage on the first address electrode or the second address electrode gradually falls from the data voltage Vd to the ground level voltage GND.
- [61] When the switch Qb is turned on and the other electrodes are turned off at the end of the third period, the ground level voltage GND is supplied to the first address electrode or the second address electrode.
- [62] Diodes D1, D2, D3, Dt and Db of FIG. 9 are body diodes of the switches Q1, Q2, Q3 Qt and Qb respectively. Diodes D5 and D6 cut off a reverse current.
- [63] FIG. 11 and FIG. 12 are screen images displayed by the plasma display apparatus to explain the relationship between the switching operation and the load of the data driver basic unit.
- [64] FIG. 11 illustrates a full black image displayed by the plasma display apparatus. In order to display the full black image of FIG. 11, the switches Qb and Qt of the data drive integrated circuit 530 in FIG. 9 respectively maintains a turn-on state and a turn-off state. Thus, the switching operation of the data driver basic unit is not performed, and the load substantially is equal to 0. That is to say, a switching frequency is substantially equal to 0, and the load substantially is equal to 0.
- [65] FIG. 12 illustrates a lattice pattern image displayed by the plasma display apparatus. In order to display the lattice pattern image, the switching frequency of the switch Qt and the switch Qb of FIG 9 and the load of the data driver basic unit 500 become the maximum. The load is proportional to the the switching frequency.
- [66] As the switching frequency increases, a noise and an electro magnetic interference increase. In order to decrease the noise and the electro magnetic interference, the data driver 120 may supply the data signals to the first address electrode and the second address electrode at different supply time points according to the load of each address electrode, which is proportional to the switching frequency of the data driver basic unit for each address electrode.
- [67] The supply time point of the data signal may be adjusted based on the load. For example, as illustrated in FIG. 13, when the load is less than a threshold, a supply start time point t1 of the first data signal for the first address electrode is substantially the

same as a supply start time point t2 of the second data signal for the second address electrode. FIG. 13 may correspond to FIG. 11.

[68] For example, as illustrated in FIG. 14, when the load is greater than the threshold, a supply start time point t1 of the first data signal for the first address electrode is earlier than a supply start time point t2 of the second data signal for the second address electrode. When the difference of the supply start time points t1 and t2 ranges from 10 ns to 300 ns, the noise and the electro magnetic interference are reduced. To implement this, the data driver basic unit 500 of FIG. 9 may further include a detection circuit to detect the load of the electrode and adjust the supply start time point accordingly. FIG. 14 may correspond to FIG. 12.

[69] FIG. 15 illustrates an exemplary relationship between the first period of the data signal and the load. The duration and the supply start time point of the data signal may be adjusted based on the load. For example, as illustrated in FIG. 15, the first period of the data signal for a high load is shorter than that for a low load. When the duration of the first period of a data signal for the lowest load ranges from 1.5 times to 5 times the duration of the first period of a data signal for the highest load, the noise and the electro magnetic interference are reduced. Therefore, a stable address discharge is generated and a driving efficiency improves. When the duration of the first period for the lowest load ranges from 2 times to 4 times the duration of the first period for the highest load, an excessive increase of the address period is prevented. In order to implement these features, the data driver basic unit 500 of FIG. 9 may further include a detection circuit to detect the load and adjust the duration of the first period of the data signal accordingly.

[70] Other implementations are within the scope of the following claims.

Claims

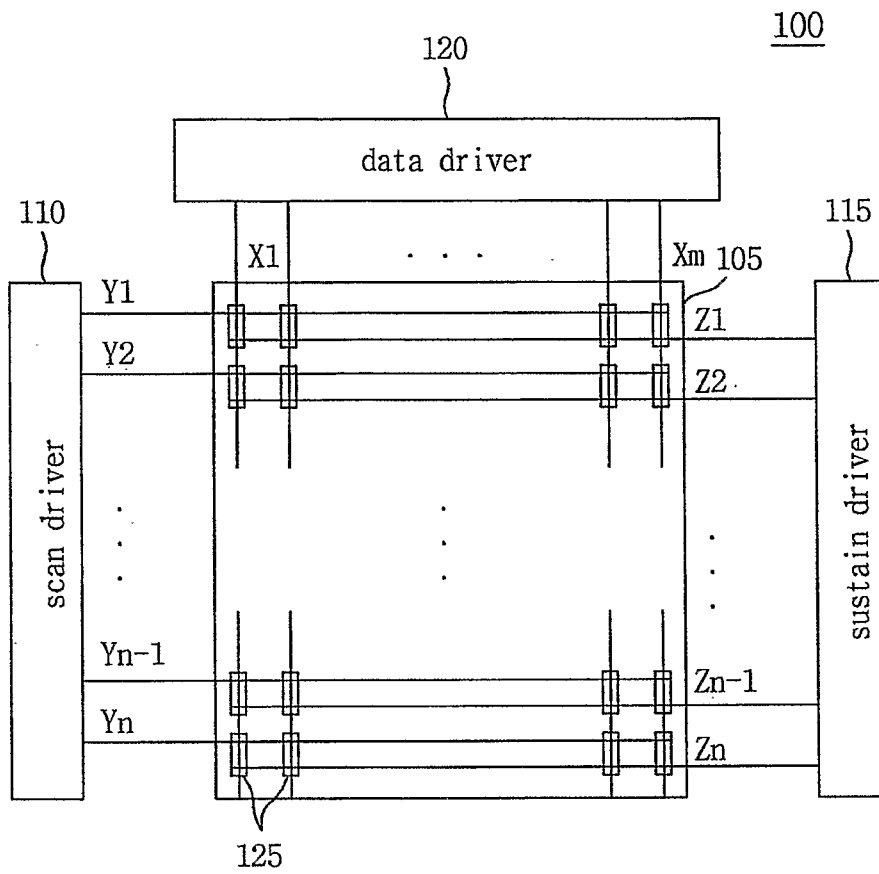
- [1] A plasma display apparatus comprising:
a plasma display panel having a first address electrode and a second address electrode; and
a data driver initiating a change in a voltage value of a first data signal supplied to the first address electrode at a first initiation time and initiating a change in a voltage value of a second data signal supplied to the second address electrode at a second, different initiation time, with each of the data signals gradually changing from a first data voltage to a second data voltage during a respective first period, maintaining at the second data voltage during a respective second period, and gradually changing from the second data voltage to a third data voltage during a respective third period.
- [2] The plasma display apparatus of claim 1, wherein the first data voltage and the third data voltage are substantially the same.
- [3] The plasma display apparatus of claim 1, wherein the first and second address electrodes are adjacent to each other.
- [4] The plasma display apparatus of claim 1, wherein a duration of the respective first period is between 5% and 20% of a duration of the respective second period.
- [5] The plasma display apparatus of claim 1, wherein a slope of each of the data signals during the respective first period ranges between 0.1V/ns and 1V/ns.
- [6] The plasma display apparatus of claim 1, wherein a difference between the first initiation time and the second initiation time ranges from 0.2 times to 1 times a duration of the first period for the first data signal.
- [7] The plasma display apparatus of claim 1, further comprising a scan driver, wherein the plasma display panel has a scan electrode, and the scan driver initiates a change in a voltage value of a scan signal supplied to the scan electrode at a third initiation time, the third initiation time being different from the first and second initiation times.
- [8] The plasma display apparatus of claim 1, further comprising a scan driver, wherein the plasma display panel has a scan electrode, wherein the scan driver initiates a change in a voltage value of a scan signal supplied to the scan electrode at a third initiation time, and wherein the scan signal gradually changes from a first scan voltage to a second scan voltage during a fourth period, maintains at the second scan voltage during a fifth period, and gradually changes from the second scan voltage to a third scan voltage during a sixth period.
- [9] The plasma display apparatus of claim 8, wherein a slope of the scan signal during the fourth period is different from a slope of the first data signal during

the first period.

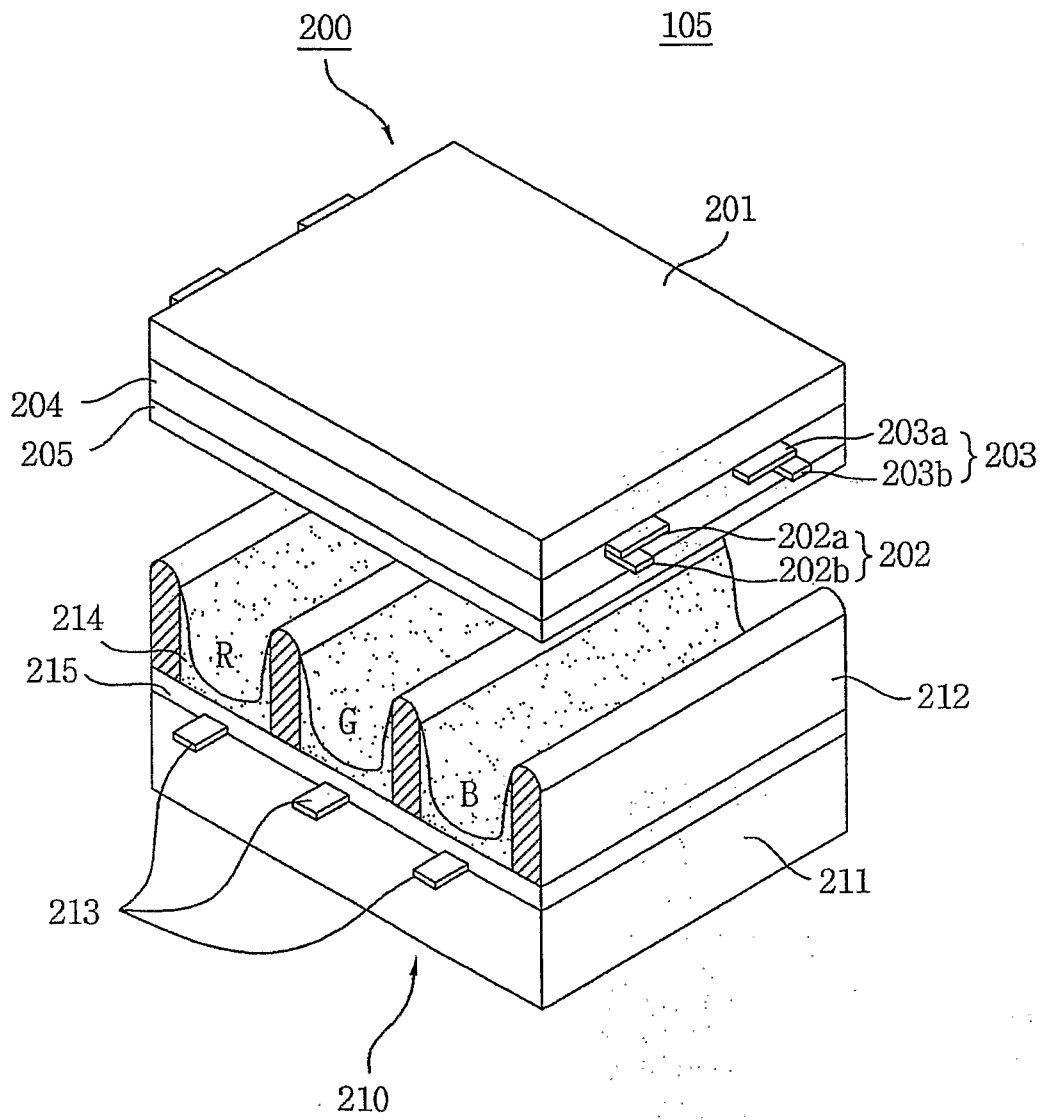
- [10] The plasma display apparatus of claim 1, wherein the data driver comprises a switch, wherein the first initiation time and second initiation time are determined based on a load of the first data electrode and a load of the second data electrode, and wherein the loads are related to a switching frequency of the switch of the data driver.
- [11] The plasma display apparatus of claim 1, wherein the data driver includes:
a data drive integrated circuit connected to the first address electrode;
a data voltage supply unit configured to supply the second data voltage to the first address electrode through the data drive integrated circuit; and
an energy recovery unit configured to supply the first data signal to the first address electrode during the first period and the third period.
- [12] The plasma display apparatus of claim 1, wherein the plasma display panel has a first group of address electrodes that includes the first address electrode and a second group of address electrodes that includes the second address electrode, and wherein the first data signal is supplied to each address electrode of the first group and the second data signal is supplied to each address electrode of the second group.
- [13] The plasma display apparatus of claim 1, wherein the data driver includes a resonant circuit to supply the first data signal to the first address electrode during the first period and the third period.
- [14] The plasma display apparatus of claim 1, wherein a duration of the respective first period varies according to a load of the respective address electrode, the load being proportional to a switching frequency of the data driver.
- [15] The plasma display apparatus of claim 14, wherein the duration of the respective first period is inversely proportion to the load.
- [16] The plasma display apparatus of claim 15, wherein the duration of the respective first period when a minimum load is applied ranges from 1.5 times to 5 times the duration of the respective first period when a maximum load is applied.
- [17] A method of driving a plasma display apparatus having a first address electrode and a second address electrode, the method comprising:
initiating a change in a voltage value of a first data signal supplied to the first address electrode at a first initiation time; and
initiating a change in a voltage value of a second data signal supplied to the second address electrode at a second, different initiation time,
wherein each of the data signals gradually changes from a first data voltage to a second data voltage during a respective first period, maintains at the second data voltage during a respective second period, and gradually changes from the

- second data voltage to a third data voltage during a respective third period.
- [18] The method of claim 17, wherein the first data voltage and the third data voltage are substantially same.
- [19] The method of claim 17, wherein a difference between the first initiation time and the second initiation time ranges from 0.2 times to 1 times a duration of the first period for the first data signal.
- [20] The method of claim 17, further comprising initiating a change in a voltage value of a scan signal supplied to a scan electrode at a third initiation time, the third initiation time being different from the first and second initiation times, wherein the scan signal gradually changes from a first scan voltage to a second scan voltage during a fourth period, maintains at the second scan voltage during a fifth period, and gradually changes from the second scan voltage to a third scan voltage during a sixth period.
- [21] The method of claim 20, wherein a slope of the scan signal during the fourth period is different from a slope of the first data signal during the first period.
- [22] The method of claim 17, further comprising:
supplying the first data signal to a first group of address electrodes including the first address electrode; and
supplying the second data signal to a second group of address electrodes including the second address electrode.

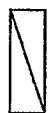
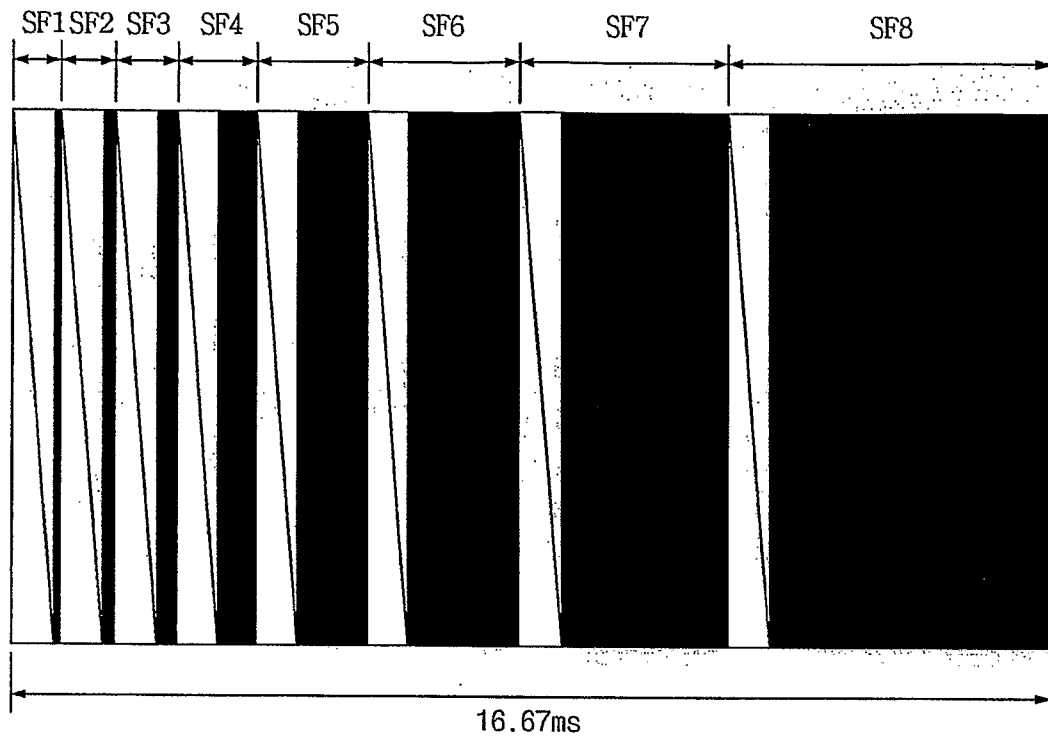
[FIG. 1]



[FIG. 2]



[FIG. 3]

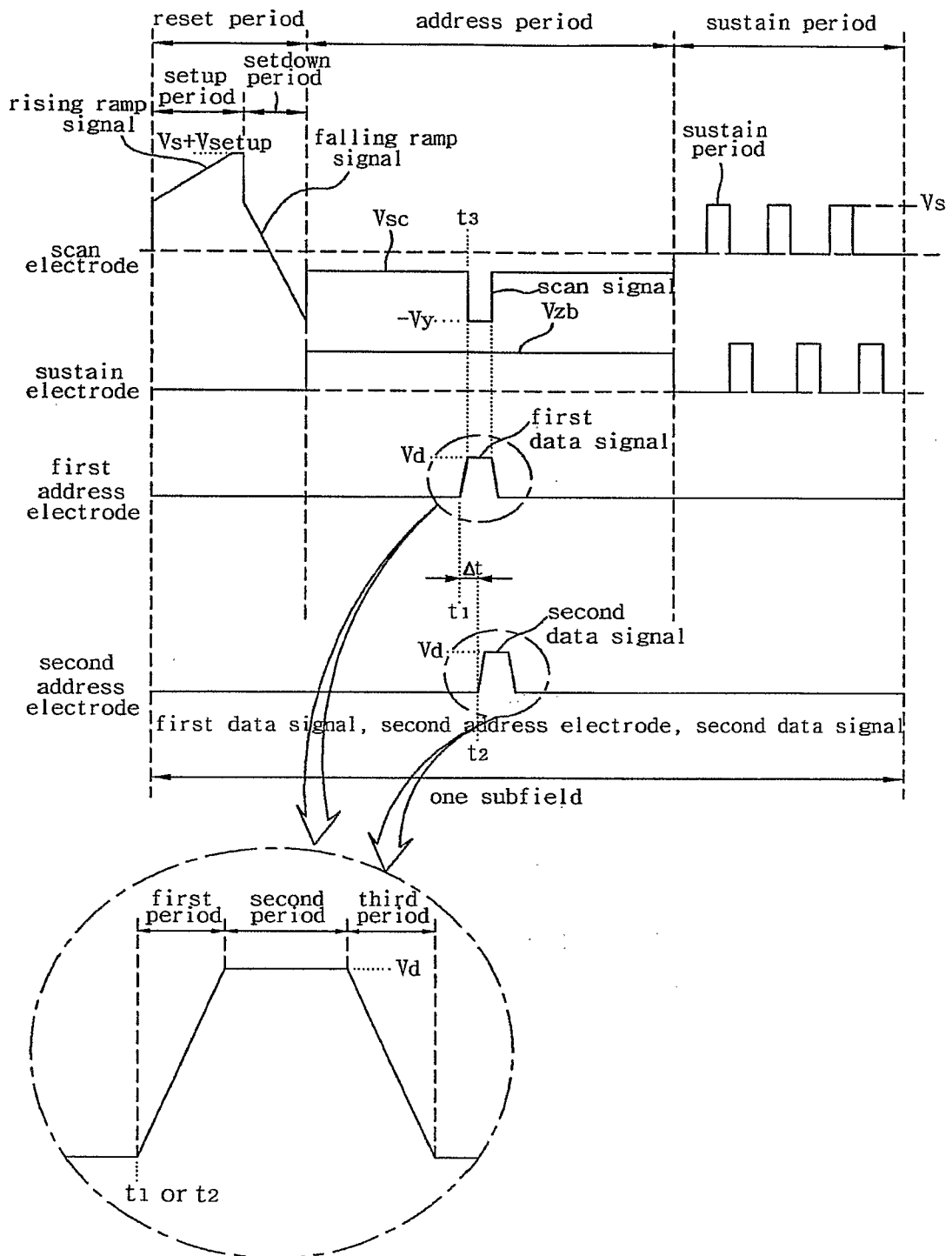


: reset period and address period

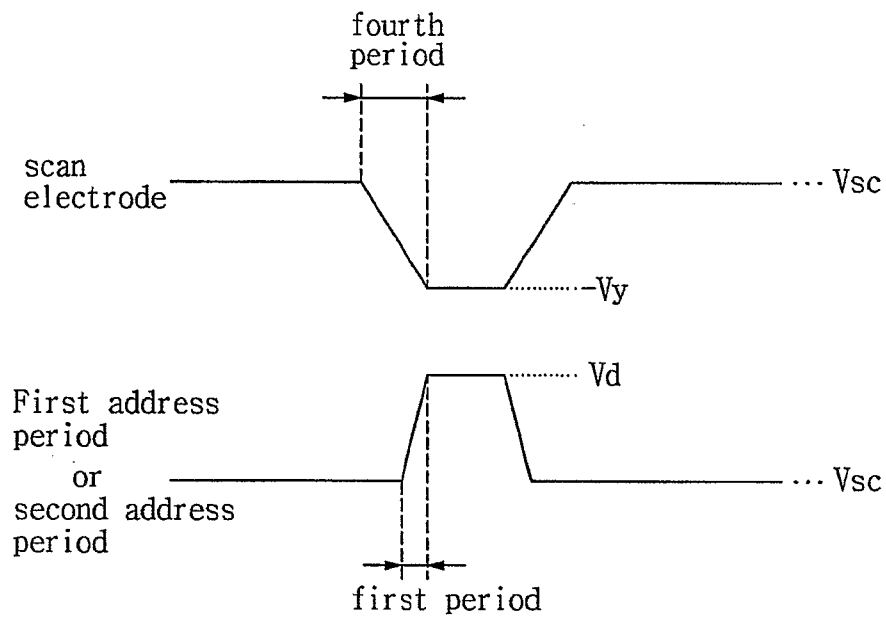


: sustain period

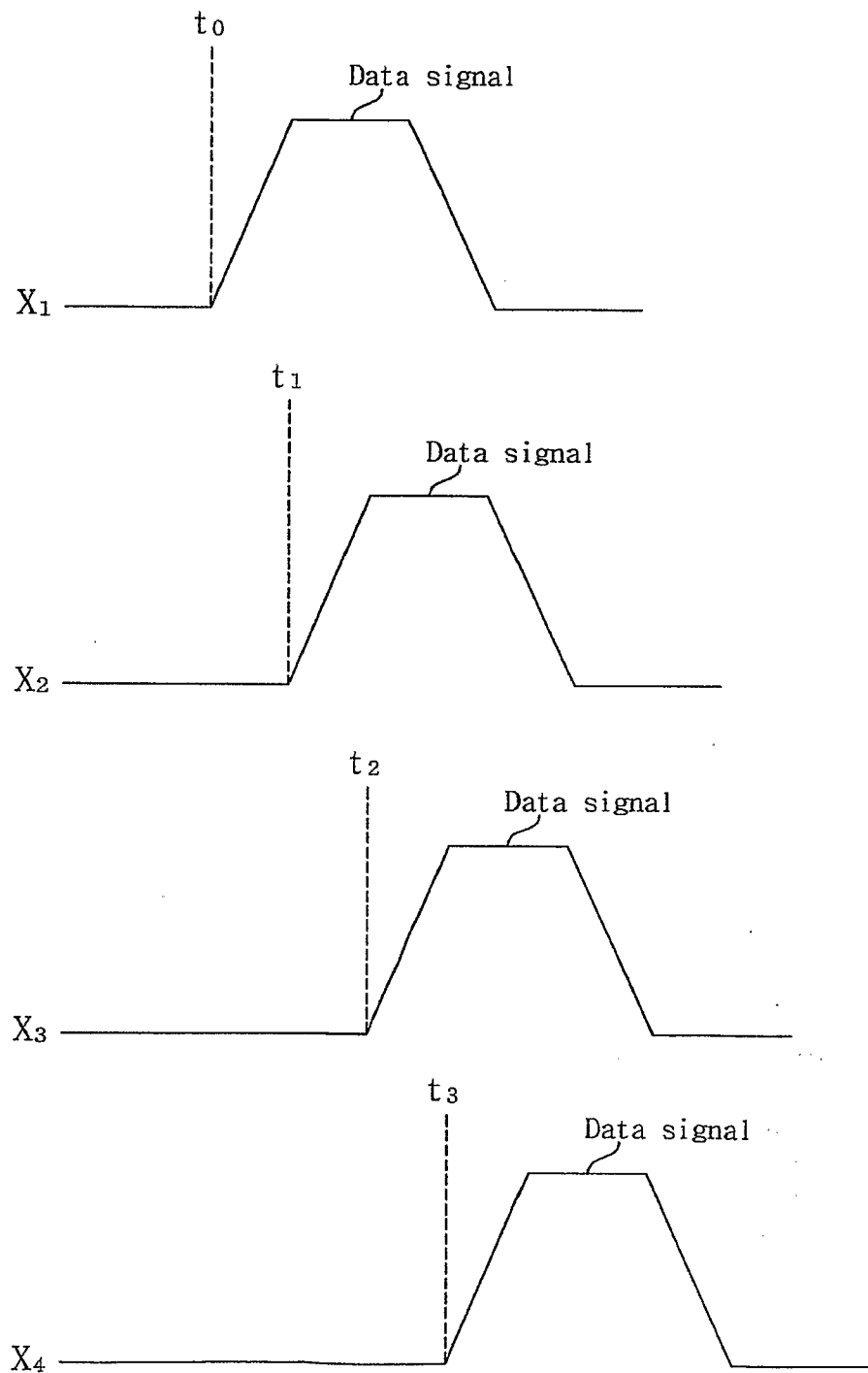
[FIG. 4]



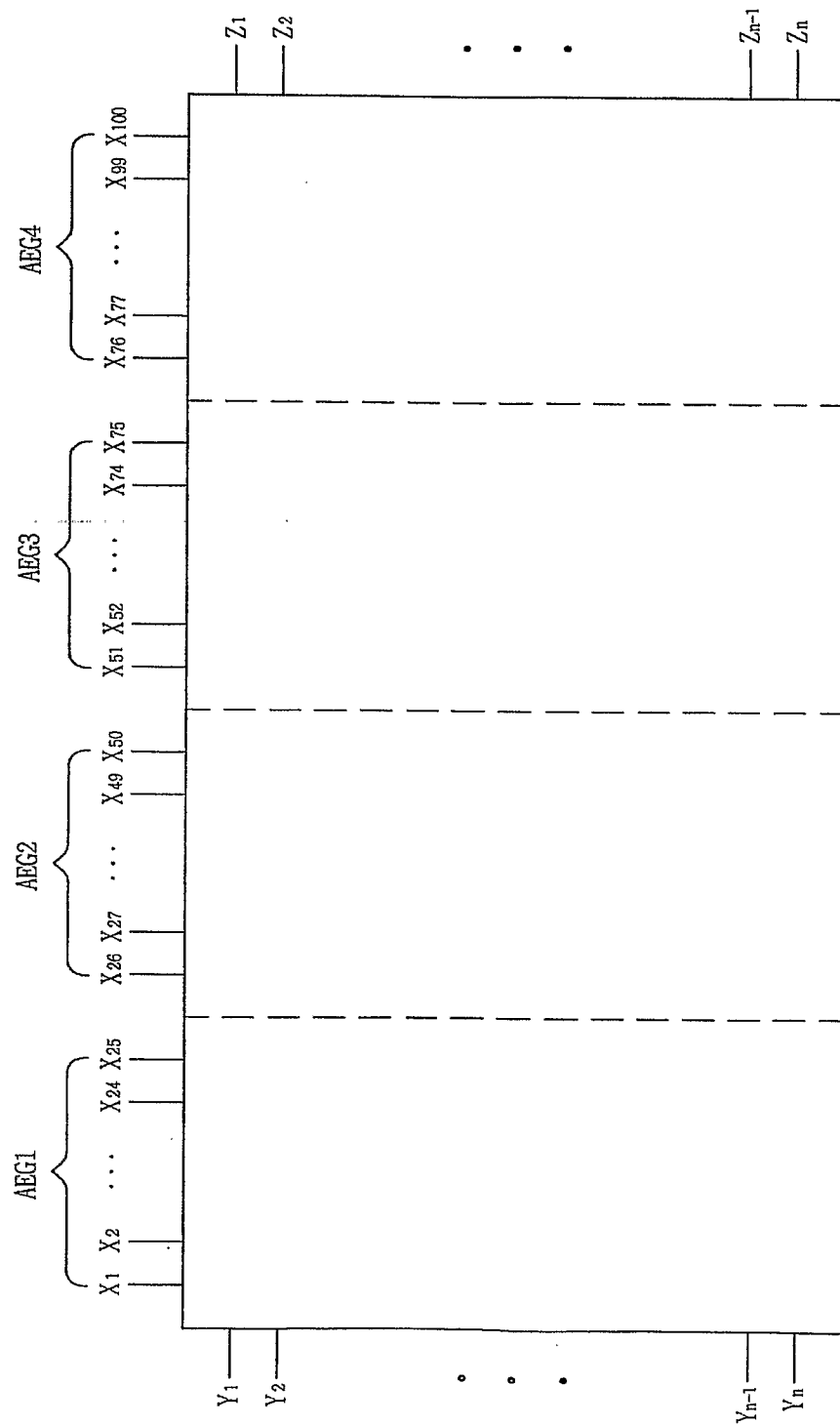
[FIG. 5]



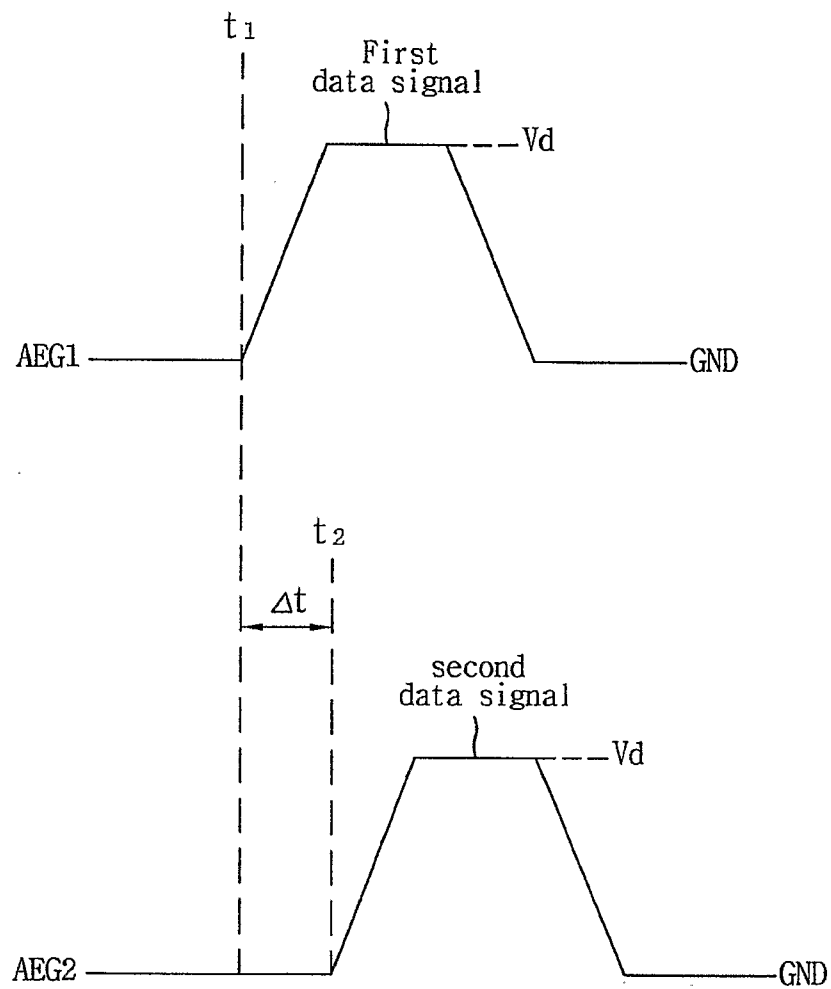
[FIG. 6]



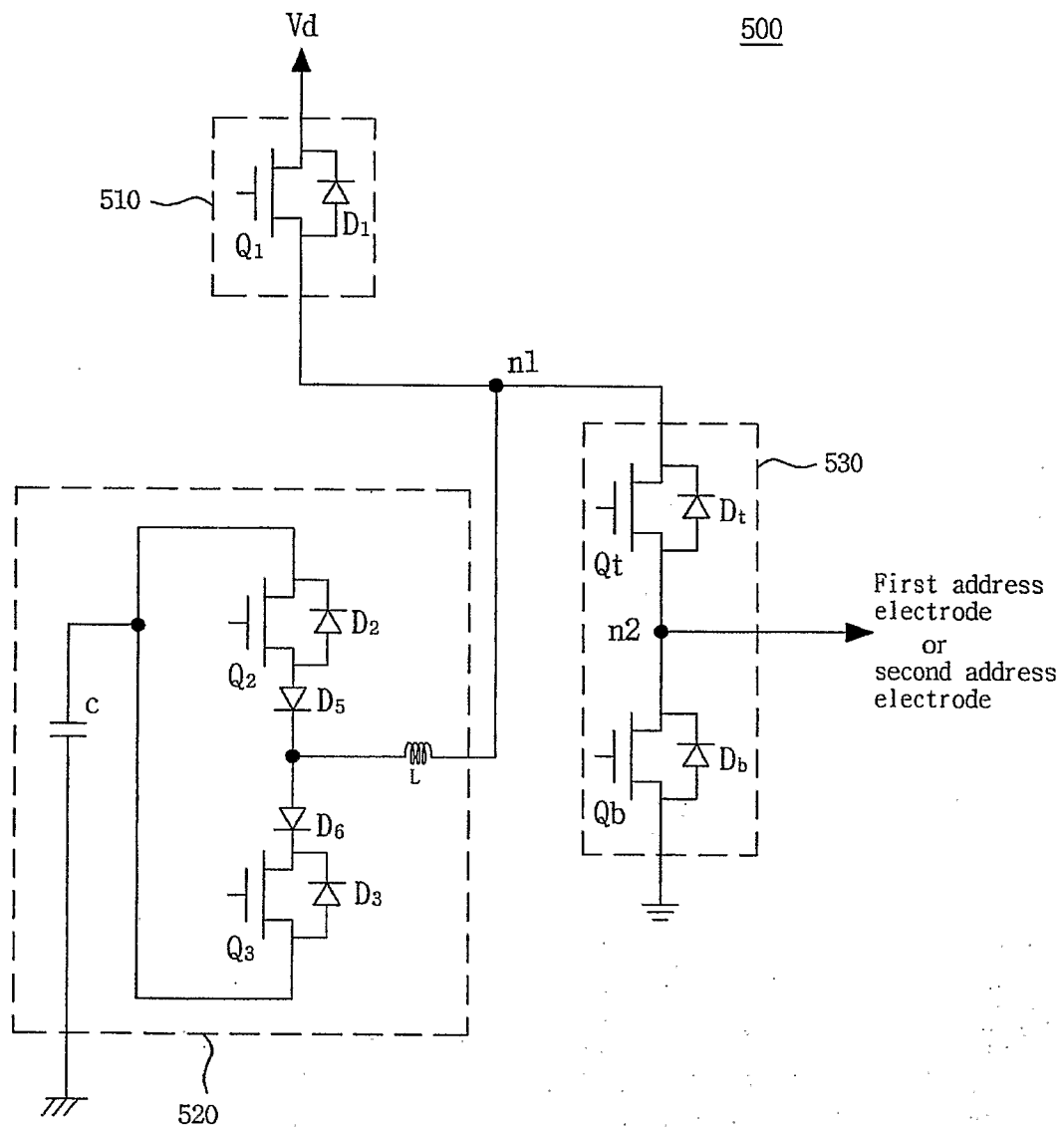
[FIG. 7]



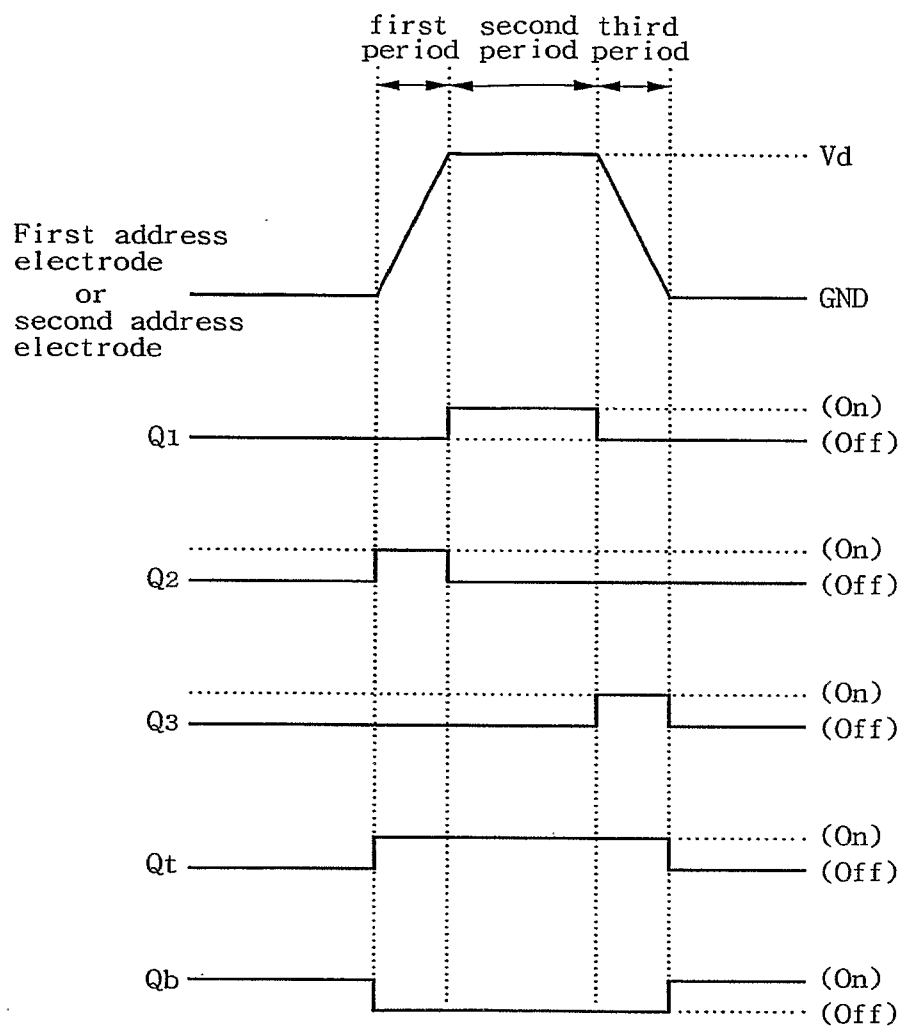
[FIG. 8]



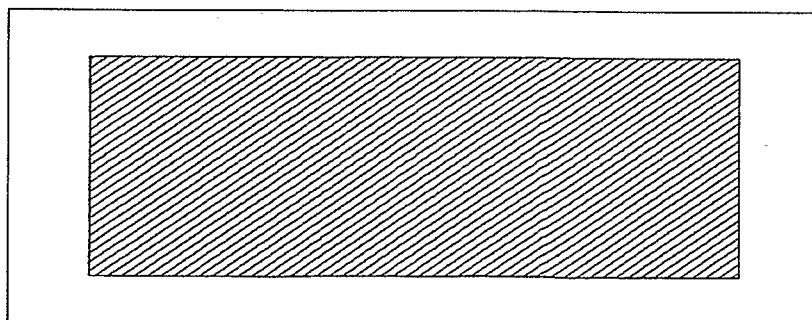
[FIG. 9]



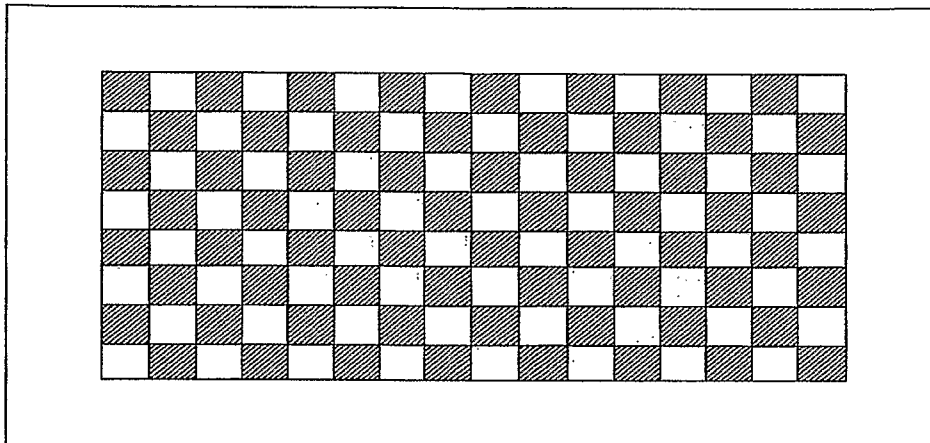
[FIG. 10]



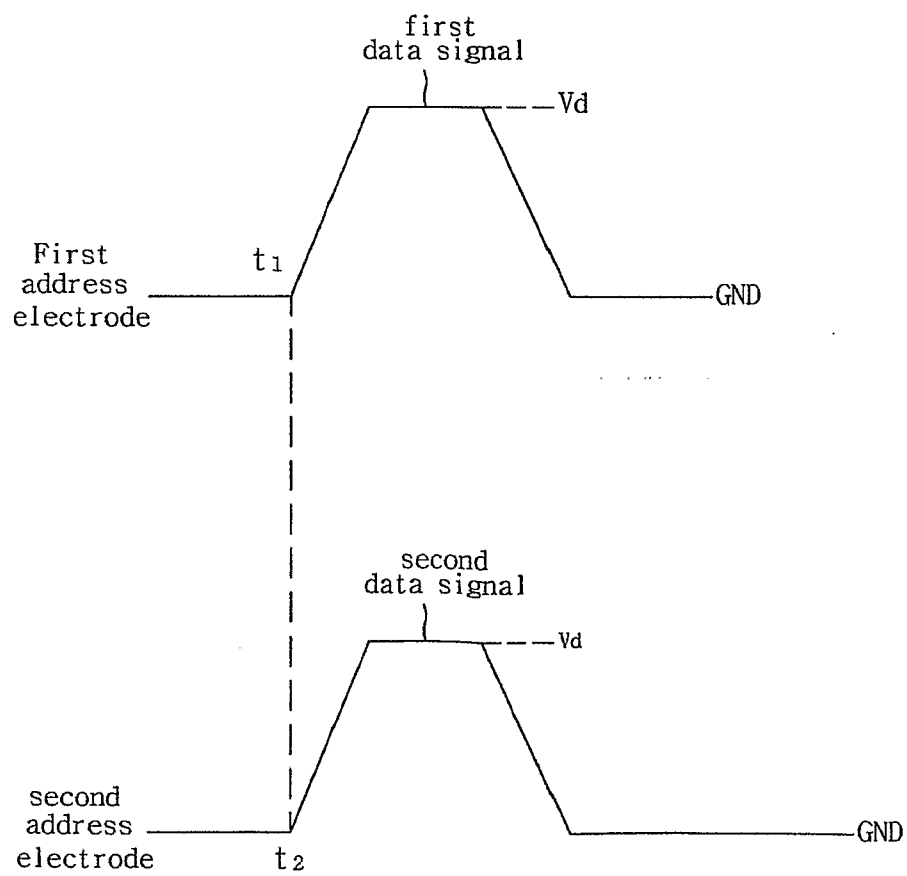
[FIG. 11]



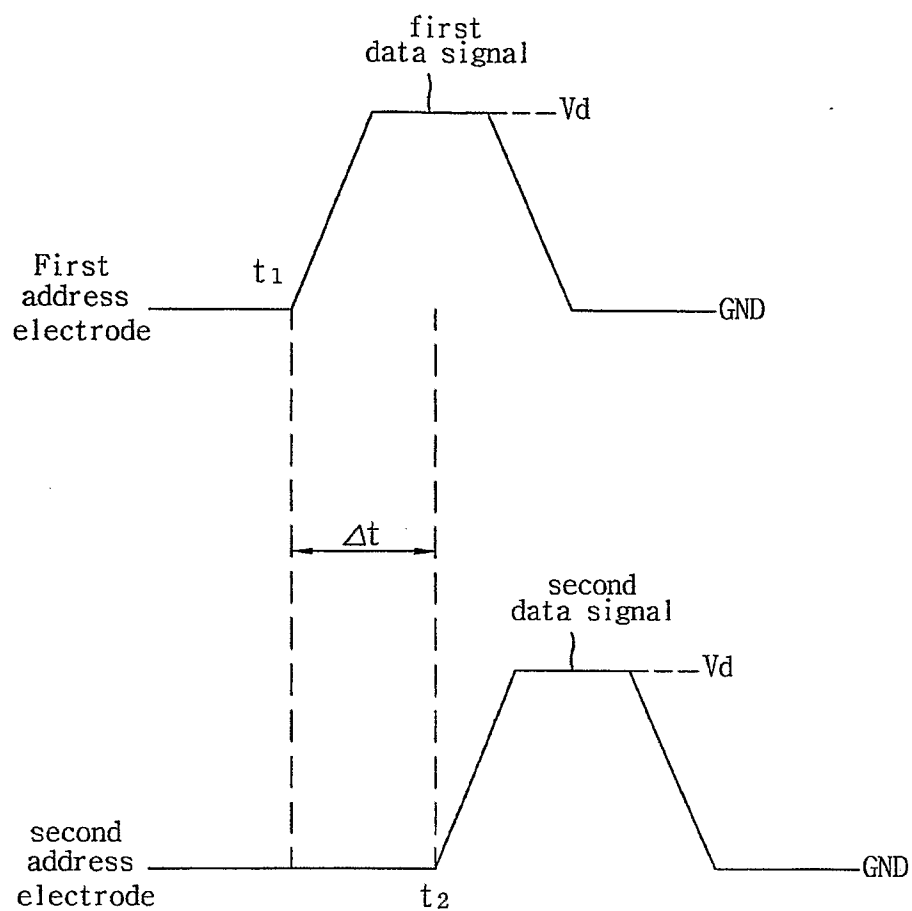
[FIG. 12]



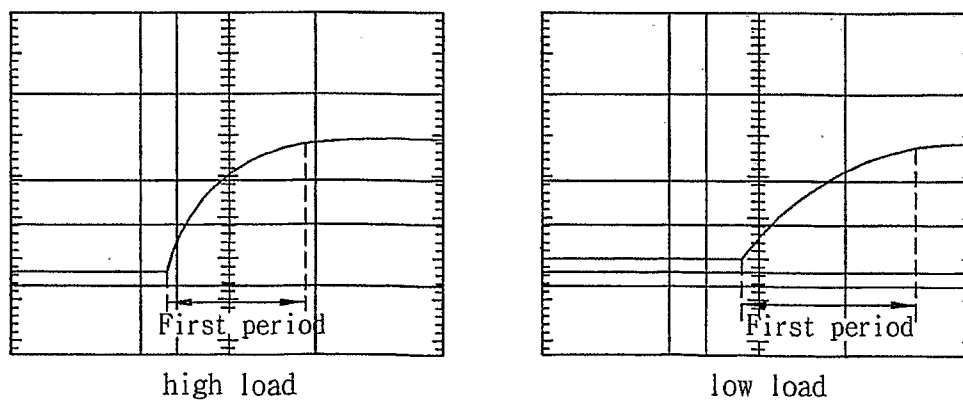
[FIG. 13]



[FIG. 14]



[FIG. 15]



A. CLASSIFICATION OF SUBJECT MATTER**G09G 3/28(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 8 : G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility Models since 1975

Japanese Utility models and applications for Utility Models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKIPASS(KIPO internal) "Keyword: address, data, pulse, delay, load, ER, recovery and similar terms"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/0110706 A1 (MYUNG-KWAN KIM et. al.) 26 MAY 2005 see the abstract, paragraphs [0064]-[0072], claims 1-8, Figs.7-8.	1-10, 12, 17-22
Y	see the abstract, paragraphs [0060]-[0072], claims 1-8, Figs.6-8.	11, 13-14
Y	JP 2004-212699 A (MATSUSHITA ELECTRIC IND. CO., LTD.) 29 JULY 2004 see the abstract, paragraphs [0042]-[0106], claims 1-4.	11, 13-14



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

28 AUGUST 2007 (28.08.2007)

Date of mailing of the international search report

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Telephone No. 82-42-481-8363



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2007/002386Patent document
cited in search reportPublication
datePatent family
member(s)Publication
date

US 2005/0110706 A1

26.05.2005

KR1020050049676 A
CN1619614 A
JP2005157348 A27.05.2005
25.05.2005
16.06.2005

JP 2004-212699 A

29.07.2004

NONE