

Sept. 10, 1968

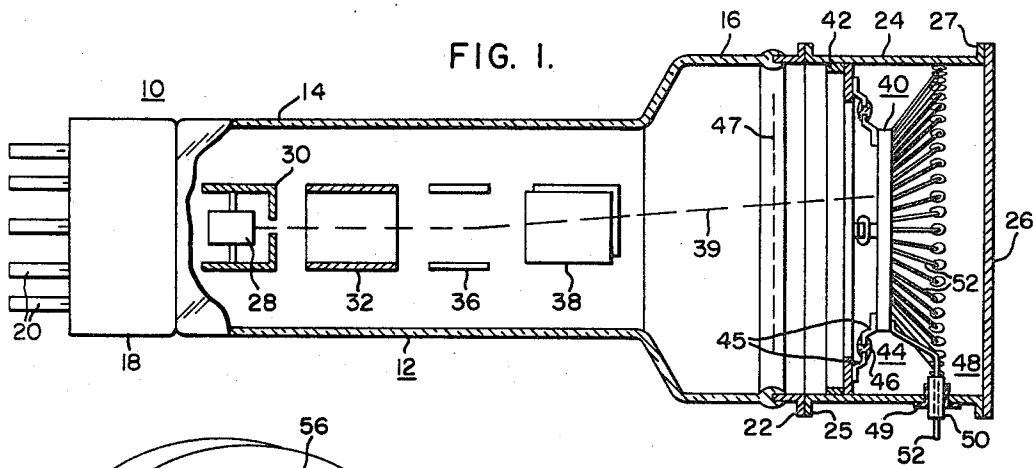
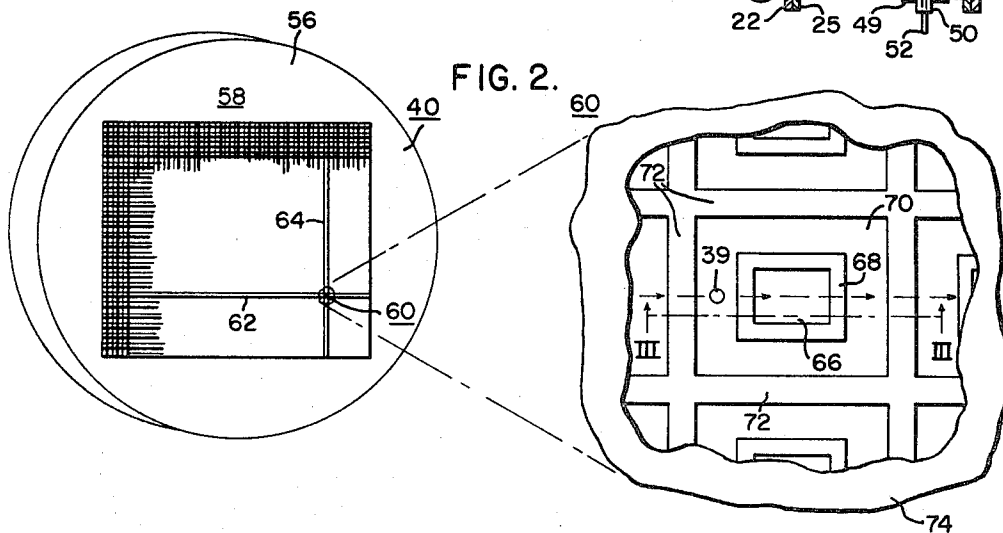
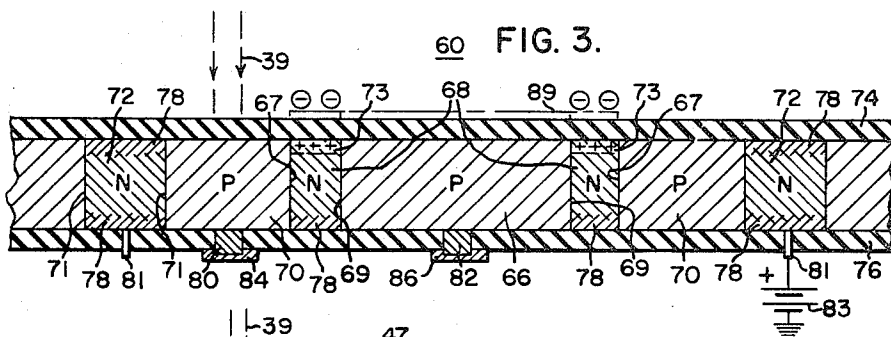
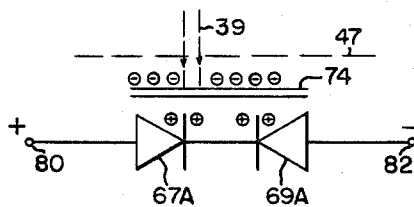
J. R. CRICCHI ET AL

3,401,294

STORAGE TUBE

Filed Feb. 8, 1965

2 Sheets-Sheet 1



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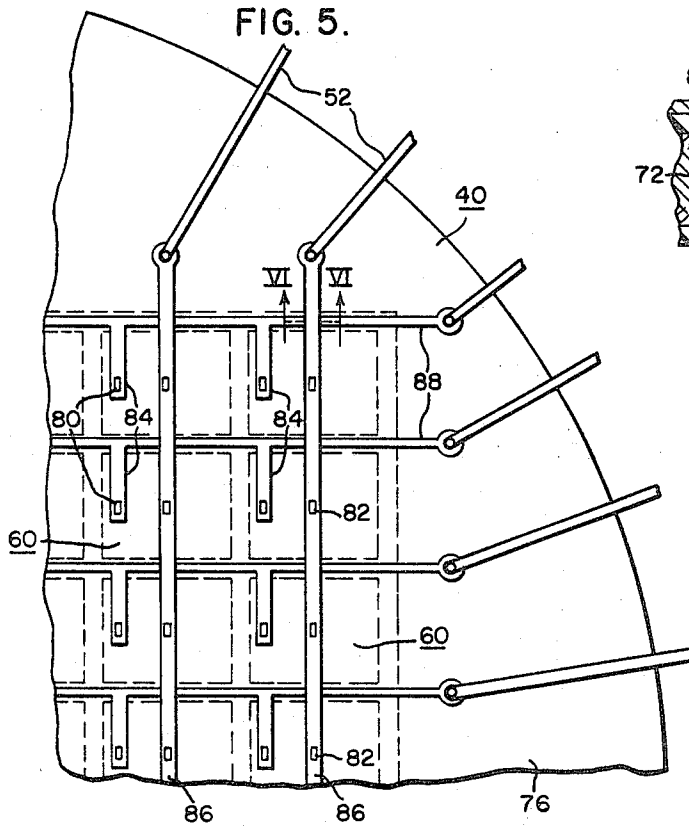
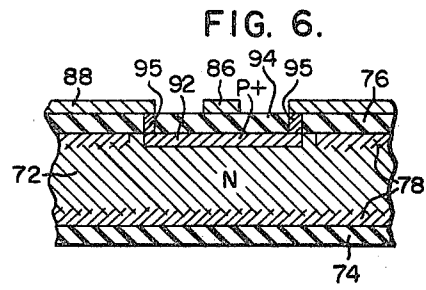
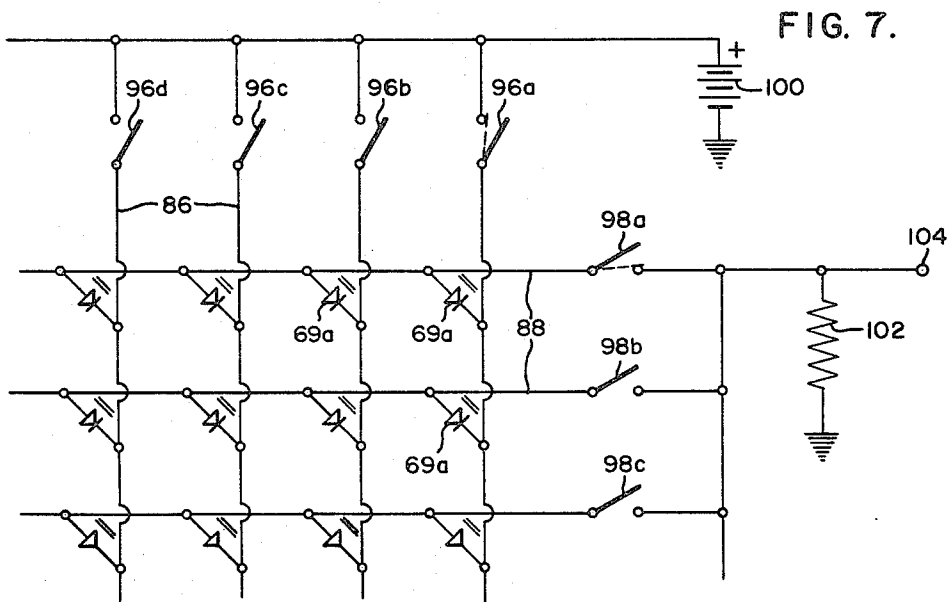
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3,401,294

STORAGE TUBE

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17 Claims. (Cl. 313-68)

This invention relates generally to electron discharge devices and more particularly to improved storage targets for use in electronic storage tubes.

In conventional electronic storage tubes, information is written onto a target element typically made of a relatively thin layer of a dielectric material. The information is written onto the surface of the dielectric target by means of an electron beam (writing beam) and is stored in the form of a pattern of charges established on the surface of that target. The establishment of these charges may be accomplished either by creating a secondary emission effect or by inducing a current within the dielectric by electron bombardment. After the elapse of a given period of time, the information may be retrieved by directing a beam of electrons (reading beam) to scan the target and derive an output signal in accordance with the pattern of charges.

As may be seen from the above discussion, the storage capability is achieved by placing a pattern of charges on the surface of the dielectric material. The pattern of charges will remain on the surface of the dielectric material until they are deliberately erased or until the charges are discharged through the dielectric material. Inherently, the capacity and resistance of the dielectric material are finite, and as a result an electrical path is established through the dielectric material to the electrodes and support structure associated with the aforementioned dielectric material to dissipate the pattern of charges placed on the surface of the dielectric material. In a typical storage tube, the dielectric material is deposited on a planar electrode of a conductive material in order to establish the target element at a specified voltage or to provide an electrode through which the output signal may be derived. In any event it may be understood that such an electrode would provide an intimate electrical path through which the surface charge on the dielectric material may be dissipated, and as a result the period for which the information may be stored is thereby limited.

Further in typical electrostatic storage tubes, it is often necessary to maintain a potential upon the target element in order that the target element will maintain its storage function; therefore considerable quantities of electrical power are often required for the operation of these devices.

Specifically, there is known in the prior art an electronic storage device in which the electric field established by a pattern or charges established on a thin layer of a dielectric material is utilized to effect the impedance across a reverse biased, rectifying junction. The reverse biased rectifying junction, as suggested by the prior art, is established by a conductive lead which is inserted through or in close proximity with the storage layer of dielectric material to a member composed of a semiconductor material to form therebetween a point contact junction. The principle of this device lies in the effect of the electric field created by the storage charges upon the impedance established by the junction of the point contact. In a typical point contact diode, a voltage source may be applied across the junction so that the junction will exhibit a high resistance by biasing the voltage source to oppose the flow of the charge carriers within the semiconductor material across the junction. In the aforementioned storage device of the prior art, the electric field established

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by the charges stored on the dielectric material will effect the impedance established by the point contact junction. Therefore, in operation, a specified charge may be placed on the layer of dielectric material which may be detected or "read out" by placing a reverse bias across the point contact junction. Further, the target element suggested by the prior art may be composed of a plurality of these point contact junctions disposed in a regular array; thus, a pattern of information may be stored on the target element and may be successively read out by applying successively a reverse bias to each of the point contact junctions.

However, the storage device as described above does have significant limitations in several aspects of its operation. First, the high resistance junctions are formed by conductive leads which are intimately associated with the storage dielectric layer and which tend to dissipate the charge from the storage layer. Thus, it may be seen that the periods of time for which a signal pattern may be stored are limited. Further due to the proximity of the storage layer and the lead, the writing electron beam may interfere with the readout operation; therefore, it is necessary to operate the reverse biasing voltage at a level whose order of magnitude is substantially above that of the reading beam of electrons. Thus, it may be understood that the dynamic range and the degree of amplification provided by such a target may be so limited so as to allow only a digital mode of operation of this target. More specifically, the dynamic range of such a target is limited by the reverse leakage currents of the point contact junctions of this target. In addition, no isolation has been provided by the storage device of the prior art to electrically separate each of the point contact junctions; therefore, such a target element would be limited to a single mode of read out in which the rectifying junctions are successively read out one at a time. Finally, it would be quite difficult and time consuming to form a sufficient number of the point contact junctions to provide a storage target having a reasonably high resolution.

Accordingly, it is an object of this invention to provide an electronic storage tube having an improved storage target.

A further object of this invention is to provide an improved storage target in which the electrical contacts thereto are substantially isolated from the storage dielectric layer thereof.

A still further object of this invention is to provide an improved storage target in which a sufficient number of reverse biased, rectifying junctions may be arrayed to provide a target element capable of very high resolution.

A still further object of this invention is to provide an improved storage target which may be easily manufactured without the necessity of performing a great number of repetitive steps to form each of the reverse biased rectifying junctions.

Still another object of this invention is to provide an improved storage target in which the high number of rectifying junctions are effectively isolated from each other.

Another object of this invention is to provide an improved storage target in which distinct rectifying junctions may be simultaneously read out to thereby allow various portions of the target element to be operated in different modes of operation.

Still another object of this invention is to provide an improved electronic storage target in which the read out of the rectifying junctions may be performed to sense the varying levels of charge stored on the dielectric layer to thereby achieve an analog mode of operation.

A still further object of this invention is to provide a storage target having great sensitivity and capable of being operated over a wide dynamic range.

Stated briefly, the electronic storage tube in accordance with the present invention comprises a cathode element for directing a writing beam of electrons onto an improved target element. The storage target of this invention is made of a first layer of a dielectric material, a memory unit formed by planar diffused junctions disposed beneath the surface of said dielectric storage layer, and a plurality of electrical contacts disposed remotely from said dielectric storage layer to provide means for applying a reverse bias voltage across the planar diffused junctions. In one particular embodiment of this invention, the planar diffused junction is formed by diffusing N carriers in one region of a semiconductor crystal and P carrier into an adjacent region of the semiconductor crystal. It is a further aspect of this invention that the planar diffused junction be isolated from the other such junctions of the target element. This may be accomplished by inserting additional PN junctions between each of the memory units formed by the planar diffused junctions.

Further objects and advantages of the invention will become apparent as the following description proceeds and features of novelty which characterize the invention will be pointed out in particularity in the claims annexed to and forming a part of this specification.

For a better understanding of the invention reference may be had to the accompanying drawings, in which:

FIG. 1 is a sectioned view of an electronic storage tube utilizing the present invention;

FIG. 2 is a perspective view of the storage target incorporated in the storage tube shown in FIG. 1;

FIG. 3 is a cross-sectional view of an embodiment of FIG. 2 taken along line III—III of FIG. 2;

FIG. 4 is a diagrammatic view of the electrical circuit of the storage target as shown in FIGS. 2 and 3;

FIG. 5 is an enlarged plan view of the reverse side of the storage target shown in FIG. 2;

FIG. 6 is a cross-sectional view of an embodiment of FIG. 5 taken along line VI—VI of FIG. 5; and

FIG. 7 is a schematic view of the interconnections made to the storage target of this invention.

Referring now to the drawings and in particular to FIG. 1, a memory tube 10 is depicted as comprising an evacuated envelope 12 having a neck portion 14 axially aligned of and interconnected to a flared portion 16. The neck portion 14 and the flared portion 16 which are made of glass or other suitable material, are respectively connected to a base 18 through which terminals 20 are inserted and to an annular flange 22 made of a suitable material such as Kovar (a Westinghouse trademark for an alloy comprised substantially of iron, nickel, and cobalt). A mounting cylinder 24 has a radially extending flange 25 which is secured to the annular flange 22 by a suitable method such as Helarc welding. The evacuated envelope 12 is completed by a circular end plate 26 which is secured to a radially extending flange portion 27 associated with the mounting cylinder 24. The mounting cylinder 24 and the plate 26 may be made of a suitable conductive material such as Kovar. Within the evacuated envelope 12, there is disposed a cathode element 28 having an emissive coating thereon for the emission of an electron beam 39. A control grid 30 is aligned with and disposed about the cathode element 28 to modulate the density of the electron beam 39. An accelerating electrode 32 and pairs of horizontal deflection plates 36 and vertical deflection plates 38 are aligned along the axis of the neck portion 14 in the order enumerated to thereby accelerate and to deflect the electron beam 39 in a regular pattern across a storage target 40 which is disposed within the opposite end of the evacuated envelope 12. Further, a collecting electrode 47 which may be formed of a wire mesh is disposed in a plane parallel and adjacent to the storage target 40.

The storage target 40 is mounted within the cylinder 24 by an annular mounting flange 42 which may be se-

cured as by welding to the inner periphery of the cylinder 24. A plurality of support brackets 44 are interconnected between the mounting flange 42 and the storage target 40. In one embodiment, the support brackets 44 are made of two Z-shaped studs 45 which are respectively connected to the mounting flange 42 and the storage target 40, and are interconnected by an insulating bead 46 of a suitable material such as glass which has been fused to the ends of the studs 45. A plurality of conductive leads 52 are electrically connected to the storage target 40. Further, a plurality of terminal elements 48 are disposed in a circular array through openings in the mounting cylinder 24 to provide a vacuum sealed exit for each of the conductive leads 52. The terminal elements 48 are comprised of an annular eyelet 49 made of a suitable material such as Kovar which may be secured to the mounting cylinder 24 as by brazing with an alloy of copper and silver. The conductive lead 52 which may likewise be made of a material such as Kovar as insulated by a sleeve 50 made of a suitable insulating material such as aluminum oxide which is disposed between the conductive lead 52 and the eyelet 49 to provide a vacuum seal therebetween.

Referring now to FIG. 2, there is shown an enlarged view of the storage target 40 which is comprised of a crystal substrate 56 made of a semiconductor material such as silicon. A plurality of memory units 60 have been diffused, as will be explained later, in a regular array 58 comprised of horizontal rows 62 and vertical rows 64 of the memory units 60. In the projected view of FIG. 2, a representation of the memory unit 60 is shown; it may be understood, as will be explained later, that an insulating layer 74 is disposed over each of the memory units 60. In one embodiment as shown in FIG. 2, the memory unit 60 has a central region 66 of a P-type semiconductive material which is successively surrounded by a region 68 of an N-type semiconductive material and a region 70 of a P-type semiconductive material. Each of the memory units 60 is electrically isolated from each other by a region 72 made of an N-type semiconductor material.

Referring now to FIG. 3, a cross-sectioned view taken through line III—III of FIG. 2, is shown. As shown in FIG. 3, the memory unit 60 has the storage insulating layer 74 of a material such as silicon dioxide disposed on one side and a second insulating layer 76 made of a similar material disposed on the other side. As explained before, the central region 66 is surrounded successively by the region 68 and the region 70. A pair of low resistance contacts 80 and 82 are inserted through the insulating layer 76 to make an electrical connection respectively with the region 70 and the region 66. In an alternate embodiment of this invention, contact 80 may be so placed to make electrical contact to both of the regions 68 and 70. Rectifying junctions 67 and 69 are formed respectively between regions 70 and 68 and between regions 68 and 66. As explained before, an isolating region 72 is disposed between each of the memory units 60; in the particular embodiment shown in FIG. 3, the region 72 is made of an N-type semiconductive material and forms rectifying junctions 71 with the P-type region 70 of the adjacent memory units 60. A low resistance contact 81 may be inserted through the insulating layer 76 upon which a positive voltage source 83 may be applied to the N-type isolating region 72 to thereby reverse bias the rectifying junction 71 and effect a great isolation between the adjacent memory units 60.

As will be explained later in detail, an inversion layer 73 is formed within the N-type region 68 due to the influence of charges deposited on the storage insulating layer 74 by the electron beam 39. Though it is desired to form such inversion layers in the region 68, this phenomena is undesired between the other regions; therefore, a plurality of diffusion regions 78 is formed by diffusing a high concentration of N-type doping material

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within the regions of the N-type isolating region 72 adjacent the insulating layers 74 and 76. Further, a diffusion region 78 is also formed within a layer of the N-type region 68 adjacent the insulating layer 76. In order to make electrical connections with the contact regions 80 and 82, a conductive leg 84 is vapor deposited over the contact regions 80, and a vertical connecting strip 86 is vapor deposited over the contact regions 82.

Referring now to FIG. 4, a schematic representation of the equivalent electrical circuit presented between the contact regions 80 and 82 is shown. Starting with contact 80, the circuit can be traced through the P-type region 70 across the rectifying junction 67, which is shown in FIG. 4 as a diode 67A. Next, a rectifying junction 69 is formed at the boundary between the N-type region 68 and the P-type region 66 and is represented in FIG. 4 as a diode 69A. Further, the storage insulating layer 74 is represented with a plurality of negative charges placed thereon. The collecting electrode 47, which has been incorporated within the tube 10 to limit the secondary current emitted by the target 40, is represented as being disposed in a plane parallel to the surface of the insulating layer 74.

In operation, the beam of electrons 39 is emitted by the cathode element 28 and is successively modulated and accelerated by the electrodes 30 and 32 respectively; further, the electron beam 39 is deflected vertically and horizontally so as to pass over each of the memory units 60 which are arrayed in the rows and columns shown in FIG. 2. As the electron beam 39 passes over each of the memory units 60, it deposits a plurality of charges on the surface of the insulating layer 74. Referring now to FIG. 3, the inversion layer 73 is formed within the region 68 due to the presence of the charges stored on the surface of the insulating layer 74. In effect, these charges create a field which repels the negative charge carriers (i.e., electrons) and attracts the positive charge carriers (i.e., holes). Thus, it may be understood that the impedance of the junctions 67 and 69 will vary under the influence of the negative charges. It has been verified by experimentation that the constant current characteristics of a rectifying junction such as the junctions 67 or 69 is proportional to the strength of an electrical field such as created by the charges placed on the surface of the insulating layer 74. With regard to the specific embodiment shown in FIG. 3, the deposition of a negative charge on the insulating layer 74 will repel the negative carriers within the N-type region 68 thereby effecting a change of the impedance presented between the contact regions 80 and 82. It is an important aspect of this invention that the voltage-current characteristic of rectifying junctions 69 may be varied at different levels according to the polarity and quantity of the charge deposited on the surface of the insulating layer 74. When a rectifying junction is impressed with a voltage in the reverse direction, the resulting saturation current is essentially independent of the magnitude of the voltage. However, the saturation current may be changed by applying an electrical field upon the junction. As explained above, the field is established by depositing a charge upon the insulation layer 74 which in turn controls the magnitude of saturation current passing through the junction 69 in accordance with the polarity and quantity of deposited charges. Thus, if a negative charge is placed upon the insulation layer 74, the saturation current of the reverse biased junction 69 is increased, and conversely if a positive charge is placed upon layer 74, the saturation current is reduced. In the preferred mode of operation of this device, the electron beam 39 is accelerated by a potential less than that of the first cross-over of the insulating material 74; thus negative charges are placed on the surface of the insulating layer 74 to thereby lower the resistance presented by the rectifying junction 69 when a reverse-bias voltage is subsequently applied thereacross. As may be seen in FIG. 4, a positive

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voltage may be applied to the contact region 80 thereby forward biasing diode 67A and reverse biasing the diode 69A. The charges deposited upon the insulating layer 74 will control, as explained above, the saturation current passing through the diode 69A.

Further, it may be understood that if the electron beam 39 is directed upon the target 40 so that the dwell time upon each memory unit 60 will be approximately equal, the density of the electron beam 39, which is controlled by the voltage applied to the control grid 30, will determine the amount of charge placed upon the surface of the insulating layer 74. The amount of charge in turn will determine the voltage-current characteristic of the rectifying junctions 67 and 69. The charges stored on the surface of the dielectric layer or the insulating layer 74 will remain substantially unaffected for extended periods of time and thereby provide a storage capability. When it is desired to retrieve the information contained in the pattern of charges stored on the insulating layer 74 of the target 40, a voltage may be applied between the contacts 80 and 82 to thereby reverse bias one of the rectifying junctions 67 and 69. In a manner to be explained later, the reverse biasing voltage may be successively applied across the memory units 60 to derive an output signal proportional to the voltage applied to the control grid 30. It has been found from actual experimentation, that a device substantially as shown in FIG. 3, was capable of storing a charge for a period of time in excess of 100 hours. This prolonged storage capability was in part due to the fact that the contacts 80 and 82 are isolated from the insulating layer 74 and thereby have little or no tendency to provide a grounding path for the storage layer 74.

In a typical mode of operation, it would be desired, if not required, that the charge deposited on the insulating surface 74 be quickly and easily removed so that a second pattern of charges could be deposited thereon. In a first mode of operation, the electron beam 39 could be accelerated by a suitable potential to cause the breakdown of the insulating layer 74 and allow the charges to be dissipated through the semiconductive regions to the various contacts associated therewith. The potential necessary to cause a breakdown of the insulating layer 74 is dependent upon the thickness of this layer; for a layer of an insulating layer 74 of silicon dioxide having a width of approximately 1000 Angstroms, a voltage level of between 60 to 100 volts has been found sufficient for this mode of operation. In a second mode of operation, the electron beam is accelerated by a potential above the first cut-off of the material of the insulating layer 74; as a result, more secondary emission electrons will be emitted than the number of electrons bombarding the insulating layer 74. Thus, an excess of electrons will be dissipated and collected by the electrode 47 which is disposed above the insulating layer 74, thereby dissipating the charges from this layer. Though it has been assumed in this discussion that the priming or erasing electrons are supplied by the cathode elements 28 which would necessitate blanking voltages being applied to the deflection electrodes, a separate electron gun could be provided within the envelope 12 to accomplish the erasing of the target 40.

In an alternative embodiment of this invention, a metal layer 89 (shown in dotted line in FIG. 3) capable of emitting secondary electrons in response to an electron bombardment is disposed upon the insulation layer 74 in proximity to that region 68 in which the inversion layer is to be formed. In such an embodiment, the region 68 would be diffused with P-type doping materials and the regions 70 and 66 would be diffused with N-type doping materials. Under the bombardment of electrons, the layer 89 would emit secondary electrons which are collected by the electrode 47. The surface of the layer 89 is thus driven positively to a magnitude controlled by the positive voltage applied to the electrode 47. Thus, with a

positive charge disposed upon the layer 89, an N-type inversion layer would be established within the region 68 and the current characteristic of the junction 69 would be accordingly effected as explained above.

Though not a primary aspect of this invention, a typical procedure for forming the target 40 of this invention will be briefly set out. First, a silicon ingot of the appropriate starting resistivity is cut, lapped to remove saw damage, polished to remove lapping damage and to approach the desired final thickness, and then chemically etched or polished to provide the appropriate wafer thickness and an essentially smooth surface. The wafer of silicon is then subjected to a high temperature usually greater than 100° C., in an oxidizing atmosphere which may consist of a wet non-oxidizing gas (such as nitrogen bubbled through water) and a dry oxygen or steam. The wafer is then coated with any of the well known acid resistance emulsions; next, a previously prepared photographic negative is positioned over the wafer to obtain a maximum number of memory units 60 on the wafer and the emulsion is exposed to a light source. The wafer is then developed and the undesired silicon dioxide may be removed in a hydrofluoric acid solution to provide an oxide pattern conforming to the negative. The remaining photoresist is thoroughly removed from the wafer by any of the well known solvents. The wafer is now placed in a quartz boat and subjected to a first diffusion step wherein appropriate doping materials are injected into those regions of the wafer in which the silicon dioxide has been removed. Typically, the doping materials for the P-type regions could be boron and the doping material for the N-type regions could be phosphorous. In coincidence with the diffusion, or in the alternative as a separate step following the diffusion, the oxide is regrown over the entire wafer. The steps of emulsion coating, alignment, developing, and oxide removal are repeated before the wafer is subjected to a second diffusion to thereby impart doping materials into different regions of the wafer. The wafer may proceed through several steps of diffusion in the same manner depending upon the complexity of the functional electronic block. Following the final diffusion, the areas of the wafer upon which contacts are to be placed may be metallized. Such materials as gold and aluminium are commonly used for metallization. In a typical method of application, aluminium may be evaporated over the entire silicon wafer. The excess aluminium is removed by photoengraving techniques as described above leaving aluminium contacts adhering to the silicon wafer and aluminium interconnections to the silicon oxide layer. Following the metallization step to form contacts, a second metallization step is provided to obtain interconnections with the conductive leads 52. Finally, the individual targets may be tested on a micromanipulator and, if satisfactory, may be inserted into the memory tube 10.

Referring now to FIG. 5, a view is shown of the reverse side of the target 40 upon which have been deposited electrical interconnections for each of the memory units 60. As may be seen in FIG. 5, a plurality of the vertical connecting strips 86 may be vaporized on the insulating layer 76 so as to cover and contact each of the contacts 82. Further, it is noted that each of the vertical connecting strips 86 are disposed parallel with each other. A plurality of horizontal connecting strips 88 are disposed in parallel rows with a plurality of conductive legs 84 aligned perpendicular to the horizontal strips 88 to overlie and connect with the contacts 80. Further, the conductive leads 52 may be connected to the connecting strips 86 and 88 as by thermocompression bonding or ultrasonic welding.

Referring now to FIG. 6, a cross-sectional view is shown of a portion of the target 40 depicting a structure by which the criss-crossing vertical and horizontal connecting strips 86 and 88 may be effectively insulated from each other. As is shown in FIG. 6, the horizontal connecting strip 88 is disposed above the isolating, N-type

region 72; further, diffusion regions 78 are disposed upon either side of the region 72, and the insulating storage layer 74 is disposed on one side of the region 72 and the insulating layer 76 is disposed on the other side. The insulated overlapping of the connecting strips is achieved by disposing contacts 95 through the insulating layer 76 and by interconnecting these contacts 95 by a region 92 having a surplus of P-type doping material diffused therein. Further, a third insulating layer 94 is disposed above the region 92, and the vertical connecting strip 86 may be deposited thereon to thereby achieve an effective insulation from the connecting strip 88.

Referring now to FIG. 7, a schematic representation of the interconnections of the memory units 60 is shown. It is noted that only a partial representation of the many memory units 60 is made, and that in an actual embodiment of this invention as many as ten thousand memory units could be mounted on a target element having a diameter of approximately one inch. As shown in FIG. 7, a positive voltage source 100 may be successively applied by switches 96a, 96b, 96c, etc., to the vertical connecting strips 86. The diodes 69a are interconnected between the vertical connecting strips 86 and the horizontal connecting strips 88 which may in turn be successively connected across a sensing impedance 102 to ground by switches 98a, 98b, 98c, etc. The signal output 104 is taken from the voltages developed across the sensing impedance 102. Though only a single diode 69a has been represented in FIG. 7 whereas two diodes are represented in FIG. 4, it may be understood that if a positive voltage was applied to the contact 80 that the diode 67a (see FIG. 4) would be forward biased and would therefore offer little or no resistance in this circuit. In operation, it may be seen that if the switches 98a and 96a are both closed at once, that the voltage source 100 will be impressed upon the diode 69a and a response therefrom will be detected upon the impedance 102. Thus, it may be seen that each of the memory units 60 (as represented by a diode 69a) can be successively read out by closing switch 98a and then by successively opening and closing the switches designated by the numeral 96. The next step would be to open the switch 98a and then close the switch 98b and then successively open and close those switches designated 96. In this manner, the pattern of charges associated with each of the memory units 60 may be successively read out one at a time.

Further, it is noted that the switching arrangement shown in FIG. 7 is only an illustrative embodiment of how the memory units may be read out. A more complicated system of interconnections to the memory units could be devised so that more than one memory unit can be detected at the same time. As previously discussed, each of the memory units are electrically isolated from each other thereby allowing sections of the array of memory units to be operated in different modes of operation. For instance, the entire surface of the target 40 would not have to be primed at a single time thereby allowing a new pattern of information to be read on selected portions of the target while maintaining another pattern of information upon other sections of the target 40. This selection could be achieved by using grid blanking voltages, primary voltages, and input voltages that are synchronized in time with the beam deflection signals.

Therefore, it may be realized that there has been disclosed a storage device in which there has been incorporated a greatly improved storage target having a storage surface which has been effectively isolated from the external or adjacent circuitry to thereby achieve greatly increased storage times. Further, this target provides extremely fine resolution; in one embodiment of this invention, it has been found practical to form a target of 10,000 units having a spacing of from center to center of approximately five mils. Further, if the effective isolation between adjacent memory units is deleted, even greater numbers of memory units may be placed upon the target.

An additional aspect of this invention is that very little power is required for the operation of this device; i.e., a signal is required for the electron gun only during the write-in cycle, while no power is required for the electron gun and associated deflection plates during the storage time or read out.

While there have been shown and described what are presently considered to be the preferred embodiments of the invention, modifications thereto will readily occur to those skilled in the art. It is not desired, therefore, that the invention be limited to the specific arrangement shown and described and it is intended to cover in the appended claims all such modifications as fall within the true spirit and scope of the invention.

We claim as our invention:

1. An apparatus for the storage of electrical signals comprising a body of semiconductor material having first and second surfaces, a rectifying junction formed by regions of said body having differing conductivity types, a layer of storage material disposed on said first surface, and electrical contacts in ohmic contact with said regions to provide a current flow to said junction, said contacts disposed on said second surface in a position electrically remote from said layer, and means for directing a flow of electrons onto said layer to produce a localized charge on said layer.

2. A storage target comprising a body of a semiconductor material having a first and second surface, a plurality of memory units formed within said body in a regular array, said memory unit including a first rectifying junction formed by regions of said body having differing types of conductivity types, a layer being disposed on said first surface and having the property of being able to store localized charges, electrical contacts in ohmic contact with said regions to provide a current flow to said junction, said contacts being disposed on said second surface in a position remote from said layer, and means for isolating said memory units from each other including a second rectifying junction formed by regions of said body having differing types of conductivity types.

3. A device for storing electrical signals comprising a body of semiconductor material having first and second surfaces, a plurality of memory units formed within said body in a regular array of vertical and horizontal rows, said memory unit including a first rectifying junction formed by first and second regions of differing conductivity types, a first layer of storage material disposed on said first surface, a second layer of insulating material disposed on said second surface, at least one contact associated with each of said first and second regions and extending through said second layer, means for isolating said memory units from each other including a second rectifying junction formed by a third and fourth region of said body having differing conductivity types, means for directing a flow of electrons onto said layer to produce a pattern of localized charges on said first layer, and means for detecting said pattern of charges including a plurality of interconnecting strips disposed on said second layer and electrically connected to said contacts.

4. A storage target comprising a body of semiconductor material having first and second surfaces, a plurality of memory units formed within said body in a regular array, said memory unit including regions of said body of differing conductivity types to form a first P-N junction therebetween, electrical contact in ohmic contact with said regions to provide a current flow to said first junction, and means for electrically isolating said memory units from each other including a second P-N junction formed by regions of said body having differing conductivity types.

5. A storage target comprising a body of semiconductor material having first and second surfaces, a plurality of memory units formed within said body in a regular array, said memory unit including first region, a second region disposed about said first region, and a third region dis-

posed about said second region, said second region having a conductivity type different from that of said first and third regions, a layer of storage material disposed on said first surface, contacts applied to said first and third regions in a position on said second surface remote from said layer, and means for isolating said memory units from each other including a P-N junction formed by a fourth region of said body and said third region, said fourth region having a conductivity type different from said third region.

6. A storage target comprising a body of semiconductor material having first and second surfaces; a plurality of memory units formed within said body in a regular array; said memory unit including a first region, a second region disposed about said first region, and a third region disposed about said second region, said first and third regions having a conductivity type different from that of said second region to form first and second rectifying junctions between said first and second regions, and between said second and third regions respectively; a layer of storage material applied to said first surface, at least one contact applied on said second surface to each of said first and third regions; and means for isolating said memory units from each other including a fourth region disposed about said third region, said fourth region having a conductivity type different from that of said third region to form third rectifying junctions therebetween.

7. A storage target comprising a body of semiconductor material having a first and second surface; a plurality of memory units formed from said body in a regular array; each of said memory units including a first P-N junction formed by first and second regions of said body having differing types of semiconductivity, a layer formed on said first surface having the capability of storing a pattern of localized charges, said charges forming an inversion layer in said second region adjacent said layer to thereby effect the impedance of said first P-N junction, electrical contacts disposed on said second surface in electrical association with said first and second regions to provide a current flow to said first P-N junction, and means for isolating said memory units from each other including a third region of said body disposed about said memory unit and a zone in said third region having a surplus quantity of a doping material diffused therein to prevent the formation of an inversion layer.

8. A storage target comprising a body of semiconductor material having first and second surfaces; a plurality of memory units formed within said body in a regular array; said memory unit including a first rectifying junction formed by first and second regions of said body having differing conductivity types, and a layer disposed on said first surface capable of storing a pattern of localized charges, said charges forming an inversion layer in said second region to effect the voltage-current characteristics of said first junction; electrical contacts disposed on said second surface in electrical association with said first and second regions to provide a current flow to said first junction; and means for isolating said memory units from each other including a second rectifying junction formed by third and fourth regions of said body having differing conductivity types and a zone within said fourth region having an added quantity of doping material diffused therein to prevent the formation of an inversion layer.

9. A storage target comprising a body of semiconductor material having first and second surfaces; a plurality of memory units formed within said body in a regular array; said memory units including a first region, a second region disposed about said first region, and a third region disposed about said second region, said first and third regions having a conductivity type differing from that of said second region to form first and second P-N junctions respectively between said first and second regions and between said second and third regions, and a

layer disposed on said first surface capable of storing a pattern of localized charges, said charges forming an inversion layer in said second region thereby effecting the impedance presented by said first and second junctions; electrical contacts disposed on said second surface in ohmic contact with said first and third regions; and means for isolating said memory units from each other including a fourth region disposed about said memory units and having a conductivity type differing from that of said third region to form a third P-N junction therebetween, and a zone formed within said fourth region adjacent said layer having an added quantity of doping material diffused therein to prevent the formation of an inversion layer.

10. A storage device comprising a body of semiconductor material having first and second surfaces; a plurality of memory units formed within said body in a regular array; said memory units including a first rectifying junction formed by first and second regions of different conductivity types, and a layer of storage material disposed on said first surface; contacts disposed on said second surface in a position remote from said layer in electrical association with said first and second regions to provide a current flow to said first junction; and means for electrically isolating said memory units from each other including a second rectifying junction formed by third and fourth regions of said body of different conductivity types; and means for applying a potential to said fourth region to increase the impedance of said second junction.

11. A storage target comprising a body of semiconductor material having first and second surfaces; a plurality of memory units formed within said body in a regular array; said memory units including a rectifying junction formed by a first region of P-type conductivity and a second region of N-type conductivity within said body, a first layer of storage material disposed on said second surface, and a second layer being disposed on said first layer in proximity to said first region and having the property of emitting secondary electrons in response to a flow of primary electrons; and contacts disposed on said second surface in electrical association with said first and second regions to provide a current flow to said junction.

12. A device for storing electrical signals comprising a target element, said target element including a body of semiconductor material having first and second surfaces, a plurality of memory units formed within said body and having a P-N junction formed by regions of said body having differing conductivity types, a storage layer formed on said first surface, and contacts disposed on said second surface in ohmic contact with said regions to provide a current flow to said junction; means for placing said electrical signals on said target including a cathode element for directing a flow of electrons on said target element; and means for retrieving said electrical signals including a plurality of electrical connections to said contacts, and means for selectively applying a reverse biasing potential in a determined order to said connections.

13. A device for storing electrical signals comprising a target element, said target element including a body of semiconductor material having first and second surfaces, a plurality of memory units formed within said body and including a first region, a second region disposed about said first region, and a third region of said body disposed about said second region, said first and third regions having conductivity types differing from that of said second region to form first and second P-N junctions respectively between said first and second regions and between said second and third regions, a storage layer disposed upon said first surface, contacts disposed upon said first and third regions on said second surface, and means for isolating said memory units from each other including a fourth region of said body having a conductivity type differing from that of said third region to form a third P-N junction between said third and fourth re-

gions; means for writing including a cathode gun for directing a beam of electrons across said target element to thereby dispose a pattern of localized charges upon said layer; and means for reading including a plurality of electrical conductors connected to said contacts, and switching means for selectively applying a reverse biasing potential to said conductors to sense said pattern of localized charges.

14. A device for storing electrical signals comprising a target element, said target element including a body of semiconductor material having first and second surfaces, a plurality of memory units formed within said body and including a first rectifying junction formed by first and second regions of said body having differing conductivity types, a storage layer disposed on said first surface, first contacts electrically associated with each of said first and second regions and disposed on said second surface; and means for isolating each of said memory units from each other including a second rectifying junction formed by third and fourth regions of said body having differing conductivity types, second contacts associated with said fourth region, and means for applying a potential to said second contacts to increase the impedance presented by said second junction, means for writing including a cathode gun for directing a beam of electrons on said target element to thereby impart a pattern of localized charges upon the surface of said layer; and means for reading including switching means for selectively applying a reverse biasing potential to said first contacts to thereby sense said pattern of localized charges.

15. A storage target comprising a body of semiconductor material in which a plurality of memory units are formed, each of said memory units including first, second and third regions, said second region disposed between said first and second regions and having a conductivity type different from that of said first and second regions to form respectively first and second junctions between said first and second regions and between said second and third regions, said second region capable of forming an inversion layer therein, a layer of storage material disposed upon said storage target and capable of storing an electrical charge thereon to induce the formation of said inversion layer in said second region, and means for isolating said memory units from each other including a fourth region disposed about each of said memory units.

16. A storage target comprising a body of semiconductor material having first and second surfaces; a plurality of memory units formed within said body in a regular array, each of said memory units including a first region, a second region disposed about said first region, and a third region disposed about said second region, said second region having a conductivity type different from that of said first and second regions to form first and second rectifying junctions between said first and second regions and between said second and third regions respectively, said second region capable of forming an inversion region therein, and a layer of storage material applied to said first surface capable of storing electrical charges to effect said inversion region within said second region.

17. A storage target as claimed in claim 16, wherein contacts are applied to said first and third regions on said second surface to effect a current flow to said first and second rectifying junctions.

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