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(54) **Title**: ISOLATED III-N SEMICONDUCTOR DEVICES

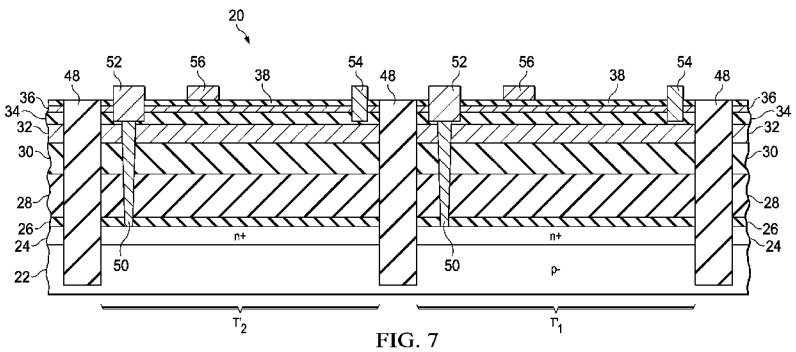

FIG. 7

(57) **Abstract**: Described examples include a semiconductor device with a substrate (22), a low defect layer (32) formed in a fixed position relative to the substrate (22), and a barrier layer (34) including III-N semiconductor material formed on the low-defect layer (32) and forming an electron gas in the low-defect layer (32). The device also has a source contact (52), a drain contact (54), and a gate contact (56) for receiving a potential, the potential for adjusting a conductive path in the electron gas and between the source contact and the drain contact. Lastly, the device has a one-sided PN junction (22/24) between the barrier layer (34) and the substrate (22).

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ISOLATED III-N SEMICONDUCTOR DEVICES

[0001] This relates generally to semiconductor devices, and more particularly to isolated III-N semiconductor devices.

BACKGROUND

[0002] Integrated circuit devices are typically formed in connection with various semiconductor materials. For some applications these materials include compound materials such as the known III-N semiconductors, which are known to include combinations of elements from group III of the periodic table. Such elements include aluminum, gallium, indium, and possibly boron, and as group III-N semiconductors they are combined with nitrogen, such that each element contributes to the overall semiconductor material. Examples of III-N semiconductor materials are gallium nitride, aluminum gallium nitride, indium nitride, and indium aluminum gallium nitride. Moreover, III-N semiconductor devices may be included with other silicon based devices by sharing a common silicon substrate or wafer, where accommodations are made for the III-N semiconductor devices due to the differences between the compound semiconductors and the underlying silicon substrate.

[0003] The above approach has various benefits, such as in connection with gallium nitride (GaN) devices. For example, such devices may include light emitting diodes (LEDs), solar cells, radiation-resistant devices, and high temperature or high voltage devices, commonly including transistors. However, these devices, may suffer from certain drawbacks, including possible instabilities when mixed with different devices based on either structure or functionality.

[0004] FIG. 1 (prior art) illustrates a schematic of a conventional half bridge 10 that may be implemented using GaN transistors, and that as implemented may suffer drawbacks. Specifically, half bridge 10 includes two GaN transistors T_1 and T_2. As is well-known, the drain $D(T_1)$ of transistor T_1 is connected to a first rail voltage (shown as V_{line}), and the source $S(T_2)$ of transistor T_2 is connected to a second rail voltage (shown as ground). Accordingly, transistor T_1 is referred to as the high side, and transistor T_2 is referred to as the low side. The source $S(T_1)$ of transistor T_1 and the drain $D(T_2)$ of transistor T_2 are connected and provide the output, V_{out}, for half bridge 10. The transistor gates may be connected to various signals as

shown by illustration with a generic input block 12. The particular signals are not especially significant for this discussion, but they allow the transistors T_1 and T_2 to operate in complementary fashion, so one is on while the other is off, and vice versa. Lastly, as is typical in various transistor configurations, each of transistors T_1 and T_2 has its source connected to the substrate of the respective transistor, where such a connection is sometimes also referred to as a backgate.

[0005] In operation, transistors T_1 and T_2 are on one at a time and typically at a 50 percent duty cycle, so V_{out} tends toward V_{line} when the high side transistor T_1 is on and toward ground when the low side transistor T_2 is on. Based on the load and input voltages, such circuit may have various uses, including power electronics such as in a converter, switching, and the like. Half bridge 10 has various uses and is well-known, but issues may arise in ideally implementing the bridge using GaN technology. Specifically, the source-to-backgate connections can cause leakage, instability, or other performance-diminishing issues due to differing voltages being connected to a same substrate. For example, consider a high-voltage application, where V_{line} is 400 volts. When the high side transistor T_1 is on, then V_{line}, minus the drop across transistor T_1, is connected to V_{out}. For example, if that voltage drop is 1 volt, then when transistor T_1 is on, V_{out}=399 volts. Accordingly, the source-to-backgate connection of transistor T_1 couples the backgate to 399 volts, while at the same time the source-to-backgate connection of transistor T_2 couples the backgate to ground, thereby creating a considerable leakage path between the two transistors. As an alternative, the backgate connections instead could be implemented by connecting each transistor drain to the backgate. While the alternative reduces the leakage issue incrementally, when the high side transistor T_1 and low side transistor T_2 are off, high voltage on the backgate would result in higher surface fields for a given design and lead to lower lifetimes and thereby diminish the transistor reliability. Additional issues with this approach will include added complexity in packaging technology needs like the need of insulating die attach.

SUMMARY

[0006] In described examples, a semiconductor device includes a substrate, a low defect layer formed in a fixed position relative to the substrate, and a barrier layer including III-N semiconductor material formed on the low-defect layer and forming an electron gas in the low-defect layer. The device also includes a source contact, a drain contact, and a gate contact

for receiving a potential, the potential for adjusting the electron gas and a conductive path, responsive to and formed by the electron gas between the source contact and the drain contact. Lastly, the device includes a one-sided PN junction between the barrier layer and the substrate.

[0007] In another aspect, each of a first dielectric barrier and a second dielectric barrier is aligned along a respective edge of the low defect layer and the barrier layer and further extends in a direction from the low defect layer toward the substrate and to an extent below the one-sided PN junction.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. 1 (prior art) illustrates a schematic of a conventional half bridge.

[0009] FIG. 2 illustrates a cross-sectional view of the formation of a transistor pair according to example embodiments, including a substrate and n+ doped layer.

[0010] FIG. 3 illustrates a cross-sectional view of the formation of a transistor pair of FIG. 2, with the addition of a mismatch isolation layer and a buffer layer.

[0011] FIG. 4 illustrates a cross-sectional view of the formation of a transistor pair of FIG. 3, with the addition of an electrical isolation layer.

[0012] FIG. 5 illustrates a cross-sectional view of the formation of a transistor pair of FIG. 4, with the addition of a low-defect layer, a barrier layer, a cap layer, and a gate dielectric layer.

[0013] FIG. 6 illustrates a cross-sectional view of the formation of a transistor pair of FIG. 5, with the addition of trenches and vias.

[0014] FIG. 7 illustrates a cross-sectional view of the formation of a transistor pair of FIG. 6, after the formation of dielectric barriers, source contacts, drain contacts, gate contacts, and electrical connections from source to the n+ layer of the one-sided PN junction.

[0015] FIG. 8 illustrates a cross-sectional view of the transistor pair of FIG. 7 when electrically connected as a half bridge.

[0016] FIG. 9 illustrates a cross-sectional view of an alternative example embodiment for the transistor pair wherein dielectric barriers are formed using plural dielectric members.

[0017] FIG. 10 illustrates a cross-sectional view of the formation of a transistor pair according to alternative example embodiments, including a substrate with etched regions.

[0018] FIG. 11 illustrates a cross-sectional view of the formation of a transistor pair of FIG. 10, with the addition of n+ regions formed along the etched region surfaces.

[0019] FIG. 12 illustrates a cross-sectional view of the formation of a transistor pair of FIG. 11,

with the addition of various GaN transistor layers formed within the area inside the n+ regions.

[0020] FIG. 13 illustrates a cross-sectional view of the formation of a transistor pair of FIG. 12, with the addition of source, drain, and gate contacts.

[0021] FIG. 14 illustrates a cross-sectional view of the formation of a transistor pair of FIG. 13, with the addition of electrically floating regions for spreading the surface electric field.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0022] FIGS. 2 through 9 illustrate cross-sectional views of the formation of a transistor pair 20 according to example embodiments, which includes two GaN field-effect transistors (FETs). Certain materials, process details, and dimensions are omitted, as they are otherwise known and not necessary to demonstrate the scope of example embodiments.

[0023] Referring to FIG. 2, transistor pair 20 is formed in connection with a semiconductor substrate 22, such as a silicon wafer or other substrate appropriate for fabrication of GaN FETs. In the example embodiment, substrate 22 is a p-semiconductor material, meaning a lightly doped p- type semiconductor material. For example, such a doping concentration may be in the range of 1e13/cm3 to 3e20/cm3. A region or layer 24 of semiconductor material, complementary to substrate 22, is formed (e.g., grown or implanted) along an upper surface of substrate 22. In the example illustrated, because substrate 22 is p-type material, then layer 24 is n-type material. Moreover, layer 24 is preferably heavily doped, relative to substrate 22, so FIG. 2 illustrates that layer 24 is n+ in doping level. For example, such a doping concentration may be in the range of 1e18/cm3 to 1e21/cm3. Therefore, given the preceding, the combination of the lesser-doped substrate 22 and the greater-doped layer 24 provides a one-sided PN junction, as described hereinbelow. Moreover, this or a comparable one-sided PN junction can be formed by growing a low doped n- type silicon ($1e13/cm^3$ to $1e18/cm^3$) layer on highly doped p+ substrate ($1e18/cm^3$ to $3e21/cm^3$) or growing a low doped ($1e13/cm^3$ to $1e18/cm^3$) p-type silicon layer on highly doped p+ substrate ($1e18/cm^3$ to $3e21/cm^3$) and subsequently forming a n+ region ($1e18/cm^3$ to $3e21/cm^3$) on top of the grown low doped silicon films.

[0024] Referring to FIG. 3, additional fabrication steps and items are represented. Specifically, a mismatch isolation layer 26 is formed on layer 24, and is so named as to establish isolation and deal with the mismatch, such as in lattice structure, between the semiconductor material of layer 24 and what will be layers that include III-N layers above layer 24. For example,

mismatch isolation layer 26 may be 10 to 1500 nanometers of aluminum nitride. A buffer layer 28 is formed on mismatch isolation layer 26. For example, buffer layer 28 may be 1 to 7 microns thick and include a stack of several layers, starting with a bottom layer of the stack that is an aluminum rich compound with lesser gallium and transitioning to one or more layers toward the top of the stack, that is, with a greater amount of gallium and a lesser amount of aluminum. Thus, without limitation to a particular stoichiometry of the elements, these materials may be indicated as AlxGa1-xN, where x decreases toward the upper surface of buffer layer 28.

[0025] Referring to FIG. 4, an additional fabrication step and corresponding item is represented. Specifically, an electrical isolation layer 30 is formed on buffer layer 28. For example, electrical isolation layer 30 may be 50 to 4000 nanometers of semi-insulating gallium nitride. The semi-insulating aspect of electrical isolation layer 30 may provide a desired level of electrical isolation between layers below electrical isolation layer 30 and layers above it. Alternatively, electrical isolation layer 30 may be doped with n-type or p-type dopants to reduce undesired effects of charge trapping on current density in transistor pair 20.

[0026] Referring to FIG. 5, additional fabrication steps and corresponding items are represented. A low-defect layer 32 is formed on electrical isolation layer 30. For example, low-defect layer 32 may be 25 to 2000 nanometers of gallium nitride. Low-defect layer 32 may be formed so as to minimize crystal defects that may have an adverse effect on electron mobility. The method of formation of low-defect layer 32 may result in the low-defect layer 32 being doped with carbon, iron, or other dopant species, such as with a doping density less than 1e17/cm3.

[0027] Continuing with FIG. 5, a barrier layer 34 is formed on low-defect layer 32. For example, barrier layer 34 may be 2 to 30 nanometers of: AlxGa1-xN; or InxAlyGa1-x-yN by including indium. For example, a composition of group III elements in the barrier layer 34 may be 15 to 35 percent aluminum nitride and 85 to 65 percent gallium nitride. Forming barrier layer 34 on low-defect layer 32 generates a two-dimensional electron gas in low-defect layer 32 just below barrier layer 34 with an electron density, that is, a sheet charge carrier density, such as 1(10)12 to 2(10)13/cm2. During formation of electrical isolation layer 30 and/or low-defect layer 32, n-type dopants are added so that a sheet charge carrier density of electrical isolation layer 30 and low-defect layer 32 provides a screen for trapped charges and image charges below the two-dimensional electron gas. For example, the added n- type dopants may include mostly silicon and/or germanium dopants. The added n-type dopants may be added during epitaxial growth of

electrical isolation layer 30 and/or low-defect layer 32. Alternatively, the added n-type dopants may be added by ion implantation after electrical isolation layer 30 and/or low-defect layer 32 is formed. For example, an average doping density of the added n-type dopants may be 1e16/cm3 to 1e17/cm3. A distribution of the added n-type dopants may be substantially uniform, or may be graded so that a doping density is higher at a bottom of the doped region than at a top of the doped region.

[0028] Completing FIG. 5, an optional cap layer 36 may be formed on barrier layer 34. For example, cap layer 36 may be 1 to 5 nanometers of gallium nitride. Lastly, a gate dielectric layer 38 may be formed over barrier layer 34, and cap layer 36 if present, to provide a desired threshold voltage. For example, gate dielectric layer 38 may include silicon nitride.

[0029] Referring to FIG. 6, additional fabrication steps are represented in anticipation of forming additional structures. Specifically, in FIG. 6, isolation trenches 40 are formed by etching an aperture through all of the above-described layers and partially into substrate 22. The dimensions of trenches 40 may be selected in view of considerations discussed below. Trenches 40 operate to provide isolation between adjacent GaN FET transistors. Also in FIG. 6, source etches 42 are formed by etching an aperture through the two uppermost layers, namely, cap layer 36 and gate dielectric 38, and further through a majority of the thickness of barrier layer 34, leaving an amount of barrier layer 34 so as to achieve a desirably low contact resistance. As either part of the same etch step that forms source etches 42, or as a separate etch, vias 44 are formed from etches 42 down to at least an upper surface of layer 24, which recall is the n+ portion of the one-side PN junction as formed also with the p- substrate 22; for purposes of illustration, such vias 44 are shown as conical in cross-section, but an acceptable alternative would be forming them with a vertical sidewall(s). Lastly, also as either part of the same etch step that forms source etches 42, or as a separate etch, drain etches 46 are formed by etching an aperture through the two uppermost layers, namely, cap layer 36 and gate dielectric 38, and further through a majority of the thickness of barrier layer 34, preferably to the same depth as source etches 42.

[0030] Referring to FIG. 7, additional fabrication steps are represented in anticipation of forming additional structures. In FIG. 7, trenches 40 from FIG. 6 are filled with dielectric material to form dielectric barriers 48, such as using silicon dioxide, silicon nitride or polyamide as the dielectric material. Further, vias 44 from FIG. 6 are filled with respective conductors 50, such as metal or doped semiconductor, providing an electrical contact to layer 24. Still further, source etches 42

from FIG. 6 are filled with conductors, preferably metal, to form source contacts 52. The bottom of each source contact 52 extends into, but not fully through, barrier layer 34, so as to form a tunneling connection to the two- dimensional electron gas in the low-defect layer 32. Similarly, drain etches 46 from FIG. 6 are likewise filled with conductors, preferably metal, to form drain contacts 54 that extend into, but not fully through, barrier layer 34, so as to form a tunneling connection to the two-dimensional electron gas in the low-defect layer 32. Finally, gate conductors 56 are formed between each respective set of a source contract 52 and a drain contact 54, where each such gate conductor 56 is in contact with gate dielectric layer 38. For example, each of gates conductors 56 may include III-N semiconductor material to provide a depletion mode FET, while other types of gates are within the scope of this example.

[0031] Given the added elements of FIG. 7, transistor pair 20 includes two GaN FETs, shown generally as T'1 and T'2. Moreover, for each such FET, its gate conductor 56 may be laterally separated from its respective source contact 52, such as by 500 to 5000 nanometers, while the lateral spacing distance between each gate 56 and a respective drain contact 54 is by a distance that depends on a maximum operating voltage of the FET. For example, in a GaN FET designed for a maximum operating voltage of 200 volts, its drain contact 54 may be laterally separated from its gate conductor 56 by 1 to 8 microns. In a GaN FET designed for a maximum operating voltage of 600 volts, its drain contact 54 may be laterally separated from its gate conductor 56 by 8 to 30 microns.

[0032] FIG. 7 also illustrates the example embodiment isolating effect of dielectric barriers 48. Looking by example to transistor T'1, the dielectric barrier 48 in the middle of the page represents a first dielectric barrier along the left edge of the transistor, where that edge occurs vertically across multiple different layers, including barrier layer 34, low defect layer 32, electrical isolation layer 30, buffer layer 28, mismatch isolation layer 26, the n+ doped layer 24, and to a depth toward substrate 22 and below the one-sided PN junction formed between substrate 22 and layer 24. Similarly, the dielectric barrier 48 to the right of the page represents a second dielectric barrier along a second edge of those same layers. These barriers, therefore, serve to isolate transistor T'1, and other comparably isolated devices like transistor T'2, by interrupting the continuity of the layers and also extending below the one-sided PN junction. The benefits of such isolation are also further discussed later.

[0033] FIG. 8 repeats the illustration of transistor pair 20 from FIG. 7, but adds a depiction of

schematic connections so that a half bridge 60 is formed using transistors T'1 and T'2. Generally, the source/drain and gate connections from half bridge 60 are comparable to those of half bridge 10 from FIG. 1, where apostrophes are added to reference identifiers in FIG. 8 to distinguish FIG. 8 from FIG. 1. Nonetheless, in general, the half bridge configuration is readily understandable. However, beyond these connections, further various aspects arise from the example embodiment structure of FIGS. 7 and 8. Specifically, in FIG. 8, each source contact 52 is electrically connected to layer 24, which recall is an n+ doped layer that, in combination with substrate 22, provides a one-sided PN junction. As is often the case for various semiconductor wafers, substrate 22 is connected to ground. Also, each dielectric barrier 48 provides isolation as between a transistor and any laterally-neighboring structure, where the dielectric barrier 48 shown in the middle of FIG. 8 separates the layers forming transistor T'_1 from the layers forming transistor T'_2. Such separated layers include layer 24. As a result of the insulating separation, and further due to the connectivity provided by conductors 50 extending downward from each respective source contact 52, different PN biases are achieved for the one-sided PN junction in each respective transistor. More specifically, for transistor T'_1, its respective segment of layer 24 receives a bias of V_{out} (from its source $S(T'_1)$), while the portion of semiconductor substrate 22 between the dielectric barriers 48 for that transistor is grounded. In contrast, for transistor T'_2, its respective segment of layer 24 receives a bias of ground (from its source $S(T'_2)$), while the portion of semiconductor substrate 22 between the dielectric barriers 48 for that transistor is also grounded. Therefore, when transistor T'_1 is on, such as when acting as the high side in half bridge 60, the one-sided PN junction between its segment of layer 24 and substrate 22 is very strongly reversed bias, thereby isolating the transistor from leakage concerns that arise, and were described above. Meanwhile, with respect to transistor T'_2, it is isolated by the example embodiment structure and has ground connected to both sides of its isolated one- sided PN junction, thereby facilitating its proper operation.

[0034] The isolating benefits achieved by the example embodiment structure, including the respective isolated one-sided PN junction for each respective transistor, also will suggest the dimensions and variations for each dielectric barrier 48. Accordingly, such dimensions are chosen to prevent a junction breakdown in the one-sided PN junction, given the anticipated or specified voltage levels. For example, in the approach of FIG. 8, each such barrier 48 may be one to three

times of Visolation/20V microns wide, where Visolation is an amount of needed isolation. Further, each such barrier 48 preferably extends to a distance in the range of one to three times of Visolation/20V microns below layer 24. Indeed, these considerations and dimensions demonstrate that other structures may be implemented within the example embodiment to achieve vertical isolation between otherwise neighboring GaN transistors. In this regard, FIG. 9 again illustrates the cross-sectional view of transistor pair 20 from FIG. 7, but each dielectric barrier 48 from FIG. 7 is replaced with a plural number of dielectric barriers 48', where each plurality in the example of FIG. 9 consists of four vertical dielectric barriers 48'. Once more, the dielectric material may be polyamide, silicon dioxide or silicon nitride, but the dimensions differ in that each dielectric barrier 48' may have a lesser width (such as 1μm to 10μm) and a lesser depth into substrate 22, such as a depth of 1μm to one to three times of Visolation/20V microns wide, by comparison to the depth given for dielectric barriers 48 in FIG. 7.

[0035] FIGS. 10 through 14 illustrate cross-sectional views of the formation of an additional alternative example embodiment transistor pair 20, which again will include two GaN FETs.

[0036] Referring to FIG. 10, transistor pair 20 is formed in connection with a semiconductor substrate 122, such as a silicon wafer or other substrate appropriate for fabrication of GaN FETs. In the example embodiment, substrate 122 is a p- semiconductor material (lightly doped p-type semiconductor material). Moreover, with appropriate masking and etching (e.g., dry etch of a <111> wafer or wet etch of a <100> waver) are performed so as to form two trenches 124 partially into substrate 122. The dimensions of trenches 124 may be selected in view of considerations discussed below, but trenches 124 operate to provide the active area, and some isolation, between a GaN FET transistor formed in each trench, as described hereinbelow. Also, the sidewalls of trenches 124 may be vertical or sloped, depending on etch conditions.

[0037] FIG. 11 illustrates additional fabrication steps and items. Specifically, a region or layer 126 of semiconductor material, complementary to substrate 122, is formed (e.g., grown or implanted) along an upper surface of each trench 124 (i.e., parallel to the plane of substrate 122), and also along each sidewall of each trench 124. For example, a quad implant may be used to alternate positioning of substrate 122 so as to implant layer 126 along these exposed trench surfaces in substrate 122, whereby layer 126 thereby extends both along the bottom of the trench and upward toward the upper surface of substrate 122. In the example illustrated, because substrate 122 is p-type material, then layer 126 is n-type material. Moreover, layer 126 is

preferably heavily doped, relative to substrate 122, so FIG. 11 illustrates that layer 126 is n+ in doping level (e.g., 1e18/cm3 to 1e21/cm3). Again, therefore, the combination of the lesser-doped substrate 122 and the greater-doped layer 126 provides a one-sided PN junction, as further appreciated from the teachings in this document. As with other example embodiments, this or a comparable one- sided PN junction can be formed by growing a low doped n-type silicon (1e13/cm3 to 1e18/cm3) layer on highly doped p+ substrate (1e18/cm3 to 3e21/cm3) or growing a low doped (1e13/cm3 to 1e18/cm3) p-type silicon layer on highly doped p+ substrate (1e18/cm3 to 3e21/cm3) and subsequently forming a n+ region (1e18/cm3 to 3e21/cm3) on top of the grown low doped silicon films.

[0038] Referring to FIG. 12, additional fabrication steps and items are represented. Specifically, in FIG. 12, the remaining open region from trenches 124 (see FIG. 10) are filled with additional layers toward ultimately forming a respective GaN FET in each trench, along the already-formed layer 126, where reference number are repeated in FIG. 12 from the embodiment of FIG. 5, where such layers were detailed. Thus, in FIG. 12, such layers include a mismatch isolation layer 26, a buffer layer 28, an electrical isolation layer 30, a low-defect layer 32, a barrier layer 34, an optional cap layer 36, and a gate dielectric layer 38.

[0039] Referring to FIG. 13, additional fabrication steps are represented. Specifically, trenches (not shown) are formed from the upper surface illustrated in FIG. 12 and filled with conductors, preferably metal, to form source contacts 128. The bottom of each source contact 128 extends into, but not fully through, barrier layer 34, so as to form a tunneling connection to the two-dimensional electron gas in the low-defect layer 32. However, each source contact 128 also contacts or, optionally through an intermediate conductor (not shown), electrically communicates with layer 126 and preferably to the portion of that layer that extended upward toward the surface of substrate 122. However, from an electrical standpoint, this connectivity is like the combination of a source contact 52 and a conductor 50 as shown in the embodiment of FIG. 7, in that the embodiment of FIG. 13 also connects the source potential to the one-sided PN junction at the bottom of the GaN transistor. Also in connection with FIG. 13, in the same (or comparable) process that forms source contacts 128, drain etches (not shown) are likewise filled with conductors, preferably metal, to form drain contacts 130 that extend into, but not fully through, barrier layer 34, so as to form a tunneling connection to the two-dimensional electron gas in the low-defect layer 32. Finally, gate conductors 132 are formed between each respective set of a

source contact 128 and a drain contact 130, where each such gate conductor 132 is in contact with gate dielectric layer 38.

[0040] FIG. 14 illustrates a final example embodiment structure added to that shown in FIG. 13. Specifically, in FIG. 13, additional electrically floating n+ regions 134 are formed through the upper surface of substrate 122 with appropriate masking (not shown), where in the example illustrated three such regions are formed between, and outside outer edges, of what is indicated generally as transistor pair 20 including two GaN FETs, shown generally as T''_1 and T''_2. Electrically floating n+ regions 134 operate to spread the electric field as depletion occurs and starts to expand at the surface, so that each region may acquire some voltage between the potential applied across each transistor (e.g., 0 to 600 volts). In this manner, the surface filed is reduced, such a below a certain level that is desired for device reliability.

[0041] From the above, various embodiments provide improvements to III-N semiconductor transistors, such as GaN FETs. While various dimensions have been provided, such measures may be adjusted according to application and other considerations. As an example, while an example embodiment half bridge has been described, the example embodiment structure may be used with individual FETs, FETs in other configurations, and an FET combined with devices other than FETs formed relative to a same substrate, yet isolating such FET from such devices using the example embodiment teachings. Indeed, various transistor components described herein also may be found in Patent No. U.S. 8,759,879, issued June 24, 2014, which is hereby incorporated herein by reference; this referenced Patent includes other transistor configurations that also may be readily combined with the teachings of this document. As still another example, while an example embodiment one-side PN junction has been described with respect to the substrate as part of the junction, in another example embodiment that junction may be achieved using GaN layers apart from the substrate. For example, a p-type/SI- GaN or AlGaN layer is grown on top of p+ silicon or suitable substrate with then an n+ layer formed on the surface of that p-type or SI-GaN by epitaxy or implant. Following this, all other layers may be similar to those described above, where the vias will be formed to contact the n+ III-nitride layer in this alternative.

[0042] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a substrate;

a low defect layer formed in a fixed position relative to the substrate;

a barrier layer comprising III-N semiconductor material formed on the low- defect layer and forming an electron gas in the low-defect layer;

a source contact;

a drain contact;

a gate contact for receiving a potential, the potential for adjusting the electron gas and a conductive path, responsive to and formed by the electron gas, between the source contact and the drain contact; and

a one-sided PN junction between the barrier layer and the substrate.

2. The semiconductor device of claim 1, further comprising:

a first dielectric barrier along a first edge of the low defect layer and a first edge of the barrier layer, the first dielectric barrier further extending in a direction from the low defect layer toward the substrate and to an extent below the one-sided PN junction; and

a second dielectric barrier along a first edge of the low defect layer and a second edge of the barrier layer, the second dielectric barrier further extending in a direction from the low defect layer toward the substrate and to an extent below the one-sided PN junction.

3. The semiconductor device of claim 2, wherein a single transistor is formed between the first dielectric barrier and the second dielectric barrier, the single transistor comprising the source contact, the drain contact, the gate contact, and the electron gas.

4. The semiconductor device of claim 3, further comprising a second transistor formed relative to the substrate and adjacent the first transistor, the second transistor isolated from the first transistor by the first dielectric layer.

5. The semiconductor device of claim 4, wherein the second transistor comprises a second one-sided PN junction, isolated from the one-sided PN junction of the first transistor by the first dielectric layer.

6. The semiconductor device of claim 5, wherein the second one-sided PN junction comprises an n-type region, and wherein the second transistor further comprises: a second source contact; and

a conductive member between the second source contact and the n-type region.

7. The semiconductor device of claim 6, further comprising electrical connectivity between the first transistor and the second transistor for forming a half bridge circuit.

8. The semiconductor device of claim 2, wherein the one-sided PN junction comprises an n-type region, and further comprising a conductive member between the source contact and the n-type region.

9. The semiconductor device of claim 8, wherein the one-sided PN junction further comprises a p-type region having a doping concentration lower than the n-type region.

10. The semiconductor device of claim 2, wherein the device has an isolation voltage, and wherein each of the first dielectric barrier and the second dielectric barrier has a width in a range of one to three times the isolation voltage divided by 20V microns wide.

11. The semiconductor device of claim 2, wherein the device has an isolation voltage, and wherein each of the first dielectric barrier and the second dielectric barrier has a depth below the one-sided PN junction in a range of one to three times the isolation voltage divided by 20V microns wide.

12. The semiconductor device of claim 2, wherein each of the first dielectric barrier and the second dielectric barrier comprises a plurality of dielectric barrier members.

13. The semiconductor device of claim 12, wherein each of the plurality of dielectric members has a width in a range of 1μm to 10μm.

14. The semiconductor device of claim 12, wherein the device has an isolation voltage, and wherein each of the plurality of dielectric members has a depth below the one-sided PN junction in a range of one to three times the isolation voltage divided by 20V microns wide.

15. The semiconductor device of claim 1, wherein the substrate comprises p-type material, and further comprising an n-type layer adjacent the substrate wherein the substrate and the n-type layer form the one-sided PN junction.

16. The semiconductor device of claim 15, further comprising a mismatch isolation layer adjacent the n-type layer.

17. The semiconductor device of claim 16, further comprising a buffer layer adjacent the mismatch isolation layer, the buffer layer comprising a first layer adjacent the mismatch isolation layer and a second layer, away from the mismatch isolation layer and adjacent the first layer; wherein the first layer and second layer comprise aluminum and gallium; and wherein the first

layer comprises more aluminum and less gallium than the
second layer.

18. The semiconductor device of claim 17, further comprising an electrical isolation layer adjacent the buffer layer.

19. The semiconductor device of claim 18, wherein the electrical isolation layer comprises semi-insulating gallium nitride.

20. The semiconductor device of claim 19, wherein the barrier layer is adjacent the electrical isolation layer.

21. The semiconductor device of claim 1, wherein the one-sided PN junction comprises a first layer comprising p-type gallium nitride and a second layer, adjacent the first layer, comprising n-type gallium nitride.

22. The semiconductor device of claim 1, wherein the one-sided PN junction comprises an n-type region.

23. The semiconductor device of claim 22, wherein the n-type region comprises a first portion substantially parallel to a plane along a length of the substrate and a second portion extending from the first portion to the barrier layer.

24. The semiconductor device of claim 22, wherein the source contact contacts the second portion.

25. A method of forming a semiconductor device relative to a substrate, comprising:

forming a low defect layer formed in a fixed position relative to the substrate;

forming a barrier layer comprising III-N semiconductor material formed on the low-defect layer and forming an electron gas in the low-defect layer;

forming a source contact;

forming a drain contact;

forming a gate contact for receiving a potential, the potential for adjusting the electron gas and a conductive path, responsive to and formed by the electron gas, between the source contact and the drain contact; and

forming a one-sided PN junction between the barrier layer and the substrate.

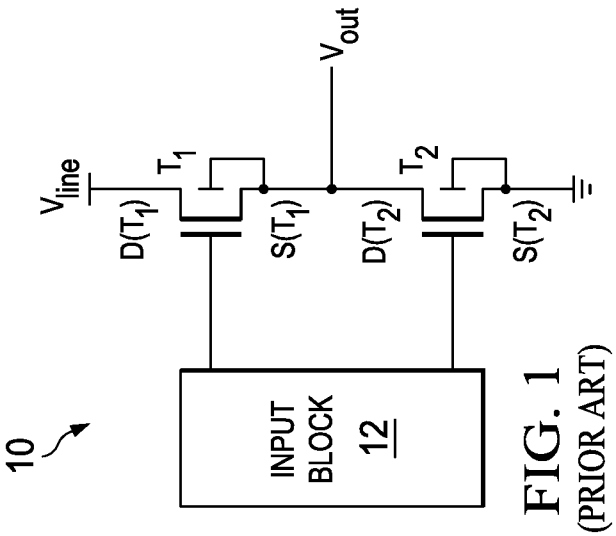


FIG. 1
(PRIOR ART)

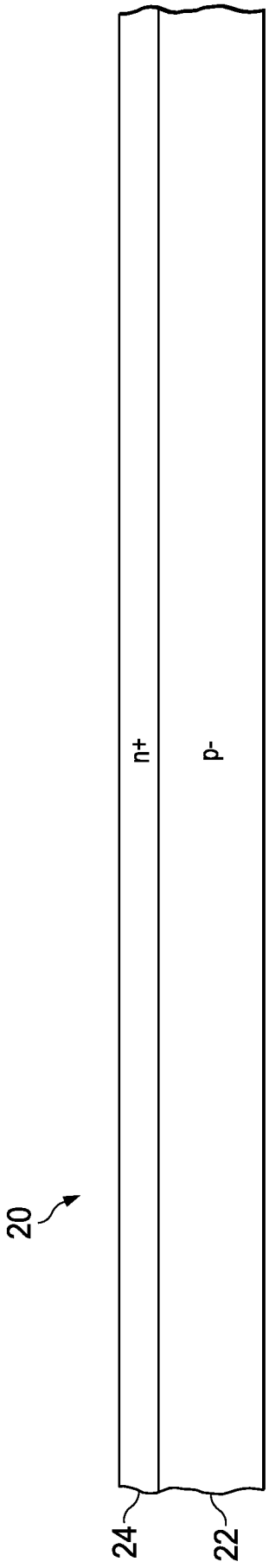


FIG. 2

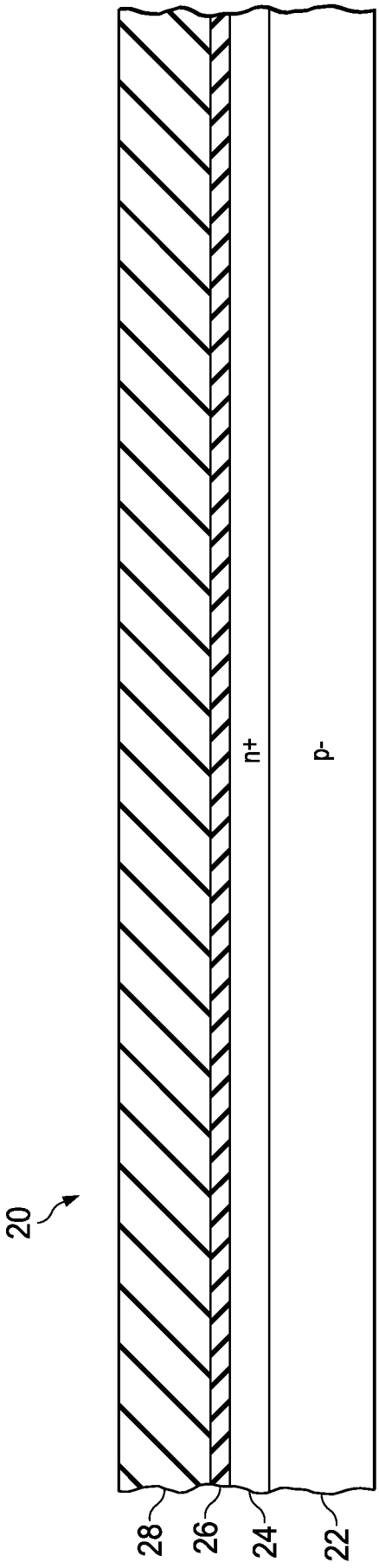


FIG. 3

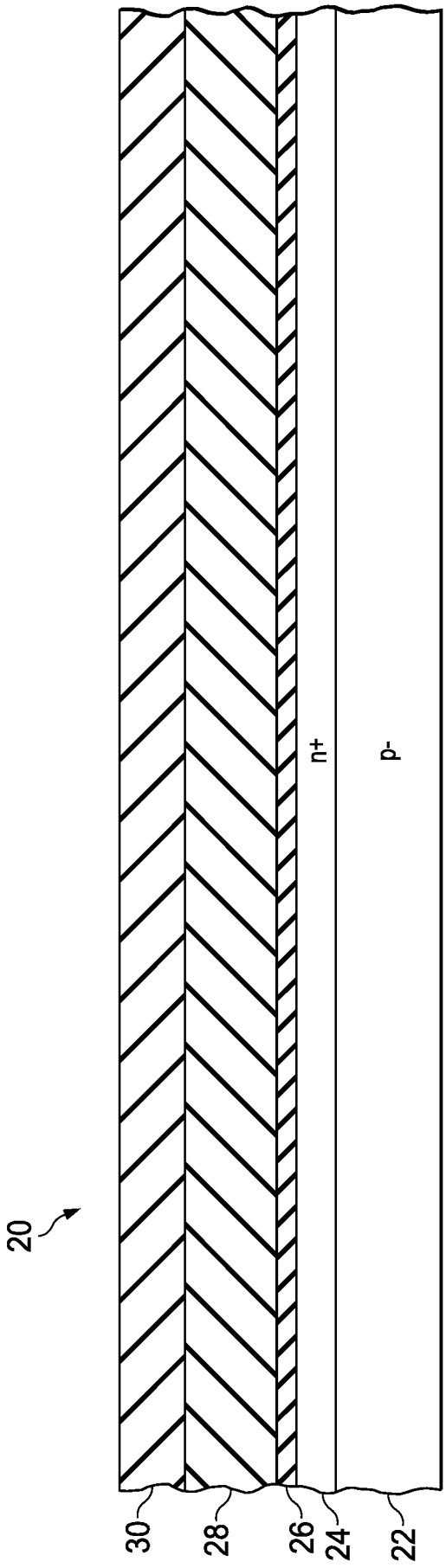


FIG. 4

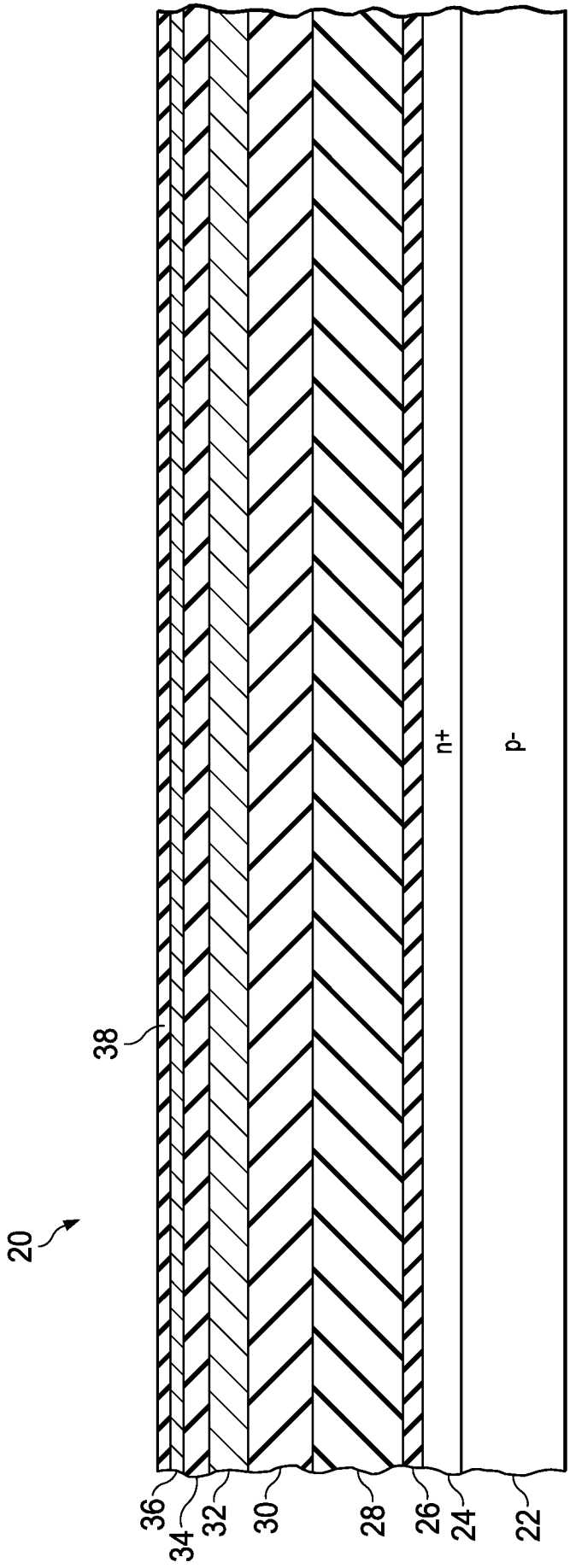


FIG. 5

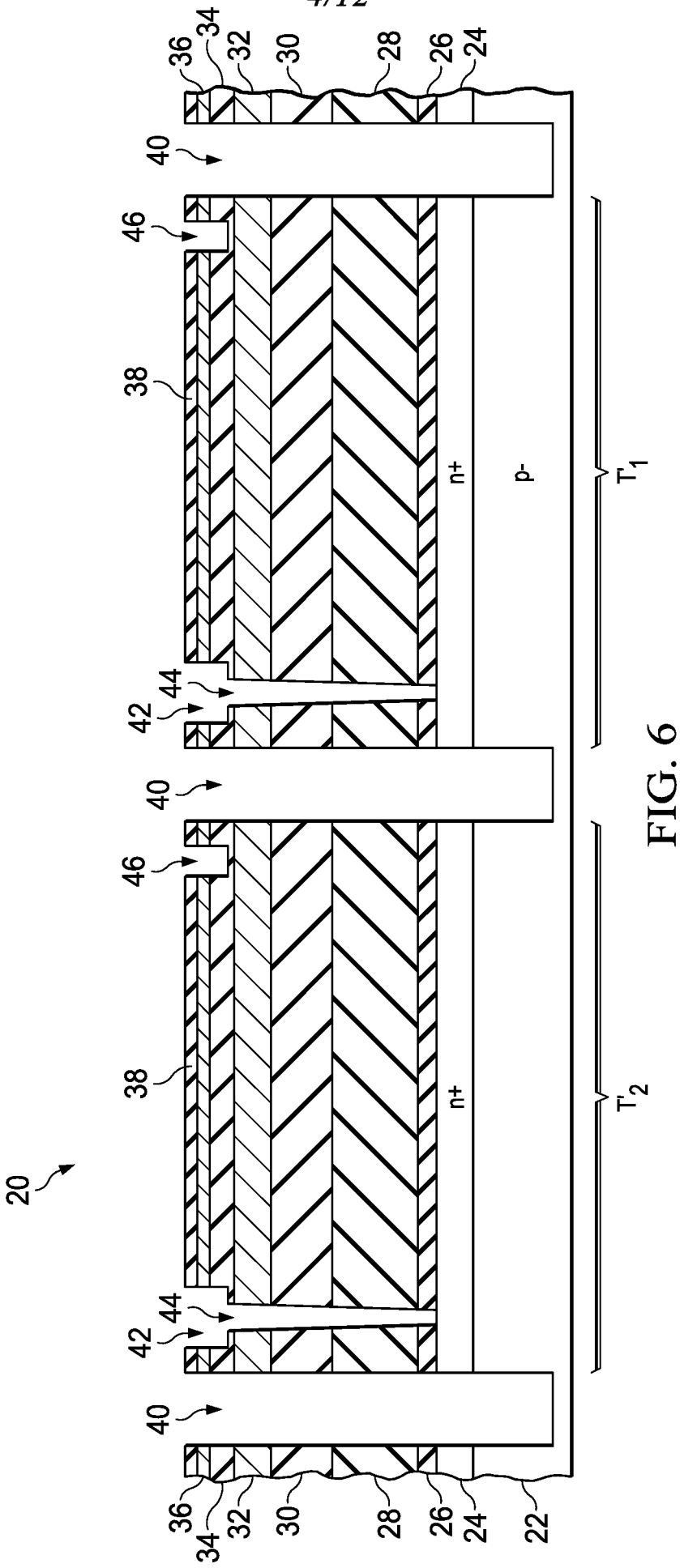


FIG. 6

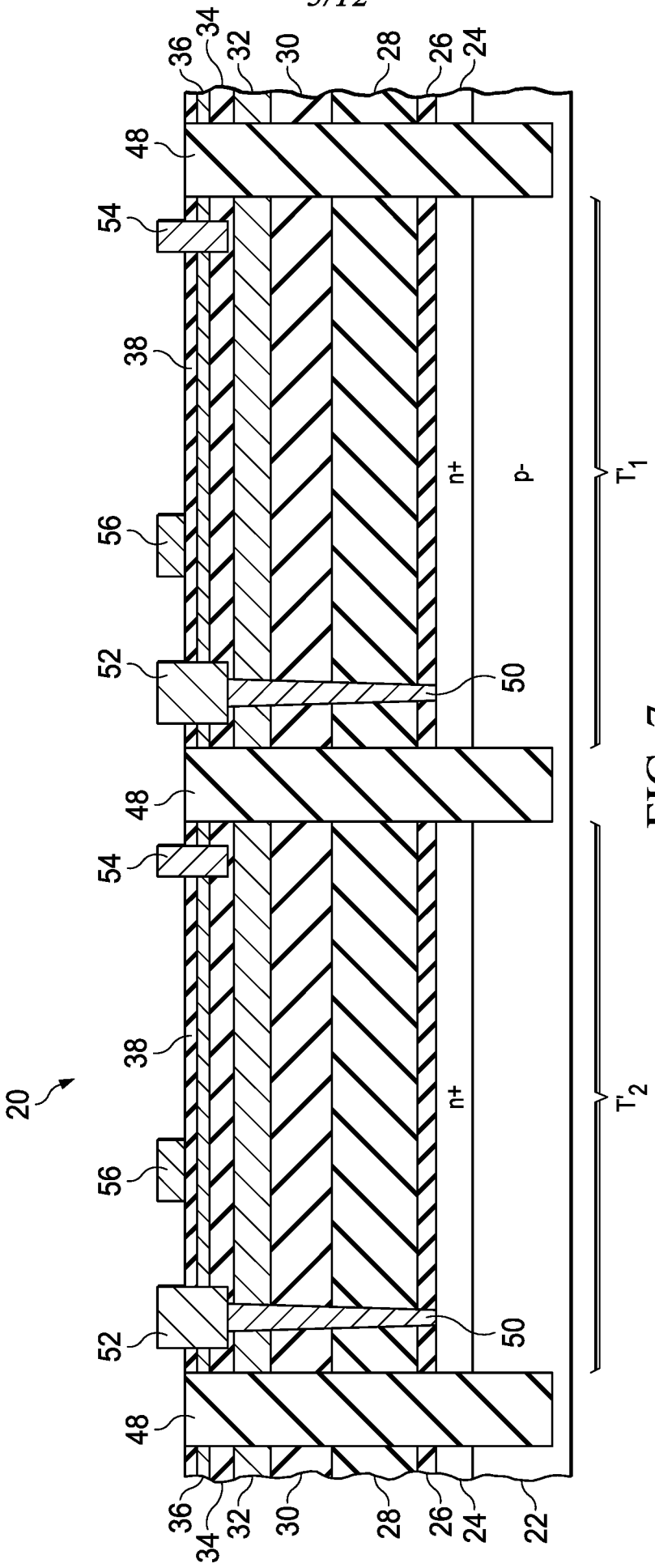
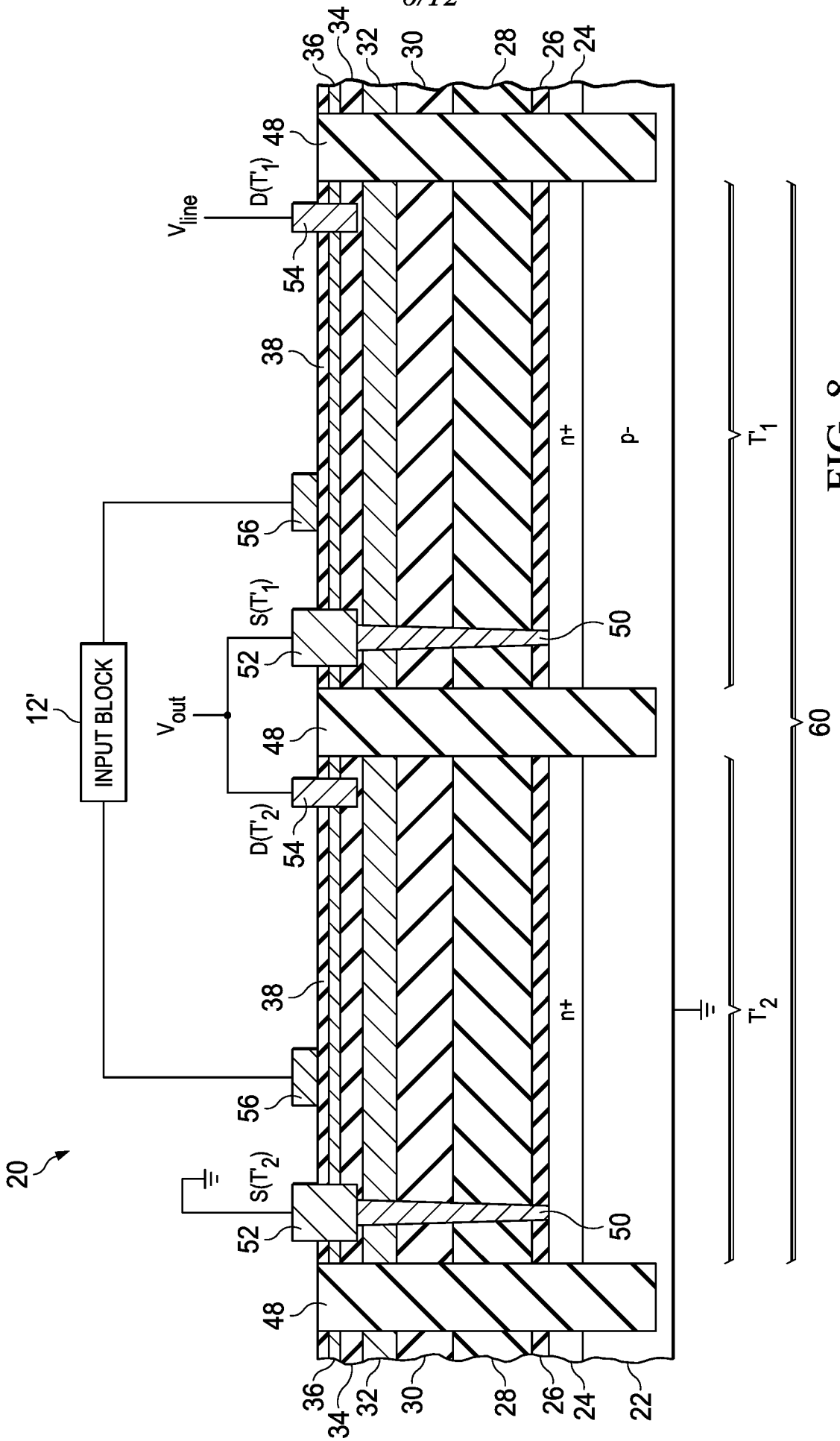


FIG. 7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12'
INPUT BLOCK
V_{line}
V_{out}
D(T'1)
D(T'2)
S(T'1)
S(T'2)
n+
p-
n+
T'1
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FIG. 8

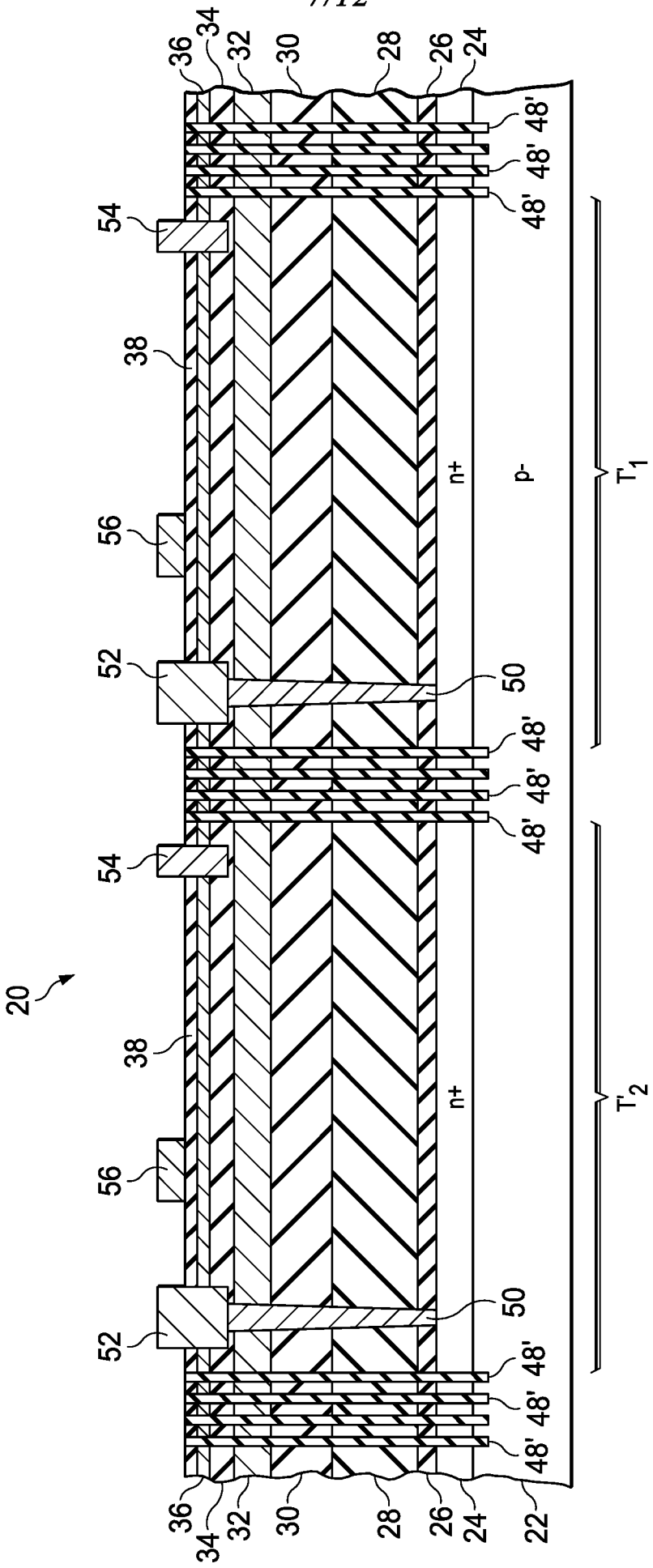


FIG. 9

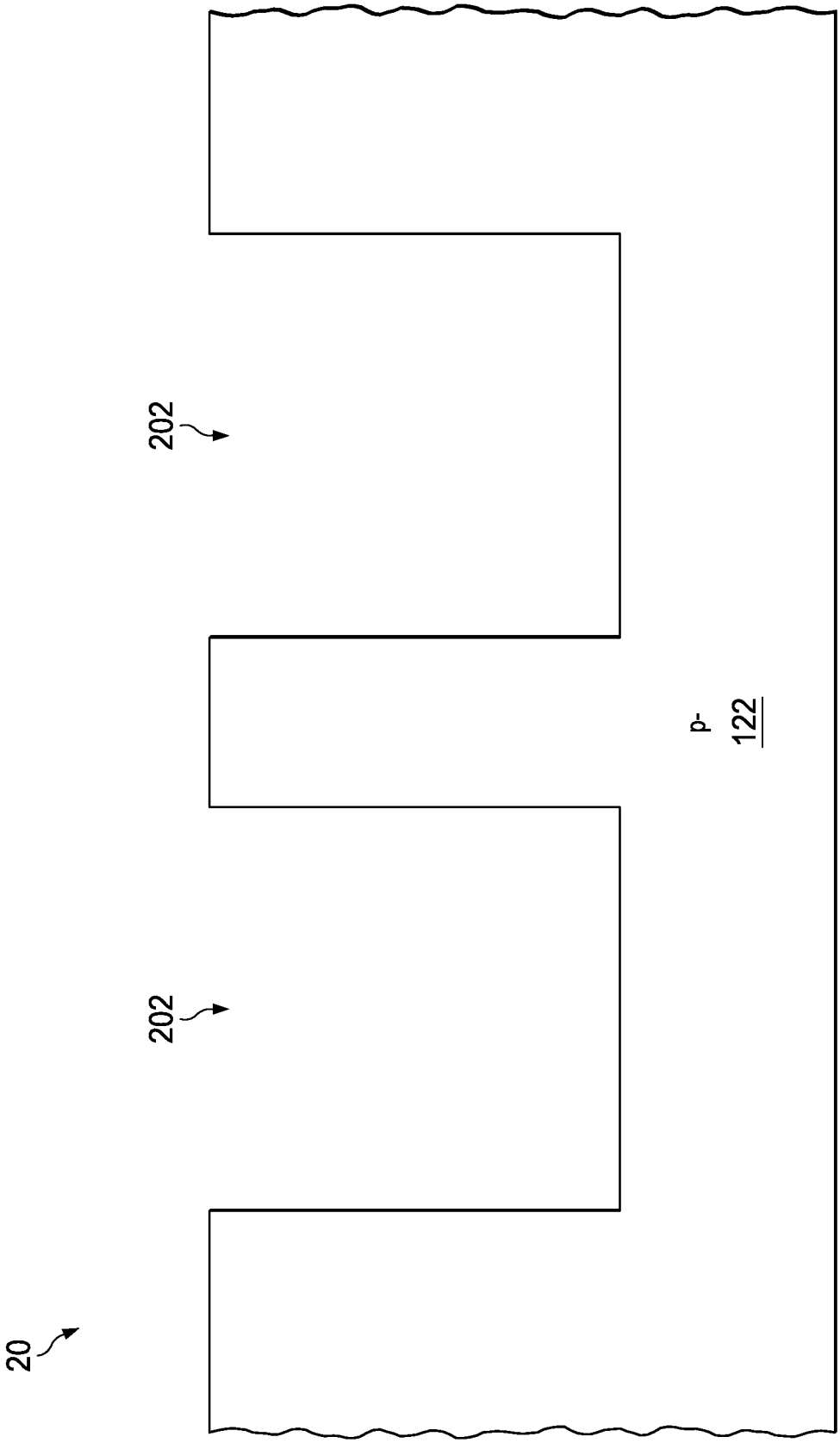


FIG. 10

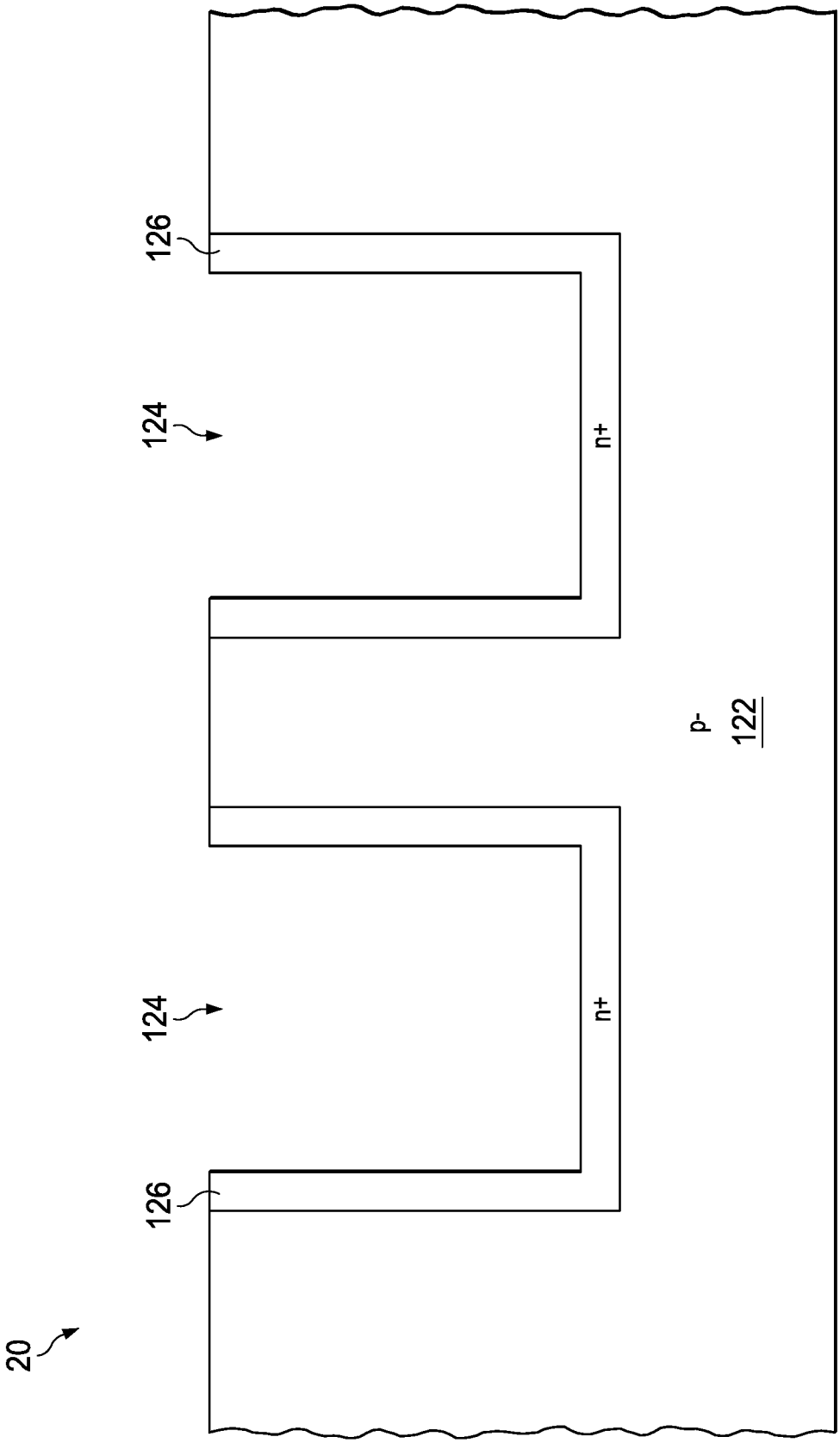


FIG. 11

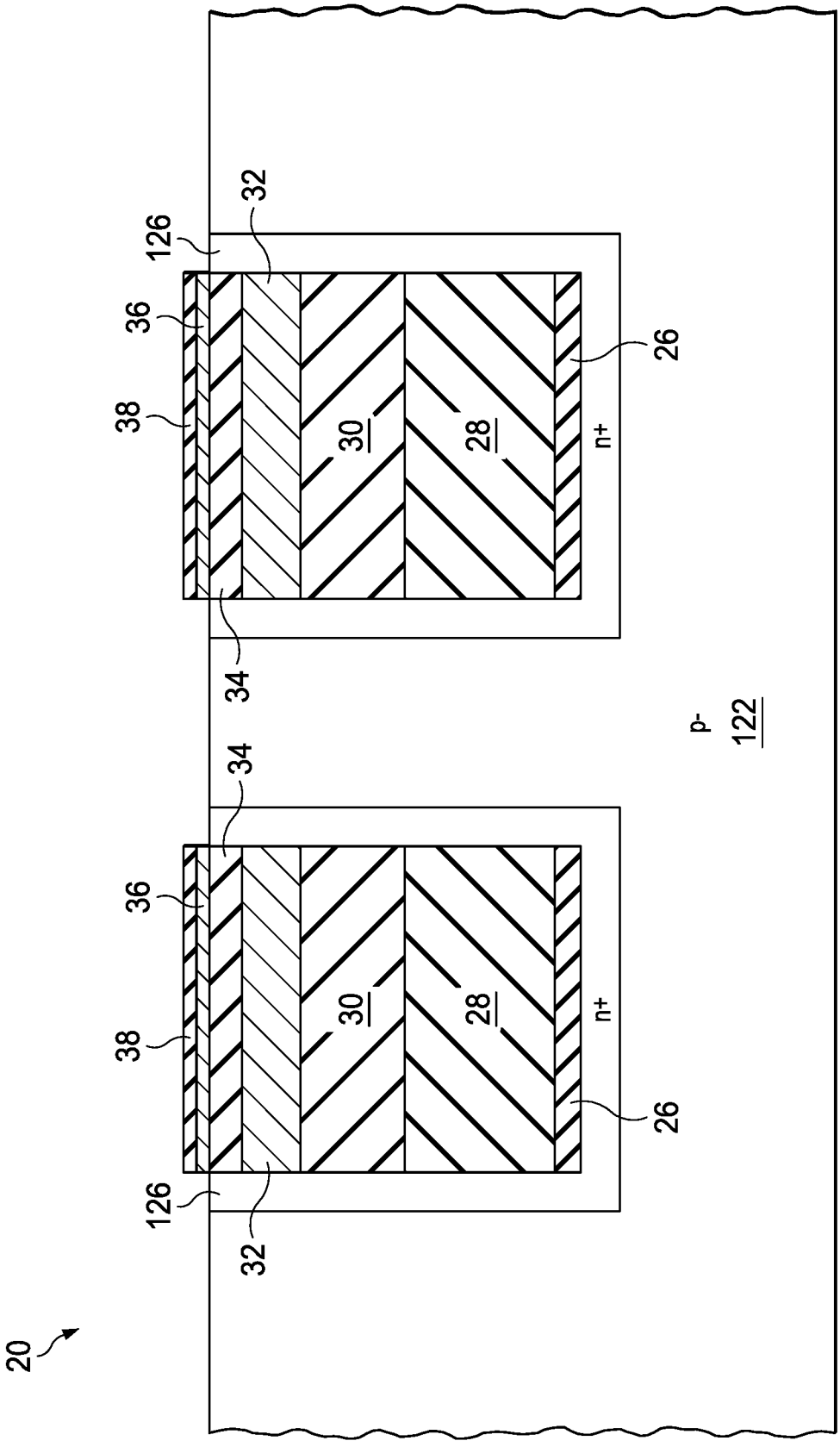


FIG. 12

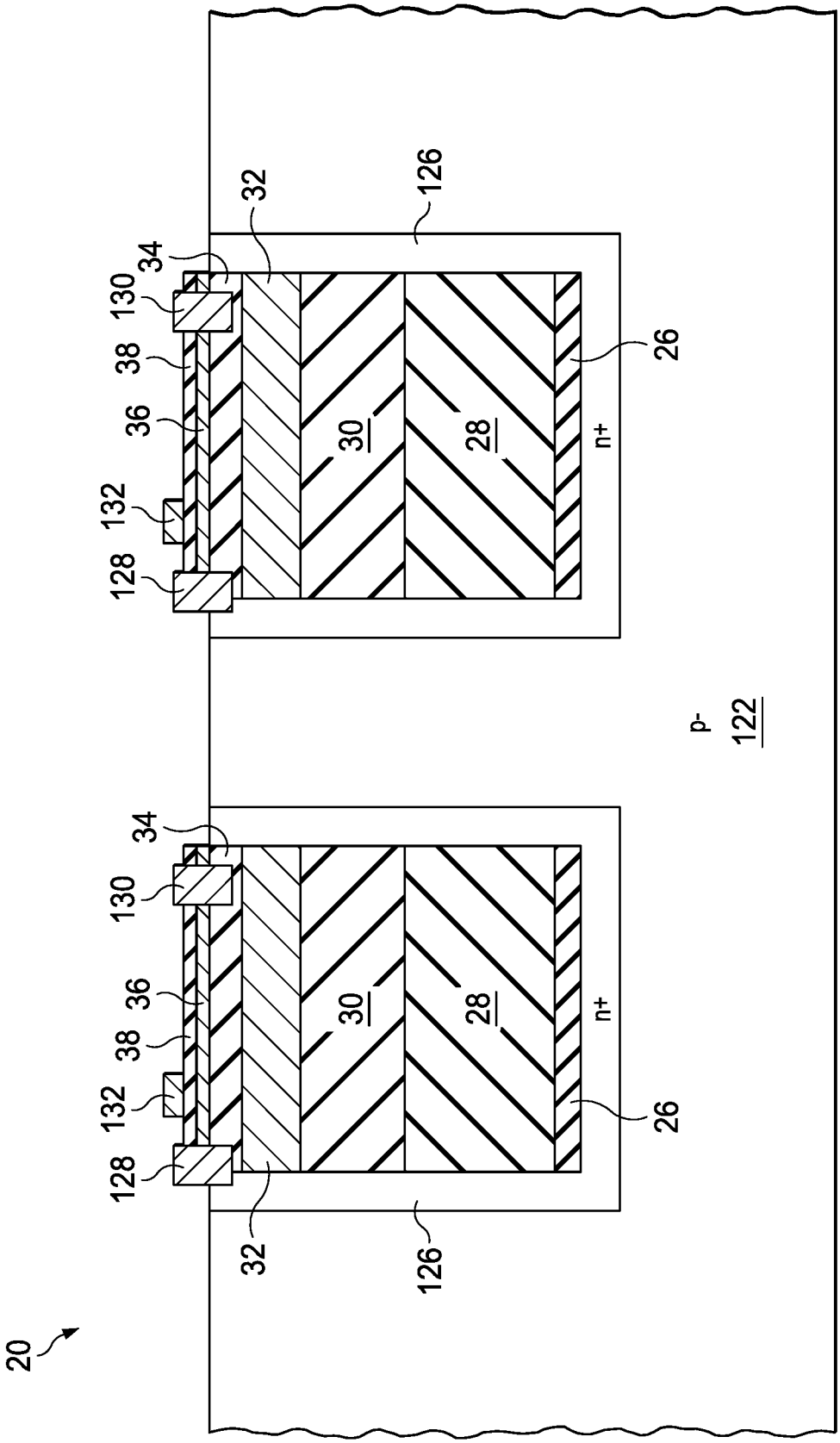
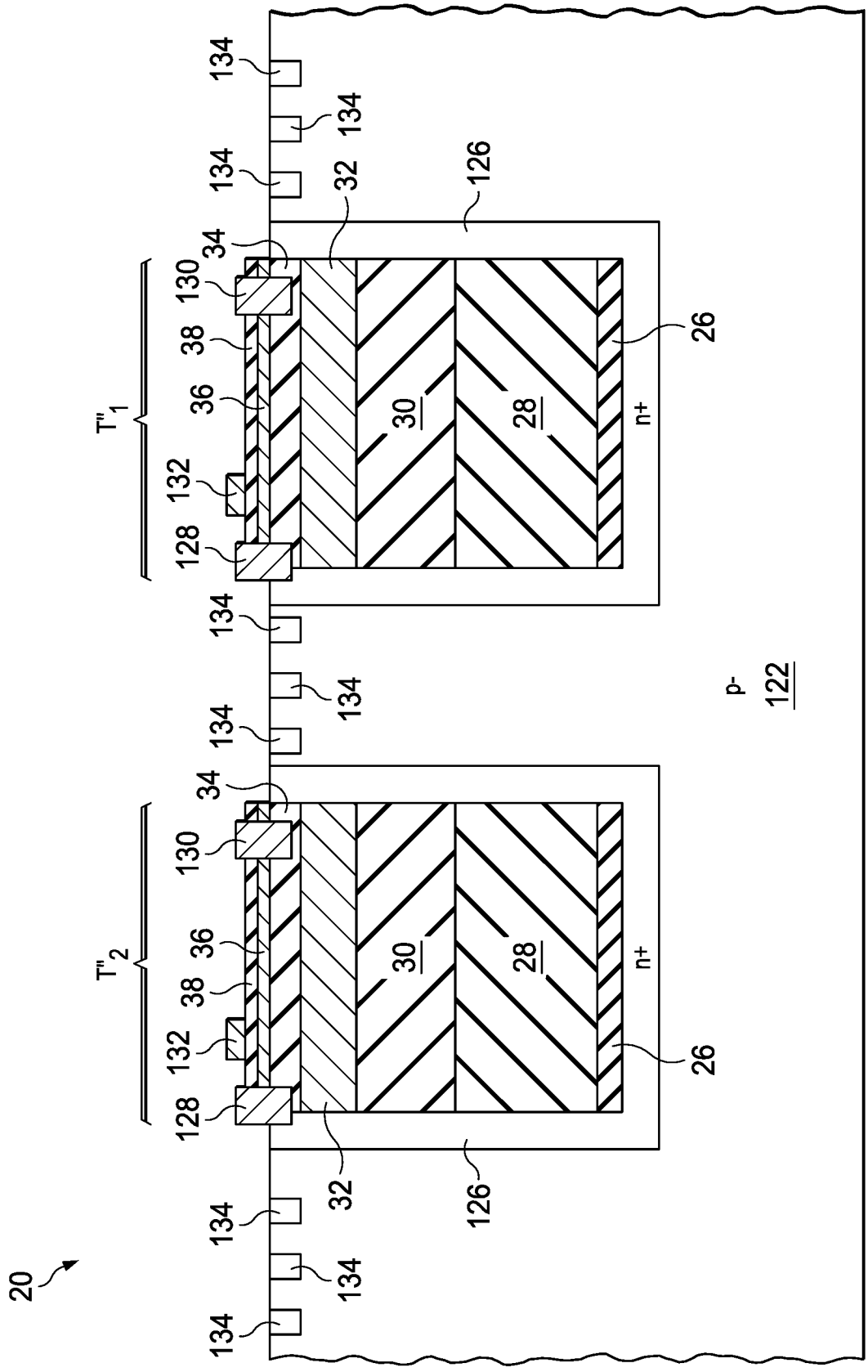


FIG. 13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T"1
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n+
26
p-
122
T"2

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2016/063778

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/335 *(2006.01)*
H01L 29/772 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/00-21/338, 29/00-29/772

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 8759879 B1 (TEXAS INSTRUMENTS INCORPORATED) 24.01.2014	1-25
A	US 2014/0327010 A1 (TEXAS INSTRUMENTS INCORPORATED) 06.11.2014	1-25
A	US 2011/0018002 A1 (THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY) 27.01.2011	1-25
A	US 2010/0117118 A1 (AMIR M.DABIRAN) 05.06.2003	1-25
A	US 2003/0102482 A1 (ADAM WILLIAM SAXLER) 13.05.2010	1-25

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 February 2017 (10.02.2017)	16 March 2017 (16.03.2017)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer I. Baginskaya Telephone No. (499) 240-25-91

Form PCT/ISA/210 (second sheet) (January 2015)