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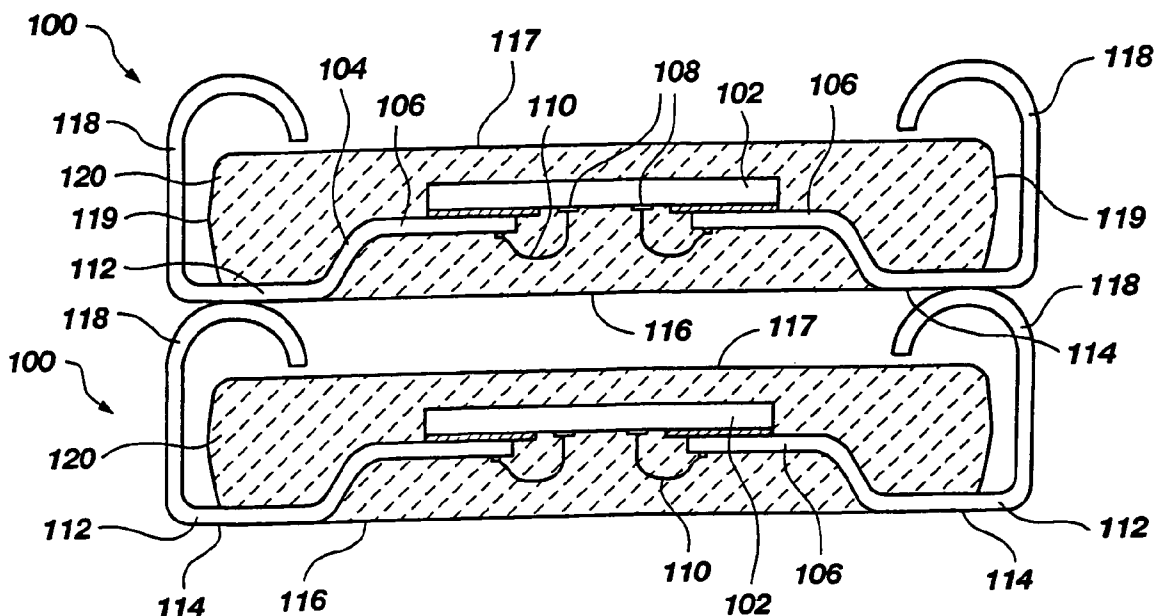
(57) **ABSTRACT**

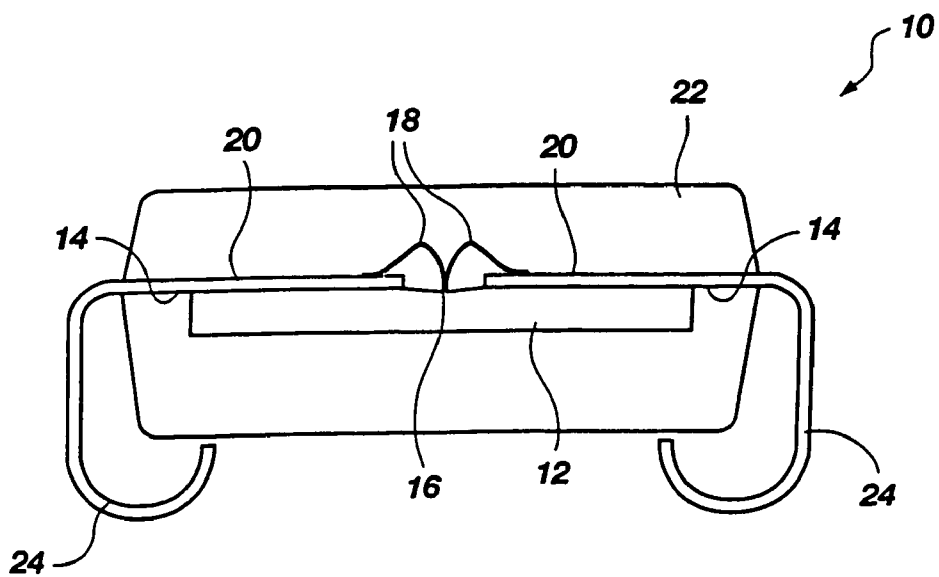
A packaged semiconductor device and method has bottom surface leads having portions of the package adjacent the lead edges excised. The outer leads may take the form of inverted-J leads, short stub leads, vertically bent leads-in-grooves, or may be entirely eliminated. Lead connections are on the bottom package surface, over the top package surface, and/or on the sides and ends of the package, enabling vertical stacking of the devices and simultaneous/alternative coplanar horizontal connections to other semiconductor devices, circuit boards, etc. A mold assembly with a castellated inner surface forms a package with alternating grooves and columns for holding side and end electrical connection surfaces.

(22) Filed: **Jan. 24, 2006**

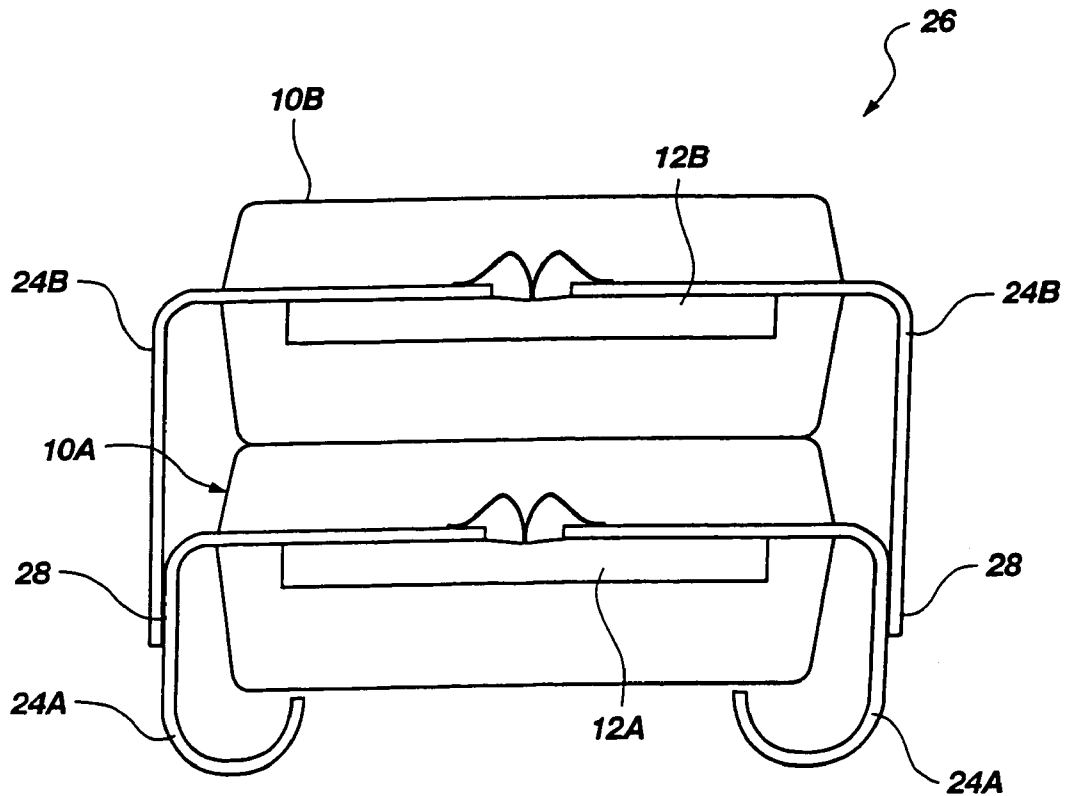
### Related U.S. Application Data

(60) Continuation of application No. 11/138,756, filed on May 25, 2005, which is a continuation of application No. 10/369,067, filed on Feb. 18, 2003, now Pat. No. 6,899,534, which is a continuation of application No. 09/819,909, filed on Mar. 28, 2001, now Pat. No. 6,537,051, which is a continuation of application No. 09/336,925, filed on Jun. 21, 1999, now Pat. No. 6,213,747, which is a division of application No.

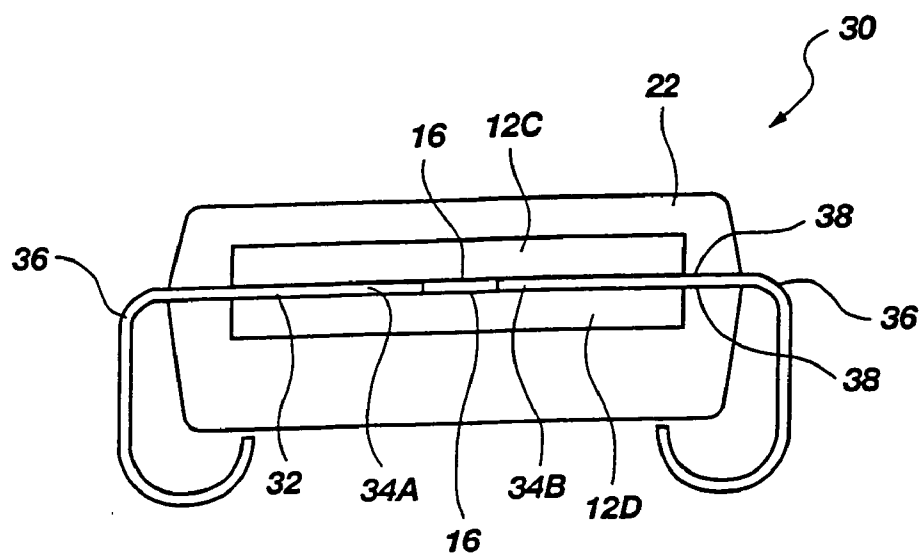




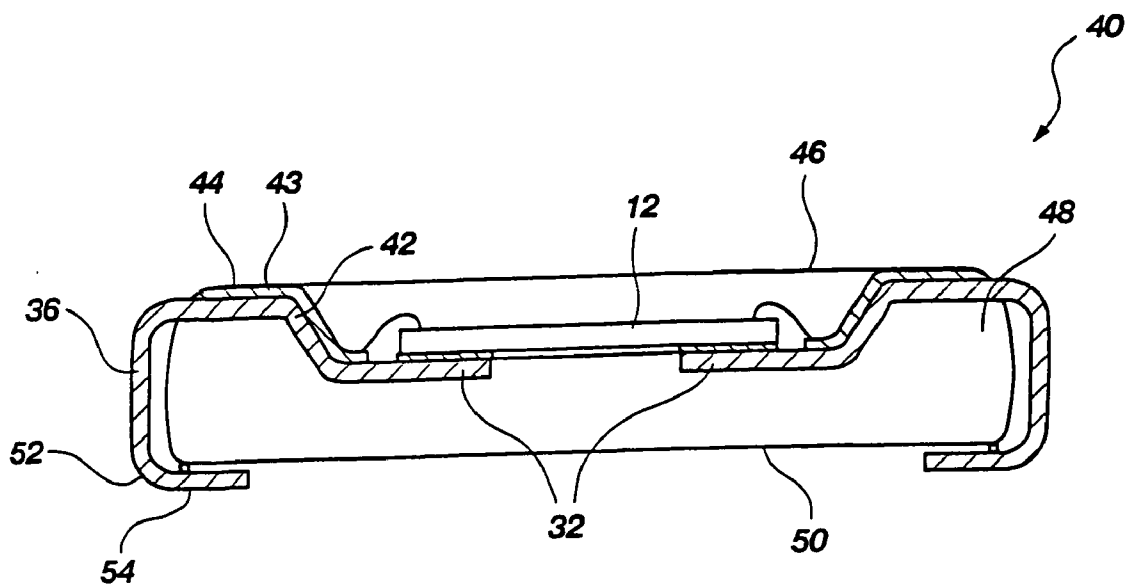
**Fig. 1**  
(PRIOR ART)



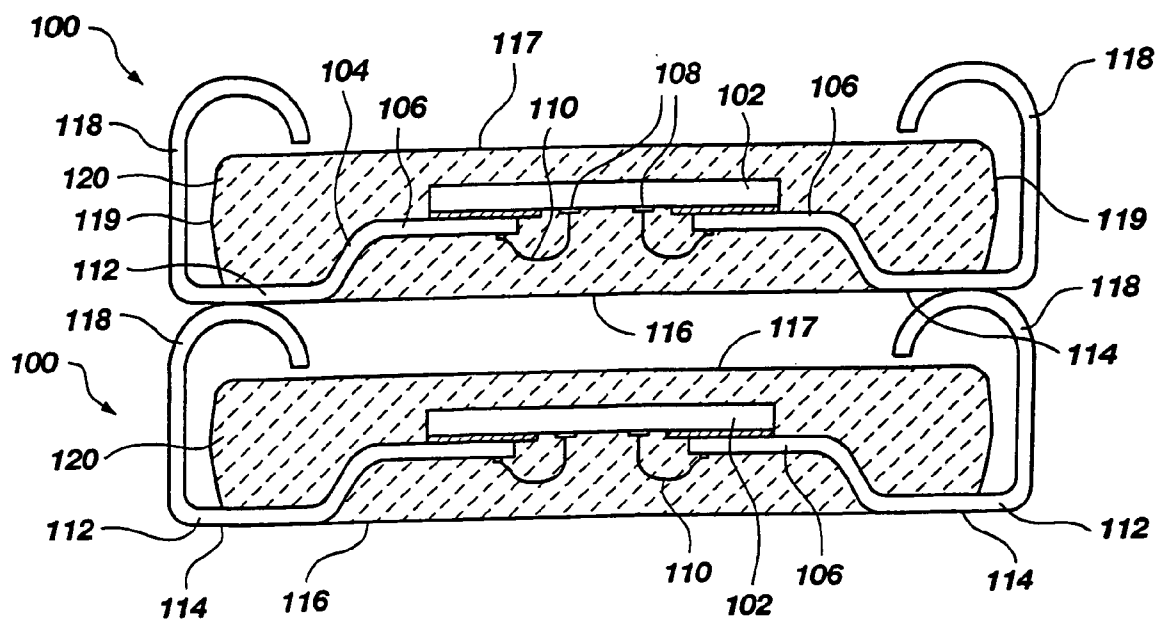
**Fig. 2**  
(PRIOR ART)



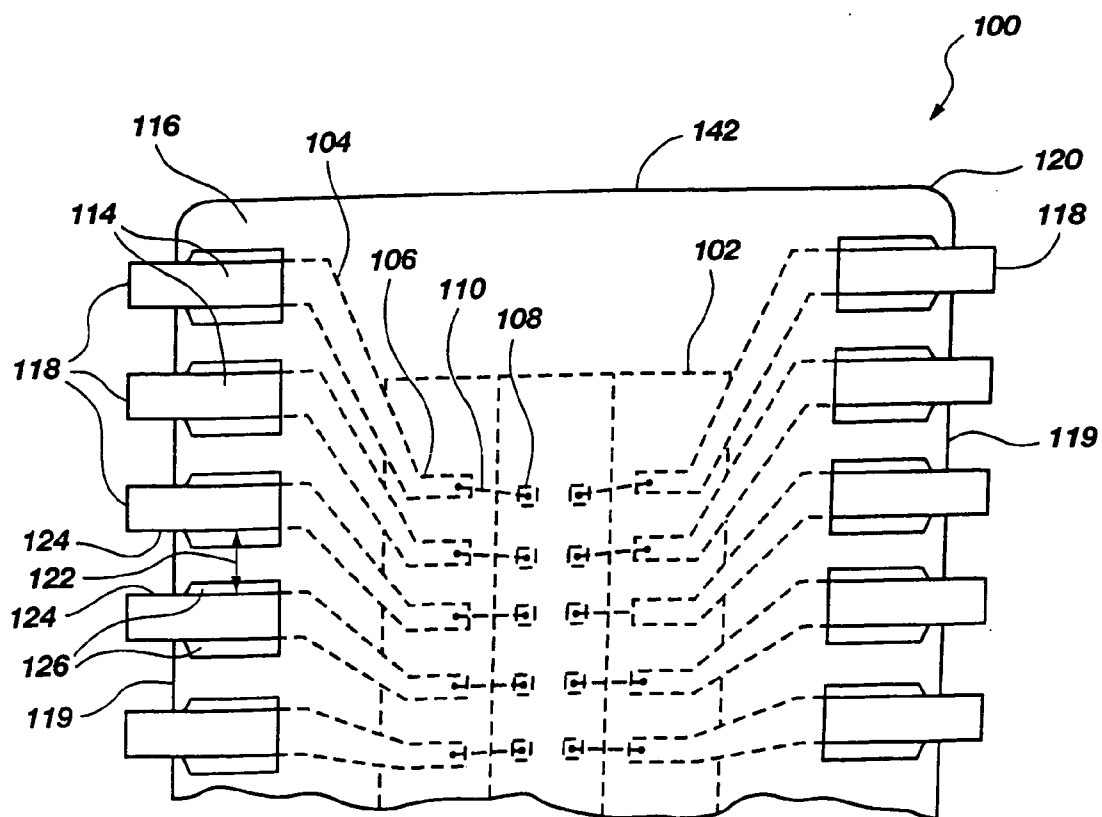
**Fig. 3**  
(PRIOR ART)



**Fig. 4**  
(PRIOR ART)



**Fig. 5**



**Fig. 6**

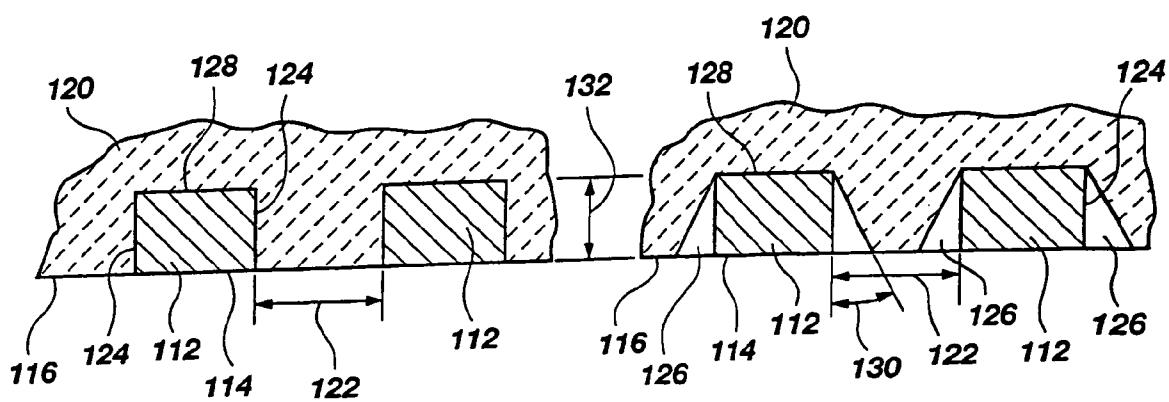


Fig. 7A

Fig. 7B

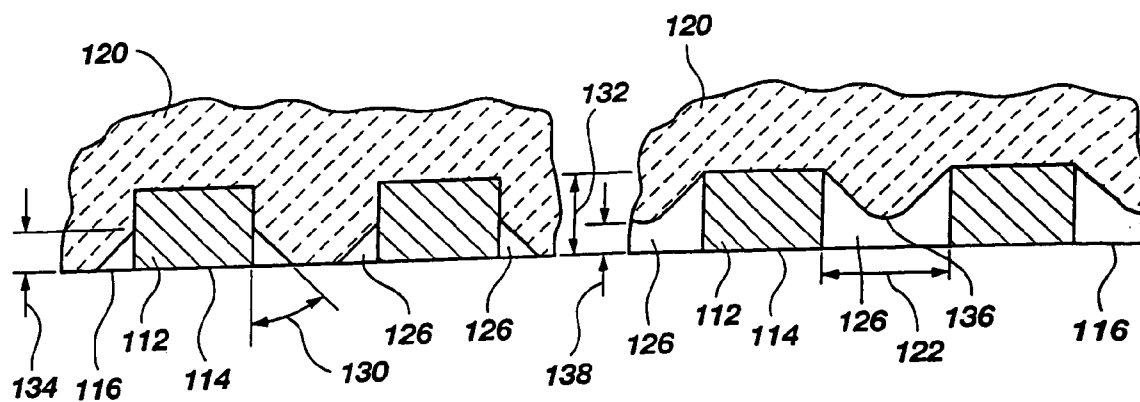


Fig. 7C

Fig. 7D

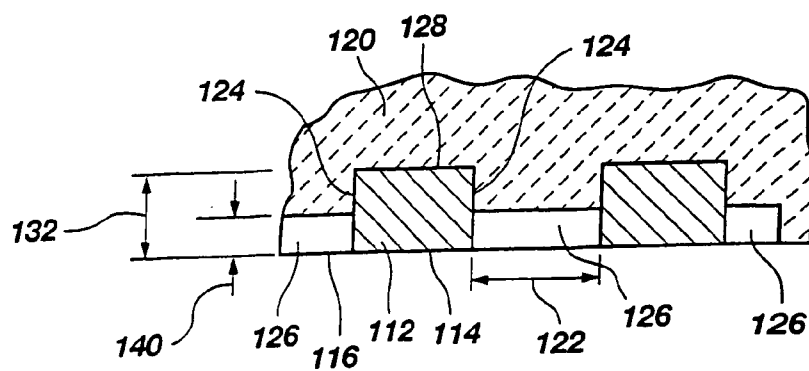
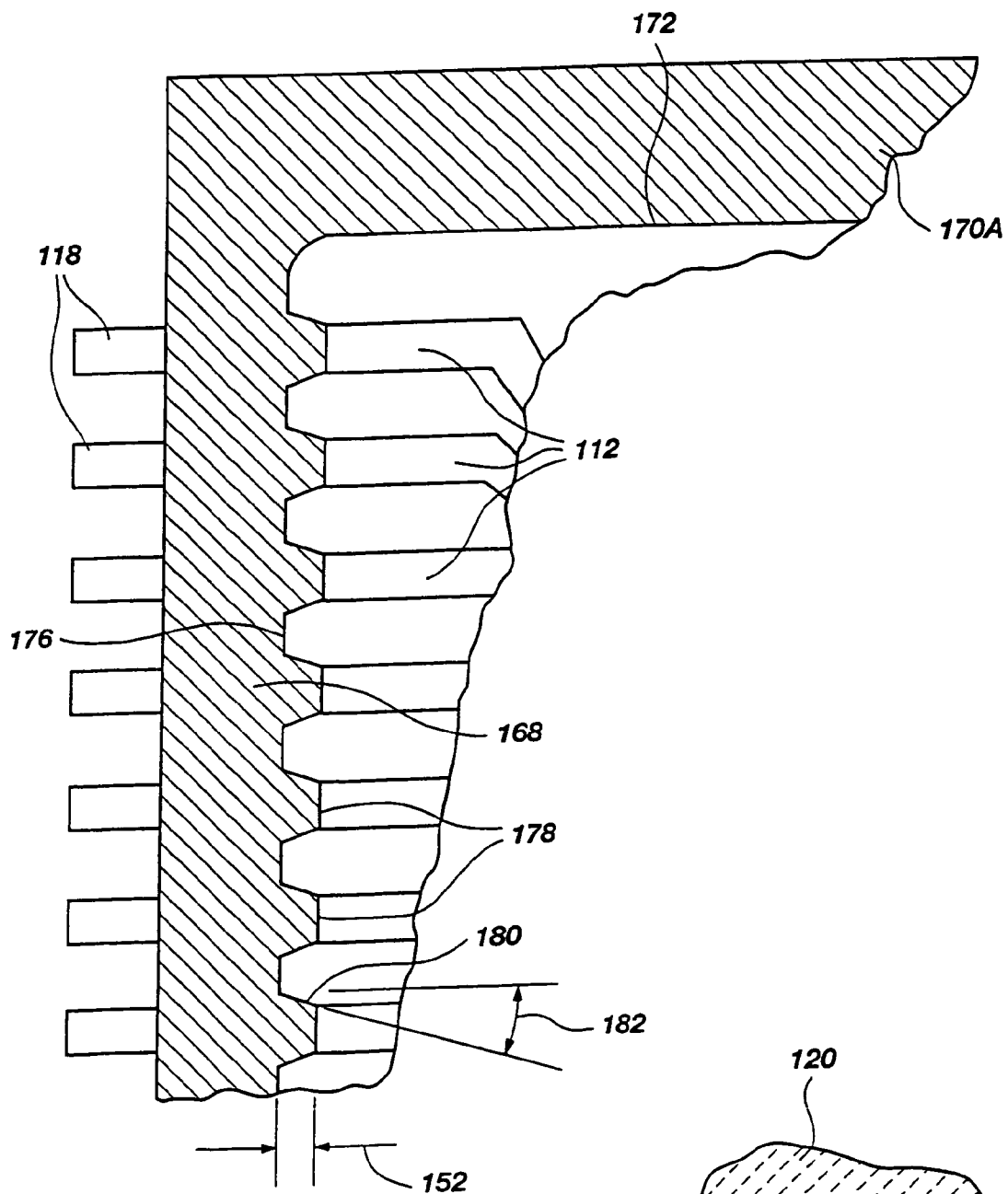
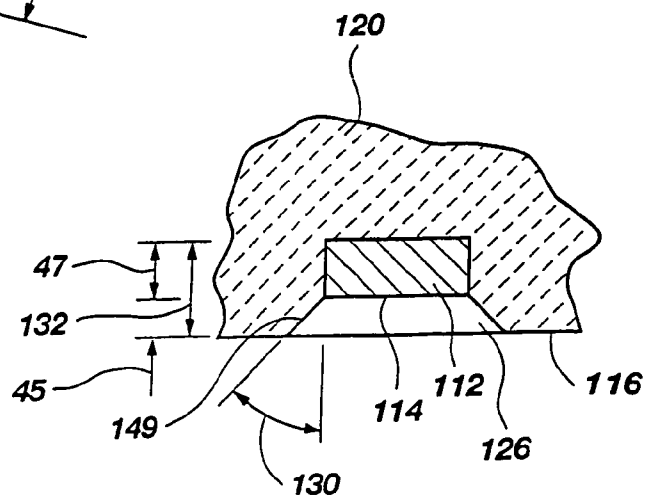


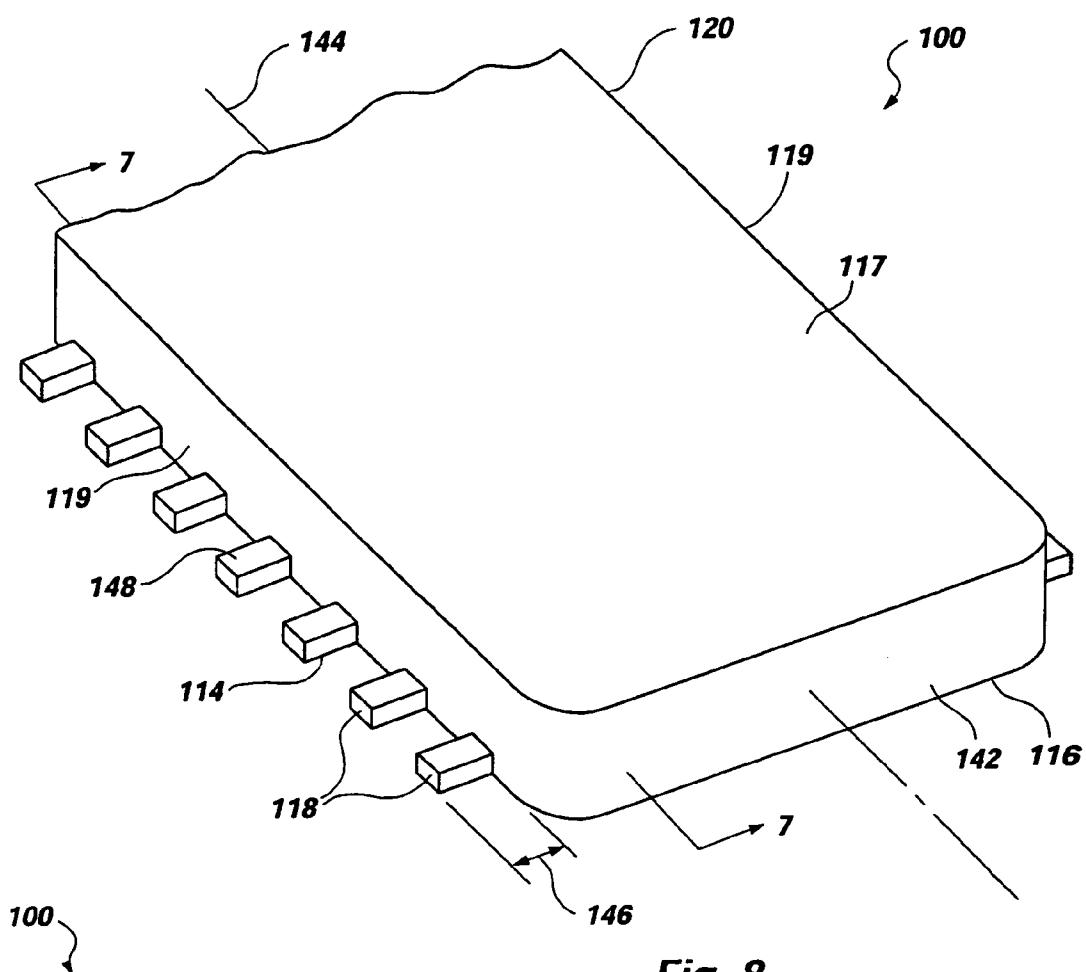
Fig. 7E



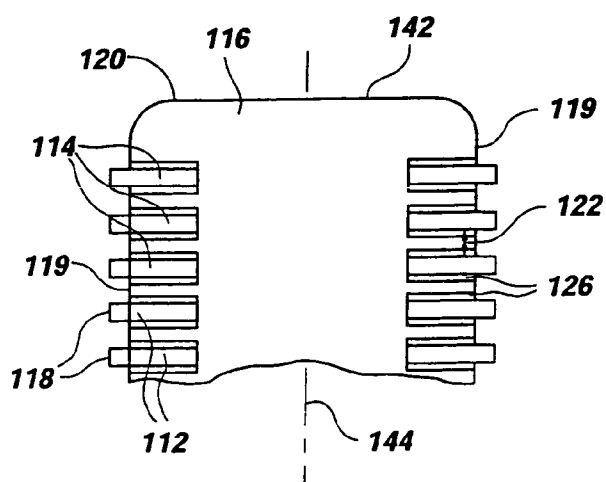
**Fig. 18**



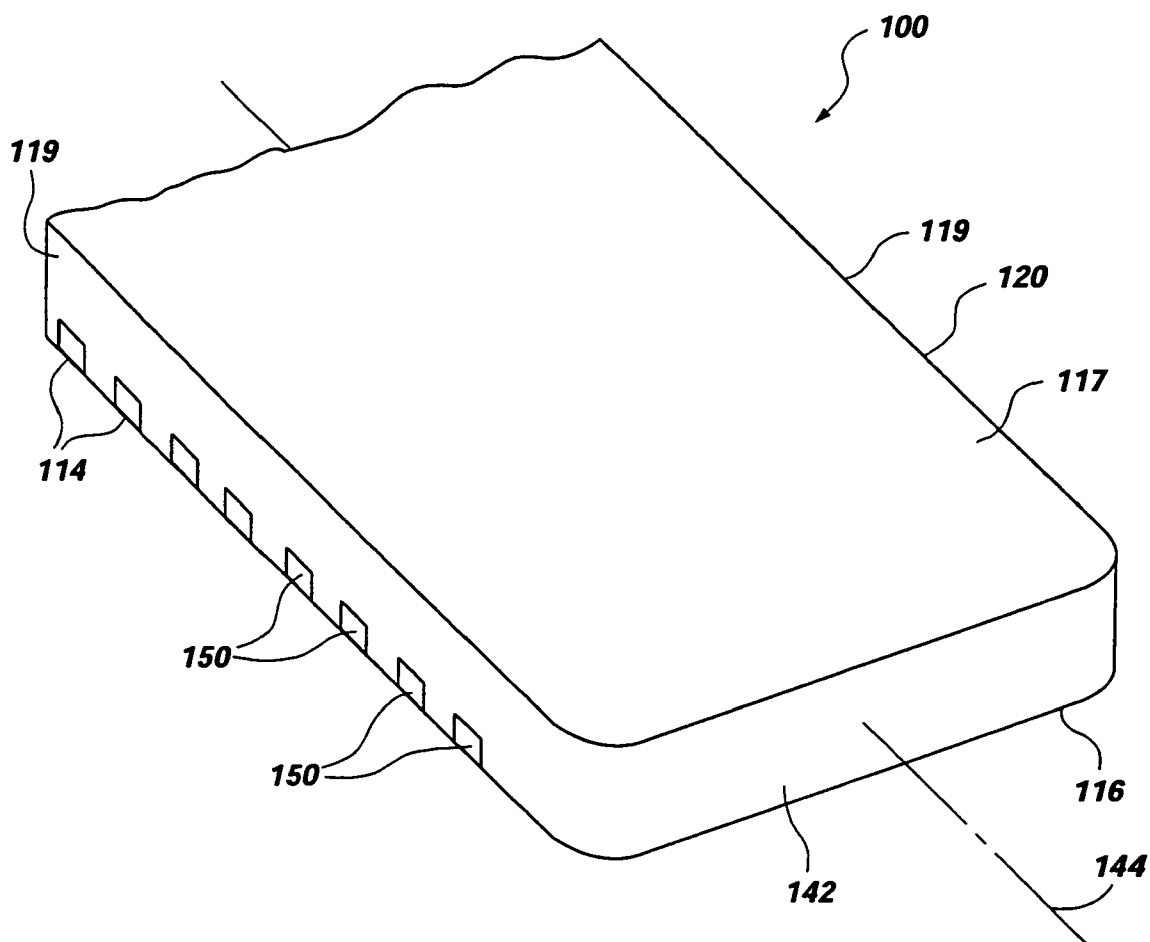
**Fig. 7F**



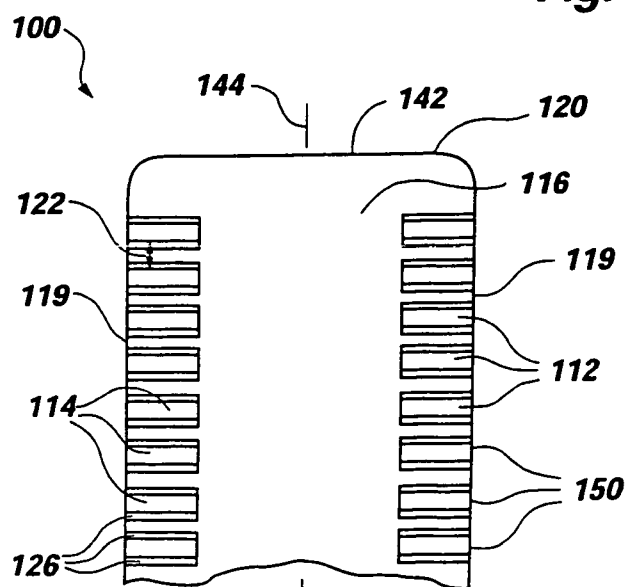
**Fig. 8**



**Fig. 9**



**Fig. 10**



**Fig. 11**

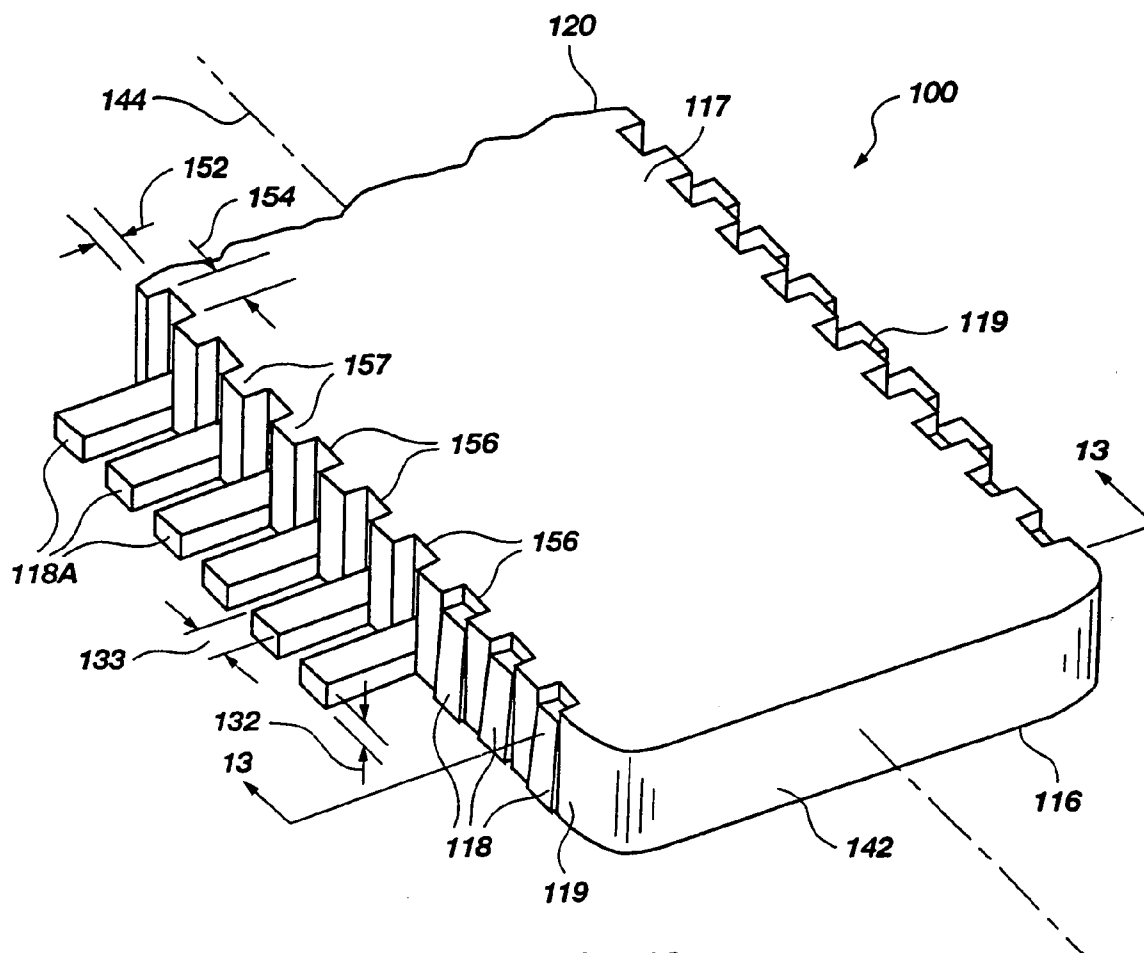


Fig. 12

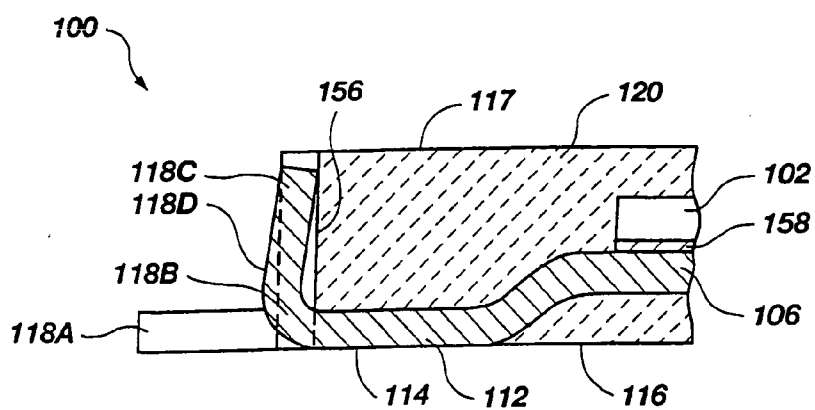
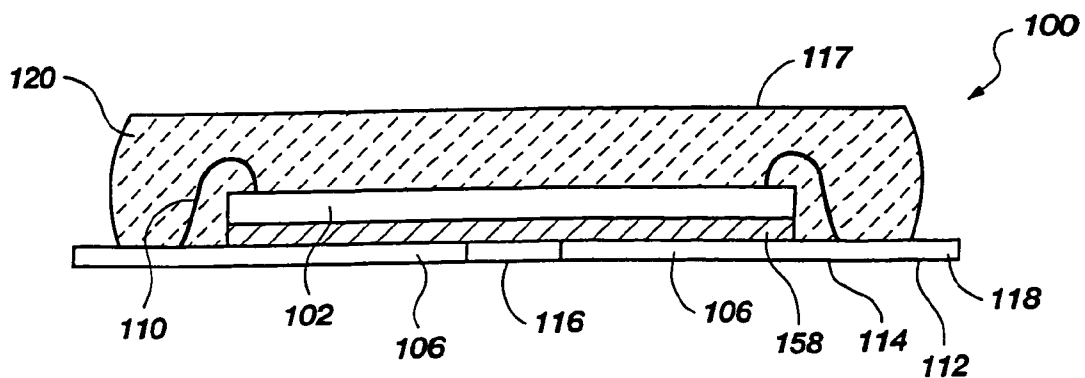
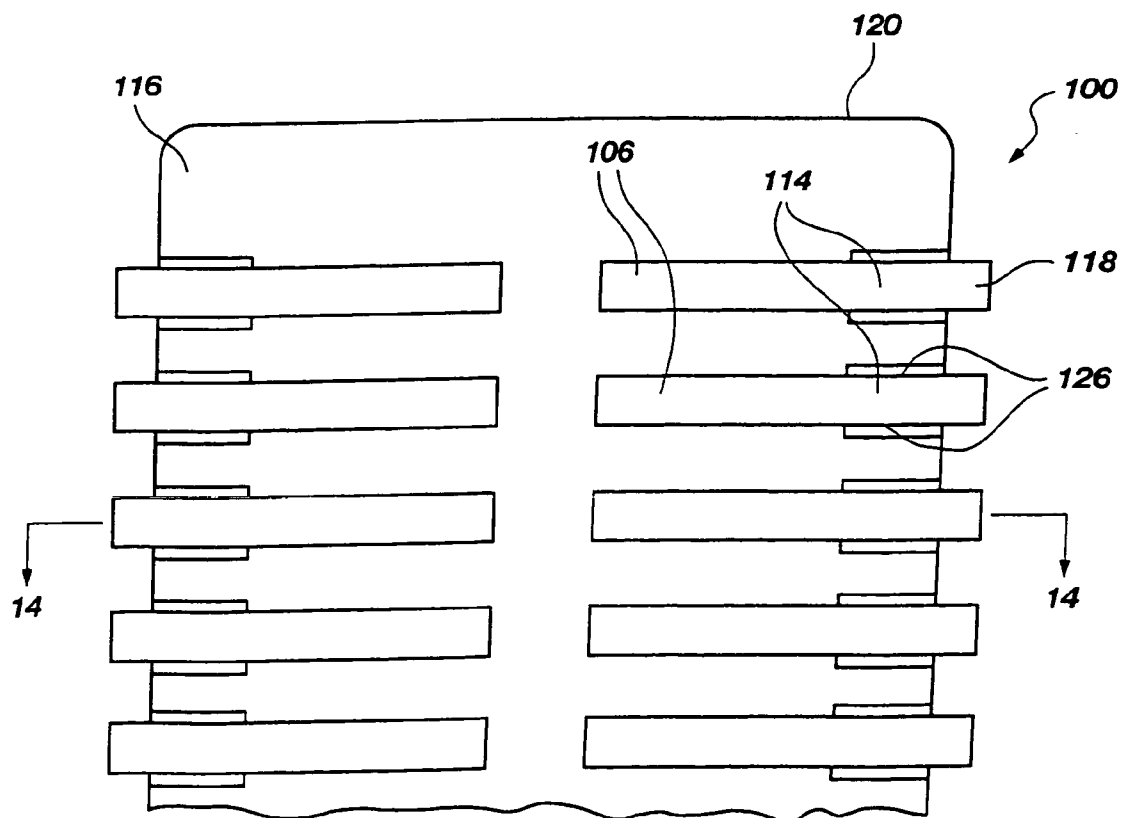


Fig. 13



**Fig. 14**



**Fig. 15**

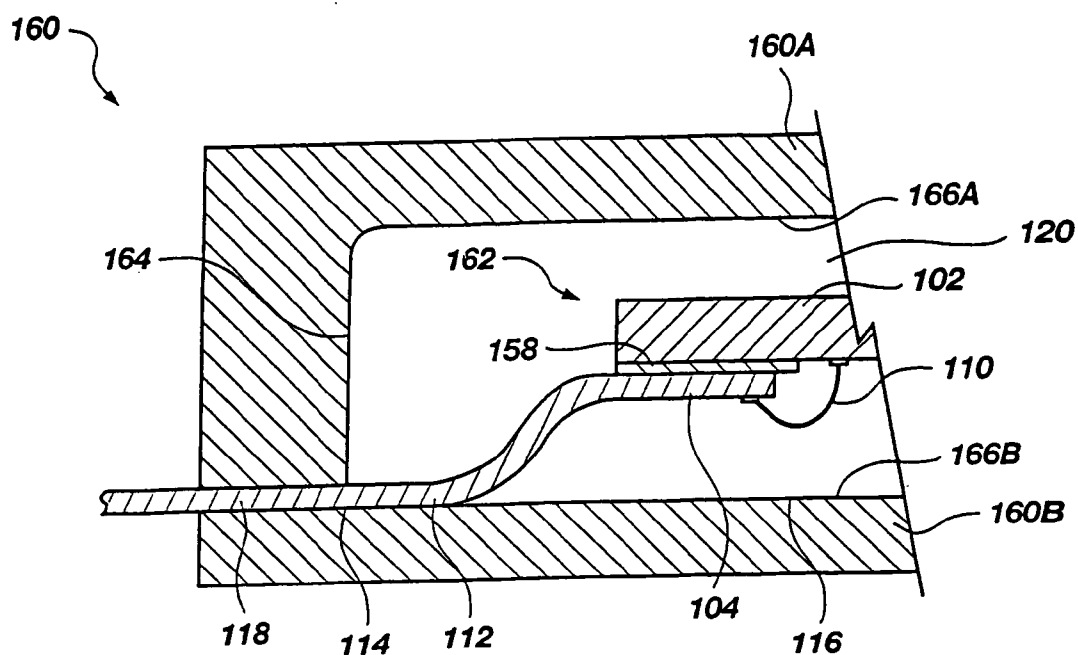


Fig. 16

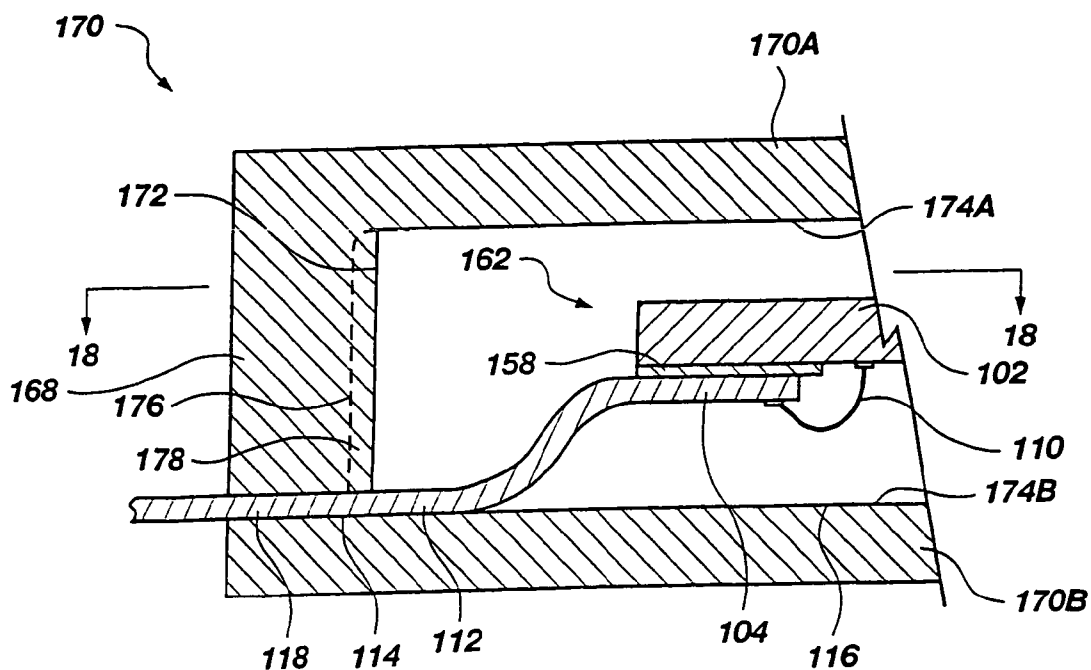


Fig. 17

# MOLD ASSEMBLY, METHOD AND A PACKAGE STACK VIA BOTTOM-LEADED PLASTIC (BLP) PACKAGING

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of application Ser. No. 11/138,756, filed May 25, 2005, pending, which is a continuation of application Ser. No. 10/369,067, filed Feb. 18, 2003, now U.S. Pat. No. 6,899,534, issued May 31, 2005, which is a continuation of application Ser. No. 09/819,909, filed Mar. 28, 2001, now U.S. Pat. No. 6,537,051, issued Mar. 25, 2003, which is a continuation of application Ser. No. 09/336,925, filed Jun. 21, 1999, now U.S. Pat. No. 6,213,747, issued Apr. 10, 2001, which is a divisional of application Ser. No. 08/890,414, filed Jul. 9, 1997, now U.S. Pat. No. 5,986,209, issued Nov. 16, 1999.

## BACKGROUND OF THE INVENTION

### [0002] 1. Field of the Invention

[0003] This invention relates generally to semiconductor devices. More particularly, the invention pertains to surface and external lead configurations of packaged semiconductor devices for electrical connection to other apparatus.

### [0004] 2. State of the Art

[0005] The continuing miniaturization of semiconductor devices is crucial to the electronics industry. Numerous improvements have contributed to the industry growth, including the development of leads-over-chip (LOC) assemblies and their inverse, chip-over-leads (COL) configurations. Thus, the die-attach support was eliminated and lead length was reduced, decreasing the package size. Further developments have included packaged devices in which a plurality of dice and leads therefor are encapsulated within a single package. Such is well illustrated, for example, in U.S. Pat. No. 5,331,235 of Chun, U.S. Pat. No. 5,471,369 of Honda et al., U.S. Pat. No. 5,483,024 of Russell et al., U.S. Pat. No. 5,498,902 of Hara, U.S. Pat. No. 5,508,565 of Hatakeyama et al., U.S. Pat. No. 5,530,292 of Waki et al., and U.S. Pat. No. 5,572,068 of Chun.

[0006] While such developments have filled a need, there remain applications wherein it is desirable to electrically attach separate, packaged semiconductor devices to each other, and to circuit boards, in combinations providing the desired results. This focuses our attention on the external electrical connections of the package by which it may be connected to other packaged devices, circuit boards, various electrical conduits, and a wide variety of electrical apparatuses.

[0007] The state of the art is illustrated by the representative prior art semiconductor devices shown in drawing **FIGS. 1-4**.

[0008] A representative example of a known packaged multi-chip semiconductor device **10** of the piggy-back type is shown in drawing **FIGS. 1 and 2**. A leads-over-chip (LOC) type construction with a small-outline-J-lead (SOJ) type package is depicted. The device includes a semiconductor chip or die **12** partially overcovered with an insulative layer(s) **14** such as polyimide. The die **12** includes a plurality of pads **16**, each of which is electrically connected

to a wire **18** whose opposite end is electrically connected to an end of an inner lead **20** of a leadframe. The die **12**, insulative layers **14**, wires **18**, and inner leads **20** are enclosed in plastic **22**, typically by a transfer molding process.

[0009] As shown in drawing **FIG. 2**, several packaged devices **10** of drawing **FIG. 1** may be stacked with their outer leads **24** connected by, e.g., soldering to form a multi-chip package **26**. As indicated, device **10B** is superposed on device **10A** and corresponding outer leads **24A** and **24B** of the devices are joined by soldering to provide a piggy-back type of package **26**. The end portions **28** of the outer leads **24B** are joined to the outer leads **24A**.

[0010] This type of construction has several disadvantages. First, the outer leads **24B** of the superposed device **10B** must be bent differently from outer leads **24A** of the underlying device **10A**. Thus, the devices **10A** and **10B** cannot be interchanged, and the outer leads **24B** of device **10B** are not configured for attachment to a printed circuit board (PCB).

[0011] In addition, each device **10C**, **10D** (not shown) to be stacked atop device **10B** requires a different outer lead configuration to enable proper joining of the stacked devices.

[0012] Turning now to drawing **FIG. 3**, a prior art semiconductor device **30** is depicted in which two dice **12C**, **12D** are combined, face-to-face, and joined to opposing sides of a single leadframe **32**. The inner lead ends **34A** which approach the electrical pads **16** from one side are positioned between the inner lead ends **34B** which approach the pads **16** from the opposite side. Layers **38** of insulative material separate the dies **12C**, **12D** and leadframe **32** from each other generally. The combination of dice **12C**, **12D** and the attached leadframe **32** is encapsulated by plastic **22** within a single small-outline-J-lead (SOJ) package with conventional outer J-leads **36**.

[0013] Drawing **FIG. 4** illustrates a prior art semiconductor device **40** shown in U.S. Pat. No. 5,554,886 of Song. The device **40** maybe vertically stacked in multiple units. A die **12** is wire-bonded to inner leads **42** of a leadframe **32**. The inner portions of leads **42** are configured to have metal laminates **43** joined thereto, wherein surface portions **44** of the laminates are coplanar with a first major surface **46** of the plastic package **48** and are meant to comprise bond areas for solder bonding to additional packages. The outer portions of J-leads **36** have lead ends **52** which are formed to be parallel to the second major surface **50**, opposite to first major surface **46**. Each lead end **52** has a surface **54** for bonding to a circuit board or another device package. Thus, multiple units of the device **40** may be stacked and have corresponding surface portions **44** and **54** joined by solder.

[0014] Although the state of the art in package configuration is continually improving, ever-increasing demands for further miniaturization, circuit complexity, production speed, reduced cost, product uniformity and reliability require further improvements in semiconductor device connections by which the devices are readily electrically connected to circuit boards, electrical apparatus, and each other.

[0015] In particular, the need for a semiconductor device capable of electrical connection to a plurality of substrates,

other devices, or various electrical apparatus in several configurations is presently needed.

#### BRIEF SUMMARY OF THE INVENTION

[0016] In accordance with the invention, a package configuration for a semiconductor device is formed wherein the package size is reduced, stacking of packages is enabled without further modification of a lower or upper package, and the bonding of the device to electrical apparatuses is enhanced.

[0017] The external package configuration may be used with any internal configuration of dice, leads, insulative layers, heat sinks, die-to-lead connections, etc. Thus, the internal assembly configuration may comprise a Leads-Over-Chip (LOC), Chip-Over-Leads (COL), single or multiple die, wire bonded leads and/or tape-automated bonding (TAB), as well as other variations or combinations in construction.

[0018] A semiconductor package is formed in which the conductive lead has an intermediate portion which is encapsulated to have its exposed surface coplanar with the bottom surface of the package.

[0019] The outer lead is then an outward extension of the intermediate portion. The intermediate portion provides a bonding surface for joining to a circuit board, device, etc. In a further improvement of the invention, the encapsulant adjacent the edges of the intermediate lead portion is excised to a depth equaling about 0.1-1.0 of the lead thickness. The excised portion may take a variety of configurations.

[0020] In another improvement, the semiconductor device is formed with subsurface intermediate leads by which the leads of the apparatus being connected are properly positioned by chamfered sides.

[0021] In another improvement, a semiconductor package is formed with castellated sides and/or ends whereby the outer leads are bent upwardly to fit in the castellation grooves, while extending slightly from the grooves to provide bonding sites for electrical connection to other devices, etc. A mold assembly is described, infra, for producing the castellated package.

#### BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0022] The invention is illustrated in the following figures, wherein the elements are not necessarily shown to scale:

[0023] **FIG. 1** is a cross-sectional end view showing a construction of a semiconductor package of the prior art;

[0024] **FIG. 2** is a cross-sectional end view showing a construction of a prior art multi-chip semiconductor device comprising a plurality of the packages of **FIG. 1** having their outer leads joined;

[0025] **FIG. 3** is a cross-sectional end view of a construction of a multi-die semiconductor package illustrative of the prior art;

[0026] **FIG. 4** is a cross-sectional end view of a construction of a prior art semiconductor package configured for multiple stacking;

[0027] **FIG. 5** is a cross-sectional end view of two bottom-leaded packaged semiconductor devices of the invention in a stacked configuration;

[0028] **FIG. 6** is a partial bottom view of a bottom-leaded packaged semiconductor device of the invention;

[0029] **FIGS. 7A-7F** are fragmentary enlarged cross-sectional side views through surface leads of differing embodiments of the bottom-leaded packaged semiconductor devices of the invention;

[0030] **FIG. 8** is a partial perspective view of another embodiment of a bottom-leaded packaged semiconductor device of the invention;

[0031] **FIG. 9** is a partial bottom view of the bottom-leaded packaged semiconductor device of **FIG. 8**;

[0032] **FIG. 10** is a partial perspective view of a further embodiment of a bottom-leaded packaged semiconductor device of the invention without external leads;

[0033] **FIG. 11** is a partial bottom view of the bottom-leaded packaged semiconductor device of **FIG. 10**;

[0034] **FIG. 12** is a partial perspective view of an additional embodiment of a bottom-leaded packaged semiconductor device of the invention;

[0035] **FIG. 13** is a partial cross-sectional end view of the bottom-leaded packaged semiconductor device of **FIG. 12**, as taken along line 13-13 thereof;

[0036] **FIG. 14** is a cross-sectional end view of an embodiment of the bottom-leaded packaged semiconductor device of the invention, as taken along line 14-14 of **FIG. 15**;

[0037] **FIG. 15** is a partial bottom view of the bottom-leaded packaged semiconductor device of **FIG. 14**;

[0038] **FIG. 16** is a partial end view of a transfer mold assembly for encapsulating a semiconductor device of the invention;

[0039] **FIG. 17** is a partial end view of a transfer mold assembly of the invention for encapsulating a semiconductor device with a castellated package for enclosing outer leads; and

[0040] **FIG. 18** is a partial cross-sectional plan view through the top plate of a transfer mold assembly of the invention, as taken along line 18-18 of **FIG. 17**.

#### DETAILED DESCRIPTION OF THE INVENTION

[0041] A new semiconductor device and method of production thereof is provided by the invention. The semiconductor device is a small footprint semiconductor package amenable to alternative conductive connection (a) in a multi-package vertical stacking configuration, (b) in a multi-package horizontal layout, and (c) to a printed circuit board (PCB) or other substrate.

[0042] With reference to the drawings of **FIGS. 5-18**, which describe the instant invention, and particularly to **FIGS. 5 and 6**, a pair of semiconductor devices **100** are shown in cross-section. In each device **100**, the particular configuration of die **102**, metalized leadframe **104**, and die-to-lead attach method may be any of the wide variety of

known constructions in the art. As represented in **FIGS. 5 and 6**, a chip-over-leads (COL) interior construction with inverted-J (IJ) outer leads **118** is shown with inner leads **106** conductively connected to die pads **108** by wires **110**. An intermediate lead portion **112** is positioned during encapsulation, e.g., transfer molding, to have a bottom lead surface **114** generally coplanar with the bottom package surface **116** of the molded polymeric package **120**. The bottom lead surface **114** of the intermediate lead portion **112** of each lead comprises a bonding surface for conductive connection to a semiconductor device, a circuit board, or other conduit or electrical apparatus. Each lead is separated from adjacent leads by a spacing **122** which may vary along the length of the lead. Preferably, the spacing **122** of the outer leads **118** is uniform.

[0043] As defined herein, the inner leads **106** are completely enclosed within the polymeric package **120**. The outer leads **118** are completely outside of the polymeric package **120**, and the intermediate lead portions **112**, as formed, are within the bottom package surface **116** of the polymeric package **120** and have a bottom lead surface **114** exposed. The outer leads **118**, shown as inverted-J (IJ) leads, of one device **100** may be joined to the intermediate lead portions **112** of another device, if desired, or either the outer leads or intermediate lead portions may be joined to a circuit board, other electrical conduits, or another electrical apparatus.

[0044] In accordance with certain embodiments of the invention, the spacing **122** of the leads of the polymeric package **120** between the lead edges **124** of the intermediate lead portions **112** is partially cut away along and adjacent to the intermediate lead edges **124**, exposing at least a portion of each edge. The excised chamfer portions **126** may take several cross-sectional forms, as depicted generally in drawing **FIGS. 7B, 7C, 7D or 7E**.

[0045] Drawing **FIG. 7A** shows an intermediate lead portion **112** as formed within the molded polymeric package **120**. The bottom lead surface **114** is generally coplanar with the bottom package surface **116**, depending upon the precision of lead placement within the mold.

[0046] A thin coating of polymer will sometimes cover the bottom lead surface **114** following removal of the device from the mold. In the manufacturing process, this coating will be subsequently removed to permit electrical connection to a conductor. The top lead surface **128** and lead edges **124** are embedded in the polymeric package **120**. The lead thickness **132** (typically between about 0.5 and 3 mils) and the lead-to-lead spacing **122** (typically at least about 2-3 mils) are indicated.

[0047] In one embodiment of the invention illustrated in drawing **FIGS. 5 and 6**, further shown in **FIG. 7B**, the lead-to-lead spacing **122** of the polymeric package **120** is chamfered adjacent the full lead thickness **132** of each lead edge **124** to expose the lead edges **124**. The chamfer angle **130** of the excised chamfer portions **126** may be between about 20 degrees and about 60 degrees, depending upon the available lead-to-lead distance between the intermediate lead portions **112**.

[0048] In another embodiment shown in drawing **FIG. 7C**, the excised chamfer portions **126** are shallower, extending to a depth **134** of as little as only about  $\frac{1}{8}$  of the lead

thickness **132**. In drawing **FIG. 7C**, the depth **134** is shown as about  $\frac{1}{2}$  of the lead thickness **132**.

[0049] In drawing **FIG. 7D**, a greater portion of the lead-to-lead spacing **122** is removed, by which an interlead ridge **136** of polymeric package material extends downwardly to a distance **138** above the bottom lead surface **114**. The ratio of distance **138** to lead thickness **132** may be between about zero and about 1.0, although a preferred ratio will be between about 0.1 and about 0.6.

[0050] Drawing **FIG. 7E** shows another embodiment of the invention, in which the lead-to-lead spacing **122** is excised to a generally uniform depth **140**. The ratio of depth **140** to the lead thickness **132** may be between about 0.1 and about 0.8, but is preferably between about 0.1 and about 0.6.

[0051] In a further embodiment shown in drawing **FIG. 7F**, the excision includes not only chamfered portions of the polymeric package **120** but the intermediate lead portion **112** itself. Thus, the exposed bottom lead surface **114** of the intermediate lead portion **112** is depressed into the polymeric package **120** a distance **45** which is up to about  $\frac{1}{2}$  of the original lead thickness **132**. The distance **47** is thus at least  $\frac{1}{2}$  (indicated as remaining lead thickness **47**) of the original lead thickness **132**. The chamfer angle **130** may be between about 20 degrees and 60 degrees, and more preferably about 30-45 degrees. This embodiment results in easier alignment of other leads which are to be joined to the intermediate lead portions **112**, the chamfer walls **149** acting as retainers of the inserted lead edges, not shown.

[0052] Use of bottom leads along the sides of a semiconductor package, together with excision of polymeric material from between the bottom leads, provides a number of improvements. For instance, the device **100** may be electrically joined to another device, piggy-back style, which is already joined to, e.g., a circuit board. Or, the device occupies a smaller amount of area for mounting purposes on a substrate.

[0053] Turning now to drawing **FIGS. 8 and 9**, another version of the improved semiconductor device **100** is shown as a polymeric package **120** having a top package surface **117**, a bottom package surface **116**, two package sides **119**, and ends **142**. A general central axis **144** passes lengthwise through the polymeric package **120**.

[0054] In this version, the outer leads **118** are truncated horizontal extensions of the intermediate lead portions **112**, extending a short distance **146** outwardly, generally no more than about 8 to about 30 mils from the package sides **119**. Preferably, distance **146** is between about 10 and about 20 mils. The outer leads **118** have several surfaces which may be electrically connected to other leads or apparatus, including the upper lead surface **148** and the bottom lead surface **114**.

[0055] The semiconductor device **100** illustrated in drawing **FIGS. 8 and 9** may incorporate excision of the polymeric package **120** along and adjacent the intermediate lead edges **124**. Thus, any of the general excision shapes illustrated in drawing **FIGS. 7B through 7E** may be used, in addition to the version of the invention illustrated in drawing **FIG. 7A** not having excised chamfer portions **126**.

[0056] The semiconductor device **100** of drawing **FIGS. 10 and 11** is similar to that illustrated in drawing **FIGS. 8**

and 9, except that it has no “outer” or external leads. Thus, it has the smallest “footprint” of the various embodiments, the footprint being merely the polymeric package 120 itself. Electrical connections may be made between the bottom lead surfaces 114 and/or the end surfaces 150 of the intermediate lead portions 112.

[0057] Like the embodiments previously described, the embodiment illustrated in drawing FIG. 11 shows excised chamfer portions 126 of the lead-to-lead spacing 122 which have been excised or removed in accordance with the embodiments illustrated in drawing FIGS. 7B through 7E to provide the advantages previously outlined.

[0058] Turning now to drawing FIGS. 12 and 13, a small-footprint semiconductor device 100 is shown with intermediate lead portions 112 having bottom lead surfaces 114 generally coplanar with the bottom package surface 116 of the molded polymeric package 120. The polymeric package 120 has a vertical groove 156 aligned with each outer lead 118 such that the outer lead may be bent upwardly to fit within the groove. Between each vertical groove 156 is a column 157 of the polymeric package 120. Thus, the semiconductor device 100 will be no larger, or just barely larger, than the molded polymeric package 120.

[0059] As shown in drawing FIGS. 12 and 13, outer leads 118A from the transfer molding process extend outwardly from the molded polymeric package 120. Vertical grooves 156 are premolded or formed after removal from a mold. Each outer lead 118A is bent upwardly at bend 118B. The outer end 118C is closely fitted within the vertical groove 156 near the top package surface 117 of the molded polymeric package 120, and a portion 118D of the lead in the area of bend 118B typically extends a short distance outwardly from the groove to provide a bonding surface for lateral electrical connection to another semiconductor device, electrical conduit, or electrical apparatus. Each vertical groove 156 is shown as extending to the top package surface 117 of the polymeric package 120, with a groove depth 152 generally about equal to the lead thickness 132, and a groove width 154 slightly larger than the lead width 133, whereby the outer lead 118 will readily fit into the vertical groove 156. Thus, the semiconductor device 100 has “surface” leads both on its bottom package surface 116 and on surfaces of the package sides 119 and/or ends 142.

[0060] Portions of bottom lead surface 114 which are to be bottom bonded may have adjacent excised chamfer portions 126 excised or removed as previously described in accordance with the embodiment illustrated in drawing FIGS. 7B-7E.

[0061] In drawing FIGS. 13 and 14, the exemplary interior construction of the packaged device 100 is shown as a chip-over-lead (COL) configuration, with chip or die 102 attached to inner lead 106 with an intervening insulative tape 158. However, as already indicated, the invention relates primarily to the configuration of an intermediate “surface” lead and the outer leads; the invention may be applied to any interior chip-lead configuration for reducing the overall size of the device 100 and providing both bottom and side/end lead bonding surfaces.

[0062] Another embodiment of the packaged semiconductor device 100 is shown in drawing FIGS. 14 and 15. The interior construction is depicted as a chip-over-leads (COL)

configuration with wires 110. The entire bottom lead surface 114 of each inner lead 106 is coplanar with the bottom package surface 116 of the polymeric package 120. Portions of bottom lead surface 114 which are to be bottom bonded may have adjacent excised chamfer portions 126 excised or removed as previously described in accordance with the embodiment illustrated in drawing FIGS. 7B-7E.

[0063] While the outer leads 118 are shown as short leads like those of the embodiment of drawing FIG. 8, they may take any useful form such as the inverted-J leads illustrated in drawing FIG. 5, the lateral leads of FIG. 12, or may be eliminated as outer leads as in drawing FIGS. 10 and 11, depending upon the apparatus to which the device 100 is to be connected.

[0064] In this embodiment, inner leads 106 are primarily supported by their adhesive attachment to the insulative tape 158.

[0065] Drawing FIG. 16 shows a mold assembly 160 for encapsulating the die/leadframe assembly 162 in polymer to form the semiconductor polymeric package 120. The die/leadframe assembly 162 is shown as including a die 102, leadframe 104, wires 110, and insulative tape 158.

[0066] The mold assembly 160 includes a top plate 160A and bottom plate 160B which are closed together to form a mold cavity 164 therein.

[0067] Mold cavity 164 is defined by an inner surface 166A of the top plate 160A and an inner surface 166B of the bottom plate 160B. A polymeric encapsulant is introduced as a hardenable fluid through openings (not shown) as known in the art.

[0068] The top plate 160A and bottom plate 160B are configured to produce a casting or polymeric package 120 (see other figures) with an intermediate lead portion 112 and outer lead 118 having bottom lead surfaces 114 which are coplanar with the bottom package surface 116 of the package.

[0069] The mold assembly 160 illustrated in drawing FIG. 16 may be used to form the packaged integrated circuit (IC) devices of the invention as described herein. The particular embodiment of FIGS. 12 and 13 may have its alternating pattern of vertical grooves 156 and columns 157 produced after molding by cutting the vertical grooves 156 by an erosion process or other method known in the art. A cutting apparatus having a plurality of spinning saw blades may be used, for example.

[0070] However, the particular groove/column pattern may also be produced in the molding step, using a mold assembly 170 as illustrated in drawing FIGS. 17 and 18. A wall 168 of the top plate 170A, which is intersected by intermediate lead portions 112, has a pattern of alternating mold grooves 176 and mold columns 178. During the molding process, the mold grooves 176 are filled with encapsulant and become the package columns 157. Likewise, the spaces occupied by the mold columns 178 become the package vertical grooves 156 into which the outer leads 118 are bent upwardly. Mold cavity 172 is defined by an inner surface 174A of the top plate 170A and an inner surface 174B of the bottom plate 170B.

[0071] While drawing FIG. 12 depicts the package vertical grooves 156 with square corners, the preferred mold

grooves **176** have angled groove sides **180** for easy release of the hardened package from the mold cavity **172**. The groove angle **182** may be any angle which permits rapid package release, but will generally be in the range of **5-15** degrees, depending upon the surface roughness of the mold cavity **172** and the particular encapsulant being used.

[0072] In the manufacture of the semiconductor devices **100** of the invention, the steps involved include:

- [0073] a. forming a leadframe with leads for the device;
- [0074] b. preparing a die/leadframe assembly including electrical connections between the die and leadframe, any insulative layers, heat sink, etc.;
- [0075] c. aligning the die/leadframe assembly within a mold assembly configured in accordance with the invention by which bottom-leaded portions have a bottom surface coplanar with the bottom of the package;
- [0076] d. closing the mold assembly and injecting fluid polymeric encapsulant to fill the mold cavity;
- [0077] e. curing the encapsulant and removing the package from the mold;
- [0078] f. deflashing the bottom of the package and portions of the outer leads to remove flash residue from attachment areas of the leads;
- [0079] g. lancing the leadframe to singulate the outer leads and/or intermediate lead portions; and
- [0080] h. bending (if necessary) the outer leads to the specified configuration.

[0081] Following step f, the attachment areas of the leads may be plated with, e.g., tin to enhance adhesion in a subsequent solder bonding step.

[0082] Where a package of the embodiment of drawing **FIGS. 12 and 13** is to be fabricated using cutting means to create the vertical grooves **156** in the polymeric package **120**, such step will typically follow one of steps e, f, or g.

[0083] Where a package of the embodiment of drawing **FIGS. 12 and 13** is to be fabricated using a mold top plate **170A** with an inner castellated wall **168**, the deflashing step may include deflashing of the vertical grooves **156** in the package, as well as connection surfaces of the outer leads **118**.

[0084] Where portions of the package adjacent the intermediate lead portions are to be removed, an erosion process or other method known in the art may be used. This step will follow removal from the mold (step e) or a subsequent step.

[0085] In the lancing/singulation step, the outer leads are cut in conformance to the particular embodiment, as illustrated in drawing **FIG. 5** (full inverted J-leads), **FIG. 8** (abbreviated leads), **FIG. 10** (leads cut at package surface), and **FIG. 12** (abbreviated lead length).

[0086] This discussion and these figures presume and show a relatively exacting removal of polymeric packaging material from adjacent the leads. As is well known in the art, the methods of removing such material at the miniature scale will not generally leave precisely flat surfaces or uniform

depths and angles. The embodiments of drawing **FIGS. 7B-7E** are representative only and illustrate preferred constructions.

[0087] As described herein, the invention provides a semiconductor package of reduced size, yet having leads for bottom and side/edge bonding or bottom and top bonding of the package. Thus, multiples of the device may be vertically stacked in parallel, and/or be electrically joined in a generally horizontal coplanar configuration. The invention may be applied to a three-dimension-lead (TDL) package having outer leads on the ends as well as the sides or top, together with bottom surface leads. The die/leadframe assembly shown and described herein is exemplary only, and may include other elements such as additional dice and leadframes, heatsinks, dielectric layers, etc., as known in the art.

[0088] It is apparent to those skilled in the art that various changes and modifications may be made in the packaging methods and products of the invention as disclosed herein without departing from the spirit and scope of the invention as defined in the following claims.

What is claimed is:

1. An assembly for a semiconductor die and a lead frame package comprising:

a top mold plate having a top and a plurality of sides of a mold assembly in a transfer molding operation; and

a generally planar bottom mold plate of a mold assembly having portions thereof engaging portions of said top mold plate during said transfer molding operation, said top mold plate and said bottom mold plate forming a mold cavity having a top, having a bottom, having sidewalls and having end walls when engaged, said top mold plate and said bottom mold plate for suspending a semiconductor die and a portion of said lead frame within said mold cavity for injecting a material to encapsulate said semiconductor die and portions of said leadframe therein, one sidewall of said sidewalls having an inner surface with grooves and columns for forming columns and grooves in at least one external surface of said molded package.

2. The assembly of claim 1, wherein the grooves in the inner surface of the one of the sidewalls have side portion surfaces angled to provide an opening dimension greater than an inner dimension of the grooves, the angle being in the range of **5** to **15** degrees.

3. A semiconductor device assembly, comprising:

a semiconductor die;

a leadframe including at least one lead with upper, lower and edge surfaces, said lead comprising:

an inner end conductively connected to said die;

an intermediate portion configured for connection to a first electrical apparatus; and

an outer lead configured for connection to second electrical apparatus; and

a package enclosure enclosing said die and the inner end of said at least one lead, said enclosure having top, bottom and side surfaces, said bottom surface of said intermediate portion of said at least one lead is generally coplanar with said bottom surface of said package

enclosure and exposed for electrical connection to a lead of another electrical apparatus.

4. The semiconductor device of claim 3, wherein portions of the package enclosure adjacent the edges of said intermediate portion of said lead are excised to expose at least a portion of said lead edges.

5. The semiconductor device of claim 4, wherein said excised portion comprises an elongate chamfer exposing a portion of the lead edge comprising between about 0.1 and about 1.0 of the lead thickness.

6. The semiconductor device of claim 5, wherein the angle formed by the chamfer with the lead edge is between about 20 and about 60 degrees.

7. The semiconductor device of claim 4, wherein the excised portions have a generally uniform depth from the surface of said package enclosure.

8. The semiconductor device of claim 3, wherein the generally coplanar bottom lead surface is excised to submerge said lead surface into said bottom surface of said package enclosure a distance of up to about one-half the lead thickness.

9. The semiconductor device of claim 8, further comprising an excised portion of said package enclosure immediately adjacent said bottom lead.

10. The semiconductor device of claim 9, wherein said excised portion of said package comprises a chamfer.

11. The semiconductor device of claim 3, wherein said another electrical apparatus comprises one of a semiconductor device, electrical conduit, and circuit board.

12. The semiconductor device of claim 3, wherein said package enclosing said die and said at least one lead comprises a polymer.

13. The semiconductor device of claim 3, wherein said outer leads are bent upwardly to form an inverted J configuration.

14. The semiconductor device of claim 3, wherein said at least one outer lead is configured to be a truncated coplanar outward extension of said intermediate lead portion.

15. The semiconductor device of claim 14, wherein said at least one outer lead extends a distance of about 8 to 30 mils from said package surface.

16. The semiconductor device of claim 14, wherein said at least one outer lead extends a distance of about 10 to 20 mils from said package surface.

17. The semiconductor device of claim 14, wherein said outer lead has top and bottom surfaces, whereby both surfaces are configured for electrical connection to other electrical apparatus.

18. The semiconductor device of claim 14, wherein portions of the package enclosure adjacent the edges of said intermediate portion of said at least one lead are excised to expose at least a portion of said lead edges.

19. The semiconductor device of claim 14, wherein the generally coplanar bottom lead surface is excised to submerge said lead surface into said bottom surface of said package enclosure.

20. The semiconductor device of claim 3, wherein said at least one lead is lanced adjacent a side surface of said package enclosure, whereby said lead has no outer lead portion.

21. The semiconductor device of claim 20, wherein the lanced lead portion coplanar with said side surface comprises an electrical connection surface.

22. The semiconductor device of claim 1, wherein a side surface of said package enclosure includes a vertical groove for enclosing said outer lead in a vertical orientation.

23. A method for forming a semiconductor device, comprising:

providing a semiconductor die;

forming a lead frame having at least one lead;

preparing a semiconductor die-leadframe assembly including electrical connections between the semiconductor die and at least one lead of the leadframe;

aligning the die-leadframe assembly in the cavity of a mold assembly having a top plate and a bottom plate wherein an intermediate portion of at least one lead is adjacent to the floor of said bottom plate;

closing the mold assembly and injecting fluid polymeric encapsulant to fill the mold cavity; removing the molded polymeric package from said mold assembly; and

configuring said outer leads to a desired configuration.

24. The method of claim 23, comprising the further step of: curing the encapsulant.

25. The method of claim 23, comprising the further step of:

deflashing the bottom of the package and portions of outer leads to remove flash residue from attachment areas of said leads.

26. The method of claim 23, comprising the further step of:

lancing the leadframe to singulate the outer leads.

27. The method of claim 23, comprising the further step of plating said attachment areas of said leads with tin.

28. The method of claim 23, comprising the further step of excising portions of said polymeric package adjacent and parallel to said intermediate portion of the at least one lead.

29. The method of claim 23, wherein said excised portions of said package are excised by an erosion method.

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