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Description

This invention relates to methods of and apparatuses for recording and/or reproducing digital data. More particularly, but not exclusively, the present invention relates to a rotary head type digital audio tape recorder (R-DAT) when used for recording data from a computer or the like.

To protect computer generated data written on a hard disc or the like, the data are sometimes transferred to a so-called data streamer (or data recorder) and are thereby recorded (or backed up) on the other recording media once per day.

In most cases, a data streamer is what might be called an analogue audio tape recorder. Such an analogue audio tape recorder, however, consumes a great quantity of recording medium, such as tape. Also, such a data streamer has a low data rate upon recording, so that it takes a long time for transferring and recording the data. Moreover, it is not easy with an analogue audio tape recorder to find the starting point of the desired recorded data.

When data, for example, from a computer is recorded using an audio tape recorder, an arbitrary file mark signal is supplied thereto from the computer. Upon reproduction, the location number of the file mark for the computer designated address is searched for. Since the analogue audio tape recorder is arranged to search for the location number of the file mark by counting the reproduced signal of the file mark in the normal reproduction operation, it takes a long time to search for the desired file mark.

A digital audio tape recorder (DAT) has been developed, as described in "ES Review", pages 11 to 14, published December, 1985 by us, Shibaura Plant: ISSN 0389-7737. Since this DAT is designated to record and/or reproduce a digital signal, that is a digitized audio signal, it is very suitable for recording the aforesaid data.

We have also proposed a data recorder using an R-DAT for a computer in EP-A-0 272 130 (published on 22.06.88) and EP-A-0 286 412 (published on 12.10.88).

With a DAT as described above, when another signal is to be recorded on a previously recorded recording medium, previously recorded signals are erased by recording new signals over them, that is, by so-called over-writing, without using an erasing head. Therefore, if over-writing is not normally effected, for example, due to clogging of the head, there is the possibility that a part of the previously recorded signals remains unerased.

To correct this problem, in the DAT format, an error detecting code is added to each recording track so as to detect an unerased portion, if any, in the track as an error. However, even with such a code added to each track, if an entire track remains unerased, no error is detected since the error detecting code within the unerased track is considered normal.

If the signal to be recorded is an audio signal, wherein adjacent data are correlated with each other due to the more or less continuous nature of an audio signal, a correlation can be effected by an interpolation technique even although the remaining unerased signal portion is removed from the track. However, if the DAT is employed as a data recorder, wherein adjacent data are not generally correlated, the interpolation technique cannot be utilized.

The above EP-A-0 286 412 proposes a technique wherein, when the DAT is employed as a data recorder, an error correcting code is generated for a plurality of frames of data signals to be supplied to the DAT and the error correcting code thus generated is supplied to the DAT to be recorded on the tape, in the same manner as the data signals. Thus, error correction is effected outside the DAT, thereby providing the DAT with a powerful error correcting performance.

This error correcting operation requires that an erroneous frame has been detected prior to the error correcting operation. However, in the above-mentioned case where one or more tracks remain entirely unerased, the error cannot be detected by this method. Therefore, although the error correcting code is generated outside the DAT, errors cannot be corrected.

According to the present invention there is provided a method of recording digital data signals in a series of track pairs on a recording medium, the method comprising the steps of:

receiving digital information signals from an external source and dividing them into frames, each frame corresponding to a different pair of tracks to be recorded on the recording medium;

for each of the two tracks forming each frame, providing header portions, having identical contents and containing at least data related to the corresponding digital information signals so as to be able to distinguish between rewritten header portions and unerased previously written header portions, which are each arranged to be recorded before the digital information signals in the respective tracks; and

recording the digital information signals and the header portions in a series of pairs of tracks on the recording medium.

According to the present invention there is also provided a method of reproducing digital data signals

recorded on a recording medium, wherein the digital data signals as recorded are formatted into frames, each frame corresponding to two tracks, with an identical header portion being provided at the beginning of each track forming one frame and containing at least data related to the corresponding digital information signals so as to be able to distinguish between rewritten header portions and unerased previously written header portions, it being intended that the digital data and the header portions of each frame are to be reproduced together, the method comprising the steps of:

reproducing the digital data signals recorded in the tracks on the recording medium;

separating the header portions from the reproduced digital data signals and comparing with each other at least parts of the header portions reproduced from the two tracks forming each frame;

determining that the digital data signals written in each frame are erroneous if the data in the parts of the header portions of the two tracks are not identical; and

correcting the erroneous digital data signals of each frame by the use of an error correcting code.

According to the present invention there is also provided an apparatus for recording digital data signals in a series of track pairs on a recording medium, the apparatus comprising:

means for receiving digital information signals from an external source and dividing them into frames, each frame corresponding to a different pair of tracks to be recorded on the recording medium;

means for providing header portions for each of the two tracks forming each frame, the header portions having identical contents and containing at least data related to the corresponding digital information signals so as to be able to distinguish between rewritten header portions and unerased previously written header portions and each arranged to be recorded before the digital information signals in the respective tracks; and

means for recording the digital information signals and the header portions in a series of pairs of tracks on the recording medium.

According to the present invention there is also provided an apparatus for reproducing digital data signals recorded on a recording medium wherein the recorded digital data signals are formatted by being divided into frames, each of which corresponds to two tracks, with each frame including a header portion which is identical in the respective two tracks forming each frame and containing at least data related to the corresponding digital information signals so as to be able to distinguish between rewritten header portions and unerased previously written header portions, the apparatus comprising:

means for reproducing the digital data signals recorded in the tracks on the recording medium;

separating and comparing means for separating the header portions from the reproduced signals for each frame and comparing at least parts of the header portions reproduced from the two tracks forming each frame with each other;

means supplied with the results of the separating and comparing means for determining whether the digital data signals written in each frame are erroneous if the comparison result shows that data in the parts of the header portions of the two tracks are not identical; and

error correcting means for correcting the erroneous digital data signals by the use of an error correcting code.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, and in which:

Figure 1 is a circuit block diagram of an embodiment of recording and/or reproducing apparatus according to the present invention:

Figure 2 is a circuit block diagram showing an example of a syndrome generating circuit;

Figures 3A to 3F are timing charts used for explaining the reproducing operation of the apparatus of Figure 1;

Figure 4 is a diagram showing a DAT recording track format;

Figure 5 (formed of Figures 5A and 5B on two separate sheets) is a diagram showing a data format in a main data area;

Figures 6A and 6B are tables showing the recording format of packs comprised in a sub-code area;

Figure 7 is a diagram showing a recording pattern made in the main data area;

Figure 8 is a flow chart illustrating a program for generating syndromes for use in error correction; and

Figures 9A and 9B are diagrams showing the ID organization of a DAT format.

Referring to Figure 1, the data recorder according to a first embodiment of the invention includes a digital audio tape recorder (DAT) 1. The DAT 1 is provided with a rotary head drum 11, and a magnetic tape 12 is wrapped around the peripheral surface of the head drum 11, over an angular range of about 90° of head travel, and is transported past the head drum 11 by a tape transport mechanism 19. Two rotary heads A and B are mounted in the head drum 11, and two oblique tracks are recorded and/or reproduced by the heads A and B once per revolution of the head drum 11 as shown more clearly in Figure 4.

Incoming digital data is supplied to an input and output (I/O) circuit 13 of the DAT 1. The digital data from the I/O circuit 13 is supplied to a digital signal processor 14, in which it is converted into the DAT format. This digital signal is supplied through a recording amplifier 15 and a recording side contact R of a recording/reproducing change-over switch 16 to the heads A and B, and is thereby recorded on the tape 12.

When the signal recorded on the tape 12 is reproduced by the heads A and B, the reproduced signal is supplied through a reproducing side contact P of the switch 16 and a playback amplifier 17 to the signal processor 14, in which the reproduced signal is reconverted into the digital data and then supplied through I/O circuit 13 to the outside.

An incoming control signal is also supplied to a system control circuit 18 of the DAT 1. On the basis of the signal from the control circuit 18, the head drum 11 is controlled to rotate, the transport mechanism 19 to transport the tape 12 and the switch 16 to change in position. Also, upon recording, the signal from the control circuit 18 is supplied to the signal processor 14 which then produces a sub-code signal or the like which will be described later. Upon reproduction, the signal extracted by the signal processor 14 is supplied to the control circuit 18, whereby the tracking control operation is made and a part of this signal is fed to the outside.

In the DAT 1, by connecting a digital-to-analogue (D/A) /analogue-to-digital (A/D) converting circuit to the output of the I/O circuit 13, and a predetermined control apparatus to the output of the control circuit 18, it is possible to record and/or reproduce, for example, an analogue audio signal.

In the embodiment, however, an interface bus 3 is connected through a controller 2 as an external apparatus to the DAT 1. The interface bus 3 may be of the type which conforms, for example, to the SCSI (small computer system interface) standard (see "NIKKEI ELECTRONICS", pages 102 to 107, published by Nihon Keizai Shinbunsha on 6 October 1986). A host computer 5 and a hard disc drive (HDD) 6 are connected to the bus 3 through a host adaptor 4.

In the controller 2, a protocol circuit circuit 21 is connected to the bus 3. Through the protocol control circuit 21, the data and the control signals are interchanged between a microcomputer 22 which controls the operation of the controller 2, a memory control or dynamic memory access (DMA) circuit 23 and the bus 3. The microcomputer 22 not only controls the operation of the controller 2 but also detects the address of the DMA circuit 23 and controls the operation thereof. Also, data is interchanged between a buffer memory 24 and the bus 3 through the DMA circuit 23. Further, data is interchanged between the buffer memory 24 and the signal processor 14 via I/O circuits 25 and 13. In addition, the control signal is interchanged between the microcomputer 22 and the control circuit 18.

Further, an error correcting code (ECC) generating circuit 26 is connected to the buffer memory 24 for generating the error correcting code for data stored in the buffer memory 24. The error correcting code generated from the ECC generating circuit 26 is stored in a predetermined area of the buffer memory 24.

Accordingly, in this apparatus, data written in the HDD 6 is supplied through the bus 3 to the controller 2 in response to the transfer request from the controller 2 during recording and is then written in the buffer memory 24 through the DMA circuit 23. The ECC generating circuit 26 generates the error correcting code for the data written in the buffer memory 24. Then, the data including the error correcting code is read out through the I/O circuit 25 and supplied to the I/O circuit 13 of the DAT 1. In the DAT 1, the data supplied from the I/O circuit 13 is regarded as being equivalent to data derived from an A/D converter when the audio signal is recorded. Then, the data is converted in accordance with the DAT format by the signal processor 14 and recorded on the tape 12 by the heads A and B.

The error correcting code is generated upon recording as follows:

It is assumed that an error generating matrix is arranged for an arbitrary data sequence supplied to the DAT 1 as follows:

1	...	1	1	1	1	1	1
α^{254}	...	α^{5}	α^{4}	α^{3}	α^{2}	α^{1}	1
α^{508}	...	α^{10}	α^{8}	α^{6}	α^{4}	α^{2}	1
α^{762}	...	α^{15}	α^{12}	α^{9}	α^{6}	α^{3}	1
Data section				Parity section			

A syndrome generating circuit is formed for the matrix thus generated, for example as shown in Figure 2. Specifically, a data signal fed to a terminal 31 on the left side of the drawing is supplied to adder circuits 32a to 32d. The output signals from the adder circuits 32a to 32d are repsectively supplied to syndrome registers 34a to 34d directly and through coefficient circuits 33b to 33d respectively having a coefficient of α, α^2 and α^3. The signals from the syndrome registers 34a to 34d are respectively fed back to the adder circuits 32a to 32d. Thus, syndromes are generated in the registers 34a to 34d by the feedback which are effected every time the data signal is supplied to the adder circuits 32a to 32d.

Therefore, every time the data signal is fed to the terminal 31, calculation is effected from the right side of the data section of the above matrix. Generally, at the time, for example, 251 symbols of data are supplied, the syndromes are generated from the registers 34a to 34d. The syndromes thus generated are supplied to a calculating circuit 35, which corresponds to the parity section of the above matrix, to generate a 4-symbol error correcting code. If the data sequence is terminated while the calculation is progressing, the registers 34a to 34d respectively generate the syndromes equivalent to the fact that zero is supplied to all the elements of the syndromes located on the left side from the point the calculation based on the data sequence has been effected. Then, at this time, the registers 34a to 34d are made inoperative and the respective contents thereof are supplied to the calculating circuit 35, thereby to generate the error correcting codes for the data which has been supplied to the syndrome generating circuit up to that time.

By this processing, the error correcting code can be smoothly generated and added to an arbitrarily variable length of data sequence. The syndrome generating circuit is realized in practice by software of a microcomputer or the like. The required hardware is solely memory areas corresponding to the syndrome registers 34a to 34d, so that the apparatus can be realized by a simple construction. That is, the memory capacity of each of the register 34a to 34d is four times the data amount for one track.

Referring now to Figure 8, a flow chart for such a syndrome generating program is illustrated. The program starts at step SP1 and the data signal is supplied at step SP2. At step SP3, the input data signal is added to the stored data signal in a memory area M1 (within buffer memory 24) and the added data signal is stored in a memory area M2 of the buffer memory 24.

The input data signal, at step SP4, is added to the stored data signal in the memory area M2. The added data signal is multiplied by α. The multiplied data signal is stored in the memory area M2. In step SP5, the input data signal is added to the stored data signal in the memory area M3, the added data signal is multiplied by α^2, and the multiplied data signal is stored in a memory area M3.

Next, the input data signal is added to the stored data signal in a memory area M4 of the buffer memory 24. The added data signal is multiplied by α^3, and the multiplied data signal is stored in the memory area M4 at step SP6. At step SP7 it is determined wherther or not the input data signal is finished. If the answer is no, the process returns to step SP2. If the answer is yes, the process goes to step SP8 where four error correcting codes are generated from the stored data signals in the memory areas M1, M2, M3 and M4 by matrix calculations. This ends the process.

The generated error correcting code is supplied to the DAT 1 subsequent to the data signals so as smoothly to record an arbitrarily variable length of the data signals, thereby rendering it possible to provide a satisfactory data recorder which employs the DAT 1.

In the above described embodiment, since two symbols are taken out from each frame of the data sequence for generating the error correcting code, the generated 4-symbol error correcting code can be recorded in two frames (four tracks).

If, as a particular example, the error correcting code is assumed to be formed of two symbols, the following matrix, for example, may be used:

$$\left[\begin{array}{ccc|ccc} 1 & \cdots & 1 & 1 & 1 & 1 \\ \alpha^{254} & \cdots & \alpha^{2} & \alpha & 0 & 1 \end{array}\right]$$

Data Section | Parity Section

With this matrix, the calculating circuit 35 becomes unnecessary.

Next, an explanation will be given of how error correcting processing is carried out during reproduction by the apparatus, with reference to Figures 1 and 3A to 3E.

Upon reproduction, the signal reproduced from the tape 12 by the heads A and B is reconverted by the signal processor 14 and thereby data corresponding to the audio signal is produced. This data is supplied

through the I/O circuit 13 to the controller 2 which writes the data into the buffer memory 24. The data written in the buffer memory 24 through the I/O circuit 25 is read out through the DMA circuit 23 and then written in the HDD through the bus 3.

The data signals and the error correcting code are reproduced as shown in Figure 3A. If the DAT 1 detects that there is a frame whose error cannot be corrected as shown in Figure 3B, a condition where the data has been directly outputted at first is halted as shown in Figure 3C. However, at this time the data signals are continuously supplied to the syndrome generating circuit, so that it generates data for correcting errors in the erroneous frame from the DAT 1 at the time the reproduction of the error correcting code has been terminated. From this condition, the DAT 1 is instructed to rewind the tape 12 as shown in Figure 3D. Then, as shown in Figure 3E the DAT 1 resumes the reproduction of the data signals from the beginning thereof, in which the error correcting data generated by the syndrome generating circuit is inserted for the detected erroneous frame and then all the data signals are reproduced.

When no error is found in the data frame, the data signals are reproduced without any processing and supplied to the bus 3. The above-described processing is effected only when errors are found in the data frames, so that the data signals as a whole can be quite rapidly reproduced.

The above-described error correction can be effected with only a small capacity of the memory area corresponding to the syndrome registers 34a to 34d by using the data signals again reproduced from the DAT 1, without providing a large capacity buffer memory for storing all data in the data section of the foregoing matrix.

The error correction as described above requires, upon reproduction, detecting at least the frame number of the error correcting code, and discriminating whether the frame contains the data signals or the error correcting code. Therefore, a signal area is reserved in the DAT format for such detection and discrimination. This DAT format, in accordance with which the data signals are recorded on the tape 12, will be explained with reference to Figure 4.

As can be seen from Figure 4, one frame is made up of two tracks Ta and Tb formed by the heads A and B. Each of the tracks Ta and Tb has a length corresponding to the rotation of each of the respective heads through an angle of 90° and is paritioned from its lower end (that is from right to left in the figure) into 5.051° of a margin area, 0.918° of a preamble area for the PLL of the sub-code, 3.673° of a first sub-code, 0.459° of a postamble area, 1.378° of an interblock gap area, 2.296° of a tracking (ATF) signal area, 1.378° of an interblock gap area, 0.918° of a preamble area for the PLL of data, 58.776° of data area, 1.378° of an interblock gap area, 2.296° of an AFT signal area, 1.378° of an interblock gap area, 0.918° of a preamble area for the PLL of the sub-code, 3.673° of a second sub-code area 0.459° of the postamble area, and 5.051° of the margin area. It should be noted that the scale of the respective areas in Figure 4 is not exact.

Data fed to the DAT 1 at the I/O circuit 13 is supplied to the processing circuit 14 which adds predetermined error detecting and correcting codes and so on to the data and then inserts it into the data areas of the tracks Ta and Tb in accordance with a predetermined interleaving relationship.

As illustrated in Figure 9A, the data area comprises an 8-bit synchronizing section at its starting portion and subsequently totals 16 bits of ID section formed of W1 and W2. The ID section is divided into eight ID areas of two bits. The first ID area (ID-O) is assigned to a format ID and is set to 01 for a data specification, for example. The next ID area (ID-1) is assigned to a sub-category ID and is set to 00 for a computer peripheral device, for example. The next ID area (ID-2) is assigned to a frame size ID and is set to 00 when the recording capacity of the frame is 5760 bytes, and 01 when the recording capacity thereof is 5292 bytes, for example. The ID area (ID-3) is assigned to a track pitch ID and set to 00 when the track pitch is 13.6 μm and 01 when the track pitch is 20.4 μm, for example.

As illustrated in Figure 9B, the sub-code area also comprises an ID section formed of W1 and W2. The first bit of W1 is assigned to a code indicative of validity (set to 1) or invalidity (set to 0) of data. The next three bits of W1 are a code indicative of a location of an area including a frame. Specifically, this code is set to 000 when the area is located at a read-in area, that is, the beginning of a tape, 001 when in the data area, 010 when in a read-out area, that is, the end of a data recording area, 011 when at the end of medium, that is, the end of the tape 12. The remaining four bits of W1 is assigned to a code indicative of an ordinary frame (set to 0"0), an amble frame used for synchronization or the like (set to 0"1), a frame other than a file mark (set to 000"), a first file mark (set to 001"), a second file mark (set to 010"), or a third file mark (set to 011"). On the other hand, W2 has its first bit set to 1, the next three bits set to 000 which indicates that the following sub-code is a pack format, as will be later referred to, and the last four bits set to a value indicative of a block address.

A variety of determinations and so on are made by means of the above-mentioned information when the DAT 1 is used as a data recorder.

In the above apparatus, the data area is provided, for example, with 5760 bytes of a recording capacity per frame which is formatted as follows:

Referring to Figure 5, the above-mentioned 5670 bytes are divided into words 0 to 1439 each formed of four bytes (32 bits). Each of the words are divided into an L-channel (left channel) and an R-channel (right channel) of 16 bits (2 bytes) each, in accordance with the DAT-formatted audio signal. The first three words (12 bytes) of the 5760 bytes are assigned to a synchronizing area in which all the bits of the first byte are set to 0, all the bits of the subsequent 10 bytes are set to 1, and all the bits of the last byte are set to 0.

Next, eight words (32 bytes) are assigned to a header portion in which the same contents are written in the L-channel and R-channel portions. Specifically, explaining the arrangement of the header portion, the beginning half byte of the fourth word (note that the fourth word is referenced 3(-), the fifth word is referenced 4(+), etc.) is assigned to an area for indicating the condition of the frame in which the same frame ID, VF, and format ID as those in the sub-code area W1 and W1 are provided. The last half byte of the fourth word is assigned to a made area which is set to 0000 to 0011 for CD-ROM and 1000 for DAT (in Figure 5A no assignment code is shown).

The fifth word and the first half byte of the sixth word, together totalling 24 bits, are assigned to a logical frame number (LFNO) area in which a binary value indicative of the serial number of a valid frame from the top of each save set is stored. If an invalid frame is concerned, all bits of this area are set to 0.

The second half byte of the sixth word is assigned to an area indicative of the data condition. Specifically, the four bits at the LSB side thereof are assigned to a code (recording ID) area indicative of a recording type and set to 0000 representing Type 1 streaming, 0001 representing Type 2 streaming and 0010 represeting Type 1 start-stop. The next one bit is assigned to a flag (DH) indicative of whether the data in the header portion is also provided in the data signal suppiled from the bus 3 (set to 1) or not (set to 0). The remaining three bits at the MSB thereof are assigned to a binary-code combination indicative of the number (PFL) of error correcting code frames.

The first half byte of the seventh word is assigned to a binary-code combination indicative of the total number (ECFL) of data signal frames and error correcting code frames. If the number of the frames is not definite, this area is filled with 0. The second half byte of the seventh word is assigned to a binary-code combination indicative of the number (OWNO) of effected over-write operations.

The first half byte of the eighth word is assigned a number (EFNO) which indicates whether the error correcting code has been added. When the first bit at the LSB side thereof is set to 0, it indicates that the concerned frame is a data signal frame. On the other hand, if the first bit is set to 1, it indicates that the concerned frame is an error correcting code frame and the subsequent seven bits thereof are set to a binary-code combination indicative of the serial number of that error correcting code frame, with the first error correcting code frame being designated by 1. If the error correcting code is not added to any frame, all of the bits are set to 0.

The second half byte of the eighth word and the first half byte of the ninth word are assigned to an area indicative of the number (EBL) of bytes of valid data contained in a frame and set to a binary-code combination indicative of the number of bytes.

The second half byte of the ninth word and the tenth and eleventh words are reserved as extended bits and are all set to 0 at the moment.

The subsequent 12th to 1439th words are assigned to a data area which totals 5712 bytes and data signals from the bus 3 are sequentially recorded in these frames in four byte increments.

The 1440th word is assigned to a cyclic redundancy check (CRC) area in which an error correcting code (CRC) is recorded for the data signals written in the header portion and the data area, that is, the error correcting code generated for signals recorded on each of the tracks.

In the DAT format, the L-channel and R-channel data signals are alternately recorded on two adjacent tracks in two byte increments. These alternate tracks are generally identified, for example, by plus and minus (+ and -) azimuth angles of the heads A and B for forming tracks which are marked on both sides of Figures 5A and 5B. Thus, the CRC is generated, for example, for the third word (L3) of the L-channel, the fourth word (R4) of the R-channel, L5, R6, L7 .... in the minus azimuth CRC area. On the other hand, in the plus azimuth CRC area, the CRC is generated for R3, L4, R5, L6, R7 .... .

Therefore, with this format, since the L-channel and R-channel of the header portion (the third to tenth words) have the same contents, that is, the data in the header portion is doubly recorded on the plus and minus azimuth tracks adjacent to each other, it is therefore possible to determine whether there remain unerased portions or not by comparing the contents of the header portion of the plus and minus azimuth tracks. The data in the OWNO area indicative of the number of the overwrite operation is rewritten every time and overwrite if effected. If one of the two adjacent plus azimuth and minus azimuth tracks of a given frame is not over-written, for example, due to clogging occurring in one of the heads for recording signals

on the track, data cannot be recorded and consequently the header data previously recorded on the unerased track is reproduced, so that the header content of the plus azimuth track is not coincident with the header content of the minus azimuth track. Also, the value in the logical frame number (LFNO) area of the plus azimuth track is different from that of the minus azimuth track when the over-write has not been effected. It is therefore possible to judge whether or not an over-write has failed by comparing these values in the plus azimuth and minus azimuth tracks of a given frame with each other. By thus picking up the frame in which data has not been over-written as an error, it is possible to correct the error outside the DAT 1 with certainty.

Incidentally, the synchronizing area provided by the DAT format enables the DAT 1 to be freely synchronized with the controller 2, thereby favourably attending to variations in the amount of data contained in one frame. However, since the same pattern as the synchronizing pattern may appear in data signals, the data in the header portion and data and CRC areas should be scrambled, for example, by adding an arbitary M succession or the like. Specifically, the controller 2 generates data to be written in the header portion for the data signal from the bus 3 and then generates the CRC from the data in the header portion. Then, the data and the CRC are scrambled, to which the synchronizing area is added, and then supplied to the DAT 1.

Further, it is appreciated that since in the above data format the CRC is added to each track, it is possible, outside of the DAT 1, to detect erroneous data in the tracks.

The data signal is formatted in accordance with the DAT rules as described above.

This apparatus allows 2048 bits of data to be recorded in the first and second sub-code areas. If the format for an audio signal is concerned, the 2048 bits of data is divided into packs each formed of 64 bits, in each of which is recorded information such as the time code, recording date and so on of the data recorded therein.

Thus, some of these packs may be assigned to record information on the data recorder. For example, two packs may be used to effect a variety of controls.

Figures 6A and 6B show an arrangement of the packs for this purpose. The 64 bits of each pack are divided into eight words of eight bits each. The four bits at the MSB side of the first word of each pack are assigned to an ITEM area, which is common to the audio signal recording format, and set to a four-bit binary-code combination indicative of the contents of the pack. However, nine of the total of sixteen combinations which can possibly be made by four bits have already been determined for audio signal recording, so that the other combinations are arbitrarily selected from the remaining seven combinations for the data recorder. For example, 0001 is set to the ITEM area of the first pack, and 0010 to the ITEM area of the second pack.

The four bits at the LSB side of the first word and the second word are assigned to an area for indicating a frame condition in which are provided the format ID, area ID, VF and frame ID which are the same as those written in the aforementioned W1 and W2.

The third to fifth words of the first pack are assigned to a file number (FNO) area and are set to a binary-coded combination indicative of the serial number of a file within all of the files of data (set save) backed up at one time.

A total 16-bit area made up of the sixth and seventh words are assigned to a set save number (SSNO) area in which is recorded a binary-code combination indicating how many times the back-up has been carried out from the initial use of the apparatus.

The eighth word of the first pack is assigned to a parity area for the first to seventh words.

A total 48-bit area made up of the third to fifth words of the second pack is assigned to an absolute frame number (AFNO) area in which is recorded a binary-coded combination indicative of the serial number of a frame from the head of the tape 12. The sixth and seventh words are reserved as extended bits and all set to 0 at the moment. The eighth word is assigned to a parity area for the first to seventh words.

Thus, the data signals can be quite smoothly reproduced by identifying these ID codes and so on as described above.

The information which can be formed in the controller 2 is written in the header portion of the data area while the information which can be formed in the DAT 1 is written in the sub-code area.

As shown in Figure 7, the audio DAT format is such that one frame is made up of two oblique tracks formed by one rotation of the head drum 11 and data is interleaved and recorded on the two tracks, wherein even-numbered data of the left channel is recorded in the first half of one (plus azimuth) track of the two tracks forming one frame, odd-numbered data of the right channel in the second half of the same, even-numbered data of the right channel in the first half of the other (minus azimuth) track and odd-numbered data of the left channel in the second half of the same. Reference C in the centre of each track in Figure 7 designates the error correcting code added to each track by the DAT 1.

As explained above, in addition to the error correcting code generated by the audio DAT 1, the data recorder is provided with the ECC generator circuit 26 in the controller 2 for increasing the fidelity thereof. The error correcting code for interleaved data can be generated in the controller 2 by taking out 2n'th data (even-numbered) and 2n-1'th data (odd-numbered) of each frame to form a data sequence. With this additional error correcting code, the error correction can be effected by these two error correcting codes if the tape 12 is horizontally scratched or the like, thereby improving the error correcting ability in such cases.

Thus, the DAT 1 can be employed, as a data recorder, wherein the drum 11 is rotated, for example, at 2000 rpm, so that data is quite rapidly recorded at 192,000 bytes per second, and consequently the consumption of the tape 12 can be reduced. Also, the data can be smoothly recorded by virtue of the error correcting code added thereto.

Since the data signal written in two tracks forming one frame in accordance with the DAT format is provided with means for determining continuity of the tracks, it is easily possible to detect unerased signals due to clogging of the head and so on.

Moreover, since the header portion of the data area is recorded in both the plus azimuth and the minus azimuth tracks forming a frame, it is easily possible to detect and correct previously recorded data signals which have not been over-written, by detecting whether or not the header portions of these tracks contain the same data, thereby providing the data recorder with a high fidelity.

Claims

1. A method of recording digital data signals in a series of track pairs on a recording medium (12), the method comprising the steps of:
receiving digital information signals from an external source and dividing them into frames, each frame corresponding to a different pair of tracks to be recorded on the recording medium (12);
for each of the two tracks forming each frame, providing header portions, having identical contents and containing at least data related to the corresponding digital information signals so as to be able to distinguish between rewritten header portions and unerased previously written header portions, which are each arranged to be recorded before the digital information signals in the respective tracks; and
recording the digital information signals and the header portions in a series of pairs of tracks on the recording medium (12).

2. A method according to claim 1 wherein said header portion providing step additionally comprises providing a frame number which varies in accordance with each frame.

3. A method according to claim 1 wherein said header portion providing step additionally comprises providing an ID signal indicative of a data format.

4. A method according to claim 1 wherein the header portion providing step additionally comprises providing a header portion which includes a signal indicative of the type of source of the digital data signals.

5. A method according to claim 1 wherein the header portion providing step additionally comprises providing a header portion which includes a signal indicative of the total number of error correcting code frames and data signal frames.

6. A method according to claim 1 wherein the header portion providing step additionally comprises providing a header portion which includes a signal indicating the number of times the track to which the header is assigned has been re-recorded with digital data signals.

7. A method according to claim 1 wherein the header portion providing step additionally comprises providing a header portion which includes a signal indicative of the number of bytes of valid data contained in the frame to which the header is assigned.

8. A method of reproducing digital data signals recorded on a recording medium (12), wherein the digital data signals as recorded are formatted into frames, each frame corresponding to two tracks, with an identical header portion being provided at the beginning of each track forming one frame and containing at least data related to the corresponding digital information signals so as to be able to distinguish between rewritten header portions and unerased previously written header portions, it being

intended that the digital data and the header portions of each frame are to be reproduced together, the method comprising the steps of:
reproducing the digital data signals recorded in the tracks on the recording medium (12);
separating the header portions from the reproduced digital data signals and comparing with each other at least parts of the header portions reproduced from the two tracks forming each frame;
determining that the digital data signals written in each frame are erroneous if the data in the parts of the header portions of the two tracks are not identical; and
correcting the erroneous digital data signals of each frame by the use of an error correcting code.

9. An apparatus for recording digital data signals in a series of track pairs on a recording medium (12), the apparatus comprising:
means (14) for receiving digital information signals from an external source and dividing them into frames, each frame corresponding to a different pair of tracks to be recorded on the recording medium (12);
means (2) for providing header portions for each of the two tracks forming each frame, the header portions having identical contents and containing at least data related to the corresponding digital information signals so as to be able to distinguish between rewritten header portions and unerased previously written header portions and each arranged to be recorded before the digital information signals in the respective tracks; and
means (11, A, B) for recording the digital information signals and the header portions in a series of pairs of tracks on the recording medium (12).

10. Apparatus according to claim 9 wherein the incoming digital data signals comprises data words of a right channel and a left channel and wherein the header portion corresponds to a part of the data words of the right and left channels, and wherein the recording means (11, A, B) includes at least two rotary heads (A, B) for recording the identical contents of the header portions.

11. Apparatus according to claim 9 wherein the header portion providing means (2) further provides a header portion which includes a frame number which varies in accordance with each frame.

12. Apparatus according to claim 9 wherein the header portion providing means (2) provides a header portion which includes an ID signal indicative of a data format.

13. Apparatus according to claim 9 wherein the header portion providing means (2) further provides a header portion which includes a signal indicative of the type of source of the digital data signals.

14. Apparatus according to claim 9 wherein the received digital data signals are formatted into frames containing an error correcting code and frames containing information data, and wherein the header portion providing means (2) further provides a header portion which includes a signal indicative of the total number of error correcting code frames and information data frames.

15. Apparatus according to claim 9 wherein the header portion providing means (2) further provides a header portion which includes a signal indicating the number of times the track to which the header is assigned has been re-recorded with digital data signals by the recording means.

16. Apparatus according to claim 9 wherein the header portion providing means (2) further provides a header portion which includes a signal indicative of the number of bytes of valid data contained in the frame to which the header is assigned.

17. Apparatus according to claim 9 wherein the header portion providing means (2) further provides a header portion which includes a logical frame number signal indicative of the serial number of a valid frame from the beginning of each save set.

18. An apparatus for reproducing digital data signals recorded on a recording medium (12) wherein the recorded digital data signals are formatted by being divided into frames, each of which corresponds to two tracks, with each frame including a header portion which is identical in the respective two tracks forming each frame and containing at least data related to the corresponding digital information signals so as to be able to distinguish between rewritten header portions and unerased previously written

header portions, the apparatus comprising:
means (11, A, B) for reproducing the digital data signals recorded in the tracks on the recording medium;
separating and comparing means (2) for separating the header portions from the reproduced signals for each frame and comparing at least parts of the header portions reproduced from the two tracks forming each frame with each other;
means (25) supplied with the results of the separating and comparing means for determining whether the digital data signals written in each frame are erroneous if the comparison result shows that data in the parts of the header portions of the two tracks are not identical; and
error correcting means (22, 21) for correcting the erroneous digital data signals by the use of an error correcting code.

Patentansprüche

1. Verfahren zum Aufzeichnen von digitalen Datensignalen in einer Reihe von Spurenpaaren auf einem Aufzeichnungsmedium (12), mit den Verfahrensschritten:
   Aufnehmen digitaler Informationssignale aus einer externen Quelle und Aufteilen dieser Signale in Rahmen, die jeweils einem unterschiedlichen Paar von auf dem Aufzeichnungsmedium (12) aufzuzeichnenden Spuren entsprechen,
   Erzeugen von Kopfteilen für jede der beiden Spuren, aus denen der Rahmen gebildet ist, wobei diese Kopfteile identische Inhalte haben und wenigstens auf die entsprechenden digitalen Informationssignale bezogene Daten enthalten, die eine Unterscheidung zwischen neu aufgezeichneten Kopfteilen und nicht gelöschten früher aufgezeichneten Kopfteilen ermöglichen, und wobei diese Kopfteile so angeordnet sind, daß sie vor den digitalen Informationssignalen in den betreffenden Spuren aufgezeichnet werden,
   Aufzeichnen der digitalen Informationssignale und der Kopfteile in einer Reihe von Spurenpaaren auf dem Aufzeichnungsmedium (12).

2. Verfahren nach Anspruch 1, bei dem der Verfahrensschritt des Erzeugens der Kopfteile zusätzlich das Erzeugen einer Rahmennummer umfaßt, die sich bei jedem Rahmen ändert.

3. Verfahren nach Anspruch 1, bei dem der Verfahrensschritt des Erzeugens der Kopfteile zusätzlich das Erzeugen eines ein Datenformat anzeigenden Identifizierungssignals umfaßt.

4. Verfahren nach Anspruch 1, bei dem der Verfahrensschritt des Erzeugens der Kopfteile zusätzlich das Erzeugen eines Kopfteils umfaßt, der ein Signal enthält, das die Art der Quelle der digitalen Datensignale anzeigt.

5. Verfahren nach Anspruch 1, bei dem der Verfahrensschritt des Erzeugens der Kopfteile zusätzlich das Erzeugen eines Kopfteils umfaßt, der ein Signal enthält, das die Gesamtzahl der Fehlerkorrekturkoderahmen und der Datensignalrahmen anzeigt.

6. Verfahren nach Anspruch 1, bei dem der Verfahrensschritt des Erzeugens der Kopfteile zusätzlich das Erzeugen eines Kopfteils umfaßt, der anzeigt, wie oft die Spur, der der Kopfteil zugeordnet ist, mit digitalen Datensignalen überschrieben wurde.

7. Verfahren nach Anspruch 1, bei dem der Verfahrensschritt des Erzeugens der Kopfteile zusätzlich das Erzeugen eines Kopfteils umfaßt, der ein Signal enthält, das die Anzahl der Bytes gültiger Daten angibt, die in dem Rahmen enthalten sind, zu dem der Kopfteil gehört.

8. Verfahren zur Wiedergabe von auf einem Aufzeichnungsmedium (12) aufgezeichneten digitalen Datensignalen, die so wie sie aufgezeichnet sind, in Rahmen formatiert sind, die jeweils zwei Spuren entsprechen und eine identischen Kopfteil besitzen, der am Beginn jeder einen Rahmen bildenden Spur angeordnet ist und wenigstens auf die entsprechenden digitalen Informationssignale bezogene Daten enthalten, die eine Unterscheidung zwischen neu aufgezeichneten Kopfteilen und nicht gelöschten früher aufgezeichneten Kopfteilen ermöglichen, wobei die digitalen Daten und die Kopfteile jedes Rahmens zusammen wiedergegeben werden sollen,
   mit den Verfahrensschritten:

Wiedergeben der in den Spuren auf dem Aufzeichnungsmedium (12) aufgezeichneten digitalen Datensignale,

Trennen der Kopfteile von den wiedergegebenen digitalen Datensignalen und Vergleichen zumindest von Teilen der von zwei jeweils einen Rahmen bildenden Spuren wiedergegebenen Kopfteile miteinander,

Feststellen, daß die in den einzelnen Rahmen aufgezeichneten digitalen Datensignale fehlerhaft sind, falls die Daten in den den genannten Teilen der Kopfteile der beiden betreffenden Spuren nicht identisch sind,

Korrigieren der fehlerhaften digitalen Datensignale jedes Rahmens durch Verwendung eines Fehlerkorrekturkodes.

9. Gerät zum Aufzeichnen von digitalen Datensignalen in einer Reihe von Spurenpaaren auf einem Aufzeichnungsmedium (12) mit

einer Einrichtung (14) zum Aufnehmen digitaler Informationssignale aus einer externen Quelle und Aufteilen dieser Signale in Rahmen, die jeweils einem unterschiedlichen Paar von auf dem Aufzeichnungsmedium (12) aufzuzeichnenden Spuren entsprechen,

einer Einrichtung (2) zum Erzeugen von Kopfteilen für jede der beiden Spuren, aus denen der Rahmen gebildet ist, wobei diese Kopfteile identische Inhalte haben und wenigstens auf die entsprechenden digitalen Informationssignale bezogene Daten enthalten, die eine Unterscheidung zwischen neu aufgezeichneten Kopfteilen und nicht gelöschten früher aufgezeichneten Kopfteilen ermöglichen, und wobei diese Kopfteile so angeordnet sind, daß sie vor den digitalen Informationssignalen in den betreffenden Spuren aufgezeichnet werden, und

einer Einrichtung (11, A, B) zum Aufzeichnen der digitalen Informationssignale und der Kopfteile in einer Reihe von Spurenpaaren auf dem Aufzeichnungsmedium (12).

10. Gerät nach Anspruch 9, bei dem die ankommenden digitalen Datensignale Datenwörter eines rechten Kanals und eines linken Kanals enthalten und bei dem der Kopfteil einem Teil der Datenwörter des rechten und des linken Kanals entspricht, wobei die Aufzeichnungseinrichtung (11, A, B) wenigstens zwei rotierende Köpfe (A, B) zum Aufzeichnen der identischen Inhalte der Kopfteile besitzt.

11. Gerät nach Anspruch 9, bei dem die Einrichtung zum Erzeugen des Kopfteils ferner einen Kopfteil erzeugt, der eine Rahmennummer umfaßt, die sich bei jedem Rahmen ändert.

12. Gerät nach Anspruch 9, bei dem die Einrichtung zum Erzeugen der Kopfteile zusätzlich ein Identifizierungssignal erzeugt, das ein Datenformat anzeigt.

13. Gerät nach Anspruch 9, bei dem die Einrichtung zum Erzeugen des Kopfteils zusätzlich einen Kopfteil erzeugt, der ein Signal enthält, das die Art der Quelle der digitalen Datensignale anzeigt.

14. Gerät nach Anspruch 9, bei dem die empfangenen digitalen Datensignale in Rahmen formatiert sind, die einen Fehlerkorrekturkode enthalten, sowie in Rahmen, die Informationsdaten enthalten, und bei dem die Einrichtung zum Erzeugen des Kopfteils außerdem einen Kopfteil erzeugt, der ein Signal enthält, das die Gesamtzahl der Fehlerkorrekturkoderahmen und der Datensignalrahmen anzeigt.

15. Gerät nach Anspruch 9, bei dem die Einrichtung zum Erzeugen des Kopfteils ferner einen Kopfteil erzeugt, der angibt, wie oft die Spur, der der Kopfteil zugeordnet ist, von der Aufzeichnungseinrichtung mit digitalen Datensignalen überschrieben wurde.

16. Gerät nach Anspruch 9, bei dem die Einrichtung zum Erzeugen des Kopfteils ferner einen Kopfteil erzeugt, der ein Signal enthält, das die Anzahl der Bytes gültiger Daten angibt, die in dem Rahmen enthalten sind, zu dem der Kopfteil gehört.

17. Gerät nach Anspruch 9, bei dem die Einrichtung zum Erzeugen des Kopfteils ferner einen Kopfteil erzeugt, der ein logisches Rahmennummernsignal enthält, das die Seriennummer eines gültigen Rahmen von Beginn jedes abgespeicherten Satzes an angibt.

18. Gerät zur Wiedergabe von auf einem Aufzeichnungsmedium (12) aufgezeichneten digitalen Datensignalen, die durch Aufteilung in jeweils zwei Spuren entsprechende Rahmen formatiert sind, wobei jeder

Rahmen einen Kopfteil enthält, der in den beiden betreffenden jeweils einen Rahmen bildenden Spuren, identisch ist, und wenigstens auf die entsprechenden digitalen Informationssignale bezogene Daten enthält, die eine Unterscheidung zwischen neu aufgezeichneten Kopfteilen und nicht gelöschten früher aufgezeichneten Kopfteilen ermöglichen, wobei die digitalen Daten und die Kopfteile jedes Rahmens zusammen wiedergegeben werden sollen,

wobei das Gerät aufweist:

eine Einrichtung (11) zum Wiedergeben der in den Spuren auf dem Aufzeichnungsmedium (12) aufgezeichneten digitalen Datensignale,

eine Trenn- und Vergleichereinrichtung (2) zum Trennen der Kopfteile von den wiedergegebenen digitalen Datensignalen und zum Vergleichen zumindest von Teilen der von zwei jeweils einen Rahmen bildenden Spuren wiedergegebenen Kopfteile miteinander,

mit den Ergebnissen der Trenn- und Vergleichereinrichtung beaufschlagte Mittel (25), die feststellen, daß die in den einzelnen Rahmen aufgezeichneten digitalen Datensignale fehlerhaft sind, falls die Daten in den genannten Teilen der Kopfteile der beiden betreffenden Spuren nicht identisch sind, und

eine Fehlerkorrekturvorrichtung (22, 21) zum Korrigieren der fehlerhaften digitalen Datensignale jedes Rahmens durch Verwendung eines Fehlerkorrekturkodes.

Revendications

1. Procédé d'enregistrement de signaux de données numériques sur une série de paires de pistes d'un support d'enregistrement (12), le procédé comprenant les étapes qui consistent à:

revevoir des signaux numériques d'information d'une source externe et les diviser en blocs, chaque bloc correspondant à une paire différente de pistes à enregistrer sur le support d'enregistrement (12);

pour chacune des deux pistes constituant chaque bloc, fournir des parties en-tête, ayant des contenus identiques et contenant au moins des données relatives aux signaux numériques d'information correspondants de manière à pouvoir faire une distinction entre des parties en-tête réécrites et des parties en-tête précédemment écrites non effacées qui sont disposées chacune pour être enregistrées avant les signaux numériques d'information sur les pistes respectives; et à

enregistrer les signaux numériques d'information et les parties en-tête sur une série de paires de pistes du support d'enregistrement (12).

2. Procédé selon la revendication 1, dans lequel ladite étape de fourniture de parties en-tête consiste en outre à fournir un numéro de bloc qui varie selon chaque bloc.

3. Procédé selon la revendication 1, dans lequel ladite étape de fourniture de parties en-tête consiste en outre à fournir un signal d'identification ID indiquant un format de données.

4. Procédé selon la revendication 1, dans lequel l'étape de fourniture de parties en-tête consiste en outre à fournir une partie en-tête qui comprend un signal indiquant le type de source des signaux de données numériques.

5. Procédé selon la revendication 1, dans lequel l'étape de fourniture de parties en-tête consiste en outre à fournir une partie en-tête qui comprend un signal indiquant le nombre total de blocs de code de correction d'erreurs et de blocs de signaux de données.

6. Procédé selon la revendication 1, dans lequel l'étape de fourniture de parties en-tête consiste en outre à fournir une partie en-tête qui comprend un signal indiquant le nombre de fois où la piste à laquelle est affectée la partie en-tête a été réenregistrée avec des signaux de données numériques.

7. Procédé selon la revendication 1, dans lequel l'étape de fourniture de parties en-tête consiste en outre à fournir une partie en -tête qui comprend un signal indiquant le nombre de multiplets de données correctes contenues dans le bloc auquel est affectée la partie en-tête.

8. Procédé de reproduction de signaux de données numériques enregistrés sur un support d'enregistrement (12), dans lequel les signaux de données numériques tels qu'enregistrés sont mis dans un format par blocs, chaque bloc correspondant à deux pistes, une partie entête identique étant prévue au début de chaque piste constituant un bloc et contenant au moins des données relatives aux signaux numériques d'information correspondants de manière à pouvoir faire une distinction entre des parties

en-tête réécrites et des parties en-tête précédemment écrites non effacées, étant entendu que les données numériques et les parties en-tête de chaque bloc doivent être reproduites ensemble, le procédé comprenant les étapes qui consistent à:

reproduire les signaux de données numériques enregistrés sur les pistes du support d'enregistrement(12);

séparer les parties en-tête des signaux de données numériques reproduits et comparer entre elles au moins des zones des parties en-tête reproduites à partir des deux pistes constituant chaque bloc;

déterminer que les signaux de données numériques écrits dans chaque bloc sont erronés si les données dans les zones des parties en-tête des deux pistes ne sont pas identiques; et à

corriger les signaux de données numériques erronés de chaque bloc par la mise en oeuvre d'un code de correction d'erreurs.

9. Appareil pour enregistrer des signaux de données numériques sur une série de paires de pistes d'un support d'enregistrement (12), l'appareil comprenant:

un moyen (14) pour recevoir des signaux numériques d'information d'une source externe et pour les diviser en blocs, chaque bloc correspondant à une paire différente de pistes à enregistrer sur le support d'enregistrement (12);

un moyen (2) pour fournir des parties en-tête pour chacune des deux pistes constituant chaque bloc, les parties en-tête ayant des contenus identiques et contenant au moins des données relatives aux signaux numériques d'information correspondants de manière à pouvoir faire une distinction entre des parties en-tête réécrites et des parties en-tête précédemment écrites non effacées et disposées chacune pour être enregistrées avant les signaux numériques d'information sur les pistes respectives; et

un moyen (11,A,B) pour enregistrer les signaux numériques d'information et les parties en-tête sur une série de paires de pistes du support d'enregistrement (12).

10. Appareil selon la revendication 9, dans lequel les signaux de données numériques en entrée comprennent des mots de données d'un canal de droite et d'un canal de gauche, dans lequel la partie en-tête correspond à une zone des mots de données des canaux de droite et de gauche, et dans lequel le moyen d'enregistrement (11,A,B) comprend au moins deux têtes rotatives (A,B) pour enregistrer les contenus identiques des parties en-tête.

11. Appareil selon la revendication 9, dans lequel le moyen de fourniture de parties en-tête (2) fournit en outre une partie en-tête qui comprend un numéro de bloc variant selon chaque bloc.

12. Appareil selon la revendication 9, dans lequel le moyen de fourniture de parties en-tête (2) fournit une partie en-tête qui comprend un signal d'identification ID indiquant un format de données.

13. Appareil selon la revendication 9, dans lequel le moyen de fourniture de parties en-tête (2) fournit en outre une partie en-tête qui comprend un signal indiquant le type de source des signaux de données numériques.

14. Appareil selon la revendication 9, dans lequel les signaux de données numériques reçus sont mis dans un format par blocs contenant un code de correction d'erreurs et des blocs contenant des données d'information, et dans lequel le moyen de fourniture de parties en-tête (2) fournit en outre une partie en-tête qui comprend un signal indiquant le nombre total de blocs de code de correction d'erreurs et de blocs de données d'information.

15. Appareil selon la revendication 9, dans lequel le moyen de fourniture de parties en-tête (2) fournit en outre une partie en-tête qui comprend un signal indiquant le nombre de fois où la piste à laquelle est affectée la partie en-tête a été réenregistrée avec des signaux de données numériques par le moyen d'enregistrement.

16. Appareil selon la revendication 9, dans lequel le moyen de fourniture de parties en-tête (2) fournit en outre une partie en-tête qui comprend un signal indiquant le nombre de multiplets de données correctes contenues dans le bloc auquel est affectée la partie en-tête.

17. Appareil selon la revendication 9, dans lequel le moyen de fourniture de parties en-tête (2) fournit en

outre une partie en-tête qui comprend un signal de numéro de bloc logique indiquant le numéro de série d'un bloc correct à partir du début de chaque jeu sauvegardé.

18. Appareil pour reproduire des signaux de données numériques enregistrés sur un support d'enregistrement (12), dans lequel les signaux de données numériques enregistrés sont mis dans un format en étant divisés en blocs dont chacun correspond à deux pistes, chaque bloc incluant une partie en-tête qui est identique sur les deux pistes respectives constituant chaque bloc et contenant au moins des données relatives aux signaux numériques d'information correspondants de manière à pouvoir faire une distinction entre des parties en-tête réécrites et des parties en-tête précédemment écrites non effacées, l'appareil comprenant:

un moyen (11,A,B) pour reproduire les signaux de données numériques enregistrés sur les pistes du support d'enregistrement;

des moyens de séparation et de comparaison (2) pour séparer les parties en-tête des signaux reproduits pour chaque bloc et comparer au moins des zones des parties en-tête reproduites à partir des deux pistes constituant chaque bloc entre elles;

un moyen (25) recevant les résultats des moyens de séparation et de comparaison pour déterminer si les signaux de données numériques écrits dans chaque bloc sont ou non erronés si le résultat de la comparaison indique que des données des zones des parties en-tête des deux pistes ne sont pas identiques; et

un moyen de correction d'erreurs (22,21) pour corriger les signaux de données numériques erronés par la mise en oeuvre d'un code de correction d'erreurs.

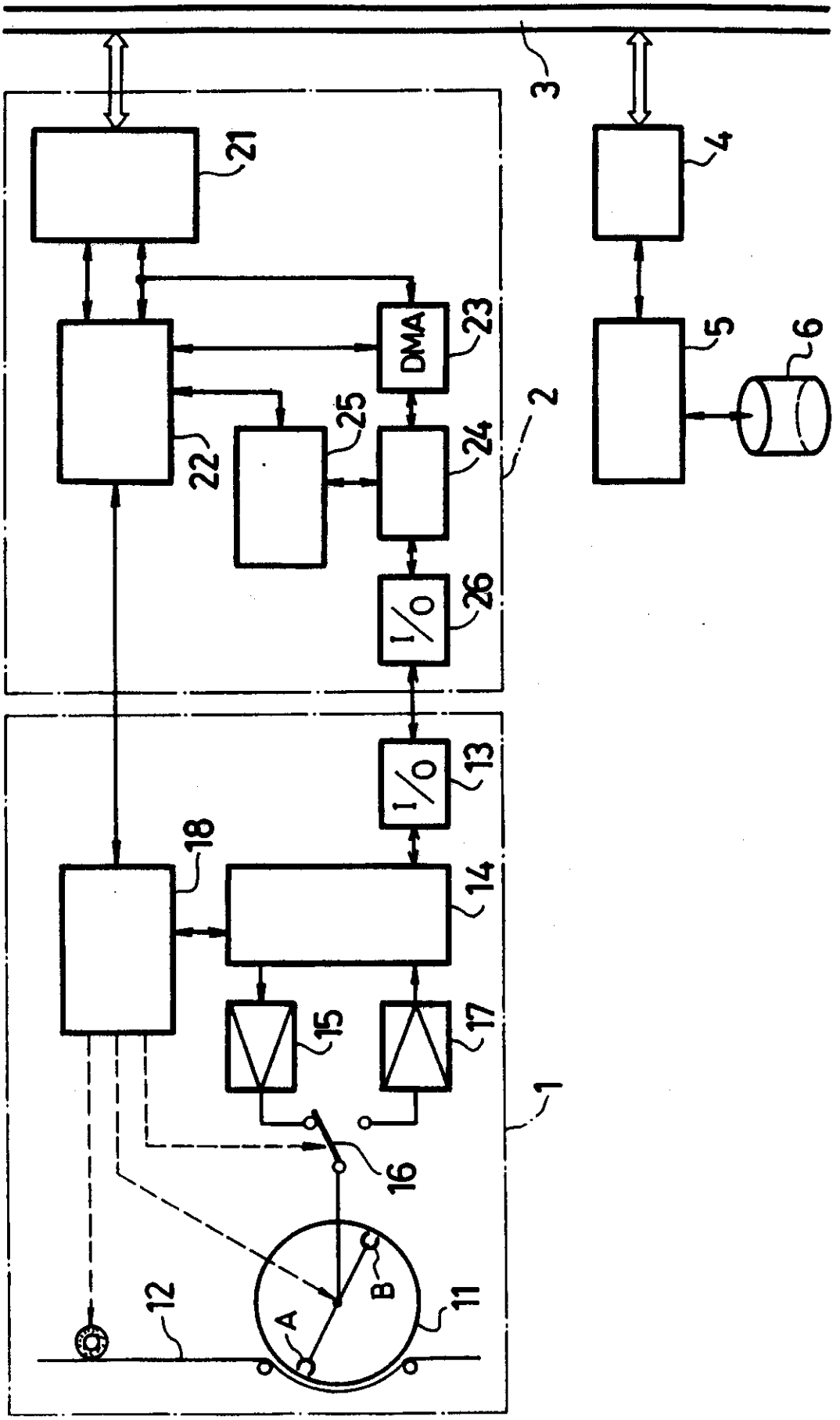


FIG. 1

FIG. 2

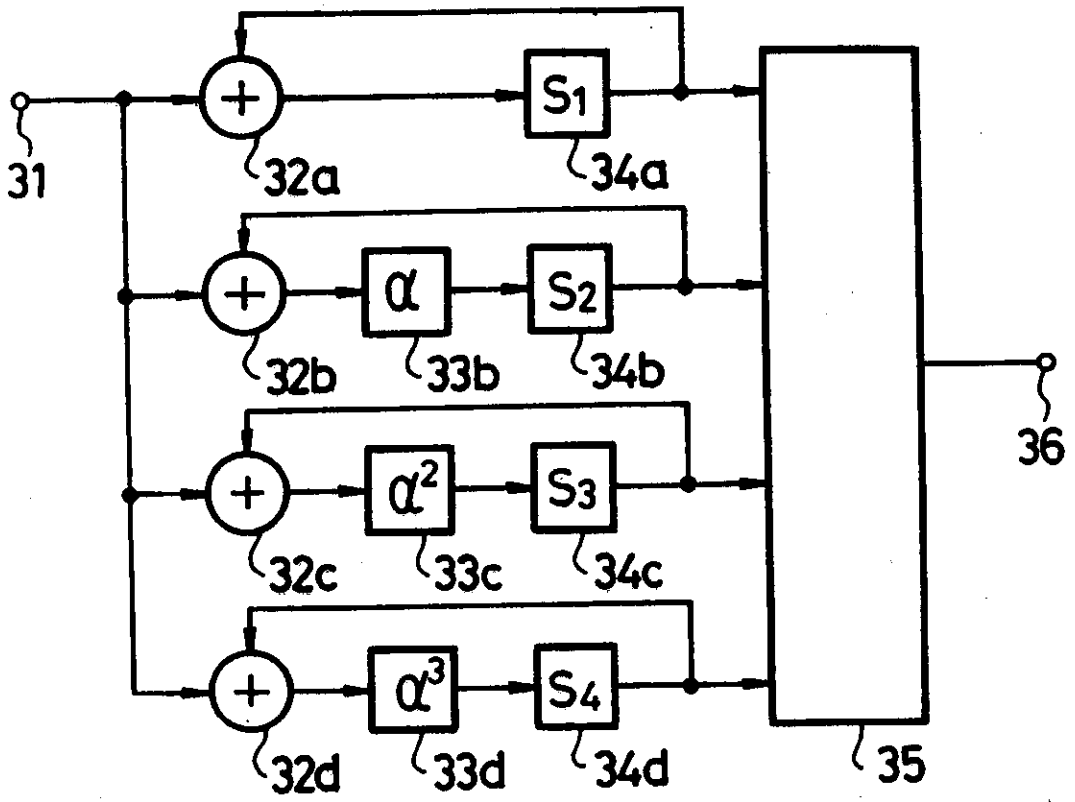
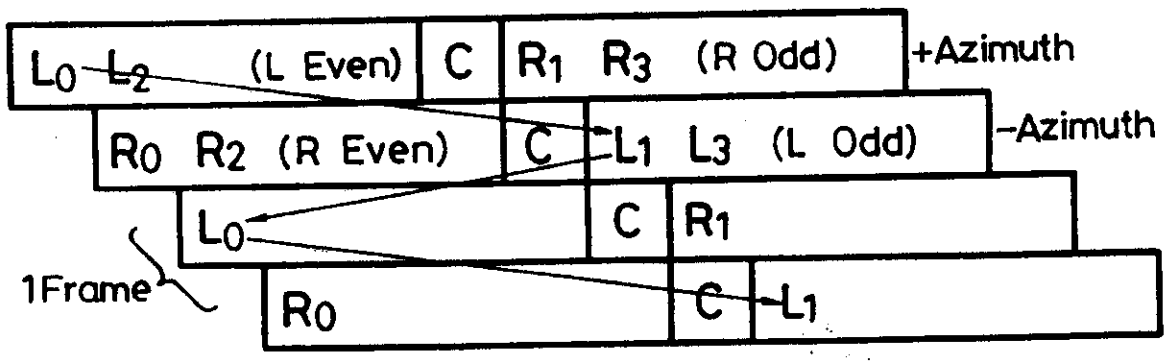

31
32a
S1
34a
32b
α
33b
S2
34b
32c
α²
33c
S3
34c
32d
α³
33d
S4
34d
35
36

FIG. 7


L0 L2 (L Even)
C
R1 R3 (R Odd)
+Azimuth
R0 R2 (R Even)
C
L1 L3 (L Odd)
-Azimuth
L0
C
R1
1Frame
R0
C
L1

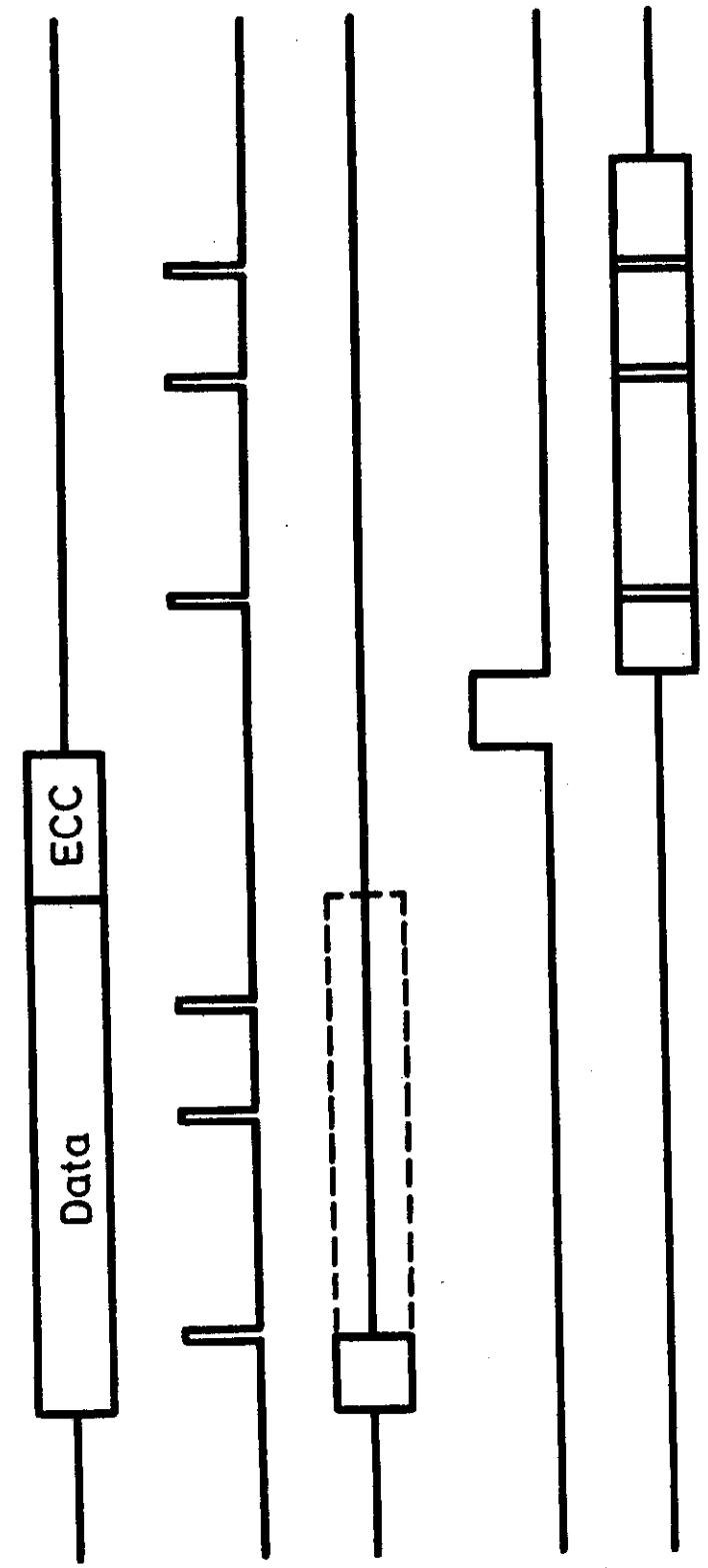


FIG. 3A

FIG. 3B

FIG. 3C

FIG. 3D

FIG. 3E

FIG. 4

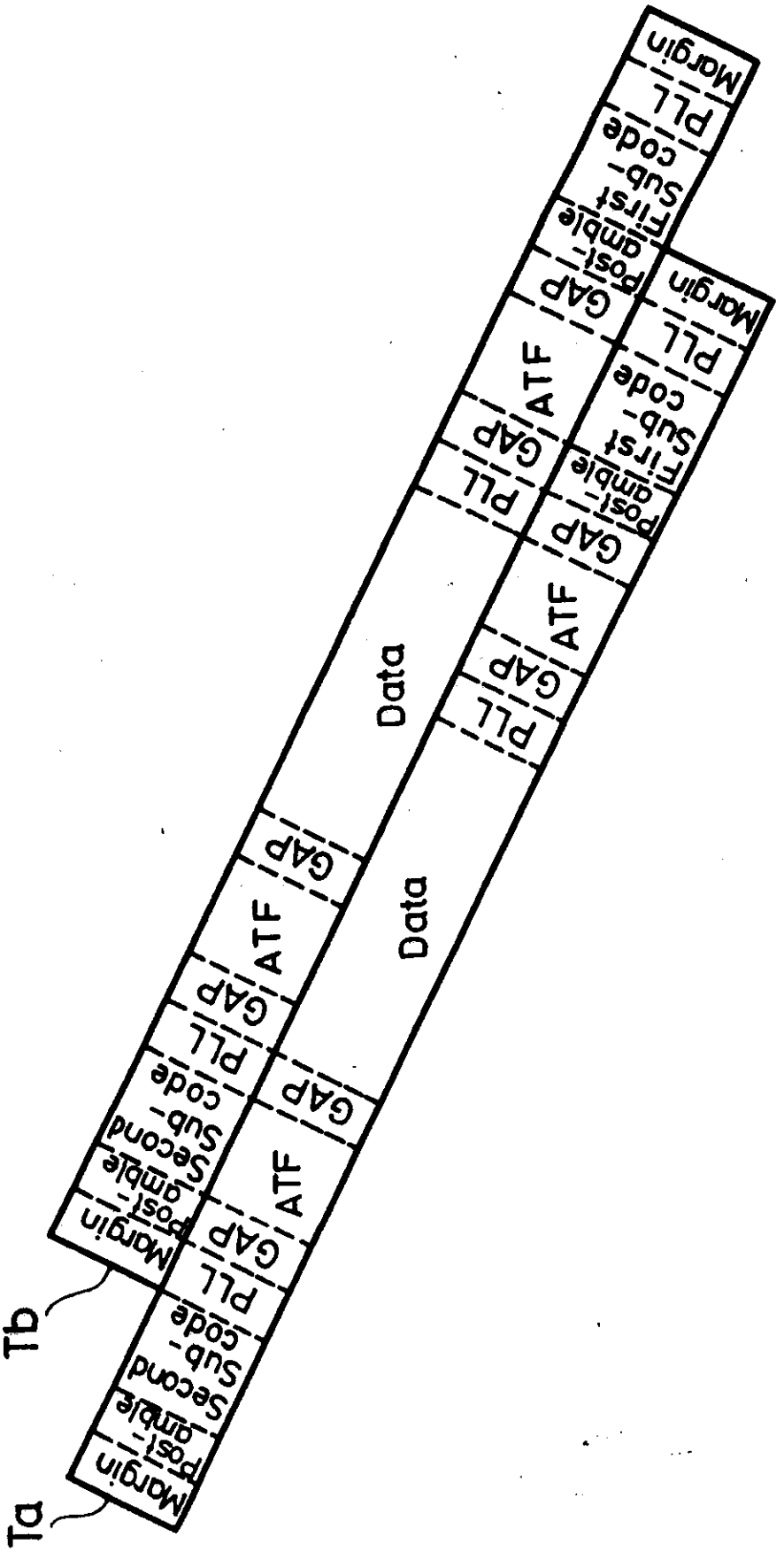

Ta
Tb
Margin
Post-amble
Second Sub-code
PLL
GAP
ATF
GAP
PLL
Data
GAP
ATF
GAP
PLL
Data
GAP
ATF
GAP
PLL
Post-amble
First Sub-code
PLL
Margin

FIG. 5A FIG. 5B

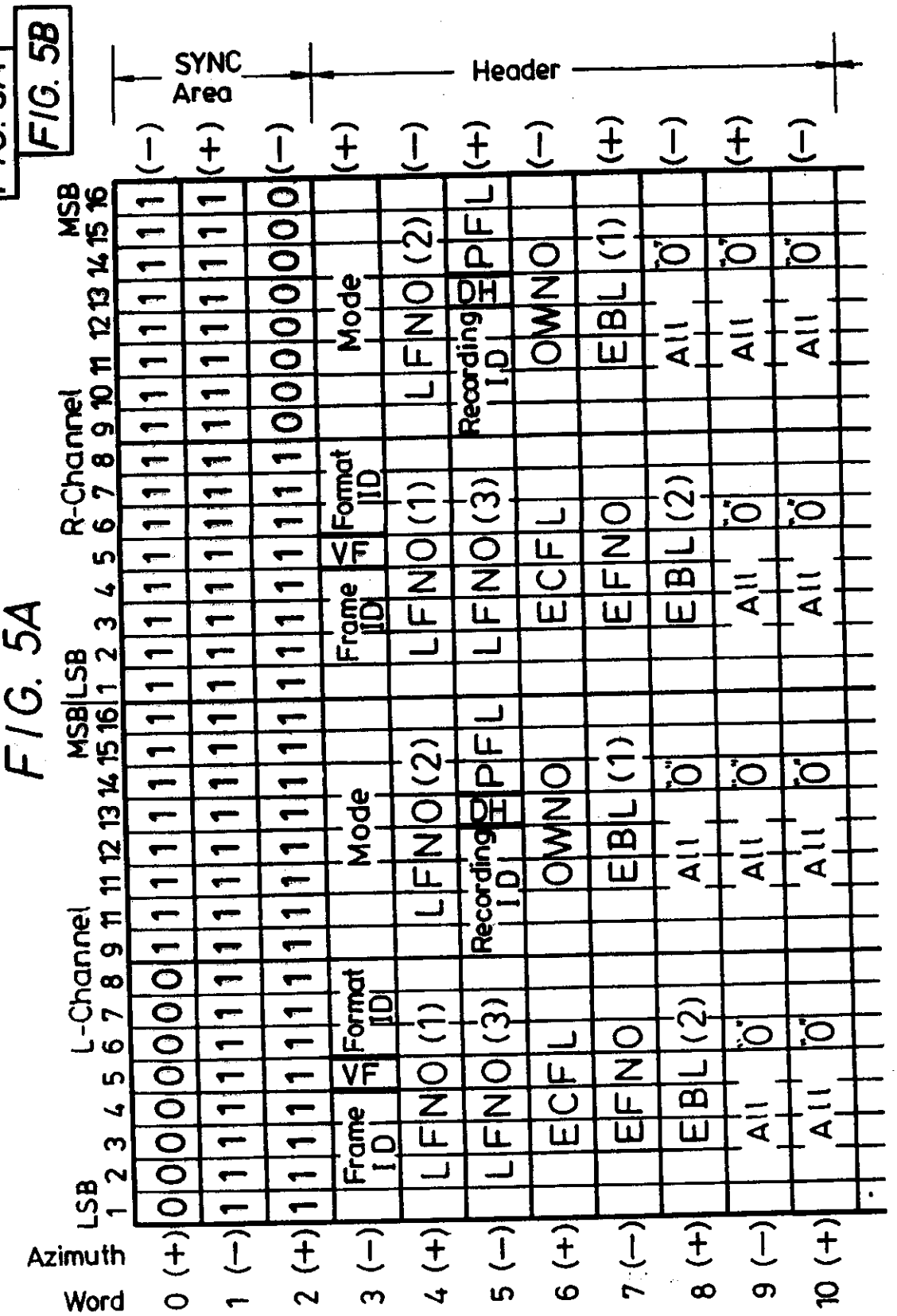


FIG. 5A

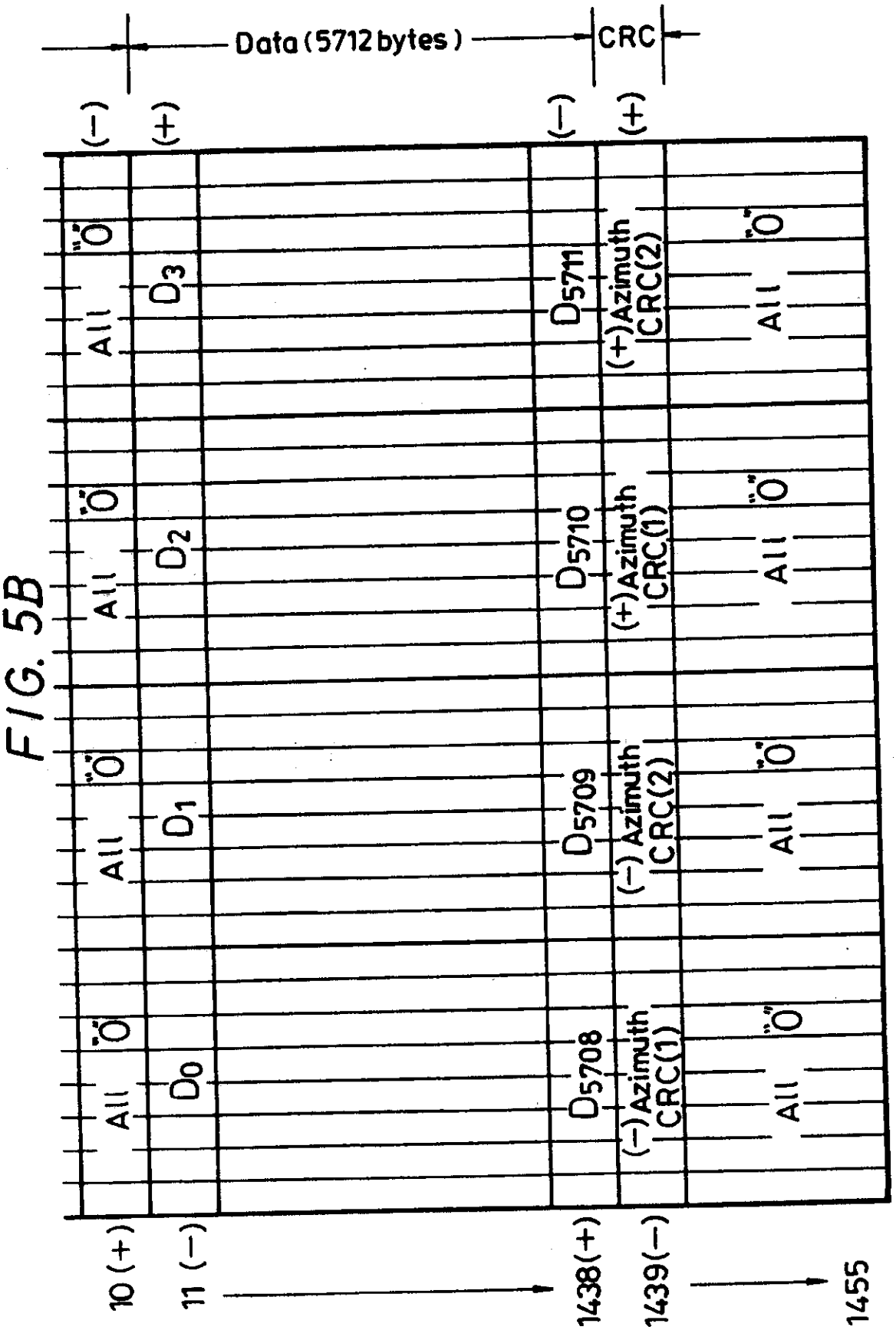

Data (5712 bytes)
CRC
(−)
(+)
"0"
All
D0
D1
D2
D3
D5708
D5709
D5710
D5711
(−) Azimuth CRC(1)
(−) Azimuth CRC(2)
(+) Azimuth CRC(1)
(+) Azimuth CRC(2)
10 (+)
11 (−)
1438(+)
1439(−)
1455

FIG. 5B

FIG. 6A

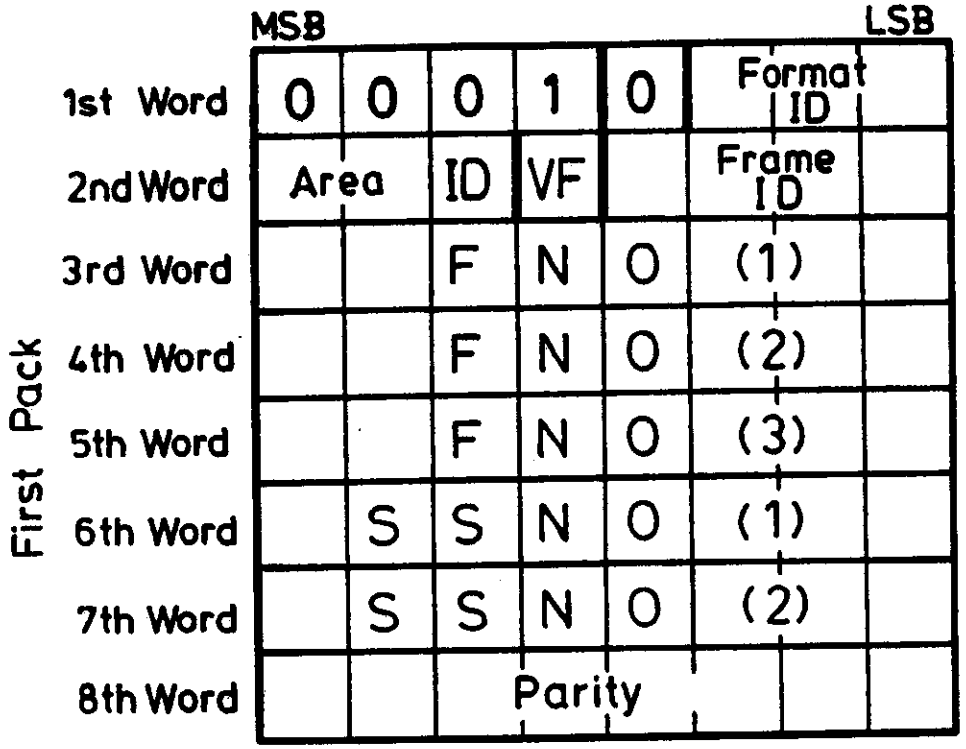

MSB
LSB
First Pack
1st Word
2nd Word
3rd Word
4th Word
5th Word
6th Word
7th Word
8th Word
0 0 0 1 0 Format ID
Area ID VF Frame ID
F N O (1)
F N O (2)
F N O (3)
S S N O (1)
S S N O (2)
Parity

FIG. 6B

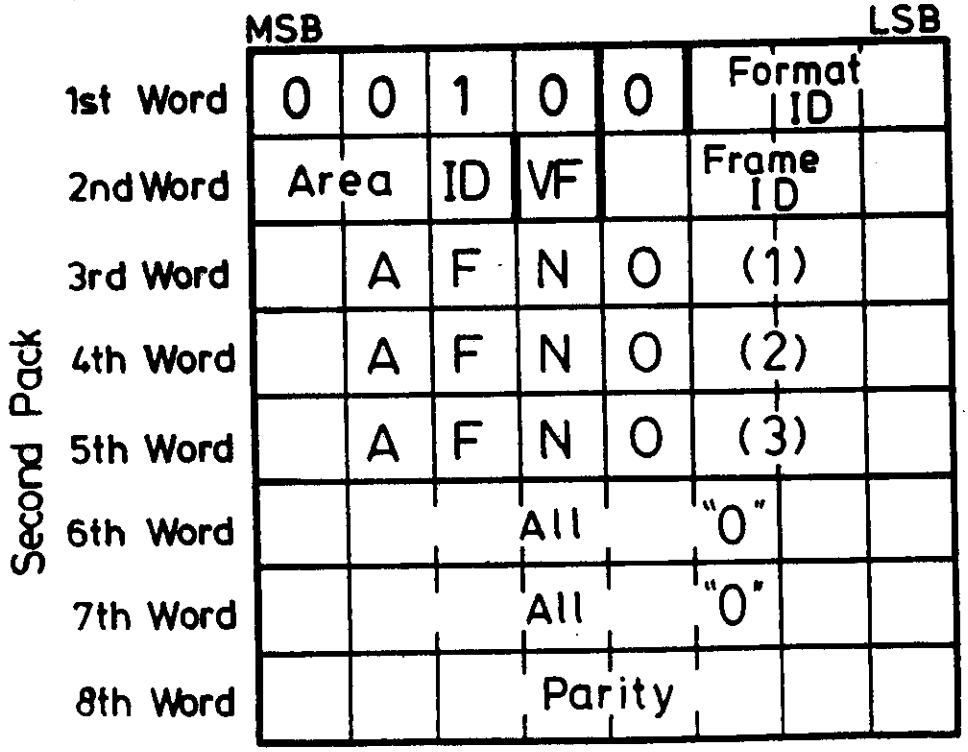

MSB
LSB
Second Pack
1st Word
2nd Word
3rd Word
4th Word
5th Word
6th Word
7th Word
8th Word
0 0 1 0 0 Format ID
Area ID VF Frame ID
A F N O (1)
A F N O (2)
A F N O (3)
All "0"
All "0"
Parity

FIG. 8

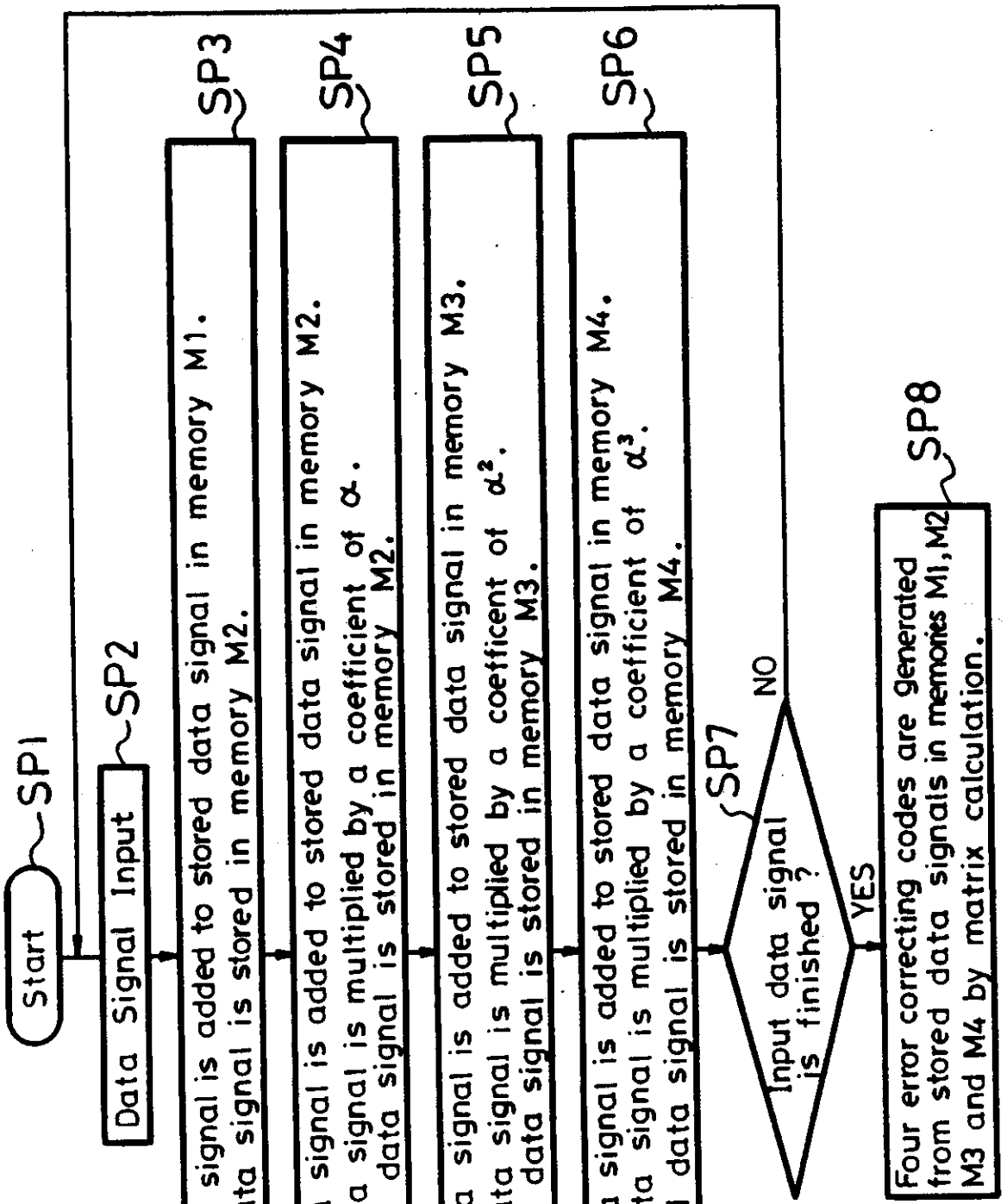

Start
SP1
Data Signal Input
SP2
An input data signal is added to stored data signal in memory M1.
The added data signal is stored in memory M2.
SP3
The input data signal is added to stored data signal in memory M2.
The added data signal is multiplied by a coefficient of α.
The multiplied data signal is stored in memory M2.
SP4
The input data signal is added to stored data signal in memory M3.
The added data signal is multiplied by a coefficent of α².
The multiplied data signal is stored in memory M3.
SP5
The input data signal is added to stored data signal in memory M4.
The added data signal is multiplied by a coefficient of α³.
The multiplied data signal is stored in memory M4.
SP6
SP7
Input data signal is finished ?
NO
YES
Four error correcting codes are generated from stored data signals in memories M1, M2 M3 and M4 by matrix calculation.
SP8

FIG. 9A

W1 (DATA-ID) 8 bit			W2 (Block Address) 8 bit
ID-0	ID-1	Frame Address	0 X X X X 0 0 0
Optional Code			0 ↑ 0 0 1
ID-2	ID-3	Frame Address	0 ↑ 0 1 0
Optional Code			0 ↑ 0 1 1
ID-4	ID-5	Frame Address	0 ↑ 1 0 0
Optional Code			0 ↑ 1 0 1
ID-6	ID-7	Frame Address	0 ↑ 1 1 0
Optional Code			0 ↑ 1 1 1

FIG. 9B

SUB-CODE ID				
W1 (8 bit)			W2 (8 bit)	
Validity	Location	Frame Filemark		Block Address
0	0 0 0	0 * * 0	1 0 0 0	X X X X

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