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- (71) Applicant: X-CELEPRINT LIMITED [IE/IE]; Lee Maltings, Dyke Parade, Cork (IE).
- (72) Inventors: BOWER, Christopher; c/o X-Celeprint Limited, Lee Maltings, Dyke Parade, Cork (IE). MEITL, Matthew; c/o X-Celeprint Limited, Lee Maltings, Dyke Parade, Cork (IE).
- (74) Agents: KIRKHAM, Nicholas et al.; St Botolph's House, 7-9 St Botolph's Road, Sevenoaks Kent TN13 3AJ (GB).
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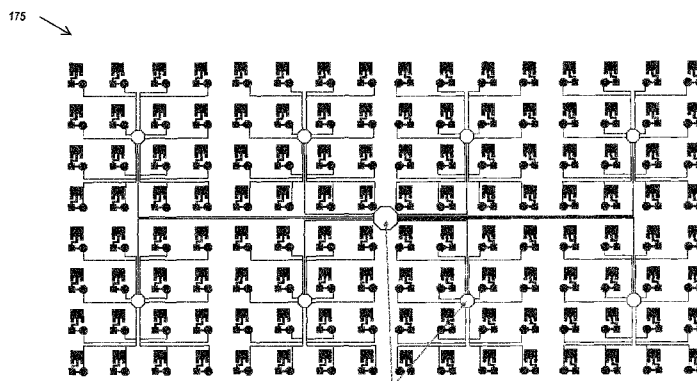
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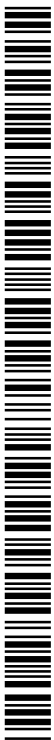
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Arrays of control elements interlaced within arrays of micro-assembled radio frequency components

FIG. 1C

(57) Abstract: Phased-array antenna systems can be constructed using transfer printed active components. Phased-array antenna systems benefit from a large number of radiating elements (e.g., more radiating elements can form sharper, narrower beams (higher gain)). As the number of radiating elements increases, the size of the part and the cost of assembly increases. High throughput micro assembly (e.g. by micro-transfer printing) mitigates costs associated with high part-count. Micro assembly is advantaged over monolithic approaches that form multiple radiating elements on a semiconductor wafer because micro assembly uses less semiconductor material to provide the active components that are necessary for the array. The density of active components on the phased-array antenna system is small. Micro assembly provides a way to efficiently use semiconductor material on a phased array, reducing the amount of non-active semiconductor area (e.g., the area on the semiconductor material that does not include transistors, diodes, or other active components).



MICRO ASSEMBLED HIGH FREQUENCY DEVICES AND ARRAYS**RELATED APPLICATIONS**

This application claims priority to and the benefit of U.S. Provisional Patent Application No. 62/014,074, filed June 18, 2014, titled "Micro Assembled High Frequency Devices and Arrays," and U.S. Provisional Patent Application No. 62/014,079, filed June 18, 2014, titled "System and Methods for Providing Micro Assembled Devices," the contents of each of which are incorporated by reference herein in their entirety.

FIELD OF THE INVENTION

The present invention relates to micro-assembled, for example using micro transfer printing technology, high frequency devices and arrays.

BACKGROUND OF THE INVENTION

A phased array is an array of antennas in which the relative phases of the respective signals supplied to the antennas are used to focus the radiation pattern of the array in a desired direction. The signals provided to the array of antennas enable the array of antennas to achieve improved performance over that of a single antenna. The antenna array can, among other things, increase overall gain, receive or transmit a greater diversity of signals, cancel out interference, steer the radiation pattern in a specific direction, or determine the direction of incoming signals. The phase relationship among the antennas can be fixed to form a tower array.

Alternatively, the phase relationship among the antennas can be adjustable to form a beam-steering array. Beam steering allows the direction of the main lobe of a radiation pattern to be changed using constructive and destructive interference between the electromagnetic signals emitted from the various antennas in the array of antennas. This is typically

accomplished by switching the antenna elements or by changing the relative phases of the signals (such as RF signals) driving each of the antenna elements.

An example of a beam-steering array is the Advanced Modular Incoherent Scatter Radar (AMISR) by SRI International of Menlo Park, CA. AMISR has three separate radar
5 faces, with each face including 128 building-block-like panels over a 30- by 30-meter roughly square surface. AMISR is made up of 4,096 antennas, giving a combined power of up to two megawatts. By controlling the relative phases of the signals coming from the individual antennas, the radar beam can be steered almost instantaneously from one position in the sky to another. This allows the study of rapidly moving features of the atmosphere. Remote operation
10 and electronic beam steering allow researchers to operate and position the radar beam to accurately measure rapidly changing space weather events. However, AMISR is roughly the size of a football field.

Phased-array radar systems are also used by the navy in ships as the phased-array radars allow the ships to use a single radar system for surface detection and tracking, finding other
15 ships, and air detection and tracking. Ship-borne phased-array radar systems can use beam steering to track many targets simultaneously while also controlling several in-flight missiles.

Phased-array antenna systems benefits from a large number of radiating elements. The use of more radiating elements enables sharper and narrower beams that provide higher gain. However, as the number of radiating elements increases, the size of the system and the cost of
20 assembly likewise increases, limiting the application of phased-array antenna systems, especially for consumer products. While many applications do exist for phased-array radars, relatively few have been explored since the size and cost of phased-array radars are prohibitive for many applications.

Among other things, as the size of the components shrinks, the difficulty of arranging
25 a plurality of diverse elements increases. Semiconductor chip- or die-automated assembly

equipment typically uses vacuum-operated placement heads, such as vacuum grippers or pick-and-place tools, to pick up and apply devices to a substrate. It is often difficult to pick up and place ultra-thin and/or small devices using this technology.

Some electronic devices are difficult to construct by conventional assembly techniques due to their ultra-thin and/or small dimensions. For example, some electronic devices (e.g., micro-integrated circuits) can be less than 0.1 mm in one lateral dimension. Moreover, some electronic devices benefit from a large number of radiating elements (e.g., phased-array radars incorporating more radiating elements can form sharper, narrower beams with higher gain). However, as the number of radiating elements increases, the area needed for the parts and the cost of assembly increases. Furthermore, the spatial distribution of elements such as antennas can result in an inefficient use of area for phased-array antenna systems.

Thus, there is a need for phased-array antenna systems and methods of manufacturing thereof that enable phased-array antenna systems to be packaged into small-scale systems utilizing less semiconductor material than monolithic approaches.

SUMMARY OF THE INVENTION

The disclosed technology provides phased-array antenna systems and methods of manufacturing thereof that enable phased-array antenna systems to be packaged into small-scale systems utilizing less semiconductor material than monolithic approaches. In some embodiments, the density of active components on the phased-array antenna system is small (e.g., 5 % or less). In other embodiments, depending on the application, the active components can be densely packed on a destination substrate. Micro assembly provides a way to efficiently use semiconductor material in a phased array, reducing the amount of non-active semiconductor area (e.g., the area on the semiconductor material that does not include

transistors, diodes, or other active components). Moreover, high-throughput micro assembly (e.g. by micro transfer printing) mitigates costs associated with large part counts and allows small, micro-scale devices in some embodiments to be accurately arranged into larger systems.

5 Micro transfer printing permits the selection and application of ultra-thin, fragile, or small devices without cause damage to the devices themselves. Micro-structured stamps can be used to pick up micro devices, transport the micro devices to a destination substrate, and print the micro devices onto the destination substrate. Surface adhesion forces are used to control the selection and printing of these devices onto the destination substrate. This process
10 can be performed in massive parallel. The stamps can be designed to transfer hundreds to thousands of discrete structures in a single pick-up-and-print operation.

 Micro transfer printing also enables parallel assembly of high-performance semiconductor devices onto virtually any substrate material, for example, glass, plastics, metals, or semiconductors. The substrates can be flexible, thereby permitting the production
15 of flexible electronic devices. Flexible substrates can be integrated in a large number of configurations, for example, configurations not possible with brittle silicon-based electronic devices. Additionally, plastic substrates, for example, are mechanically rugged and can be used to provide electronic devices that are less susceptible to damage or electronic performance degradation caused by mechanical stress. Thus, these materials can be used to
20 fabricate electronic devices by continuous, high-speed printing techniques capable of generating electronic devices over large substrate areas at low cost (e.g., roll-to-roll manufacturing).

 Moreover, these micro transfer printing techniques can be used to print semiconductor devices at temperatures compatible with assembly on plastic polymer substrates. In addition,
25 semiconductor materials can be printed onto large areas of substrates thereby enabling

continuous, high-speed printing of complex integrated electrical circuits over large substrate areas. Furthermore, fully flexible electronic devices with good electronic performance in flexed or deformed device orientations can be provided to enable a wide range of flexible electronic devices.

5 In one aspect, the invention is directed to a method of forming a phased-array antenna structure using printed micro assembled active components, the method comprising: providing a plurality of antennas on a destination substrate; forming a plurality of amplifiers on a first substrate; forming a plurality of phase-control devices on a second substrate; contacting the first substrate with an etchant, thereby removing at least one of a portion of a
10 first sacrificial layer underneath the plurality of amplifiers and forming a plurality of printable amplifiers, each printable amplifier connected to the first substrate by one or more tethers; contacting the second substrate with an etchant, thereby removing at least one of a portion of a second sacrificial layer underneath the plurality of phase-control devices and forming a plurality of printable phase-control devices, each printable phase-control device
15 connected to the second substrate by one or more tethers; exposing at least a portion of the plurality of printable amplifiers and plurality of printable phase-control devices to chemical agents for conditioning or processing the newly exposed surfaces of the plurality of printable amplifiers and plurality of printable phase-control devices; and transferring, by micro
20 assembly, at least a portion of the plurality of printable amplifiers and plurality of printable phase-control devices to the destination substrate and electrically interconnecting the antennas, the amplifiers, and the phase-control devices, to thereby form a phased-array antenna system using an array of high-frequency micro-scale devices from multiple source wafers.

 In certain embodiments, transferring at least a portion of the plurality of printable
25 amplifiers and plurality of printable phase-control devices to a destination substrate

comprises: contacting the portion of the plurality of printable amplifiers with a transfer device, wherein contact between the transfer device and the portion of the plurality of printable amplifiers temporarily binds the portion of the plurality of printable amplifiers to the transfer device; contacting the portion of the plurality of printable amplifiers disposed on the transfer device with the receiving surface of the destination substrate; separating the transfer device from the portion of the plurality of printable amplifiers, thereby transferring the portion of the plurality of printable amplifiers onto the destination substrate; contacting the portion of the plurality of printable phase-control devices with a transfer device, wherein contact between the transfer device and the portion of the plurality of printable phase-control devices temporarily binds the portion of the plurality of printable phase-control devices to the transfer device; contacting the portion of the plurality of printable phase-control devices disposed on the transfer device with the receiving surface of the destination substrate; and separating the transfer device from the portion of the plurality of printable phase-control devices, thereby transferring the portion of the plurality of printable phase-control devices onto the destination substrate.

In certain embodiments, the plurality of antennas comprise a plurality of patch antennas.

In certain embodiments, the method further comprises: forming anchoring structures and tethering structures in each of the native substrates, such that the released or releasable structures are connected to their respective native substrates by the anchoring structures or tethering structures following contact of each of the native substrates with the etchant.

In certain embodiments, the method further comprises: forming anchoring or tethering structures from non-epitaxial materials such that the released or releasable structures are connected to their respective native substrate by the anchoring structures or tethering structures following contact of the substrate with the etchant.

In certain embodiments, the method further comprises: forming one or more encapsulating structures to encapsulate at least a portion of the released or releasable structure.

5 In certain embodiments, the first sacrificial layer comprises a portion of the first substrate. In certain embodiments, the second sacrificial layer comprises a portion of the second substrate. In certain embodiments, the chemical etch gains access to the sacrificial layer through points of ingress formed in the one or more tethers.

In certain embodiments, the chemical etch exits the space formerly occupied by at least a portion of the sacrificial layer through points of egress in the one or more tethers.

10 In certain embodiments, the points of egress are the same as the points of ingress.

In certain embodiments, the destination substrate is a member selected from the group consisting of polymer, plastic, resin, polyimide, PEN, PET, metal, metal foil, glass, a semiconductor, and sapphire. In certain embodiments, the destination substrate has a transparency greater than or equal to 50%, 80%, 90%, or 95% for visible light.

15 In another aspect, the invention is directed to a device comprising: a destination substrate; and a multilayer structure on the destination substrate, wherein the multilayer structure comprises a plurality of printed capacitors stacked on top of each other with an offset between each capacitor along at least one edge of the capacitors.

20 In certain embodiments, the offset is in one dimension. In certain embodiments, the offset is in two dimensions. In certain embodiments, the offset is such that a portion of a top surface of each capacitor is exposed.

In certain embodiments, each capacitor of the plurality of capacitors has a capacitance between 100 nF/mm² and 400 nF/mm². In certain embodiments, each capacitor of the plurality of capacitors has a thickness of from 1 μm to 10 μm, 10 μm to 30 μm, 30 μm to 50
25 μm, or 50 μm to 100 μm. In certain embodiments, each capacitor of the plurality of

capacitors has a width of from 10 μm to 50 μm , 50 μm to 100 μm , or 100 μm to 200 μm . In certain embodiments, each capacitor of the plurality of capacitors has a length of from 10 μm to 50 μm , 50 μm to 100 μm , or 100 μm to 200 μm . In certain embodiments, the plurality of capacitors are a same shape and size.

5 In certain embodiments, the plurality of printed capacitors are connected in at least one of parallel or series.

In certain embodiments, the destination substrate is a member selected from the group consisting of polymer, plastic, resin, polyimide, PEN, PET, metal, metal foil, glass, a semiconductor, and sapphire.

10 In certain embodiments, the destination substrate has a transparency greater than or equal to 50%, 80%, 90%, or 95% for visible light.

In another aspect, the invention is directed to a wafer of printable capacitors, the wafer comprising: a source substrate; a first sacrificial layer on a process side of the source substrate; a first set of printable capacitors on the first sacrificial layer; a second sacrificial layer on the first set of printable capacitors; and a second set of printable capacitors on the
15 second sacrificial layer.

In certain embodiments, each printable capacitor of the second set of printable capacitors is disposed above a printable capacitor of the first set of printable capacitors. In certain embodiments, each of the first and second sets of printable capacitors forms an array
20 of capacitors. In certain embodiments, the density of each of the first and second sets of printable capacitors is 5 to 15 capacitors per square millimeter.

In certain embodiments, each capacitor of the plurality of capacitors has a thin metal-insulator-metal structure with a thickness of from 1 μm to 10 μm , 10 μm to 30 μm , 30 μm to 50 μm , or 50 μm to 100 μm . In certain embodiments, each capacitor of the plurality of
25 capacitors has a width of from 10 μm to 50 μm , 50 μm to 100 μm , or 100 μm to 200 μm . In

certain embodiments, each capacitor of the plurality of capacitors has a length of from 10 μm to 50 μm , 50 μm to 100 μm , or 100 μm to 200 μm .

In certain embodiments, each of the first and second sacrificial layers comprises at least one member selected from the group consisting of SiN, SiO₂, and Si.

5 In certain embodiments, the substrate is a member selected from the group consisting of: glass, sapphire, Al₂O_x, gallium arsenide, gallium nitride, silicon, and germanium, silicon carbide, plastic, silicon wafer, silicon on insulator wafer, polycrystalline silicon wafer, GaAs wafer, silicon on substrate wafer, germanium wafer, thin films of polycrystalline silicon wafer, and silicon wafer.

10 In certain embodiments, each capacitor of the plurality of printable capacitors has a capacitance from 100 nF/mm² to 400 nF/mm². In certain embodiments, each of the plurality of printable capacitors have a same shape and size.

In another aspect, the invention is directed to a method for assembling a plurality of capacitors on a receiving surface of a substrate, the method comprising: contacting a first
15 capacitor of the plurality of capacitors with a transfer device having a contact surface, thereby temporarily binding the capacitor to the contact surface such that the contact surface has the capacitor temporarily disposed thereon; contacting the first capacitor disposed on the contact surface of the transfer device with the receiving surface of the substrate; separating the contact surface of the transfer device and the capacitor, wherein the capacitor is transferred
20 onto the receiving surface, thereby assembling the capacitor on the receiving surface of the substrate; contacting a second capacitor of the plurality of capacitors with the transfer device, thereby binding the second capacitor to the contact surface such that the contact surface has the second capacitor disposed thereon; contacting the second capacitor disposed on the contact surface of the transfer device with a surface of the first capacitor assembled on the
25 receiving surface of the substrate; and separating the contact surface of the transfer device

and the second capacitor, wherein the second capacitor is transferred onto the capacitor assembled on the receiving surface of the substrate, thereby assembling the second capacitor on the capacitor assembled on the receiving surface of the substrate.

In certain embodiments, the second capacitor is offset from the first capacitor. In
5 certain embodiments, the offset is in one dimension. In certain embodiments, the offset is in two dimensions. In certain embodiments, the offset is such that a portion of the top surface of each capacitor is exposed. In certain embodiments, each capacitor of the plurality of capacitors has a capacitance from 100 nF/mm² to 400 nF/mm². In certain embodiments, the plurality of capacitors are a same shape and size. In certain embodiments, each capacitor of
10 the plurality of capacitors has a thin metal-insulator-metal structure with a thickness of from 1 μm to 10 μm, 10 μm to 30 μm, 30 μm to 50 μm, or 50 μm to 100 μm. In certain embodiments, each capacitor of the plurality of capacitors has a width of from 10 μm to 50 μm, 50 μm to 100 μm, or 100 μm to 200 μm. In certain embodiments, each capacitor of the plurality of capacitors has a length of from 10 μm to 50 μm, 50 μm to 100 μm, or 100 μm to
15 200 μm.

In certain embodiments, the first capacitor and the second capacitor are electrically connected via thin-film wafer-level interconnections.

In certain embodiments, the first capacitor and the second capacitor are connected in parallel. In certain embodiments, the first capacitor and the second capacitor are connected in
20 series. In certain embodiments, the first capacitor is electrically connected via thin-film wafer-level interconnections. In certain embodiments, the first capacitor disposed on the transfer device is contacted with a region of the receiving surface with a placement accuracy greater than or equal to 25 microns.

In certain embodiments, an adhesive layer is provided on the receiving surface, wherein the first capacitor is contacted with the adhesive layer during transfer of the capacitor to the receiving surface of the substrate.

In certain embodiments, the transfer device comprises a conformable transfer device.

5 In certain embodiments, the transfer device comprises an elastomeric stamp.

In certain embodiments, contacting the first capacitor disposed on the transfer device with the receiving surface of the substrate is performed at a temperature of less than 400° C.

The disclosed technology, in certain embodiments, relates to providing phased arrays of antennas using driven with printable micro-scale active components. In certain
10 embodiments, the disclosed technology includes a phased array of individual radio frequency (RF) or microwave components, each element including a patch antenna, a printed (e.g., micro transfer printed) amplifier, and a printed phase- control device. In certain
embodiments, the printable devices have a width, length, or height (e.g., or two or three
dimensions) of from 2 to 5 μm , 5 to 10 μm , 10 to 20 μm , or 20 to 50 μm . Control elements
15 can have a wide range of sizes depending on the circuit complexity, integration technology, and design rules. For example, Ccontrol elements can have dimensions in the tens to
hundreds of microns and areas of 50 to 50,000 square microns, or even larger. The control
elements can be interlaced within the array of micro assembled micro-scale active radio
frequency components or within the array of antennas.

20 The disclosed technology, in certain embodiments, includes a method of preparing released or releasable heterogeneously integrated monolithic microwave integrated circuits. The method can include: forming a diverse set of two or more devices (e.g., the set
comprising two or more different kinds of devices) on respective native substrates (e.g., in
and/or with an epitaxial material deposited on the first native substrate by the addition and/or
25 patterning of dielectric and/or conductive thin- film materials; e.g., SiGe, GaN, GaAs, InP,

CMOS) (e.g., in an area-dense configuration on their native substrates, with each area-dense configuration supplying components for a much larger area device on a non-native destination substrate); delineating releasable structures on the native substrates, partially exposing the native substrates; contacting each of the native substrates (e.g., and the devices included thereon) with an etchant (e.g. heated tetramethyl ammonium hydroxide or potassium hydroxide, or sodium hydroxide or other basic solution for performing anisotropic silicon etch), thereby removing at least one of a portion of the substrate material and a sacrificial layer underneath the structures and forming released or releasable (e.g., connected to the substrate via tethers), micro assemble-able materials and/or devices (e.g., an array of devices); optionally, exposing each of the native substrates and the released or releasable structures (e.g., connected to the substrate by anchoring structures and/or tethering structures) to chemical agents for conditioning or processing the newly exposed surface of the released structures (e.g., to impart surface roughness by exposure to heated phosphoric acid); and transferring, by micro assembly, the diverse set of two or more devices to a non-native destination substrate (e.g., non-native to some or all of the components of the integrated circuit; e.g., and including one or more of aluminum oxide ceramic, aluminum nitride ceramic, silicon nitride ceramic, sapphire, glass, diamond, diamond-like carbon, silicon, beryllium oxide, glass-resin composite, or copper), thereby producing an array of high frequencydiverse integrated circuits from multiple source wafers on a different, non-native destination substrate that supports the diverse set. The integrated circuits can include integrated circuits that process or control high-frequency or radio-frequency signals.

The diverse set of two or more devices can include at least one of: a heterojunction bipolar transistors at least partially formed on gallium arsenide or indium phosphide substrates and transferred to the non-native destination substrate; high electron- mobility transistors based on GaAs, InP, or GaN related materials at least partially formed on their

native substrates and transferred to the native destination substrate; SiGe transistors at least partially formed on silicon-on-insulator substrates and transferred to their non-native destination substrates; and diodes, passive components, and signal-processing integrated circuits, at least partially formed on their native substrates, for example silicon or silicon-on-insulator wafers, and transferred to the non-native destination substrate.

The disclosed technology, in certain embodiments, includes a method of preparing released or releasable transistors. The method can include: forming transistors (e.g., RF transistors, heterojunction bipolar transistors and/or high-electron mobility transistors) on a release layer with selective etching characteristics that allow the release layer to be chemically removed chemically, at least partially separating the releasable device from a native substrate (e.g., GaAs or InP); forming anchoring structures and/or tethering structures (e.g., comprising photodefinable materials, photoresist materials, epoxies, polyimides, dielectrics, metals, and/or semiconductors; e.g., or made from photoresist material that also encapsulates the transistors from the chemistries used in the release process) on the native substrate, such that the released or releasable structures are connected to the native substrate by the anchoring structures and/or tethering structures following contact of the native substrate with the etchant, thereby maintaining the spatial configuration of the transistors through the release process; after formation of the anchoring, tethering, and/or encapsulation structures, removing the release layer by chemically etching, thereby at least partially releasing the transistors such that the transistors are ready for retrieval removal by a transfer element; contacting a transfer element (e.g., that is made at least in part of a conformable material, for example, PDMS rubber, such that the transfer element makes intimate contact with at least a portion of the topography of the releasable object) to the transistors and adhering the transfer element to at least the partially released transistors; after adhering to the at least partially released transistor, moving the transfer element moves away from the native

substrate while, maintaining adhesion to the released object, thereby retrieving, removing, separating, or picking the transistor from its native substrate, wherein the anchor or tether structures fracture and/or lose connection to the native substrate and/or the released object in the process of retrieving and/or moving the transfer element away from the native substrate;

5 and contracting the transistors to the non-native substrate and removing the transfer element, thereby placing the transistor on the non-native substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects, features, and advantages of the present disclosure will become more apparent and better understood by referring to the following description taken in conjunction with the accompanying drawings, in which:

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FIG. 1A is a schematic illustration of an individual element for use in a phased array that uses printed active components;

FIG. 1B is a schematic illustration of an example array of 16 printed elements of a phased array that uses printed active components;

15

FIG. 1C is a schematic illustration of an example array of 128 printed elements of a phased array that uses printed active components;

FIG. 2 is a cross section of a transfer-printable heterojunction bipolar transistor;

FIG. 3 is a cross section of a transfer-printable heterojunction bipolar transistor with anchors, tethers and encapsulation;

20

FIG. 4 is a cross section of release and removal of a transfer-printable heterojunction bipolar transistor;

FIG. 5 is a cross section of placement and printing of a transfer printable heterojunction bipolar transistor;

FIG. 6 is a schematic of transfer-printed heterogeneously integrated monolithic microwave integrated circuits;

FIG. 7 is a schematic of transfer-printed heterogeneously integrated monolithic microwave integrated circuits including native source substrates and a destination substrate;

5 FIG. 8 is a cross section of a capacitor stack, according to an embodiment of the present disclosure;

FIG. 9 is a perspective of a capacitor stack with two-dimensional offset, according to an embodiment of the present disclosure;

10 FIG. 10 is an optical micrograph of an example of offset-printed silicon membranes, according to an embodiment of the present disclosure;

FIG. 11 is an optical micrograph of an alternative example of off-set printed silicon membranes, according to an embodiment of the present disclosure;

FIG. 12 is a cross section of a wafer, according to an embodiment of the present disclosure;

15 FIG. 13 is a cross section of a patterned and etched wafer of devices that has been undercut, according to an embodiment of the present disclosure;

FIG. 14 is a perspective of an array of devices on a wafer, according to an embodiment of the present disclosure;

20 FIG. 15 is a perspective of a capacitor stack with exposed electrical contacts, according to an embodiment of the present disclosure; and

FIG. 16 is a cross-section of a plurality of stacked wafers, according to an embodiment of the present disclosure.

The features and advantages of the present disclosure will become more apparent
25 from the detailed description set forth below when taken in conjunction with the drawings, in

which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements.

5

DETAILED DESCRIPTION OF THE INVENTION

As used herein the expression “semiconductor element” and “semiconductor structure” are used synonymously and broadly refer to a semiconductor material, structure, device, or component of a device. Semiconductor elements include high-quality single crystalline and polycrystalline semiconductors, semiconductor materials fabricated via high-temperature processing, doped semiconductor materials, organic and inorganic
10 semiconductors, and composite semiconductor materials and structures having one or more additional semiconductor components and/or non-semiconductor components, such as dielectric layers or materials and/or conducting layers or materials. Semiconductor elements include semiconductor devices and device components including, but not limited to,
15 transistors, photovoltaics including solar cells, diodes, light-emitting diodes, lasers, p-n junctions, photodiodes, integrated circuits, and sensors. In addition, semiconductor element can refer to a part or portion that forms an functional semiconductor device or product.

“Semiconductor” refers to any material that is a material that is an insulator at a very low temperature, but which has an appreciable electrical conductivity at temperatures of
20 about 300 Kelvin. The electrical characteristics of a semiconductor can be modified by the addition of impurities or dopants and controlled by the use of electrical fields. In the present description, use of the term semiconductor is intended to be consistent with use of this term in the art of microelectronics and electronic devices. Semiconductors useful in the present invention can include elemental semiconductors, such as silicon, germanium and diamond,
25 and compound semiconductors, for example group IV compound semiconductors such as SiC

and SiGe, group III-V semiconductors such as AlSb, AlAs, Aln, AlP, BN, GaSb, GaAs, GaN, GaP, InSb, InAs, InN, and InP, group III-V ternary semiconductor alloys such as $\text{Al}_x\text{Ga}_{1-x}\text{As}$, group II-VI semiconductors such as CsSe, CdS, CdTe, ZnO, ZnSe, ZnS, and ZnTe, group I-VII semiconductors CuCl, group IV-VI semiconductors such as PbS, PbTe and SnS, layer semiconductors such as PbI_2 , MoS_2 and GaSe, oxide semiconductors such as CuO and Cu_2O . The term semiconductor includes intrinsic semiconductors and extrinsic semiconductors that are doped with one or more selected materials, including semiconductor having p-type doping materials and n-type doping materials, to provide beneficial electronic properties useful for a given application or device. The term semiconductor includes composite materials comprising a mixture of semiconductors and/or dopants. Specific semiconductor materials useful for in some applications of the present invention include, but are not limited to, Si, Ge, SiC, AlP, AlAs, AlSb, GaN, GaP, GaAs, GaSb, InP, InAs, GaSb, InP, InAs, InSb, ZnO, ZnSe, ZnTe, CdS, CdSe, ZnSe, ZnTe, CdS, CdSe, CdTe, HgS, PbS, PbSe, PbTe, AlGaAs, AlInAs, AlInP, GaAsP, GaInAs, GaInP, AlGaAsSb, AlGaInP, and GaInAsP. Porous silicon semiconductor materials are useful for applications of the present invention in the field of sensors and light-emitting materials, such as light-emitting diodes (LEDs) and solid-state lasers. Impurities of semiconductor materials are atoms, elements, ions or molecules other than the semiconductor material(s) themselves or any dopants provided in the semiconductor material. Impurities are undesirable materials present in semiconductor materials that can negatively impact the electronic properties of semiconductor materials, and include but are not limited to oxygen, carbon, and metals including heavy metals. Heavy-metal impurities include, but are not limited to, the group of elements between copper and lead on the periodic table, calcium, sodium, and all ions, compounds and/or complexes thereof.

“Substrate” refers to a structure or material on which, or in which, a process is (or has been) conducted, such as patterning, assembly or integration of semiconductor elements.

Substrates include, but are not limited to: (i) a structure upon which semiconductor elements are fabricated, deposited, transferred or supported (also referred to as a native substrate); (ii) a device substrate, for example an electronic device substrate; (iii) a donor substrate having elements, such as semiconductor elements, for subsequent transfer, assembly or integration; and (iv) a target substrate for receiving printable structures, such as semiconductor elements. A donor substrate can be, but is not necessarily, a native substrate.

“Destination substrate” as used herein refers to the target substrate (e.g., non-native substrate) for receiving printable structures, such as semiconductor elements. Examples of destination substrate materials include polymer, plastic, resin, polyimide, polyethylene naphthalate, polyethylene terephthalate, metal, metal foil, glass, flexible glass, a semiconductor, and sapphire.

The terms “micro” and “micro-device” as used herein refer to the descriptive size of certain devices or structures in accordance with embodiments of the invention. As used herein, the terms “micro” and “micro-device” are meant to refer to structures or devices on the scale of .5 to 250 μm (e.g., from .5 to 2 μm , 2 to 5 μm , 5 to 10 μm , 10 to 20 μm , 20 to 50 μm , 50 to 100 μm , or 100 to 250 μm). However, it is to be appreciated that embodiments of the present invention are not necessarily so limited, and that certain aspects of the embodiments can be applicable to larger or smaller size scales.

As used herein, “micro-LED” refers to an inorganic light-emitting diode on the scale of .5 to 250 μm . For example, micro-LEDs can have at least one of a width, length, and height (or two or all three dimensions). Micro-LEDs emit light when energized. The color of the light emitted by an LED varies depending upon the structure of the micro-LED. For example, when energized a red micro-LED emits red light, a green micro-LED emits green

light, a blue micro-LED emits blue light, a yellow micro-LED emits yellow light, and a cyan micro-LED emits cyan light.

“Printable” relates to materials, structures, device components, or integrated functional devices that are capable of transfer, assembly, patterning, organizing, or
5 integrating onto or into substrates without exposure of the substrate to high temperatures (i.e. at temperatures less than or equal to about 400, 200, or 150 degrees Celsius). In one embodiment of the present invention, printable materials, elements, device components, or devices are capable of transfer, assembly, patterning, organizing and/or integrating onto or into substrates via solution printing, micro-transfer printing, or dry transfer contact printing.

10 “Printable semiconductor elements” of the present invention comprise semiconductor structures that can be assembled or integrated onto substrate surfaces, for example by using dry transfer contact printing, micro-transfer printing, or solution printing methods. In one embodiment, printable semiconductor elements of the present invention are unitary single crystalline, polycrystalline or microcrystalline inorganic semiconductor structures. In the
15 context of this description, a unitary structure is a monolithic element having features that are mechanically connected. Semiconductor elements of the present invention can be undoped or doped, can have a selected spatial distribution of dopants and can be doped with a plurality of different dopant materials, including p- and n-type dopants. The present invention includes microstructured printable semiconductor elements having at least one cross-sectional
20 dimension greater than or equal to about 1 micron and nanostructured printable semiconductor elements having at least one cross-sectional dimension less than or equal to about 1 micron. Printable semiconductor elements useful in many applications comprise elements derived from “top down” processing of high-purity bulk materials, such as high-purity crystalline semiconductor wafers generated using conventional high-temperature
25 processing techniques. In one embodiment, printable semiconductor elements of the present

invention comprise composite structures having a semiconductor operationally connected to at least one additional device component or structure, such as a conducting layer, dielectric layer, electrode, additional semiconductor structure, or any combination of these. In one embodiment, printable semiconductor elements of the present invention comprise stretchable
5 semiconductor elements or heterogeneous semiconductor elements.

The term “flexible” refers to the ability of a material, structure, device or device component to be reversibly deformed into a curved shape, e.g., without undergoing a transformation that introduces significant strain, such as strain characterizing the failure point of a material, structure, device, or device component.

10 “Plastic” refers to any synthetic or naturally occurring material or combination of materials that can be molded or shaped, generally when heated, and hardened into a desired shape. Exemplary plastics useful in the devices and methods of the present invention include, but are not limited to, polymers, resins and cellulose derivatives. In the present description, the term plastic is intended to include composite plastic materials comprising one or more
15 plastics with one or more additives, such as structural enhancers, fillers, fibers, plasticizers, stabilizers or additives which can provide desired chemical or physical properties.

“Dielectric” and “dielectric material” are used synonymously in the present description and refer to a substance that is highly resistant to flow of electric current and can be polarized by an applied electric field. Useful dielectric materials include, but are not limited to, SiO₂,
20 Ta₂O₅, TiO₂, ZrO₂, Y₂O₃, SiN₄, STO, BST, PLZT, PMN, and PZT.

“Polymer” refers to a molecule comprising a plurality of repeating chemical groups, typically referred to as monomers. Polymers are often characterized by high molecular masses. Polymers useable in the present invention can be organic polymers or inorganic polymers and can be in amorphous, semi-amorphous, crystalline or partially crystalline states.
25 Polymers can comprise monomers having the same chemical composition or can comprise a

plurality of monomers having different chemical compositions, such as a copolymer. Cross-linked polymers having linked monomer chains are particularly useful for some applications of the present invention. Polymers useable in the methods, devices and device components of the present invention include, but are not limited to, plastics, elastomers, thermoplastic
5 elastomers, elastoplastics, thermostats, thermoplastics and acrylates. Exemplary polymers include, but are not limited to, acetal polymers, biodegradable polymers, cellulosic polymers, fluoropolymers, nylons, polyacrylonitrile polymers, polyamide-imide polymers, polyimides, polyarylates, polybenzimidazole, polybutylene, polycarbonate, polyesters, polyetherimide, polyethylene, polyethylene copolymers and modified polyethylenes, polyketones,
10 poly(methyl methacrylate, polymethylpentene, polyphenylene oxides and polyphenylene sulfides, polyphthalamide, polypropylene, polyurethanes, styrenic resins, sulphone based resins, vinyl-based resins or any combinations of these.

“Micro-transfer printing” as used herein refers to systems, methods, and techniques for the deterministic assembly of micro- and nano-materials, devices, and semiconductor
15 elements into spatially organized, functional arrangements with two-dimensional and three-dimensional layouts. It is often difficult to pick up and place ultra-thin or small devices, however, micro-transfer printing permits the selection and application of these ultra-thin, fragile, or small devices, such as micro-LEDs, without causing damage to the devices themselves. Microstructured stamps (e.g., elastomeric, electrostatic stamps, or hybrid
20 elastomeric/electrostatic stamps) can be used to pick up micro devices, transport the micro devices to a destination substrate, and print the micro devices onto the destination substrate. In some embodiments, surface adhesion forces are used to control the selection and printing of these devices onto the destination substrate. This process can be performed massively in parallel. The stamps can be designed to transfer a single device or hundreds to thousands of
25 discrete structures in a single pick-up-and-print operation. For a discussion of micro-transfer

printing generally, see U.S. Patent Nos. 7,622,367 and 8,506,867, each of which is hereby incorporated by reference in its entirety.

5 Phased-array antenna systems can be constructed using transfer printed active components. Phased-array antenna systems benefit from a large number of radiating elements (e.g., more radiating elements can form sharper, narrower beams and provide higher gain). As the number of radiating elements increases, the size of the system and the cost of assembly increases. High-throughput micro assembly (e.g. by micro transfer printing) mitigates costs associated with large part count.

10 Micro assembly is advantaged over monolithic approaches that form multiple radiating elements on a semiconductor wafer because micro assembly uses less semiconductor material to provide the active components that are necessary for the array. The density of active components on the phased-array antenna system is small (a few % or less). Micro assembly provides a way to efficiently use semiconductor material in a phased-array antenna system, reducing the amount of non-active semiconductor area (e.g., the area on the semiconductor material that does not include transistors, diodes, or other active components) in an original native source substrate. Micro-transfer methods are described in U.S. Patent Nos. 8,722,458, 7,622,367 and 8,506,867, each of which is hereby incorporated by reference.

20 In some embodiments, it is advantageous to place active components near each individual antenna in the phased array of antennas. In some embodiments, the cost of each active component is reduced by miniaturizing the active components, for example in an integrated circuit, permitting a greater number of components to be produced on a given semiconductor wafer.

25 The active components can be released from the native substrate, facilitating thin-film interconnection to the active component and reducing their cost by enabling substrate re-use.

Thin film interconnection to the active component is advantaged in RF applications by providing a reduced parasitic compared to other means of interconnection, including wire bonding and bump bonding.

Phased-array antenna system systems that use transfer-printed micro-assembled active components can be used to provide radar for self-driving cars, power transmission for wireless unmanned vehicles, power transmission for wireless cameras, heating for microwave ovens, power transmission for wireless lighting devices, data transmission, power transmission from handsets and personal computers to auxiliary mobile devices, or power and data transmission to modular information display elements, including bi-stable or multi-stable display elements such as electrophoretic displays. For example, control systems for driverless vehicles benefit from radar with high-gain beam forming capabilities. Micro-assembly provides an economical route to high-gain phased arrays useful in tactical aerospace precision. Advantages of transfer-printed phased arrays include, among other things, monolithic integration & efficient material utilization of best-in-class materials—SiGe, GaN, GaAs, InP, CMOS, etc., and low-inductance interconnection of amplifiers to antennas.

FIG. 1A is an illustration of an individual element 100 for use in a phased antenna array system that includes printed active components. An array of individual elements 100 can be micro assembled onto a substrate to form a phased-array antenna system. In some embodiments, the element 100 includes an antenna 102, such as a patch antenna. Patch antennas can be mounted on a flat surface and have a low profile. The antenna 102 is connected to an amplifier 104 that is micro assembled (e.g., micro transfer printed) onto the substrate. A phase-control device 106 is connected to the amplifier 104 such that the phase of the signal broadcast using the antenna 102 can be controlled. The phase-control device

106 can be integrated with the amplifier 104 in a common device, such as an integrated circuit, or separate, for example in separate integrated circuits.

In some embodiments, the individual elements are formed using compound micro assembly techniques. Compound micro assembly, for example, allows arrays of micro-
5 systems containing small devices (e.g., width, length, and height from 1 micron to 100 microns) to be formed on an intermediate substrate, for example by micro-transfer printing the individual elements from one or more native substrates on which the individual elements are formed to one or more intermediate substrates. The micro-systems on the intermediate substrates can then be micro-transfer printed to the destination substrate to form a macro-
10 system formed of several micro-systems each on its own separate intermediate substrate.

FIG. 1B is an illustration of an example array of 16 printed elements of a phased-array antenna 150 that uses printed active components. FIG. 1C is an illustration of an example array of 128 printed elements of a phased-array antenna system 175 that uses printed active components. The phased-array antenna can include an array of control elements 180
15 interlaced within arrays of micro-assembled radio-frequency components. The control elements can be used to send a signal to the antennas. The control elements can also be used to send a control signal to the phase-control devices 106 to control or adjust the phase of a signal sent through the antennas 102 enabling electronic beam steering.

FIGS. 2 through 5 illustrate releasable radio-frequency transistors that are suitable for
20 micro assembly, formed on compound semiconductor materials, such as those grown on a GaAs or InP substrate. In some embodiments, as illustrated in FIG. 2, transistors are formed on a release layer 204 with selective etching characteristics that allow the release layer 204 to be removed chemically, at least partially separating the releasable device 212 from its growth or native substrate 202. The releasable device 212 can include an emitter 210 formed on a
25 collector 208 that is itself, in certain embodiments, formed on a sub-collector 206 formed

over the release layer 204. The collector 208 can include layers of doped semiconductor material as can the sub-collector. The sub-collector can be doped to increase the conductivity of the semiconductor. The transistor can be a radio-frequency transistor such as a heterojunction bipolar transistor or high electron-mobility transistor.

5 FIG. 3 is an illustration of a transfer-printable heterojunction bipolar transistors with anchors, tethers and encapsulation. In the process of preparing releasable objects such as a radio-frequency transistor for micro assembly, structures that maintain the spatial configuration of the object through the release process can be used. Structures that maintain the spatial configuration, often referred to as anchors, tethers, or other stabilization structures,
10 can include photoresist materials, epoxies, polyimides, dielectrics, metals, and/or semiconductors. Such structures maintain contact to the native substrate 302 or other fixed body throughout the release process. FIG. 3 is an example illustration that shows the formation of such structures, e.g. made from photoresist that also encapsulate the active components of the device from the chemistries used in the release process, thereby providing
15 additional benefit. Photodefinable materials are advantageous for this kind of anchoring, tethering, or encapsulation structures, offering ease of formation, and in many cases ease of removal by dissolution in wet chemicals, organic solvents or aqueous mixtures, or by ashing in oxygen and/or fluorine compounds. In the example shown in FIG. 3, two tethers 320a and 320b (collectively 320) secure the device to substrate 302. Each tether 320a and 320b is
20 connected to an anchor, such as anchors 322a and 322b (collectively 322), respectively. The chemical selectivity of the tethers 320 and anchors 322 is such that it is not impacted (e.g., or minimally impacted) when the release layer 304 is removed (e.g., with an etch).

FIG. 4 is an illustration of release and removal of a transfer-printable heterojunction bipolar transistor from a native substrate 402. After formation of anchoring, tethering, or
25 encapsulation structures, the release layer (304 in FIG. 3) can be removed chemically.

Chemical reactants etch the release layer, gaining access through points of ingress (not shown) formed in the anchoring, tethering, and or encapsulation structures. Etch reaction products exit the space under the releasable object through points of egress (not shown) that are in many but not all cases the same as the points of ingress. When the release layer is fully or partially removed, the releasable object is said to be at least partially released and ready for retrieval by a transfer element 414. The spatial configuration is maintained by the tethers (e.g., 320 in FIG. 3) and the anchors (e.g., 322 in FIG. 3). The transfer element 414 contacts and adheres to the at least partially released object. It is advantageous for the transfer element 414 to be conformable to make intimate contact with at least a portion of the topography of the releasable object. For example, the transfer element 414 can include a conformable material, such as PDMS. After adhering to the at least partially released object, the transfer element 414 moves away from the native substrate 402, maintaining adhesion to the released object, thereby retrieving, removing, separating, or picking the object from its native substrate 402. In the process of removal, the anchor or tether structures fracture or lose connection to the native substrate 402 or the released object. Selection of materials with specific fracture properties, adhesion properties, or definition of geometries with stress-concentration features in the anchoring and tethering structures are beneficial for controlling the points of separation or fracture. In the example shown in FIG. 4, two tethers 420a and 420b (collectively 420) secure the device to substrate 402. Each tether 420a and 420b is connected to an anchor, such as anchors 422a and 422b (collectively 422), respectively. As shown in FIG. 4, when a transfer element 414 picks up the device, the tethers 420 are fractured.

FIG. 5 is an illustration of placement and printing of a transfer printable heterojunction bipolar transistor. The transfer element 514 (corresponding to element 414 of FIG. 4) places the radio-frequency device on a non-native substrate 516 by contacting the

device to the non-native substrate 516 and removing the transfer element 514. Kinetically switchable adhesion to the transfer element 514, compression against the non-native substrate 516, contact between flat surfaces of the device and the non-native substrate 516, addition of flat or conformable adhesion-promoting layers 518, exposure to electromagnetic radiation, mechanical shear, heat, plasma-activation, metallic bonds, or softening, flow, or ablation of a material at the interface between the released object and the transfer element 514 facilitate the separation of the released device from the transfer element 514 and transfer to the non-native substrate 516. Adhesion-promoting layers 518 might include planarization layers, for example BCB, polyimide, polybenzoxazole, flux, conformable dielectric or conductive materials, or spin-on glass materials. Adhesion-promoting layers 518 can also have mechanical properties that facilitate intimate contact to a surface of the released object, for example, silicones, epoxies, polyimides, polybenzoxazole, soft or liquid metals, flux, or BCB. Adhesion-promoting layers 518 might also be photo-active, for example, cross-linkable by exposure to light. In those embodiments, it is advantageous to expose some or all of the adhesion-promoting layers 518 to light during or after the transfer process to maintain the spatial location and orientation of the transferred device.

FIG. 6 is an illustration of transfer-printed heterogeneously integrated monolithic integrated circuits 602a-602g, such as microwave integrated circuits. Micro assembly of a diverse set of devices from multiple source wafers can produce high-frequency integrated circuits on a different substrate, non-native substrate 600 that supports the diverse set of integrated circuits 602a-602g. The non-native substrate 600 is non-native to some or all of the components of the integrated circuits 602a-602g. For example, the non-native substrate 600 can be aluminum oxide ceramic, aluminum nitride ceramic, silicon nitride ceramic, sapphire, glass, diamond, diamond-like carbon, silicon, beryllium oxide, glass-resin composite, polymer, plastic, polymer, metal, or copper. The non-native substrate 600 can be

selected for thermal properties, cost, radio-frequency response characteristics, size, mechanical properties, or other desirable attributes. In some embodiments, the non-native substrate 600 is flexible. As an example, the integrated circuits 602a-602g might include a heterojunction bipolar transistor at least partially formed on gallium arsenide or indium phosphide substrates and transferred to the non-native substrate 600, high electron-mobility transistors based on GaAs, InP, or GaN related materials at least partially formed on their native substrates (e.g., 402 in FIG. 4) and transferred to the non-native destination substrate, SiGe transistors at least partially formed on silicon-on-insulator substrates and transferred to their non-native destination substrates, or diodes, passive components, and signal processing integrated circuits at least partially formed on their native substrates, for example silicon or silicon-on-insulator wafers, and transferred to the non-native destination substrate .

This configuration of a diverse set of devices 602a-602g on a single non-native substrate 600 offers materials reduction cost and performance advantages because many of these kinds of integrated circuits require only a small fraction of their area to be populated with active components. The process of forming the active components can be costly on a per-area basis, and the micro-assembled set described herein can facilitate the formation of the active components in an area-dense configuration on their native source substrates, with each area-dense configuration supplying components for a much larger area device on a non-native destination substrate. Micro assembly provides benefit because many of the components of these integrated circuits are miniaturize-able to sizes that are difficult to assemble by conventional assembly techniques, for example, less than 0.1 mm in one lateral dimension, or less than 0.05 mm or 0.02 mm in at least one lateral dimension. The micro-assembled devices can be interconnected using thin-film interconnections, thereby providing interconnections with reduced parasitic effects.

FIG. 7 is an illustration of transfer-printed heterogeneously integrated monolithic microwave integrated circuits. FIG. 7 illustrates a diverse set of components formed in an area-dense configuration on multiple native substrates suitable for micro assembling multiple integrated circuits on non-native destination substrates.

5 Radars and other electronic systems often utilize capacitors to supply and store energy. For example, capacitors, (e.g., capacitors with high power density) are used to meet the high current-pulse requirements of pulse radar and laser applications and are also useful for phased-array antenna systems. The disclosed technology can provide capacitors and capacitor stacks that can be incorporated into micro-scale systems, such as radar systems and
10 other electronic systems, using micro-assembly technology.

FIG. 8 is a drawing of a capacitor stack 804 on a substrate 806, according to an embodiment of the present disclosure. Assembling thin capacitors in an offset stack leaves surface area exposed such that the capacitors can be connected to a circuit. Capacitor stack 804 includes the capacitors 804a, 804b, 804c, 804d. Each of the capacitors 804a-804d is a
15 thin metal-insulator-metal structure. Each of capacitors 804a-804d are micro transfer printed to their respective destinations. In the example shown in FIG. 8, capacitor 804c is stacked atop capacitor 804d at an offset, which leaves an area exposed on the surface of capacitor 804d. The exposed surface area of 804d includes an electrical contact that is joined with interconnection 802d. The remaining capacitors 804a and 804b are similarly stacked with an
20 offset, enabling interconnections 802a, 802b, and 802c to be joined with the electrical contacts on the exposed surface areas of the capacitors 804a, 804b, and 804c, respectively. Each of capacitors 804 is connected to the silicon substrate 806 using interconnections 802a, 802b, 802c, and 802d (collectively, interconnections 802) in order to assemble a circuit. The capacitors can be interconnected in a parallel or series circuit. Thus, capacitors with a variety
25 of capacitances can be provided using the appropriate number of capacitors in a stack, the

appropriate physical size of each capacitor in a stack, and the appropriate wiring scheme. For example, when each of capacitors 804 has a capacitance of 250 nF/mm^2 and the capacitor 804a are interconnected in a parallel circuit, the capacitance of the complete stacked capacitor is $1 \mu\text{F/mm}^2$.

5 In certain embodiments, the offset can be along one dimension as shown in FIG. 8. For example, when the thin capacitors are stacked atop each other so that the width and length of each capacitor are parallel, the capacitors are offset along the length of the capacitor only, or offset along the width of the capacitor only. In some embodiments, the offset can be along two dimensions, for example along both the width dimension and the length dimension,
10 for example as shown in FIG. 9. FIG. 9 is an illustration of a capacitor stack with offset printing, according to an embodiment of the present disclosure. The capacitor stack 900 show the capacitors 804 stacked using micro transfer printing in an offset arrangement. The capacitors 804 are stacked vertically and offset along the two remaining axes. For example, when the thin capacitors are stacked atop each other so that the width and length of each
15 capacitor are parallel, the capacitors are offset along the length of the capacitor and offset along the width of the capacitor. In either of the embodiments of FIG.8 or FIG. 9, the offset exposes a portion of the top surface of each capacitor (e.g., not covered by a capacitor stacked thereon) and the exposed portions can be used for contact terminals and wiring.

 In some embodiments, each capacitor of the plurality of capacitors has a capacitance
20 per unit area from 100 nF/mm^2 and 400 nF/mm^2 . In other embodiments, each capacitor of the plurality of capacitors has a thickness of from $1 \mu\text{m}$ to $10 \mu\text{m}$, $10 \mu\text{m}$ to $30 \mu\text{m}$, $30 \mu\text{m}$ to $50 \mu\text{m}$, or $50 \mu\text{m}$ to $100 \mu\text{m}$. In further embodiments, each capacitor of the plurality of capacitors has a width of from $10 \mu\text{m}$ to $50 \mu\text{m}$, $50 \mu\text{m}$ to $100 \mu\text{m}$, or $100 \mu\text{m}$ to $200 \mu\text{m}$. In some embodiments, each capacitor of the plurality of capacitors has a length of from $10 \mu\text{m}$
25 to $50 \mu\text{m}$, $50 \mu\text{m}$ to $100 \mu\text{m}$, or $100 \mu\text{m}$ to $200 \mu\text{m}$.

FIG. 10 is an optical micrograph of an example of offset printing of silicon membranes, in this case an optical micrograph of a capacitor stack 1000 according to an embodiment of the present disclosure. In this embodiment, not only are the capacitors in each layer of the stack exposed in both the length and width dimensions, but the capacitors are each rotated by a different amount about a vertical axis perpendicular to the length and width directions of the capacitors.

FIG. 11 is an optical micrograph of an alternative example of offset printing of silicon membranes. Membrane stack 1100 is another capacitor stack arrangement according to an embodiment of the present disclosure. These arrangements can be used to form capacitors with varying capacitance using micro transfer printed capacitor stacks.

FIGS. 12 and 13 illustrate the process of forming capacitors using a source substrate 1210. The process starts with a substrate 1210, such as a silicon (111) substrate. A bottom electrode 1206 is deposited and patterned onto the silicon wafer substrate 1210. In some embodiments, the substrate is gallium arsenide, gallium nitride, silicon, germanium, or a dielectric material. After the bottom electrode 1206 is deposited and patterned, a dielectric 1204 (e.g., polyethylene, BCB, Polycarbonate, Mylar, SiO₂, Polyimide, Epoxies, FR4, SiO, Si₃N₄, AlN, Al₂O₃, Si₃N₄, BaTiO₃, NbO_x, Ta₂O₅, SiC, HfO, WO₂, Ta₂O₅, TiO₂, BaTiO₃, BaSrTiO₃, PbZr_xTi_{1-x}O₃, Ba_{0.8}Pb_{0.2}(Zr_{0.12}Ti_{0.88})O₃) is deposited, annealed, and patterned. After the dielectric 1204 has been deposited, annealed, and patterned, a top electrode 1202 is deposited and patterned to form a capacitor structure 1208. In some embodiments, the capacitor structure 1208 is a capacitor that has not been partially released (e.g., by etching a sacrificial layer). In other embodiments, the capacitor structure 1208 is delineated into a plurality of capacitors using, for example, a pattern-and-etch process.

After the appropriate materials to form the capacitor 1208 have been deposited and prepared as shown in FIG. 12, in some embodiments, a plurality of capacitors are delineated

on the substrate 1210. This delineation can be accomplished using a pattern and etching the material. In some embodiments, the materials are deposited such that the delineation step is not necessary. As shown in FIG. 13, the substrate 1210 is etched to undercut a capacitor structure 1308 (e.g., by etching, such as a KOH etching) to at least partially separate a thin silicon membrane 1304 from the substrate 1210, leaving the thin-film capacitor 1302 attached only to the thin silicon membrane 1304. The printable capacitor structure 1308 includes the thin-film capacitor 1302 attached to the thin silicon membrane 1304 and remains partially attached to the substrate 1210 by a tether (not shown) to hold the unit in place. The tether is subsequently broken during the micro transfer printing process such that the capacitor structure 1308 can be transferred to a destination substrate.

FIG. 14 is an illustration of an array of printable capacitors 1302 secured to a substrate 1210 by tethers 1404a (see e.g., capacitor 1302 is secured by tethers 1404a and 1404b (collectively tethers 1404). Individual capacitors can be transferred by the transfer device (e.g., an elastomer stamp) to a destination substrate. In certain embodiments, the destination substrate (e.g., substrate 1210) is non-native to the capacitors. In certain embodiments, the capacitors are stacked to create an offset stacked capacitor as shown in FIGS. 8 and 9 above. The microtransfer printing device attaches to the microtransfer printable capacitor 1402, thus breaking the tether 1404a and leaving an empty space in the array of capacitors on the silicon substrate 1210. In subsequent microtransfer printing steps, the microtransfer printing device is configured to remove a second capacitor from a different location of the array. Each of the plurality of printable capacitors comprises a top surface coated with a bonding layer that facilitates bonding of the printable capacitor to a contact surface of a microtransfer printing device (e.g., conformable transfer device, elastomer stamp). In certain embodiments, the density of capacitors is 5 to 15 capacitors per square millimeter.

The array 1400 is used by the microtransfer printing process to transfer the capacitors to a receiving surface of a substrate (e.g., glass, plastic, or sapphire). The microtransfer printing device contacts the first capacitor with a transfer device (e.g., a conformable transfer device) having a contact surface, thereby temporarily binding the capacitor to the contact surface such that the contact surface has the capacitor temporarily disposed thereon. The transfer device travels to the non-native destination substrate, and by separating the contact surface of the conformable transfer device and the capacitor, assembles the capacitor on the receiving surface of the non-native destination substrate. In some embodiments, the receiving surface comprises an adhesive layer that is contacted by the capacitor. In certain embodiments, the contacting is performed at a temperature of less than 400° C. Next, the transfer device contacts a second capacitor of the array 1400, binds the capacitor, then travels to the non-native destination substrate and separates the contact surface of the transfer device and the capacitor, assembling the second capacitor atop the surface of the first capacitor at an offset. The two capacitors are then electrically connected by thin-film wafer-level interconnections, in either parallel or series. In certain embodiments, a plurality of capacitors are stacked. In some embodiments, the capacitor comprises a top surface coated with a release layer that facilitates bonding of the capacitor to the contact surface of the conformable transfer device (such as a photoresist). The capacitors are assembled with placement accuracy greater than or equal to 25 microns.

FIG. 15 is a drawing of a capacitor stack with exposed electric contacts, according to an embodiment of the present disclosure. The individual offset stacked capacitors 804a, 804b, 804c, and 804d include first electrical contacts 1502a, 1502b, 1502c, and 1502d, respectively. The individual offset stacked capacitors 804a, 804b, 804c, and 804d also include second electrical contacts 1504a, 1504b, 1504c, and 1504d, respectively. As the

offset stack is assembled, the micro transfer printing process is configured to leave the electrical contacts exposed for the purpose of interconnecting the stacked capacitors 804.

FIG. 16 is a cross-sectional view of a stacked wafer, according to an embodiment of the present disclosure. A stacked wafer is a wafer multi-layer stack of capacitors on a wafer.

5 A plurality of capacitor structures 1208a-1208c (collectively 1208) are formed on one another. A first capacitor structure 1208c is formed on a first substrate 1210c, a second capacitor structure 1208b is formed on a second substrate 1210b, and a third capacitor structure 1208a is formed on a third substrate 1210a. In some embodiments, additional capacitor structures and substrates are formed thereon as desired. In some implementations,
10 each capacitor structure is separated from the substrate above by a buffer layer, such as buffer layers 1606a 1606b, and 1606c (collectively 1606). In some implementations, the buffer layers 1606 are sacrificial layers. In some embodiments, as explained above, a capacitor structure is delineated to form several capacitors. Thereafter, the capacitors are micro assembled as desired. Once each capacitor is formed the top capacitor structure 1208a is
15 removed, and then any remaining substrate 1210a material and the buffer layer 1606a are removed. The process of forming, printing, and removing substrates and buffer layers can continue for as many structures as are present.

Radar systems and other electronic devices also benefit from low-cost interposer technologies. The interposer serves as an intermediating layer between advanced chips and
20 the underlying printed circuit board. In some embodiments, functionalities are integrated into the interposers. For example, power distribution can be integrated into the interposer such that power is efficiently and smartly distributed about the system. In another example, capacitors, resistors, inductors, and diodes can be integrated into the interposers. The interposer itself can be formed of many materials, such as glass, plastic, and sapphire.
25 Materials such as glass are beneficial because of the cost and potential for panel-level

processing. However, it is difficult to integrate active components into glass interposers, compared to silicon. The disclosed technology, in some embodiments, utilizes micro assembly techniques (e.g., micro transfer printing) with both glass and silicon interposers to generate “active” interposers. For example, micro transfer printing can be used to integrate
5 small diodes or transistors onto the glass or silicon interposers. The micro-scale nature of the printed elements allows for the elements to be interconnected using the standard metallization processes (integration without any additional process steps).

Having described various embodiments of the disclosed technology, it will now
10 become apparent to one of skill in the art that other embodiments incorporating the concepts can be used. It is felt, therefore, that these embodiments should not be limited to the disclosed embodiments, but rather should be limited only by the spirit and scope of the following claims.

Throughout the description, where apparatus and systems are described as having,
15 including, or comprising specific components, or where processes and methods are described as having, including, or comprising specific steps, it is contemplated that, additionally, there are apparatus, and systems of the disclosed technology that consist essentially of, or consist of, the recited components, and that there are processes and methods according to the disclosed technology that consist essentially of, or consist of, the recited processing steps.

20 It should be understood that the order of steps or order for performing certain action is immaterial so long as the disclosed technology remains operable. Moreover, two or more steps or actions can be conducted simultaneously.

What is claimed:

1. A method of forming a phased-array antenna structure using printed micro assembled active components, the method comprising:

5 providing a plurality of antennas on a destination substrate;

forming a plurality of amplifiers on a first substrate;

forming a plurality of phase-control devices on a second substrate;

10 contacting the first substrate with an etchant, thereby removing at least one of a portion of a first sacrificial layer underneath the plurality of amplifiers and forming a plurality of printable amplifiers, each printable amplifier connected to the first substrate by one or more tethers;

15 contacting the second substrate with an etchant, thereby removing at least one of a portion of a second sacrificial layer underneath the plurality of phase-control devices and forming a plurality of printable phase-control devices, each printable phase-control device connected to the second substrate by one or more tethers;

20 exposing at least a portion of the plurality of printable amplifiers and plurality of printable phase-control devices to chemical agents for conditioning or processing the newly exposed surfaces of the plurality of printable amplifiers and plurality of printable phase-control devices; and

25 transferring, by micro assembly, at least a portion of the plurality of printable amplifiers and plurality of printable phase-control devices to the destination substrate and electrically interconnecting the antennas, the amplifiers, and the phase-control devices, to

thereby form a phased-array antenna system using an array of high-frequency micro-scale devices from multiple source wafers.

25

2. The method of claim 1, wherein transferring at least a portion of the plurality of printable amplifiers and plurality of printable phase-control devices to a destination substrate comprises:

contacting the portion of the plurality of printable amplifiers with a transfer device,

5 wherein contact between the transfer device and the portion of the plurality of printable amplifiers temporarily binds the portion of the plurality of printable amplifiers to the transfer device;

contacting the portion of the plurality of printable amplifiers disposed on the transfer device with the receiving surface of the destination substrate;

10 separating the transfer device from the portion of the plurality of printable amplifiers, thereby transferring the portion of the plurality of printable amplifiers onto the destination substrate;

contacting the portion of the plurality of printable phase-control devices with a transfer device, wherein contact between the transfer device and the portion of the plurality of
15 printable phase-control devices temporarily binds the portion of the plurality of printable phase-control devices to the transfer device;

contacting the portion of the plurality of printable phase-control devices disposed on the transfer device with the receiving surface of the destination substrate; and

20 separating the transfer device from the portion of the plurality of printable phase-control devices, thereby transferring the portion of the plurality of printable phase-control devices onto the destination substrate.

3. The method of claims 1 or 2, wherein the plurality of antennas comprise a plurality of patch antennas.

25

4. The method of any one of claims 1 to 3, comprising:
forming anchoring structures and tethering structures in each of the native substrates,
such that the released or releasable structures are connected to their respective native
substrates by the anchoring structures or tethering structures following contact of each of the
5 native substrates with the etchant.
5. The method of any one of claims 1 to 4, comprising;
forming anchoring or tethering structures from non-epitaxial materials such that the
released or releasable structures are connected to their respective native substrate by the
10 anchoring structures or tethering structures following contact of the substrate with the
etchant.
6. The method of any one of claims 1 to 5, comprising:
forming one or more encapsulating structures to encapsulate at least a portion of the
15 released or releasable structure.
7. The method of any one of claims 1 to 6, wherein the first sacrificial layer comprises a
portion of the first substrate.
- 20 8. The method of any one of claims 1 to 7, wherein the second sacrificial layer
comprises a portion of the second substrate.
9. The method of any one of claims 1 to 8, wherein the chemical etch gains access to the
sacrificial layer through points of ingress formed in the one or more tethers.

25

10. The method of claim 9, wherein the chemical etch exits the space formerly occupied by at least a portion of the sacrificial layer through points of egress in the one or more tethers.
11. The method of claim 10, wherein the points of egress are the same as the points of
5 ingress.
12. The method of any one of claims 1 to 11, wherein the destination substrate is a member selected from the group consisting of polymer, plastic, resin, polyimide, PEN, PET, metal, metal foil, glass, a semiconductor, and sapphire.
- 10
13. The method of any one of claims 1 to 12, wherein the destination substrate has a transparency greater than or equal to 50%, 80%, 90%, or 95% for visible light.
14. A device comprising:
15 a destination substrate; and
a multilayer structure on the destination substrate, wherein the multilayer structure comprises a plurality of printed capacitors stacked on top of each other with an offset between each capacitor along at least one edge of the capacitors.
- 20 15. The device of claim 14, wherein the offset is in one dimension.
16. The device of claim 14 or 15, wherein the offset is in two dimensions.
17. The device of any one of claims 14 to 16, wherein the offset is such that a portion of a
25 top surface of each capacitor is exposed.

18. The device of any one of claims 14 to 17, wherein each capacitor of the plurality of capacitors has a capacitance between 100 nF/mm^2 and 400 nF/mm^2 .
- 5 19. The method of any one of claims 14 to 18, wherein each capacitor of the plurality of capacitors has a thickness of from $1 \text{ }\mu\text{m}$ to $10 \text{ }\mu\text{m}$, $10 \text{ }\mu\text{m}$ to $30 \text{ }\mu\text{m}$, $30 \text{ }\mu\text{m}$ to $50 \text{ }\mu\text{m}$, or $50 \text{ }\mu\text{m}$ to $100 \text{ }\mu\text{m}$.
20. The method of any one of claims 14 to 19, wherein each capacitor of the plurality of
10 capacitors has a width of from $10 \text{ }\mu\text{m}$ to $50 \text{ }\mu\text{m}$, $50 \text{ }\mu\text{m}$ to $100 \text{ }\mu\text{m}$, or $100 \text{ }\mu\text{m}$ to $200 \text{ }\mu\text{m}$.
21. The method of any one of claims 14 to 20, wherein each capacitor of the plurality of capacitors has a length of from $10 \text{ }\mu\text{m}$ to $50 \text{ }\mu\text{m}$, $50 \text{ }\mu\text{m}$ to $100 \text{ }\mu\text{m}$, or $100 \text{ }\mu\text{m}$ to $200 \text{ }\mu\text{m}$.
- 15 22. The device of any one of claims 14 to 21, wherein the plurality of capacitors are a same shape and size.
23. The device of any one of claims 14 to 22, wherein the plurality of printed capacitors are connected in at least one of parallel or series.
- 20 24. The device of any one of claims 14 to 23, wherein the destination substrate is a member selected from the group consisting of polymer, plastic, resin, polyimide, PEN, PET, metal, metal foil, glass, a semiconductor, and sapphire.

25. The device of any one of claims 14 to 24, wherein the destination substrate has a transparency greater than or equal to 50%, 80%, 90%, or 95% for visible light.
26. A wafer of printable capacitors, the wafer comprising:
- 5 a source substrate;
- a first sacrificial layer on a process side of the source substrate;
- a first set of printable capacitors on the first sacrificial layer;
- a second sacrificial layer on the first set of printable capacitors; and
- a second set of printable capacitors on the second sacrificial layer.
- 10
27. The wafer of claim 26, wherein each printable capacitor of the second set of printable capacitors is disposed above a printable capacitor of the first set of printable capacitors.
28. The wafer of claim 26 or 27, wherein each of the first and second sets of printable
- 15 capacitors forms an array of capacitors.
29. The wafer of any one of claims 26 to 28, wherein the density of each of the first and second sets of printable capacitors is 5 to 15 capacitors per square millimeter.
- 20 30. The method of any one of claims 26 to 29, wherein each capacitor of the plurality of capacitors has a thin metal-insulator-metal structure with a thickness of from 1 μm to 10 μm , 10 μm to 30 μm , 30 μm to 50 μm , or 50 μm to 100 μm .
31. The method of any one of claims 26 to 30, wherein each capacitor of the plurality of
- 25 capacitors has a width of from 10 μm to 50 μm , 50 μm to 100 μm , or 100 μm to 200 μm .

32. The method of any one of claims 26 to 31, wherein each capacitor of the plurality of capacitors has a length of from 10 μm to 50 μm , 50 μm to 100 μm , or 100 μm to 200 μm .
- 5 33. The wafer of any one of claims 26 to 32, wherein each of the first and second sacrificial layers comprises at least one member selected from the group consisting of SiN, SiO₂, and Si.
34. The wafer of any one of claims 26 to 33, wherein the substrate is a member selected
10 from the group consisting of: glass, sapphire, Al₂O_x, gallium arsenide, gallium nitride, silicon, and germanium, silicon carbide, plastic, silicon wafer, silicon on insulator wafer, polycrystalline silicon wafer, GaAs wafer, silicon on substrate wafer, germanium wafer, thin films of polycrystalline silicon wafer, and silicon wafer.
- 15 35. The wafer of any one of claims 26 to 34, wherein each capacitor of the plurality of printable capacitors has a capacitance from 100 nF/mm² to 400 nF/mm².
36. The wafer of any one of claims 26 to 35, wherein each of the plurality of printable capacitors have a same shape and size.
- 20 37. A method for assembling a plurality of capacitors on a receiving surface of a substrate, the method comprising:
- contacting a first capacitor of the plurality of capacitors with a transfer device having a contact surface, thereby temporarily binding the capacitor to the contact surface such that
25 the contact surface has the capacitor temporarily disposed thereon;

contacting the first capacitor disposed on the contact surface of the transfer device
with the receiving surface of the substrate;

separating the contact surface of the transfer device and the capacitor, wherein the
capacitor is transferred onto the receiving surface, thereby assembling the capacitor on the
5 receiving surface of the substrate;

contacting a second capacitor of the plurality of capacitors with the transfer device,
thereby binding the second capacitor to the contact surface such that the contact surface has
the second capacitor disposed thereon;

contacting the second capacitor disposed on the contact surface of the transfer device
10 with a surface of the first capacitor assembled on the receiving surface of the substrate; and

separating the contact surface of the transfer device and the second capacitor, wherein
the second capacitor is transferred onto the capacitor assembled on the receiving surface of
the substrate, thereby assembling the second capacitor on the capacitor assembled on the
receiving surface of the substrate.

15

38. The method of claim 37, wherein the second capacitor is offset from the first
capacitor.

39. The method of claim 37 or 38, wherein the offset is in one dimension.

20

40. The method of any one of claims 37 to 39, wherein the offset is in two dimensions.

41. The method of any one of claims 37 to 40, wherein the offset is such that a portion of
the top surface of each capacitor is exposed.

25

42. The method of any one of claims 37 to 41, wherein each capacitor of the plurality of capacitors has a capacitance from 100 nF/mm² to 400 nF/mm².

43. The method of any one of claims 37 to 42, wherein the plurality of capacitors are a
5 same shape and size.

44. The method of any one of claims 37 to 43, wherein each capacitor of the plurality of capacitors has a thin metal-insulator-metal structure with a thickness of from 1 μm to 10 μm, 10 μm to 30 μm, 30 μm to 50 μm, or 50 μm to 100 μm.

10

45. The method of any one of claims 37 to 44, wherein each capacitor of the plurality of capacitors has a width of from 10 μm to 50 μm, 50 μm to 100 μm, or 100 μm to 200 μm.

46. The method of any one of claims 37 to 45, wherein each capacitor of the plurality of
15 capacitors has a length of from 10 μm to 50 μm, 50 μm to 100 μm, or 100 μm to 200 μm.

47. The method of any one of claims 37 to 46, wherein the first capacitor and the second capacitor are electrically connected via thin-film wafer-level interconnections.

20 48. The method of any one of claims 37 to 47, wherein the first capacitor and the second capacitor are connected in parallel.

49. The method of any one of claims 37 to 48, wherein the first capacitor and the second capacitor are connected in series.

25

50. The method of any one of claims 37 to 49, wherein the first capacitor is electrically connected via thin-film wafer-level interconnections.
51. The method of any one of claims 37 to 50, wherein the first capacitor disposed on the transfer device is contacted with a region of the receiving surface with a placement accuracy greater than or equal to 25 microns.
52. The method of any one of claims 37 to 51, wherein an adhesive layer is provided on the receiving surface, wherein the first capacitor is contacted with the adhesive layer during transfer of the capacitor to the receiving surface of the substrate.
53. The method of any one of claims 37 to 52, wherein the transfer device comprises a conformable transfer device.
54. The method of any one of claims 37 to 53, wherein the transfer device comprises an elastomeric stamp.
55. The method of any one of claims 37 to 54, wherein contacting the first capacitor disposed on the transfer device with the receiving surface of the substrate is performed at a temperature of less than 400° C.

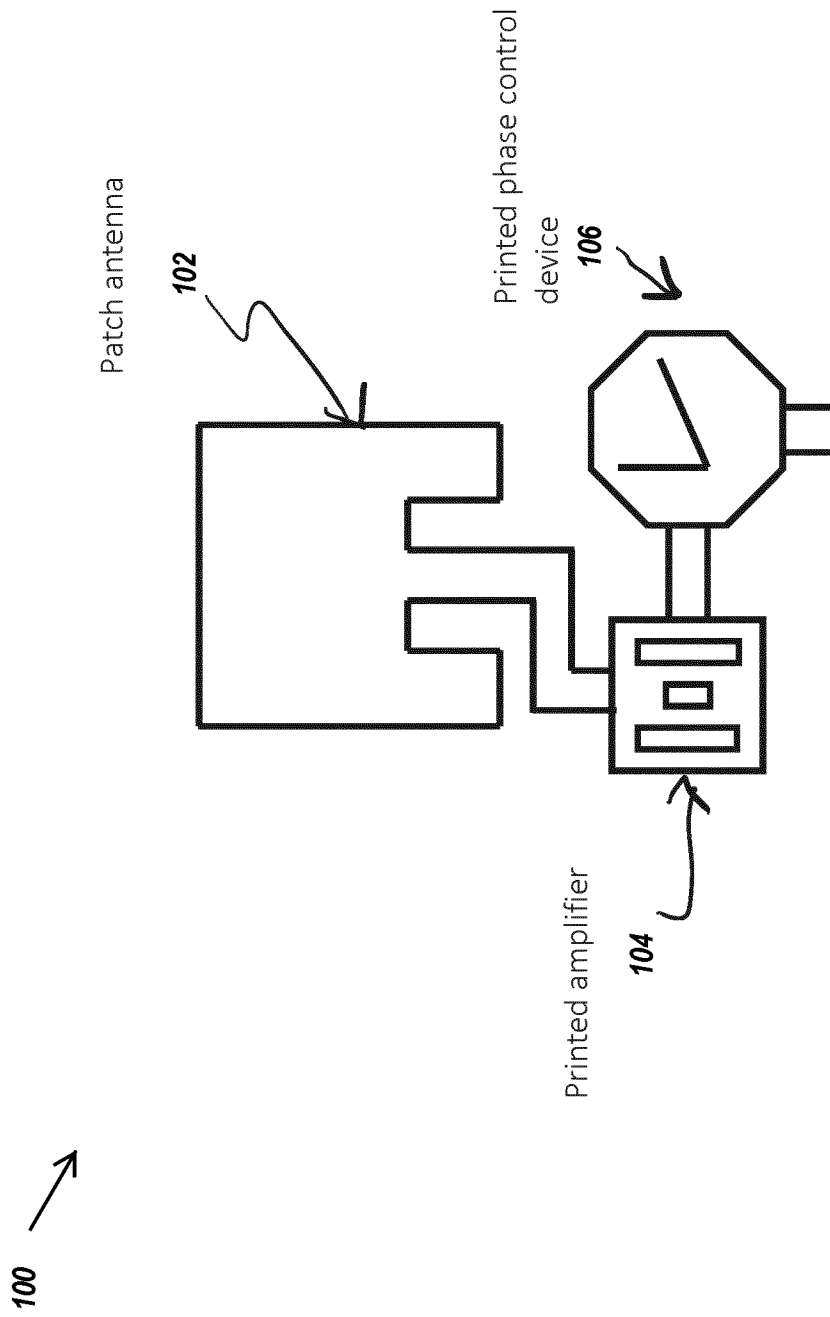


FIG. 1A

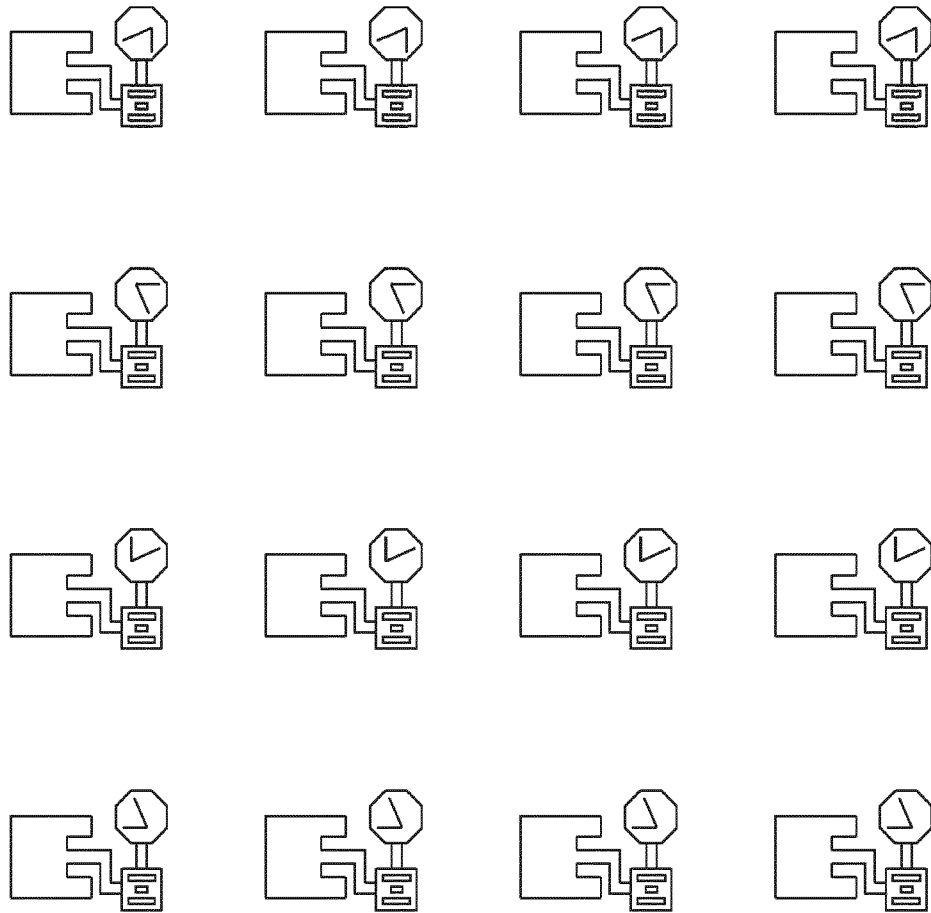

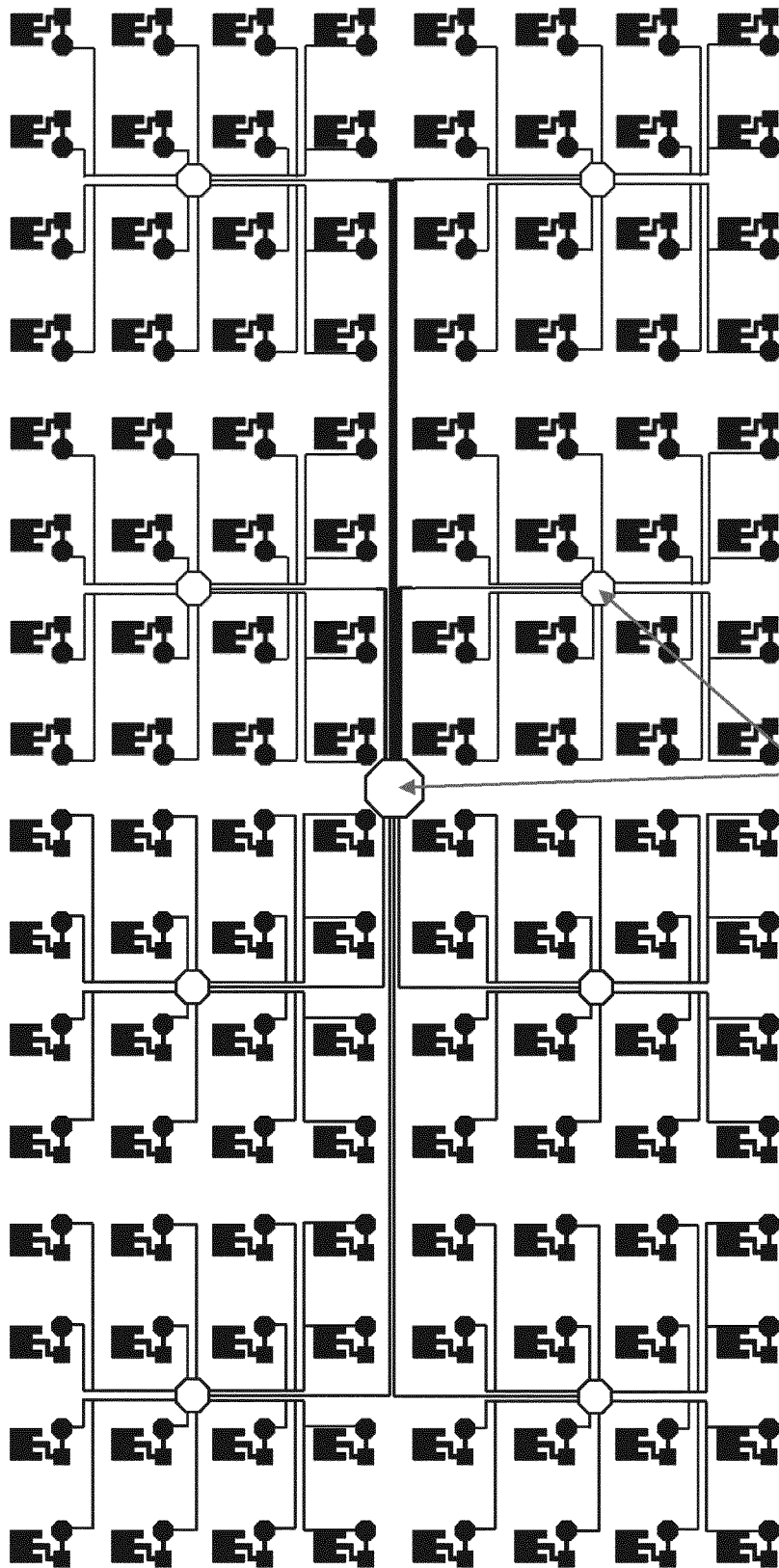


FIG. 1B

150 

175 ↗



180
Arrays of control elements interlaced within arrays of
micro assembled radio frequency components

FIG. 1C

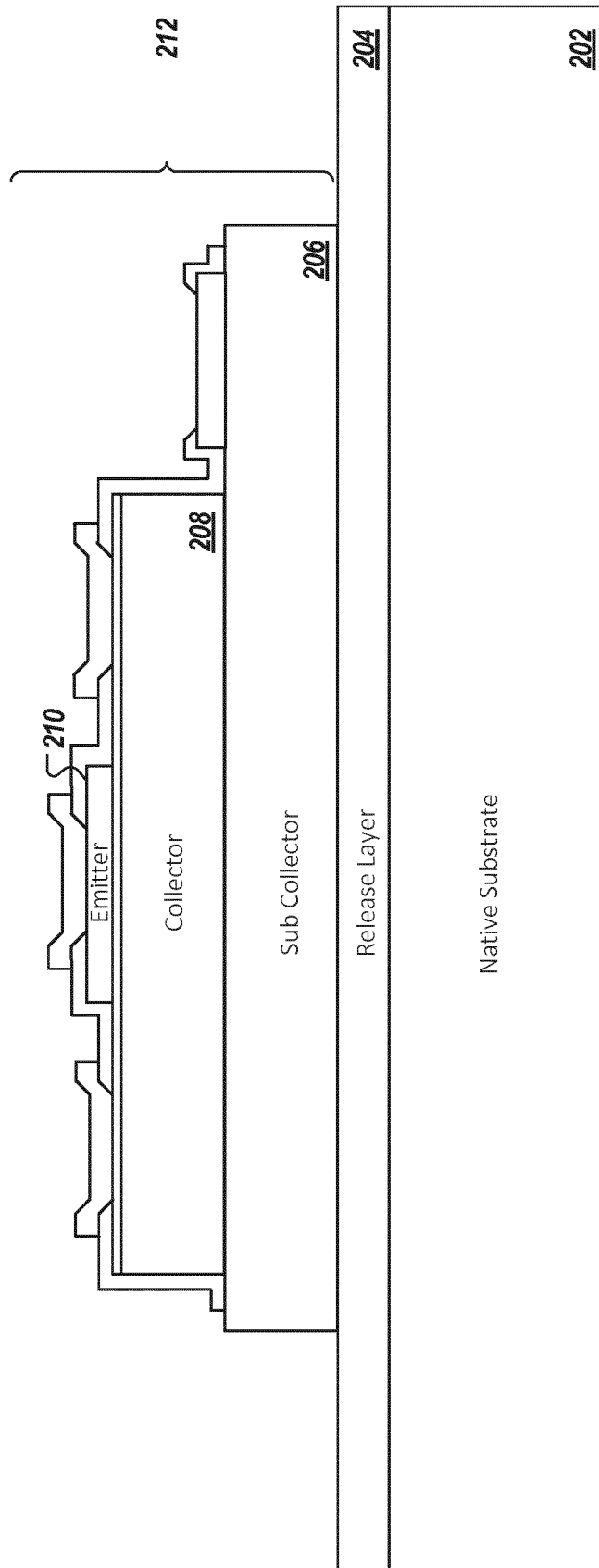


FIG. 2

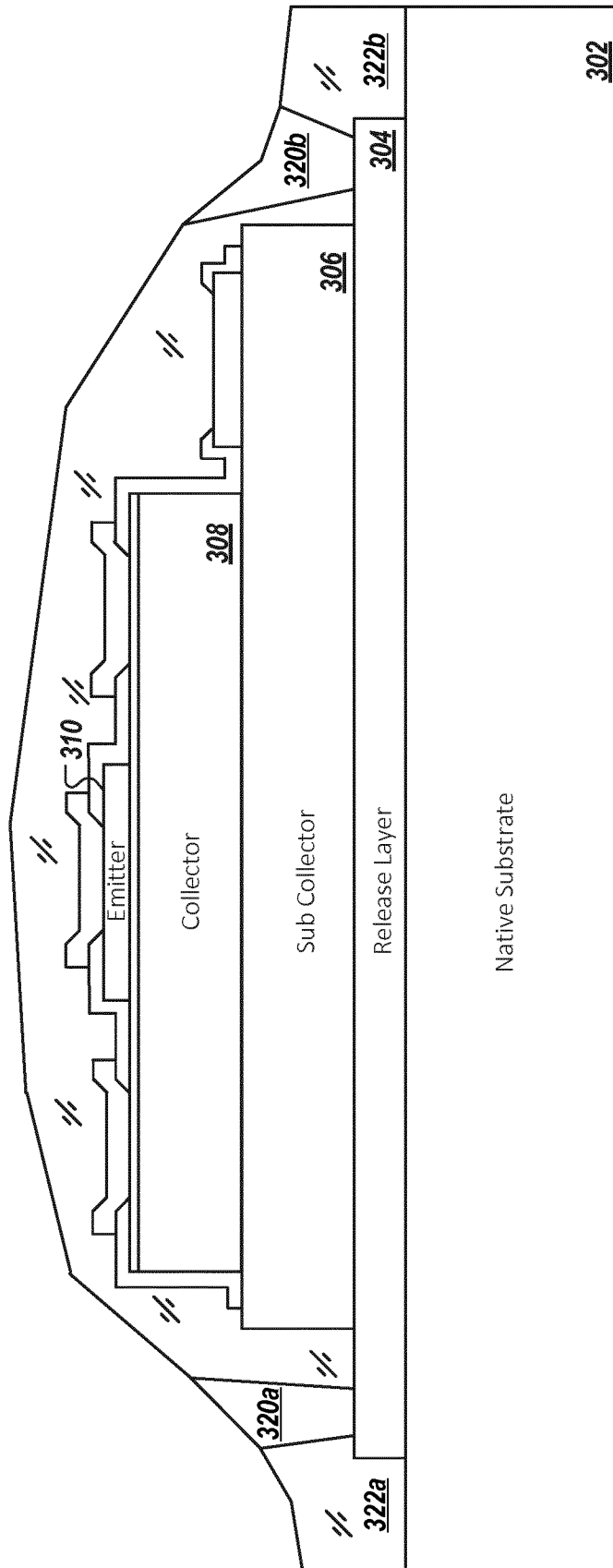


FIG. 3

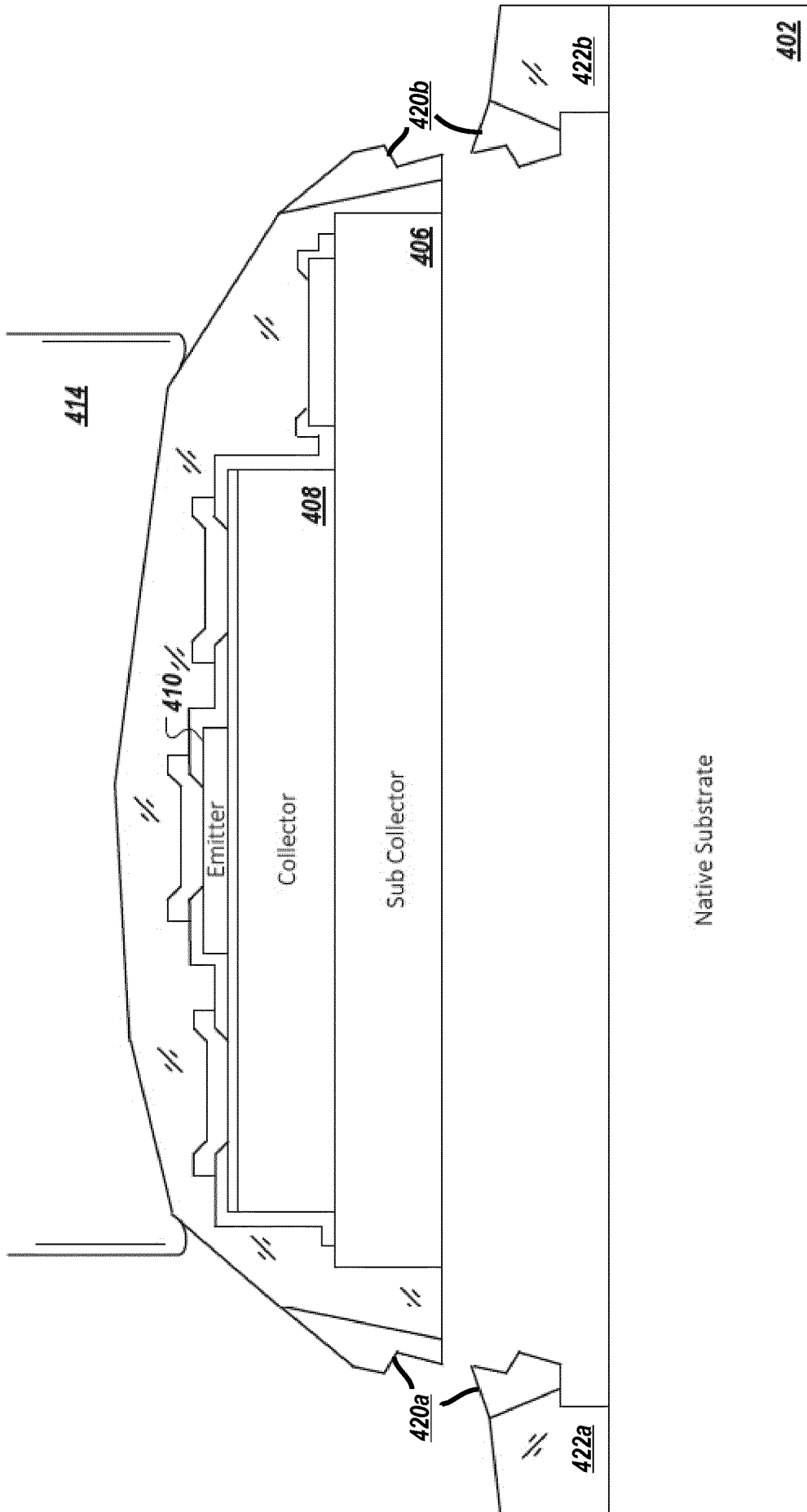


FIG. 4

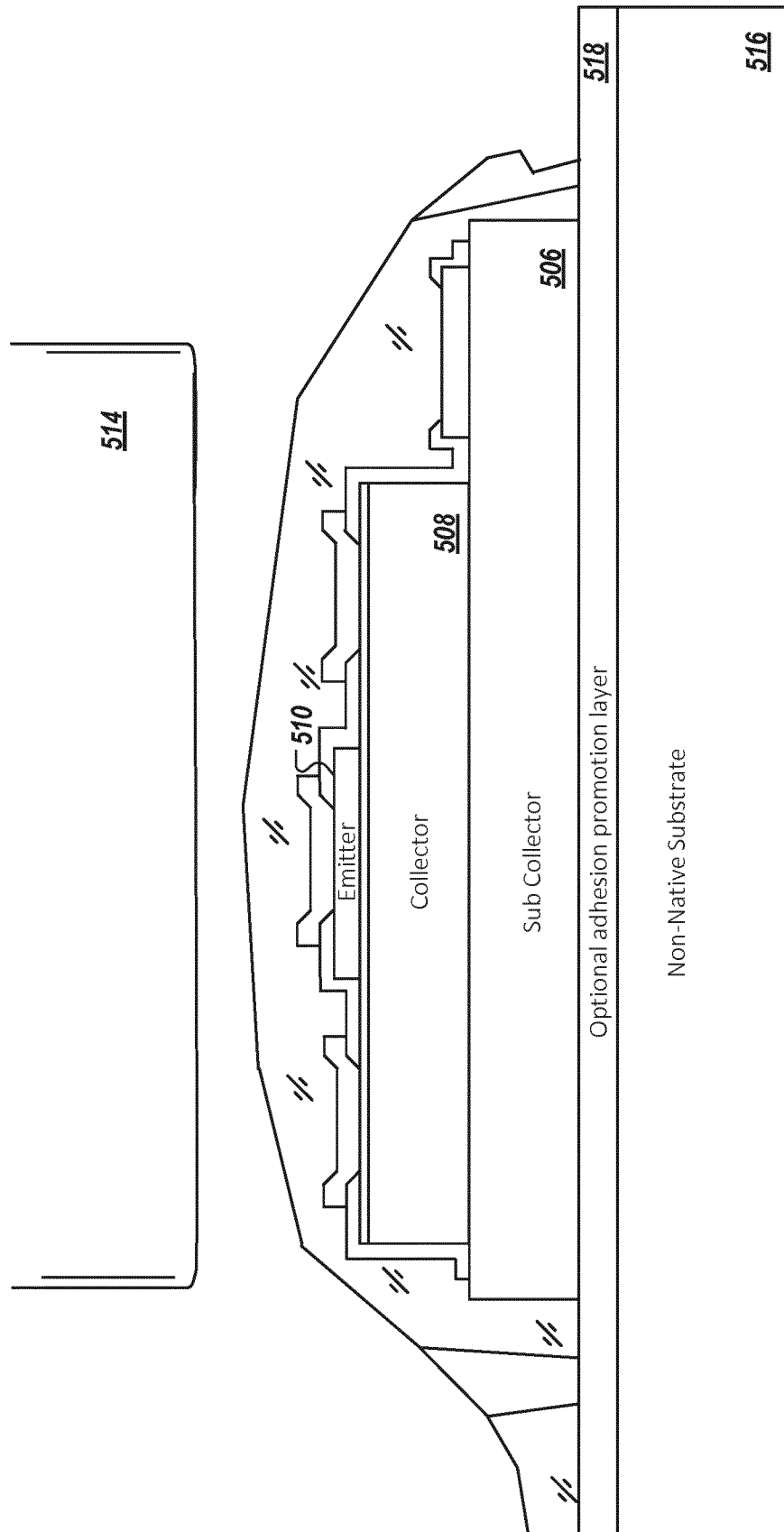


FIG. 5

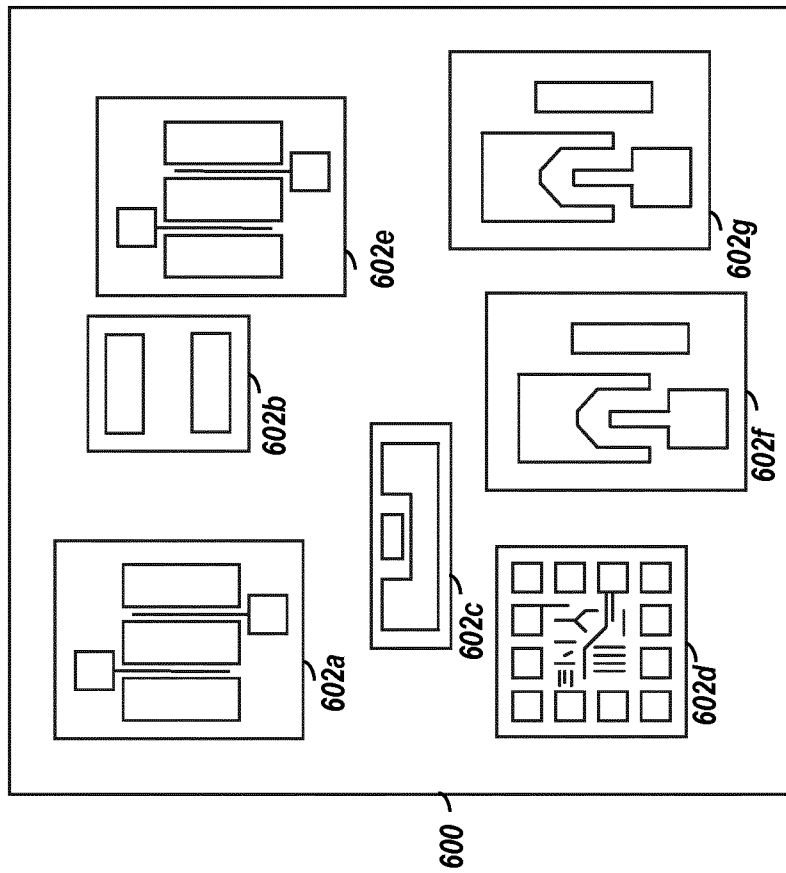


FIG. 6

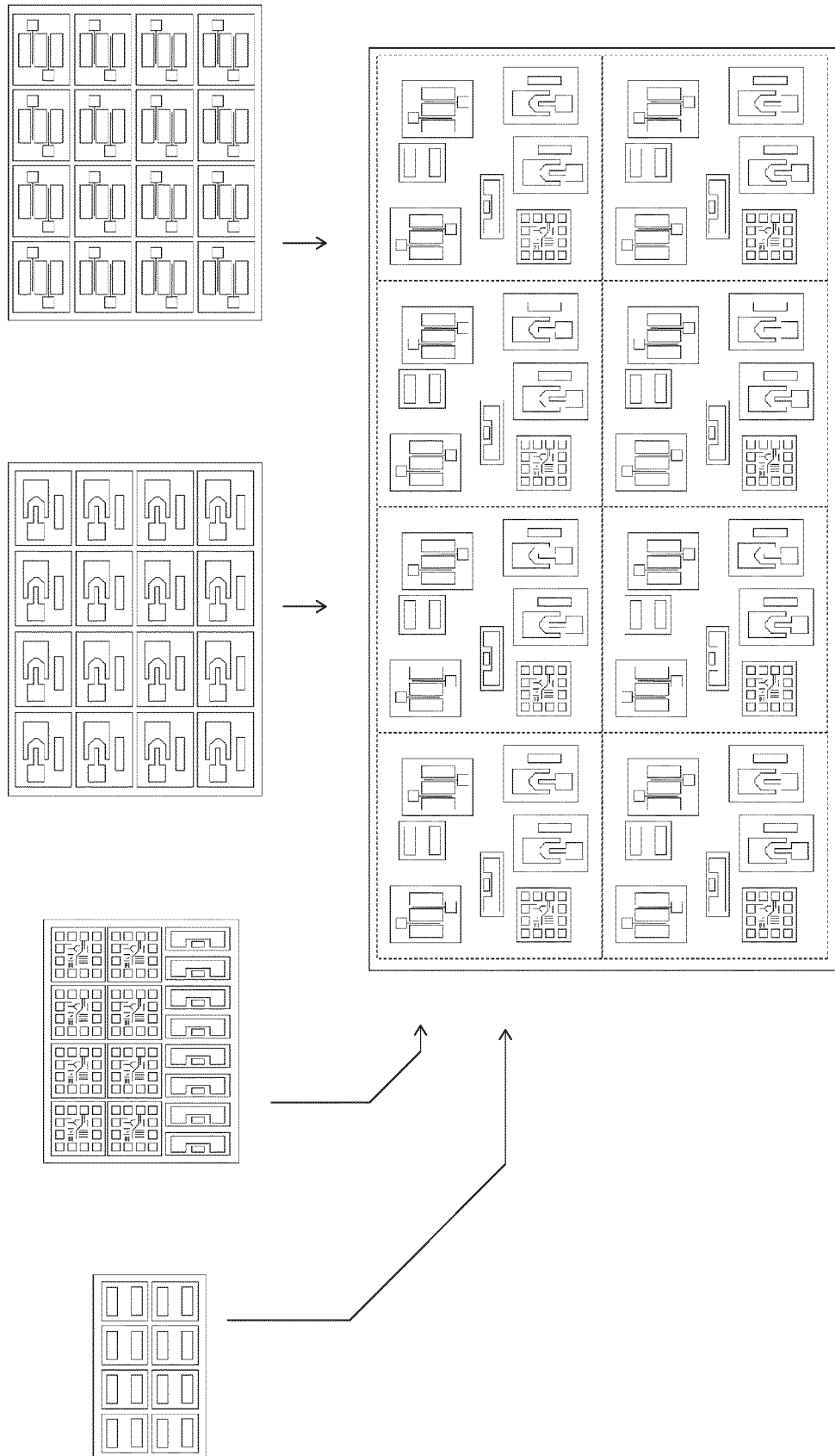


FIG. 7

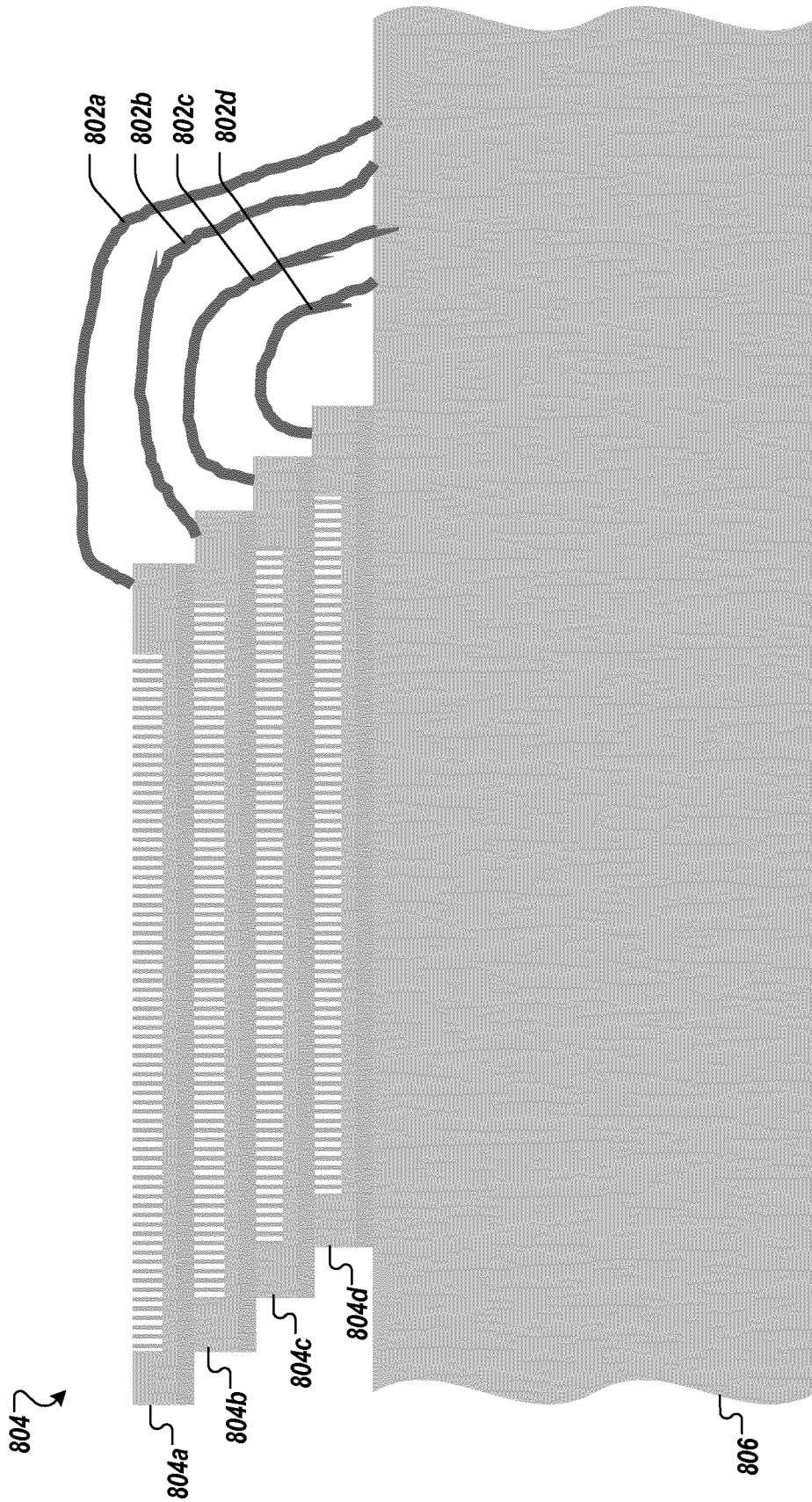


FIG. 8

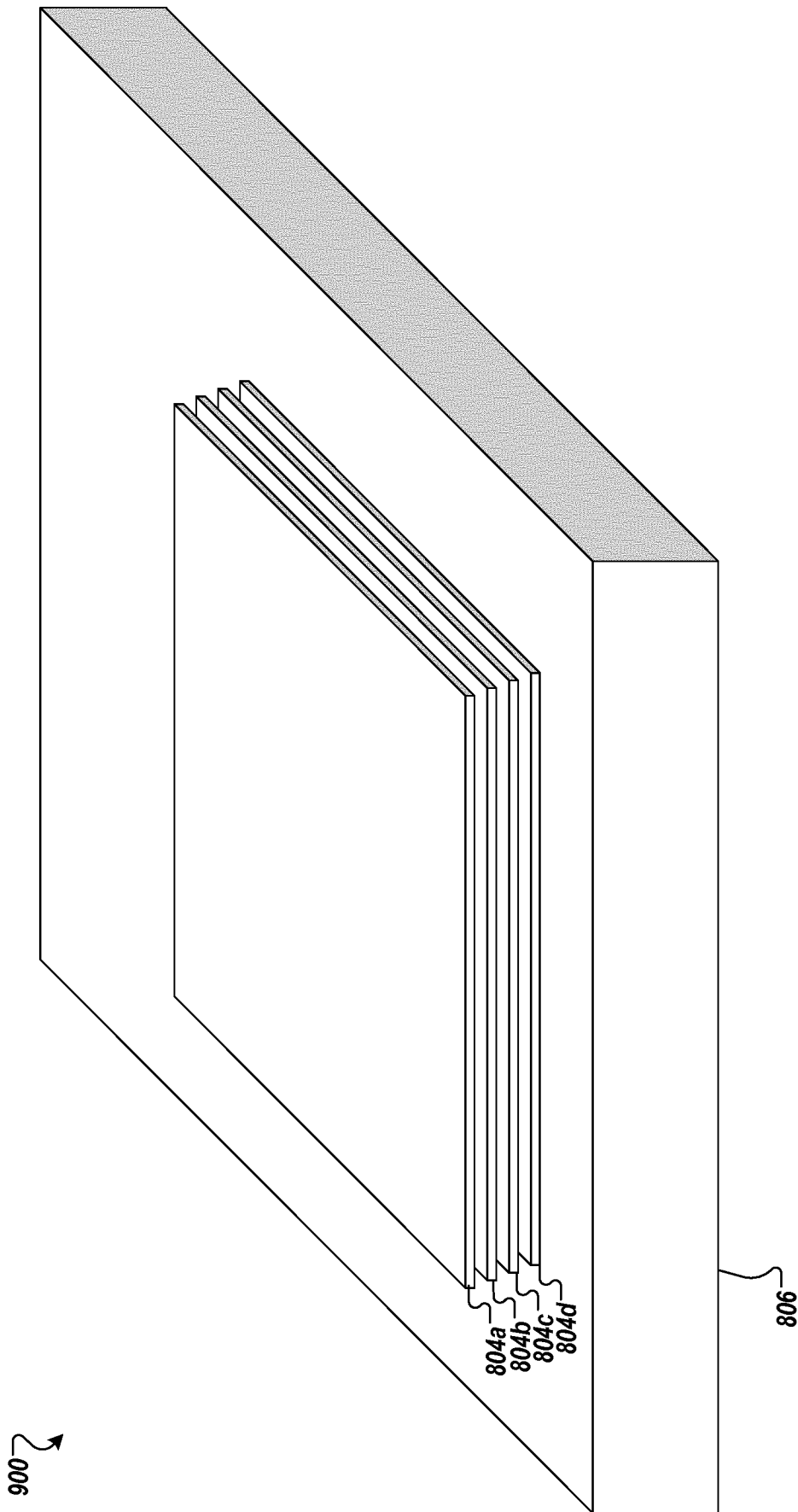


FIG. 9

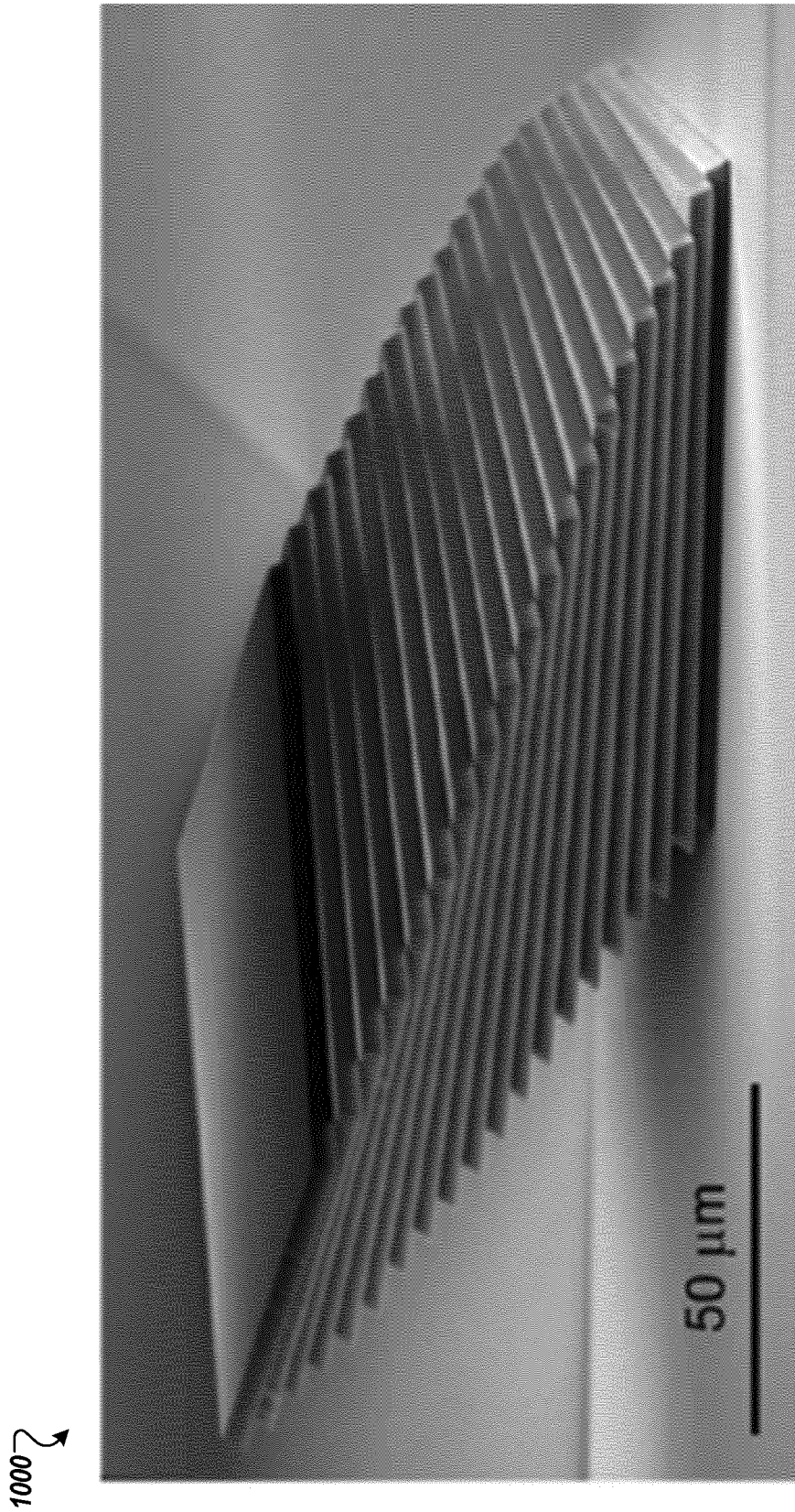


FIG. 10

1100 ↗

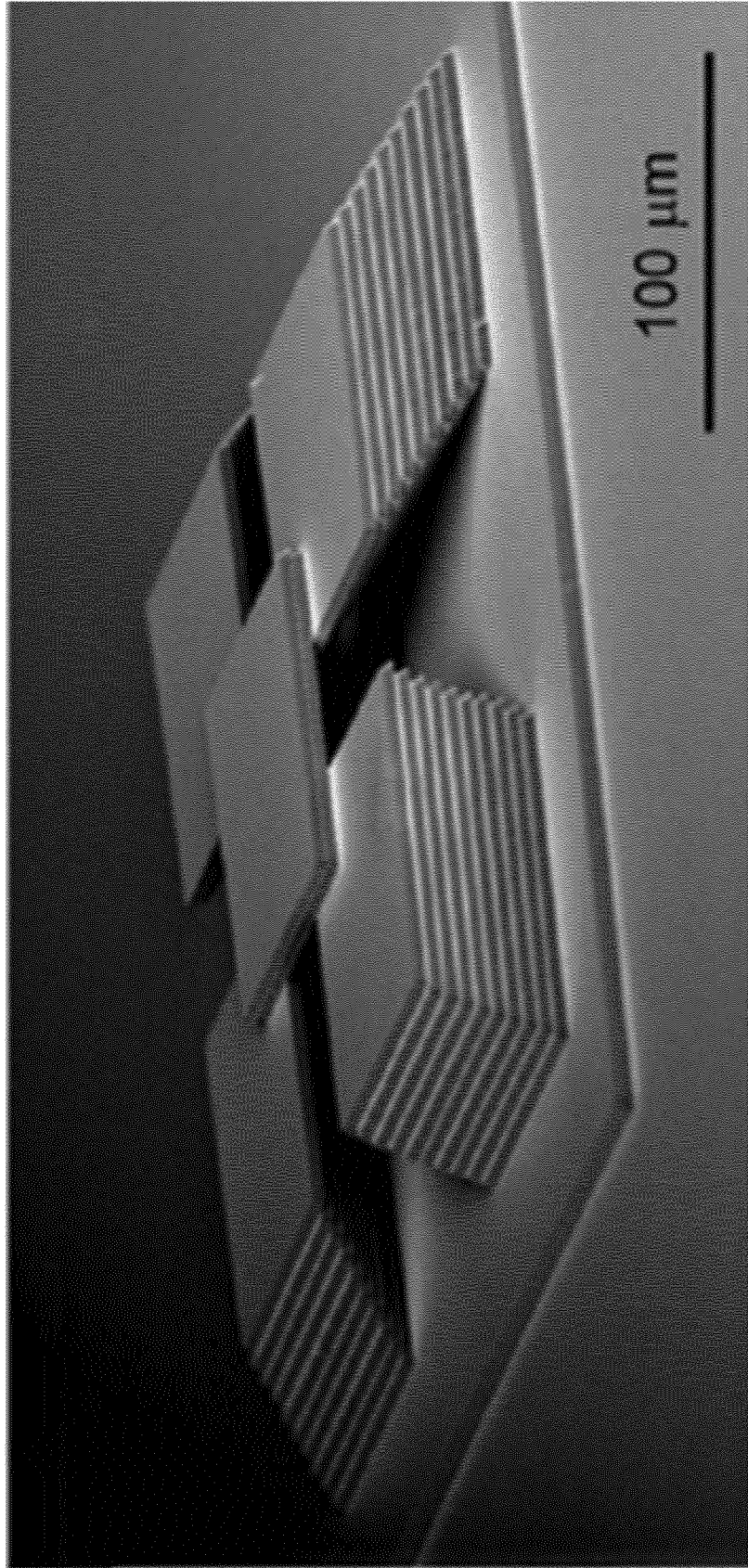


FIG. 11

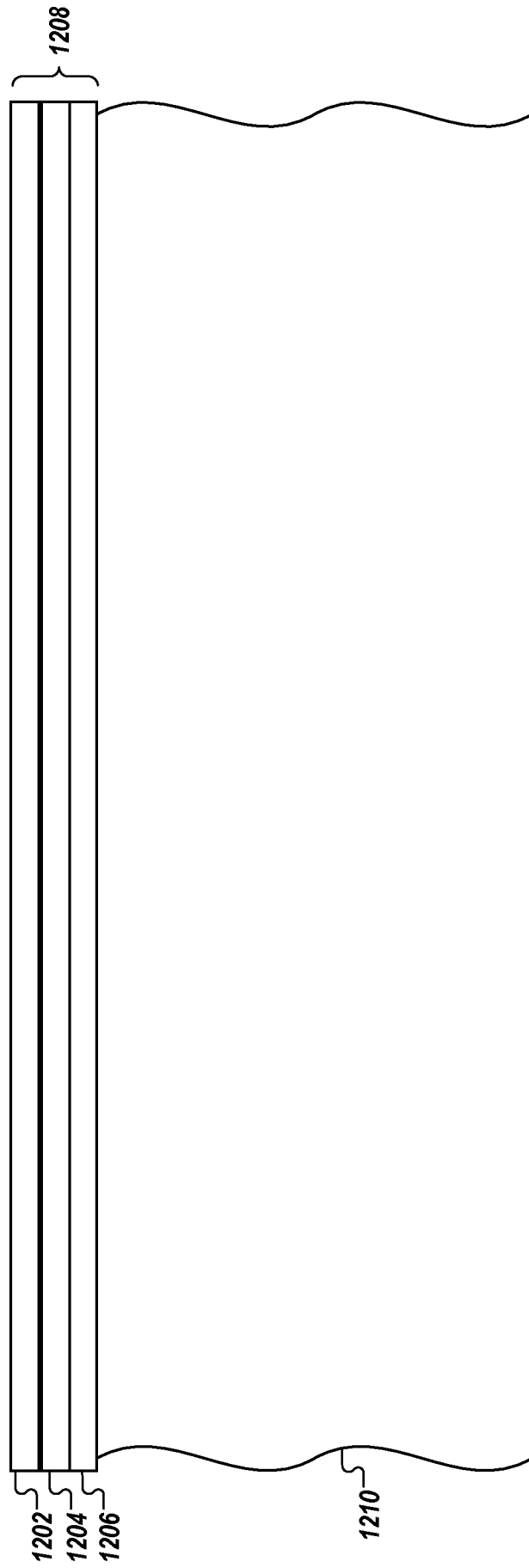


FIG. 12

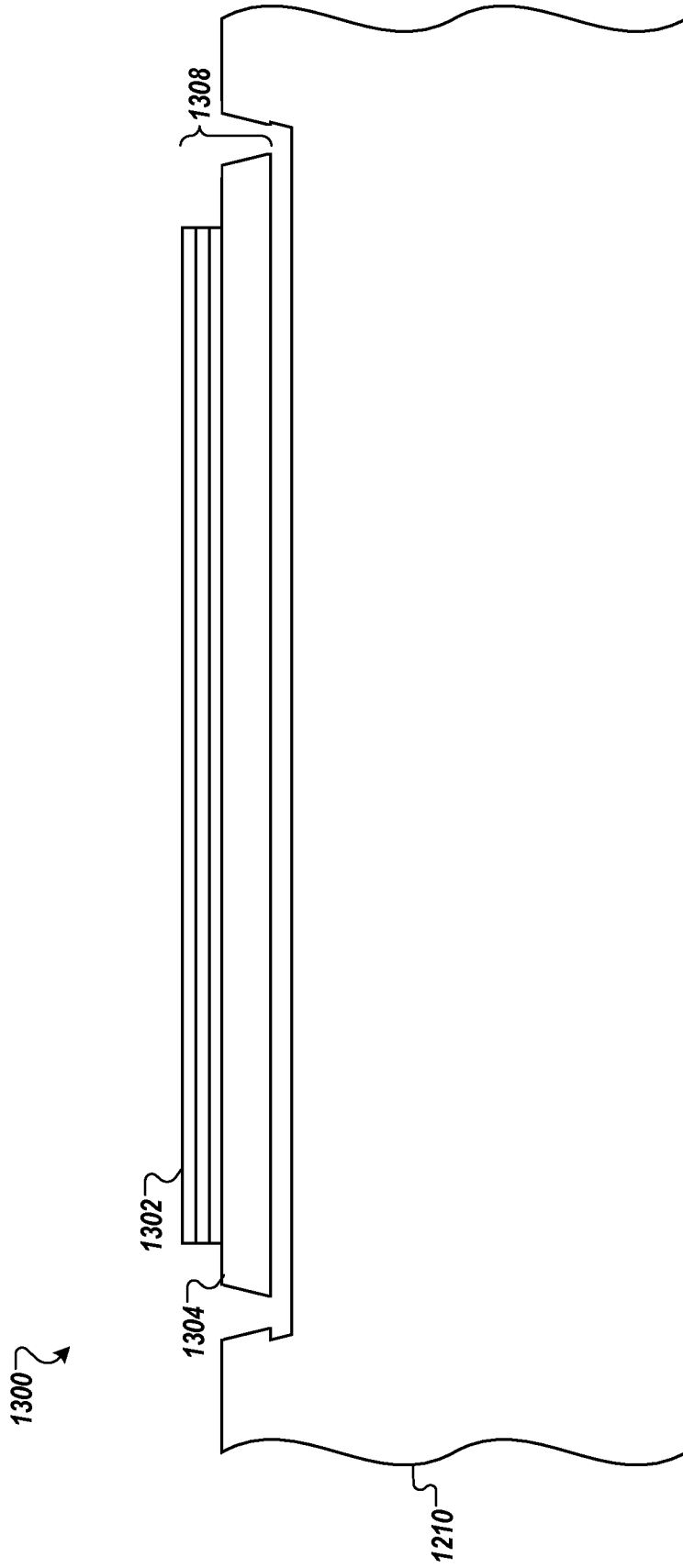


FIG. 13

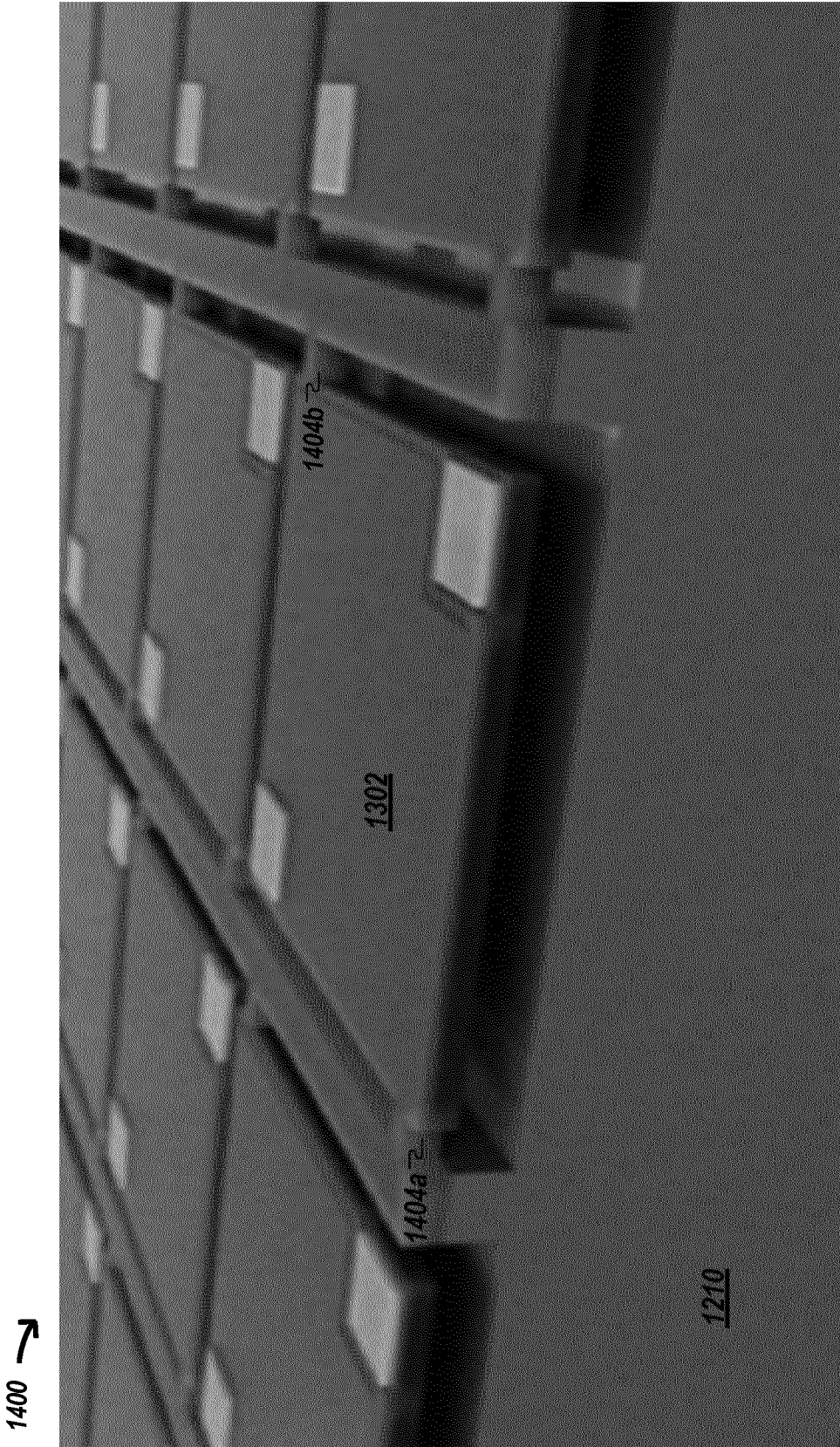


FIG. 14

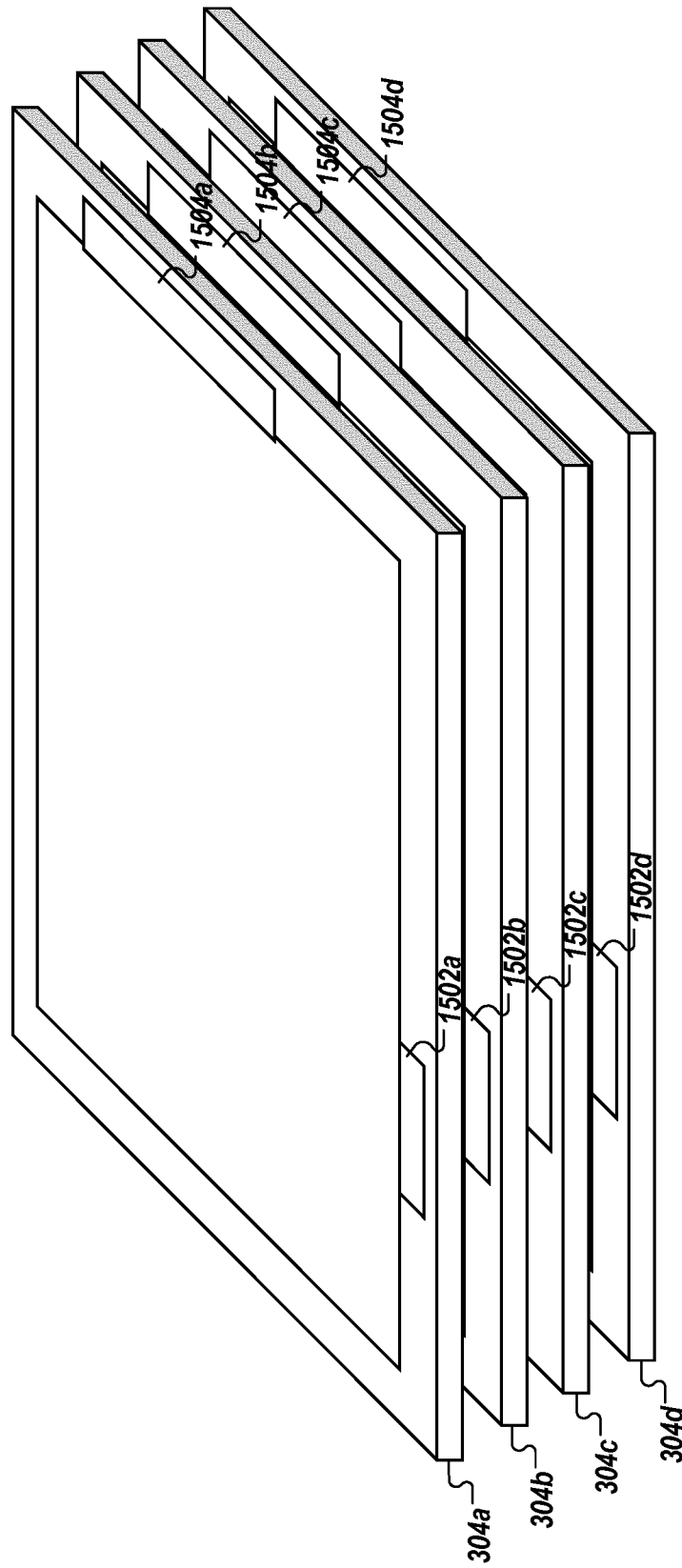


FIG. 15

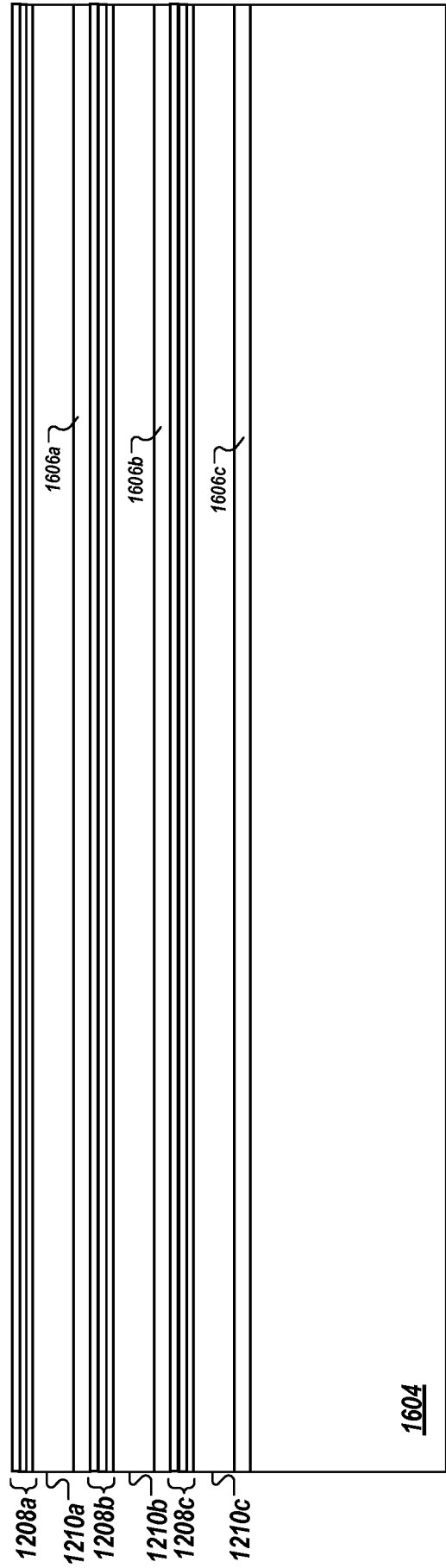


FIG. 16