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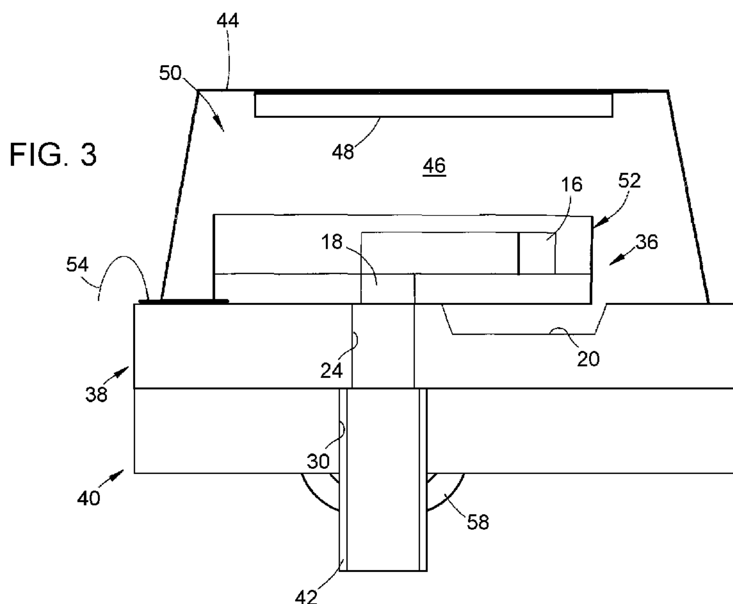
(54) **Title**: PROCESS OF FABRICATING MICROFLUIDIC DEVICE CHIPS AND CHIPS FORMED THEREBY



(57) **Abstract**: A process for fabricating multiple microfluidic device chips (50). The process includes fabricating multiple micromachined tubes (52) in a semiconductor device wafer (12). The tubes (52) are fabricated so that each tube (52) has an internal fluidic passage (16) and an inlet and outlet (18) thereto defined in a surface of the device wafer (12). The device wafer (12) is then bonded to a glass wafer (14) to form a device wafer stack (10), and so that through-holes (24) in the glass wafer (14) are individually fluidically coupled with the inlets and outlets (18) of the tubes (52). The glass wafer (14) is then bonded to a metallic wafer (26) to form a package wafer stack, so that through-holes (30) in the metallic wafer (26) are individually fluidically coupled with the through-holes (24) of the glass wafer (14). Multiple microfluidic device chips (50) are then singulated from the package wafer stack. Each device chip (50) has a continuous flow path for a fluid therethrough that is preferably free of organic materials.

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PROCESS OF FABRICATING MICROFLUIDIC DEVICE CHIPS AND CHIPS FORMED THEREBY

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 61/127,303, filed May 13, 2008, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention generally relates to semiconductor devices and methods for their fabrication. More particularly, this invention relates to a micromachined microfluidic device and method that integrate a metallic packaging substrate to provide a fluid path through the device that is preferably free of organic materials. As nonlimiting examples, the microfluidic device can be configured as a Coriolis mass flow sensor, density sensor, specific gravity sensor, fuel cell concentration meter, chemical concentration sensor, temperature sensor, drug infusion device, fluid delivery device, gas delivery device, gas sensor, bio sensor, or medical sensor.

[0003] Processes for fabricating microelectromechanical system (MEMS) devices using silicon micromachining techniques are disclosed in commonly-assigned U.S. Patent Nos. 6,477,901, 6,647,778, 7,351,603 and 7,381,628. As used herein, micromachining is a technique for forming very small elements by bulk etching a substrate (e.g., a silicon wafer), and/or by surface thin-film etching, the latter of which generally involves depositing a thin film (e.g., polysilicon or metal) on a sacrificial layer (e.g., oxide layer) on a substrate surface and then selectively

removing portions of the sacrificial layer to free the deposited thin film. In the processes disclosed in U.S. Patent Nos. 6,477,901, 6,647,778, 7,351,603 and 7,381,628, plasma and wet etching, photolithography, and wafer bonding techniques are used to produce micromachined microfluidic devices comprising a micromachined tube supported above a surface of a substrate. The tube is fabricated to have an inlet, outlet, and fluid passage therebetween through which a fluid flows. The tube can be vibrated at resonance, by which the mass flow rate, density, and/or other properties or parameters of the fluid can be measured as it flows through the tube.

[0004] The micromachined tubes disclosed in U.S. Patent Nos. 6,477,901, 6,647,778, 7,351,603 and 7,381,628 can be fabricated from a semiconductor material, for example, doped or undoped silicon, and bonded to a substrate that may be formed of, for example, Pyrex, borofloat, quartz, or other glass-type inorganic amorphous solid, silicon, silicon-on-oxide (SOI), plastic, ceramic, or another material. Metal electrodes and runners used to carry electrical signals to and from the tube can be fabricated on the substrate. For purposes of conducting the fluid to and from the tube, the substrate may be further fabricated to have through-holes fluidically connected to the inlet and outlet of the fluid passage within the tube. For mass production, numerous micromachined tubes are preferably simultaneously fabricated in a semiconductor device wafer, which is then bonded to a substrate wafer, for example, by anodic, eutectic, solder, or fusion bonding. The resulting wafer stack then undergoes a dicing operation to singulate individual microfluidic device chips from the wafers.

[0005] In applications requiring protection of the micromachined tube, a capping die is preferably bonded to each microfluidic device to enclose and protect the tube.

For the resonating tubes disclosed in U.S. Patent Nos. 6,477,901, 6,647,778, 7,351,603 and 7,381,628, the tube may be enclosed in a vacuum, which requires that the capping die is bonded (for example, anodically) to the device die to form a hermetic seal. For mass production, numerous capping dies can be simultaneously fabricated in a capping wafer, which is then bonded to the device-substrate wafer stack prior to the dicing operation such that dicing singulates individual capped microfluidic device chips from the capping-device-substrate wafer stack.

[0006] Device chips fabricated in the manner described above are typically attached to a package using an adhesive or solder. For example, a thin metal film can be deposited on the back of the device chip to provide a solderable surface, allowing the chip to be soldered to a package in a subsequent packaging step, for example, an IC packaging process using a packaging material such as a plastic or metal (for example, KOVAR®). Anodic bonding of individual device chips to a metal substrate has also been proposed, as disclosed in Briand et al., "Metal to glass anodic bonding for microsystems packaging," Transducers 2003, Vol. 2, 4C2.2, pp. 1824-1827 (2003).

[0007] The use of a metallic instead of plastic package can be advantageous if packaging stresses are of concern, including those attributable to differing coefficients of thermal expansion (CTE), or if the fluid operated on by the microfluidic device, for example, a low or high pH liquid, a high temperature or corrosive gas or biofluid, solvent, etc., is incompatible with common plastic materials due to the risk of corrosion, contamination, or biocompatibility issues. For example, the presence of plastic and other organic materials in the package or the fluid flow path can lead to contamination, out-gassing, melting or decomposition of the organic materials.

BRIEF DESCRIPTION OF THE INVENTION

[0008] The present invention provides a process for fabricating multiple microfluidic device chips, and particularly micromachined microfluidic device chips that integrate a metallic packaging substrate and preferably provide a fluid flow path through the device chip that is free of organic materials.

[0009] According to a first aspect of the invention, the process includes fabricating a plurality of micromachined tubes in a device wafer formed of a semiconductor material. The micromachined tubes are fabricated so that each tube has an internal fluidic passage and an inlet and outlet thereto defined in a surface of the device wafer. The surface of the device wafer is then bonded to a first surface of a second wafer to form a device wafer stack, and so that a plurality of through-holes in the second wafer are individually fluidically coupled with the inlets and the outlets of the micromachined tubes and define a plurality of openings at a second surface of the second wafer. The second surface of the second wafer is then bonded to a first surface of a metallic wafer to form a package wafer stack, so that a plurality of through-holes in the metallic wafer are individually fluidically coupled with the through-holes of the second wafer and define a plurality of ports at a second surface of the metallic wafer. Multiple microfluidic device chips are then singulated from the package wafer stack. Each device chip includes a package substrate formed by a singulated portion of the metallic wafer, a singulated portion of the second wafer, a singulated portion of the device wafer, one of the micromachined tubes, a package inlet and a package outlet defined by a pair of the ports at the second surface of the metallic wafer, and a continuous flow path between the package inlet and outlet thereof and defined by, in series, one of the plurality of through-holes in the metallic wafer, one of the plurality of through-holes

in the second wafer, the inlet, the passage and the outlet of the micromachined tube, one of the plurality of through-holes in the second wafer, and one of the through-holes of the metallic wafer.

[0010] A second aspect of the invention is microfluidic device chips produced by the process described above.

[0011] A significant advantage of this invention is that the use of a metallic package substrate in a microfluidic device chip allows for the elimination of any organic materials within the fluid flow path through the microfluidic device chips. By eliminating organic materials, a wider variety of fluids can be flowed through the device chips, including low or high pH liquids, high-temperature fluids, corrosive fluids, biofluids, solvents, and other fluids that tend to be incompatible with plastics and other organic materials due to potential corrosion, contamination, biocompatibility issues and the risk of out-gassing, melting or decomposition of the organic materials. Another important aspect of the invention is the wafer-level attachment of the metallic package substrate, which enables high volume production applications to lower manufacturing costs of a wide variety of microfluidic devices, nonlimiting examples of which include Coriolis mass flow sensors, density sensors, specific gravity sensors, fuel cell concentration meters, chemical concentration sensors, temperature sensors, drug infusion devices, fluid delivery devices, gas delivery devices, gas sensors, bio sensors, and medical sensors.

[0012] Other aspects and advantages of this invention will be better appreciated from the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIGS. 1 through 3 are cross-sectional views of processing steps carried out to produce multiple microfluidic device chips in accordance with a preferred embodiment of this invention.

DETAILED DESCRIPTION OF THE INVENTION

[0014] FIGS. 1 through 3 represent steps in a process carried out to produce microfluidic device chips 50 (one of which is shown in FIGS. 2 and 3) equipped with micromachined tubes (microtubes) 52. The microtubes 52 are depicted and will be described in reference to the use of the device chips 50 as Coriolis-based microfluidic devices, such as of the types disclosed in commonly-assigned U.S. Patent No. 6,477,901, 6,647,778, 7,351,603 and 7,381,628. However, it should be understood that the principles of this invention are applicable to microfluidic devices adapted for use in a variety of applications, nonlimiting examples of which include mass flow sensors, density sensors, specific gravity sensors, fuel cell concentration meters, chemical concentration sensors, temperature sensors, drug infusion devices, fluid delivery devices, gas delivery devices, gas sensors, bio sensors, and medical sensors, as well as references, actuators and other types of microfluidic devices through which a liquid or gas flows. The drawings are drawn for purposes of clarity when viewed in combination with the following description, and therefore are not necessarily to scale.

[0015] FIG. 1 depicts a limited portion of a device wafer stack 10 formed by a pair of wafers 12 and 14. The wafer 12 will be termed a device wafer 12 for the reason that the microtubes 52 are fabricated in the wafer 12. The device wafer 12 is preferably formed of a semiconductor material, most preferably silicon, though other semiconducting materials could be used. The wafer 12 may be single-crystal

or polycrystalline and may be undoped, though in a preferred embodiment the wafer 12 is doped so that the microtubes 52 are conductive and therefore can be electrically actuated, as disclosed in commonly-assigned U.S. Patent No. 6,477,901, 6,647,778, 7,351,603 and 7,381,628. Suitable methods for fabricating the device wafer 12 and its microtubes 52 include processes disclosed in U.S. Patent Nos. 6,477,901, 6,647,778, 7,351,603 and 7,381,628. As such, the contents of these patents relating to the fabrication and operation of microfluidic devices are incorporated herein by reference. The second wafer 14 will be termed a glass wafer 14, in that preferred materials for the wafer 14 are Pyrex, borofloat, quartz, or other glass-type inorganic amorphous solid materials. The wafers 12 and 14 are preferably sufficiently thick to permit handling, while the lateral dimensions of the wafers 12 and 14 are generally large enough such that, after the bonding processes discussed below, the resulting package wafer stack can be subsequently diced into a number of individual device chips, of which the chip 50 in FIGS. 2 and 3 is an example.

[0016] The microtubes 52 can be fabricated to have a variety of configurations that enable the microtubes 52 to be operable for sensing properties of a fluid, for example, using Coriolis principals. For example, when viewed from above (normal to the upper or frontside surface of the device wafer 12) each microtube 52 may be U-shaped to comprise a pair of parallel legs (one of which is shown in longitudinal cross-section) and an interconnecting distal portion. Other notable shapes for the microtubes 52 include C-shaped tubes of U.S. Patent Application Serial Nos. 11/620,908, 12/267,263 and 12/369,118, double tubes of U.S. Patent Application Serial No. 12/143,942 and 12/267,263, S-shaped tubes of U.S. Patent Application Serial No. 11/620,411 and 12/267,263, and straight tubes of U.S. Patent Application Serial No. 12/369,510. The contents of these applications relating to the

configurations and uses of their microtubes are incorporated herein by reference. FIG. 1 shows each microtube 52 as having an internal passage 16 fluidically connected to inlet and outlet holes 18 (only one of which is shown). Each internal passage 16 and its outer walls can be fabricated in the device wafer 12 by plasma etching, wet etching, grinding, bead blasting, ultrasonic machining, deep reactive ion etching (DRIE), laser machining and other methods known to those skilled in the art. The inlet and outlet holes 18 can be formed in the device wafer 12 by etching, preferably DRIE.

[0017] The shape and size of the microtubes 52 are preferably chosen to provide a suitable flow capacity and, if appropriate, have suitable vibration parameters for the fluid to be evaluated with the device chips 50. Because micromachining technologies are employed to fabricate the microtubes 52, their size can be extremely small, such as lengths of about 0.5 mm and cross-sectional areas of about 250 square micrometers, with smaller and larger tubes also being within the scope of this invention. Because of the ability to produce the microtubes 52 at such miniaturized sizes, the device chips 50 can be used to process very small quantities of fluid for analysis.

[0018] Bonding of the wafers 12 and 14 can be accomplished by a variety of techniques, such as anodic, fusion, solder, glass frit, and eutectic bonding, each of which is well known in the art and does not require any detailed discussion here. As a result of bonding the wafers 12 and 14, the microtubes 52 are cantilevered over recesses 20 formed in the surface of the glass wafer 14, thereby allowing for movement of the microtubes 52 relative to the wafer 14. FIG. 1 also shows the glass wafer 14 as having grooves 22 etched in its surface along which the device chips 50 can be singulated with a saw, laser, electric discharge, water jet, bead

blasting, or any other suitable process. Finally, the glass wafer 14 has a number of through-holes 24 corresponding in number, location and approximate cross-sectional area to the inlets and outlets 18 of the microtubes 52. The through-holes 24 define openings at the lower or backside surface of the glass wafer 12, which defines the lower or backside surface of the device wafer stack 10.

[0019] FIG. 1 shows the device wafer stack 10 prepared and aligned for bonding to a third wafer 26, which on completion will form what will be referred to herein as a package substrate (40 in FIGS. 2 and 3) of a package wafer stack comprising the device, glass and third wafers 12, 14 and 26. According to a preferred aspect of the invention, the third wafer 26 is formed of a metallic material, most preferably a corrosion-resistant metal alloy having a coefficient of thermal expansion (CTE) that approximates the CTE of the glass wafer 14. For this reason, iron-nickel based alloys are preferred, including but not limited to iron-nickel alloys commercially available under the names Alloy 42 and INVAR®. and iron-nickel-cobalt alloys commercially available under the name KOVAR®, though it is foreseeable that other alloys could be used, for example, a nickel-based superalloy such as Hastelloy, or a titanium, tungsten, molybdenum, or stainless steel alloy. Similar to the glass wafer 14, the metallic wafer 26 is shown in FIG. 1 as having grooves 28 etched or otherwise formed in its surface along which the device chips 50 will be singulated from the package wafer stack. The grooves 28 also potentially serve to reduce thermomechanical stress that occurs during bonding of the metallic wafer 26 to the glass wafer 14. It may also be desirable to tailor the thicknesses of the glass wafer 14 and/or metallic wafer 26 to further reduce thermomechanical stresses between the wafers 14 and 26.

[0020] The metallic wafer 26 is also shown as having a number of through-holes

30 corresponding in number and location to the through-holes 24 of the glass wafer 14, such that after bonding the aligned through-holes 24 and 30 define a continuous flow path with the internal passages 16 of the microtubes 52. The through-holes 30 also define ports 32 at the lower surface of the metallic wafer 12, which defines the lower or backside surface of the package wafer stack. The upper surface of the metallic wafer 26 is shown in FIG. 1 as provided with an optional bonding layer 34 containing one or more bonding materials for bonding the metallic wafer 26 to the glass wafer 14. The bonding layer 34 may be in the form of a thin-film stack formed of one or more solder or eutectic alloys for bonding of the wafers 14 and 26 by solder attachment or eutectic bonding. Other methods for bonding the wafers 14 and 26 that do not require a bonding layer 34 are foreseeable and also within the scope of the invention. To promote bonding of the metallic wafer 26 to the glass wafer 14, the upper surface of the metallic wafer 26 to be mated with the glass wafer 14 preferably undergoes polishing to provide a good bonding surface.

[0021] As evident from FIG. 1, the continuous flow path defined by the through-holes 24 and 30 of the wafers 13 and 26 and the inlets/outlets 18 and internal passages 16 of the microtubes 52 are free of any organic materials. Most notably, the metallic wafer 26 serves as the package substrate 40 for each device chip 50 (as shown in FIGS. 2 and 3), thus eliminating the use of plastic packaging that would come in contact with the fluid flowing through the device chips 50. In addition, the flow path is preferably free of epoxies, silicones and other adhesives often used to attach MEMS chips to a package surface. Subsequent assembly of one of the chips 50 with a fluid system is also preferably performed without the use of elastomeric o-rings, gaskets and grommets to seal the metallic package substrate 40 of the chip 50 to the remainder of the fluid system. As a result, preferred device chips 50 of this invention can be employed to handle fluids that would otherwise raise corrosion,

contamination or biocompatibility issues, such as low and high pH liquids, high-temperature fluids, corrosive fluids, biofluids, etc., which can cause organic materials to out-gas, melt, decompose or otherwise contaminate the fluid. Because the metallic wafer 26 is bonded to the device wafer stack 10 at the wafer level, the process described above is ideal for high-volume production applications to lower manufacturing costs.

[0022] FIG. 2 represents the appearance of a single device chip 50 following bonding of the metallic wafer 26 to the device wafer stack 10 to form the package wafer stack, and then singulation to separate the multiple chips 50 from the package wafer stack by cutting through the glass and metallic wafers 14 and 26. As previously noted, singulation can be achieved by sawing (or another suitable technique) along the grooves 22 and 28 provided in the surfaces of the glass and metallic wafers 14 and 26. From the forgoing, it should be apparent that the singulation step is preferably performed after MEMS processing of the device chips 50 has been completed. For clarity, the portions of the device chip 50 defined by singulated portions of the device, glass and metallic wafers 12, 14 and 26 are identified in FIG. 2 as the device layer 36, glass layer 38, and package substrate 40 of the device chip 50.

[0023] FIG. 2 further shows one of two tubes 42 that are preferably attached to the device chip 50 after singulation. The tubes 42 are received in the ports 32 of the package substrate 40 defined by the through-holes 30 of the metallic wafer 26. As with the metallic wafer 26, the tubes 42 are also preferably formed of a metallic material and secured to the package substrate 40 without the use of any organic materials. For example, the tubes 42 can be formed of a stainless steel alloy or any other metallic material that is compatible with the fluid that will flow through the

device chip 50. The tubes 42 can be of any desired length and configured as package inlet and outlet conduits for direct connection to a fluidic system via welding, fittings, couplers, or any other suitable method.

[0024] The through-holes 30 of the package substrate 40 (formed by a singulated portion of the metallic wafer 26) are shown in FIG. 2 as being oversized relative to the through-holes 24 in the glass layer 38 (formed by a singulated portion of the glass wafer 14), such that the tubes 42 extend completely through the package substrate 40 and the ends of the tubes 42 abut the glass layer 38 of the chip 50. Alternatively, the through-holes 24 in the glass layer 38 could also be oversized, so that the ends of the tubes 42 abut the device layer 36 of the chip 50. The tubes 42 may be attached to the metallic package substrate 40 by welding, brazing, soldering, or bonding by some other method that does not introduce an organic material into the flow path through the device chip 50. A localized weldment 56 formed by laser welding is believed to be preferred for securing the tubes 42 due to the capability of laser welding causing only localized heating. Alternatively or in addition, the tubes 42 and their mating ports 32 can be configured to provide a retention feature, for example, complementary threads to provide a threaded coupling between the tubes 42 and their mating ports 32. A reinforcement 58 is shown in FIG. 3 as encapsulating the tube-to-wafer joint to prevent leakage and reduce mechanical wear, fatigue and breakage. The reinforcement 58 can be formed by, for example, soldering, welding, or brazing, or with an adhesive, collar, potting material, jig, etc.

[0025] Finally, FIG. 3 shows the microtube 52 as being enclosed by a capping die 44. The capping die 44 can be provided by bonding a capping wafer (not shown) to the device wafer stack 10 prior to singulation, or individually bonding the capping die 44 to the singulated device chip 50. The capping die 44 serves to

provide a protective enclosure 46 surrounding the microtube 52. In applications where device performance can be enhanced by maintaining a vacuum within the enclosure 46, the die 44 can be vacuum sealed to the frontside surface of the glass layer 38. For example, the dynamic performance of a vibrating microtube 52 in accordance with U.S. Patent Nos. 6,477,901, 6,647,778, 7,351,603 and 7,381,628 can be significantly enhanced by maintaining a vacuum within the enclosure 46. A variety of materials can be considered for the capping die 44, including but not limited to silicon, glass, ceramic, and plastic wafers that can be processed to have a sufficiently deep cavity to accommodate the microtube 52. The capping die 44 is shown as having an integrated getter 48 to improve vacuum quality in accordance with known practices. Depending on the materials of the glass wafer 14 and capping die 44, attachment and sealing of the capping die 44 to the glass layer 38 can be by glass frit, eutectic, solder, anodic, or another bonding technique known in the art. Alternatively, this step can be omitted if an acceptable vacuum can be formed without wafer-to-wafer bonding. In addition, the capping die 44 can be omitted and enclosure of the microtube 52 can be performed in a subsequent packaging step, such as but not limited to IC packaging (e.g., an IC package with a KOVAR® lid) or product packaging.

[0026] The microtube 52 can be electrically interconnected by conductive runners, wirebonds, or any other suitable means to drive and sensor electrodes (not shown) located within the recess 20 or elsewhere to enable driving and sensing of the microtube 52. The drive electrodes can drive the microtube 52 electrostatically or by any other suitable technique, including but not limited to piezoelectric, piezoresistive, acoustic, ultrasonic, magnetic, and optic actuation techniques. Movement of the microtube 52 can also be sensed using a variety of techniques, such as capacitively, piezoelectrically, piezoresistively, acoustically, ultrasonically,

magnetically, optically, etc. FIG. 3 shows one of any number of wirebonds 54 provided for electrically connecting the device chip 50 to external circuitry (not shown), such as printed circuit boards, ASICs, amplifiers, and/or signal conditioning circuitry. ASICs may be mounted on a circuit board or on the glass layer 38, cap die 44, or elsewhere. If so desired, the metallic package substrate 40 can be grounded to provide an electromagnetic shield for the device chip 50.

[0027] While the invention has been described in terms of a particular embodiment, it is apparent that other forms could be adopted by one skilled in the art. Therefore, the scope of the invention is to be limited only by the following claims.

CLAIMS:

1. A process of fabricating multiple microfluidic device chips (50), the process comprising:

fabricating a plurality of micromachined tubes (52) in a device wafer (12) formed of a semiconductor material, the micromachined tubes (52) being fabricated so that each micromachined tube (52) has an internal fluidic passage (16) and an inlet and outlet (18) thereto defined in a surface of the device wafer (12);

bonding the surface of the device wafer (12) to a first surface of a second wafer (14) to form a device wafer stack (10) and so that a plurality of through-holes (24) in the second wafer (14) are individually fluidically coupled with the inlets (18) and the outlets (18) of the micromachined tubes (52) and define a plurality of openings at a second surface of the second wafer (14);

bonding the second surface of the second wafer (14) to a first surface of a metallic wafer (26) to form a package wafer stack so that a plurality of through-holes (30) in the metallic wafer (26) are individually fluidically coupled with the through-holes (24) of the second wafer (14) and define a plurality of ports (32) at a second surface of the metallic wafer (26);

singulating multiple microfluidic device chips (50) from the package wafer stack, each of the multiple microfluidic device chips (50) comprising a package substrate (40) formed by a singulated portion of the metallic wafer (26), a singulated portion (38) of the second wafer (14), a singulated portion (36) of the device wafer (12), one of the micromachined tubes (52), a package inlet and a package outlet port defined by a pair of the ports (32) at the second surface of the metallic wafer (26), and a continuous flow path between the package inlet and outlet thereof and defined by, in series, one of the plurality of through-holes (30) in the metallic wafer (26), one of the plurality of through-holes (24) in the second wafer (14), the inlet (18), the passage (16) and the outlet (18) of the micromachined tube (52), a second

of the plurality of through-holes (24) in the second wafer (14), and a second of the through-holes (30) of the metallic wafer (26).

2. The process according to claim 1, further comprising the step of bonding a cap wafer (44) to the device wafer (12), the cap wafer (44) defining cavities (46) that enclose the micromachined tube (52) of each device wafer stack (10), whereby each of the microfluidic device chips (50) formed by the singulating step comprises a cap die (44) enclosing the micromachined tube (52) thereof.

3. The process according to claim 2, wherein the bonding of the cap wafer (44) results in a vacuum within each of the cavities (46) and hermetic seals between the cap wafer (44) and the device wafer (12).

4. The process according to claim 1, further comprising defining a plurality of grooves (28) in at least the second surface of the metallic wafer (26), the singulating step comprising severing the metallic wafer (26) along the grooves (28) to singulate the microfluidic device chips (50).

5. The process according to claim 4, wherein only the second and metallic wafers (14,26) are severed during the singulating step.

6. The process according to claim 1, wherein the second wafer (14) is formed of a glass-type inorganic amorphous solid.

7. The process according to claim 1, wherein the metallic wafer (26) is formed of an iron-nickel alloy, an iron-nickel-cobalt alloy, a nickel-based superalloy, a titanium alloy, a tungsten alloy, a molybdenum alloy, or a stainless steel alloy.

8. The process according to claim 1, further comprising inserting ends of package inlet and outlet tubes (52) into each of the package inlets and package outlets of the microfluidic device chips (50), and bonding the ends of the inlet and outlet tubes (42) to the package substrates (40) formed by the singulated portions of the metallic wafer (26) to define inlet and outlet conduits to the microfluidic device chips (50).

9. The process according to claim 8, further comprising bonding the ends of the inlet and outlet tubes (42) to the package substrates (40) with a bonding material (56) chosen from the group consisting of weld, braze, and solder materials.

10. The process according to claim 9, further comprising performing an additional step to reinforce the bonding material.

11. The process according to claim 10, wherein the additional step comprises encapsulating the bonding material (56) with a second material (58) chosen from the group consisting of solder, weld, brazing, and adhesive materials.

12. The process according to claim 1, wherein all surfaces of the continuous flow path of each microfluidic device chip (50) that are contacted by a fluid flowing therethrough are free of organic materials.

13. The process according to claim 1, further comprising electrically grounding the package substrate (40) of at least one of the microfluidic device chips (50).

14. The process according to claim 1, wherein the micromachined tubes (52) are adapted for vibrational movement relative to the second wafer (14).

15. A microfluidic device chip (50) formed by the process of claim 1.

16. The microfluidic device chip (50) according to claim 15, wherein the microfluidic device chip (50) is chosen from the group consisting of Coriolis mass flow sensors, density sensors, specific gravity sensors, fuel cell concentration meters, chemical concentration sensors, temperature sensors, drug infusion devices, fluid delivery devices, gas delivery devices, gas sensors, bio sensors, and medical sensors.

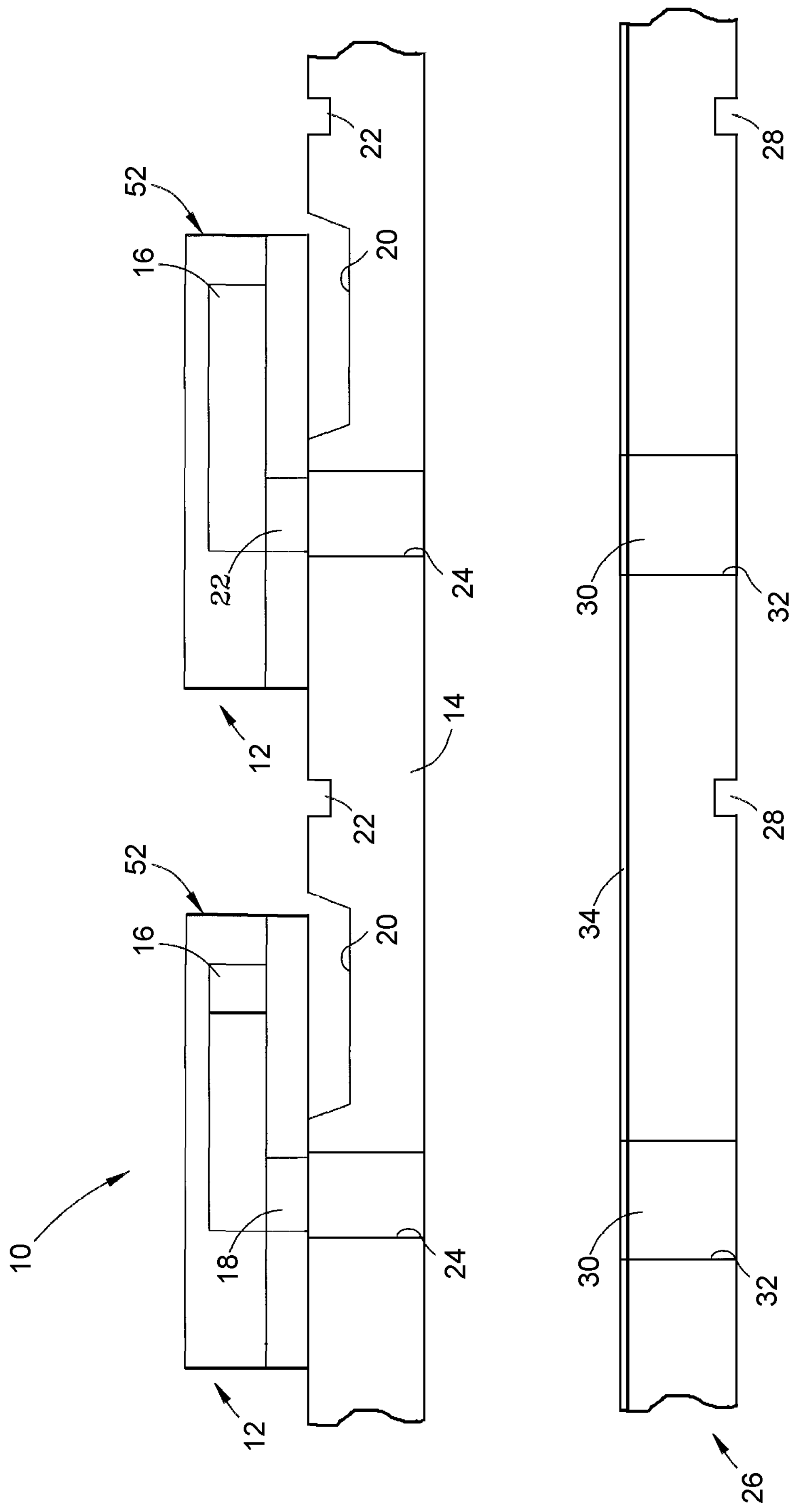

FIG. 1

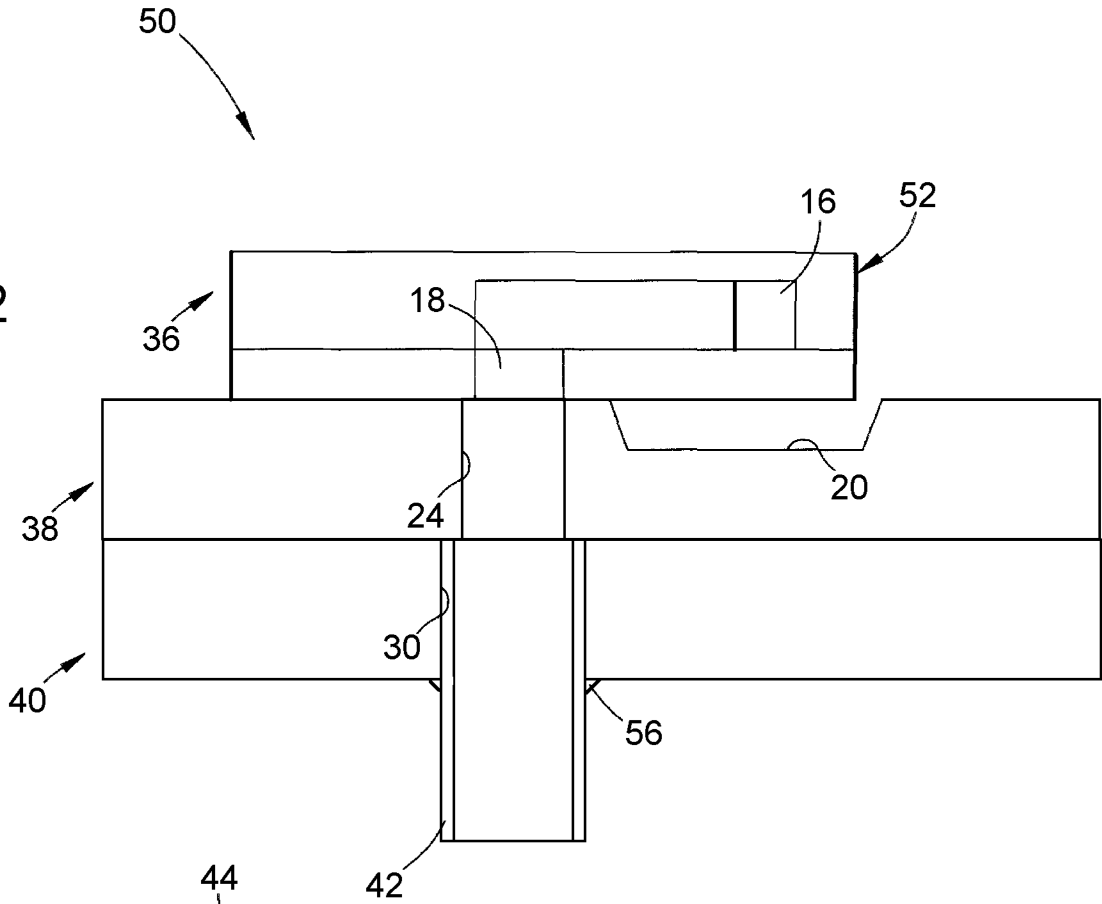

FIG. 2

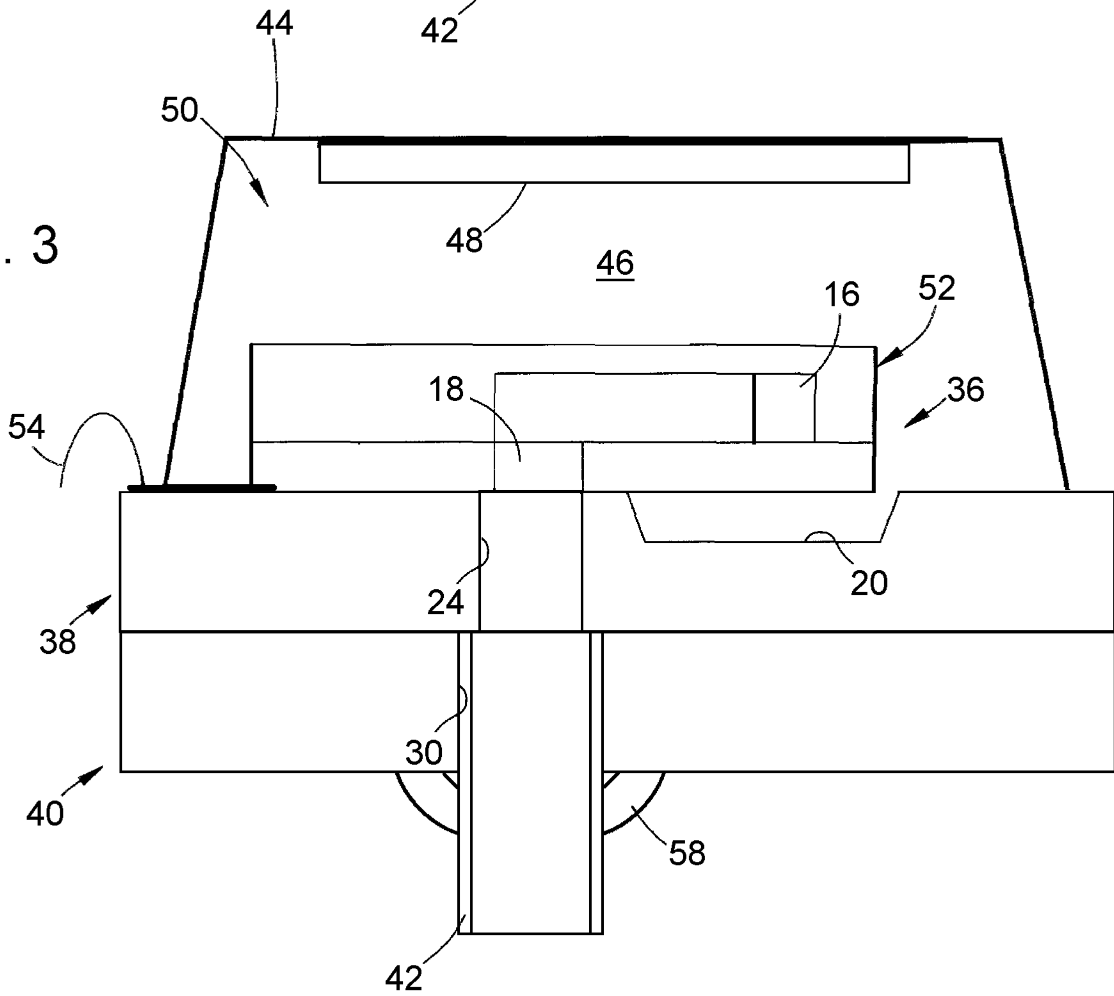

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2009/043720

A. CLASSIFICATION OF SUBJECT MATTER

B81C 1/00(2006.01)i, H01L 23/12(2006.01)i, H01L 21/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC :B23K 9/00, B23K 9/02, G01F 5/00, G01F 1/68, C12M 1/34, G01N 1/10, B81C 1/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Utility Models and applications for Utility Models since 1975
Japanese Utility Models and applications for Utility Models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS (KIPO internal) & keywords: "microfluidic", "chip", "wafer stack", "microtube", "package"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 20060175303A1 (SPARKS, D. and NAJAFI, N.) 10 AUGUST 2006 see figures 1-9, pages 1-4	1-16
Y	US 20070151335A1 (SPARKS, D. and NAJAFI, N.) 05 JULY 2007 see figures 1-13, pages 1-4	1-16
A	SPARKS, D. et al. A variable temperature, resonant density sensor made using an improved chip-level vacuum package. Sensors and Actuators A 107, 2003, pp. 119-124. see the whole document	1-16
A	US 06647778 B2 (SPARKS, D.) 18 NOVEMBER 2003 see the whole document	1-16
A	US 20040005628 A1 (FOSTER, J. S.) 08 JANUARY 2004 see the whole document	1-16

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 AUGUST 2009 (25.08.2009)	**25 AUGUST 2009 (25.08.2009)**

Name and mailing address of the ISA/KR

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Facsimile No. 82-42-472-7140

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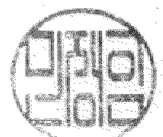
Telephone No. 82-42-481-5545



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2009/043720

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