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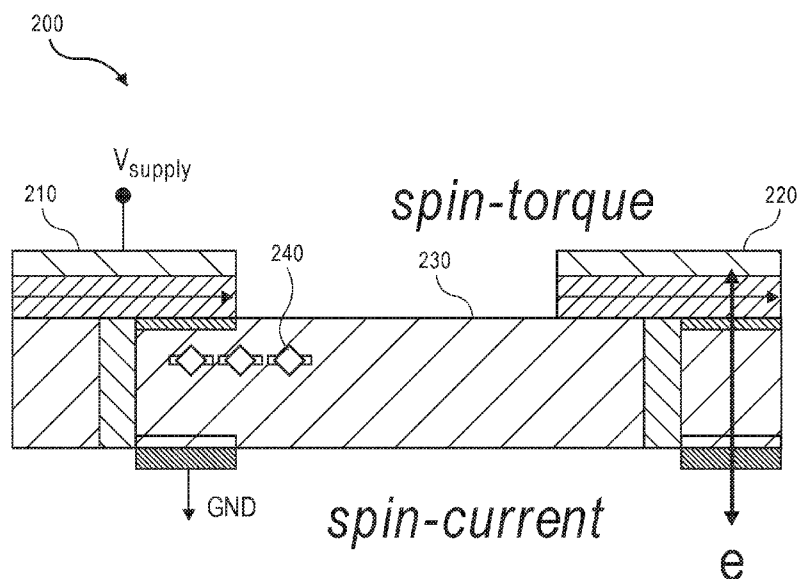


FIG. 2

(57) Abstract: Embodiments are generally directed to enhanced materials processing for magneto-electric spin orbit (MESO) devices. An embodiment of an apparatus includes a first transistor and a second transistor, each transistor including a gate electrode, a first junction region, and a second junction region; a set of lines including alternating ferromagnetic material lines and non-magnetic metal interconnect lines fabricated in a wafer, the plurality of lines including metal interconnect lines to provide connections for the junction regions of the first and second transistors, including connections to provide power and control; and a MESO device including a first magnet and a second magnet, the set of lines including ferromagnetic material lines for fabrication of the MESO device magnets.



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ENHANCED MATERIALS PROCESSING FOR MAGNETO-ELECTRIC SPIN LOGIC DEVICES**TECHNICAL FIELD**

Embodiments described herein generally relate to the field of electronic devices and, more particularly, enhanced materials processing for magneto-electric spin orbit (MESO) devices.

BACKGROUND

With electronics approaching the nanometer scale, a scalable spintronic logic device that operates via spin-orbit transduction combined with magneto-electric switching has been developed as a technology to move beyond complementary metal-oxide semiconductor (CMOS) computing. The magneto-electric spin orbit (MESO) logic, or spintronic logic, enables the continued scaling of logic device to smaller scales. Spintronic logic can enable energy and computational efficiency by utilizing a new state variable for computation.

Spintronic logic belongs to the class of devices utilizing a new physical quantity (magnetization or spin, in this case) as computation variable. Such new variables can be non-volatile, i.e. preserving the computation state when the power to the integrated circuit is switched off. Non-volatile logic can improve the power and computational efficiency by allowing architects to put the processor to un-powered sleep states more often with less energy.

Existing spintronic logic technologies suffer from high energy and long time necessary for switching due to the inefficiency of mechanism for converting charge to spin variables and vice versa. In particular the conversion inefficiency results in large write currents ($\sim 100 \mu\text{A/bit}$) producing high Joule heat dissipation and slow switching time ($\sim 10\text{ns}$) over which the current needs to be “on”.

However, the fabrication of improved spintronic logic technologies is complicated by the extreme scaling of such devices, including the need for extremely fine lines of material for the fabrication of MESO devices and connected elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments described here are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1A through 1P are illustrations of an improved process for fabrication of fine pitch ferromagnetic and metal microelectronics for improved spin logic devices according to an embodiment;

Figure 2 is an illustration of spin polarized current in a magneto-electric spin orbit

device according to an embodiment;

Figures 3A and 3B illustrate operation of a spin orbit logic device as a logic inverter or repeater according to an embodiment;

Figure 4 is an illustration of CMOS integration of a spin orbit logic device according to an embodiment;

Figure 5 illustrates a charge mediated majority gate according to an embodiment;

Figure 6 illustrates a table and an apparatus for a state machine using spin orbit logic with CMOS integration according to an embodiment;

Figures 7A and 7B illustrate a methodology for fabrication of an apparatus including spin orbit logic devices according to an embodiment;

Figure 8 is an illustration of a system on chip including spin orbit logic devices according to an embodiment; and

Figure 9 is an illustration of a computing system including spin logic devices according to an embodiment.

DETAILED DESCRIPTION

Embodiments described herein are generally directed to enhanced materials for magneto-electric spin orbit (MESO) logic devices.

In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper,” “lower,” “above,” “below,” “bottom,” and “top” refer to directions in the drawings to which reference is made. Terms such as “front,” “back,” “rear,” and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

For the purposes of this description:

“Magnetoelectric spin orbit logic device” or “MESO logic device” refers to a logic device that operates via spin-orbit transduction combined with magnetoelectric switching, the MESO logic device utilizing magnetic state (or spin state) for logical operation. MESO devices may also be referred to in general as spin orbit logic (SOL) devices or spintronic devices.

5 In some embodiments, an apparatus, system, or method provide for improved material processing for MESO logic devices. In some embodiments, a process provides for fabrication of fine pitch ferromagnetic and metal microelectronics for spin logic devices according to an embodiment.

Spintronic logic belongs to the class of devices utilizing a new physical quantity
10 (magnetization or spin, in this case) as computation variable. Such new variables can be non-volatile, i.e. preserving the computation state when the power to the integrated circuit is switched off. Non-volatile logic can improve the power and computational efficiency by allowing architects to put the processor to un-powered sleep states more often with less energy.

Existing spintronic logic options suffer from high energy and long time necessary for switching
15 due to the inefficiency of mechanism for converting charge to spin variables and vice versa. In particular this results in (1) Large write currents ($\sim 100 \mu\text{A/bit}$) producing high Joule heat dissipation; and (2) Slow switching time ($\sim 10\text{ns}$) over which the current needs to be “on”.

Spin polarized current is conducted between nanomagnets to switch magnetization by the spin torque effect. In this and multiple other spintronic devices, the signal is sent from one node to
20 the other as a spin quantity (spin polarized current, a domain wall, or a spin wave). These signals are slow ($\sim 1000 \text{ m/s}$) and, more importantly, they exponentially attenuate over the length of $\sim 1 \mu\text{m}$.

In some embodiments, a signal is instead sent over an electrical interconnect. Through use of the electrical interconnect, the charge current does not attenuate and the communication is
25 much faster (limited by the RC delay). In conventional technology, current induced injection of spin current from a magnet is used as the charge-to-spin conversion, and spin torque is used to switch magnetization in the output magnet, the effect of magnetoresistance detected by a sense amplifier is used as the spin-charge conversion. Due to much more efficient conversion mechanisms, the switching time of spin logic devices is $\sim 100 \text{ ps}$ (picoseconds), versus $\sim 1 \text{ ns}$
30 (nanoseconds) in conventional devices, and the switching energy is $\sim 10 \text{ aJ}$ (attojoules), versus 100 fJ (femtojoules) in conventional devices.

However, among the issues faced in the implementation of MESO devices and connected transistor devices at the required scaling is the requirement for generation of a resulting wafer with finely pitched ferromagnetic (FM) material and non-ferromagnetic
35 conductive material for the fabrication of devices.

In some embodiments, fabrication of lines includes the use of pitch division to achieve the finely pitched arrangement for FM and non-ferromagnetic conductive material. A tight pitch that is not achievable directly through conventional lithography is achieved using pitch division. In an example, a pattern based on conventional lithography may first be formed. The pitch may then be halved (which may be referred to as pitch halving) by the use of spacer mask patterning, as is known in the art. Further, the original pitch may then be quartered (which may be referred to as pitch quartering) by a second round of spacer mask patterning, and so on. In this manner, patterns may be fabricated to provide laterally adjacent lines spaced at a constant pitch and having a constant width.

In some embodiments, ferromagnetic material comprises a material selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), and Gadolinium (Gd). In some embodiments, the ferromagnetic material comprises a Heusler alloy of the form X_2YZ or XYZ where X, Y, and Z are elements selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), Aluminum (Al), Germanium (Ge), Gallium (Ga), Gadolinium (Gd), and Manganese (Mn).

In some embodiments, the result of the enhanced materials processing includes finely pitched and laterally adjacent FM and MOS material lines placed as required within a hard mask (HM) layer and interlayer dielectric (ILD) of a wafer. In some embodiments, the finely pitched lines are utilized in the fabrication of for magneto-electric spin orbit (MESO) devices and connected devices, including connected CMOS transistors for clocking or power of logic devices.

Figure 1A through 1P are illustrations of an improved process for fabrication of fine pitch ferromagnetic and metal microelectronics for improved spin logic devices according to an embodiment. In some embodiments, a fabrication process includes:

Figure 1A – Backbone Lithography: Fabricate or obtain a microelectronics wafer including a first antireflective coating (ARC) 112, a first backbone layer (Backbone-1) 110, a spacer cap 108 (such as titanium oxide, TiO), a second backbone layer (Backbone-2) 106, a first hard mask layer (HM1) 104, and an interlayer dielectric (ILD) layer 102.

Further, apply lithographic masking 114 to the first ARC 112 of the wafer 100, and apply an etching process to etch through the non-masked portions of the Backbone-1 110.

Figure 1B – Tri-layer Etching: Perform tri-layer etch, etching through the non-masked portions of the first antireflective coating 112 and first backbone layer 110, thus creating first set of pillars 113.

Figure 1C – Si-ARC Removal: The antireflective coating 112 is removed from the first backbone layer 110 of the first set of pillars 113.

Figure 1D – Spacer Deposition: A first spacer material (Spacer1) 114 is deposited on the surface of the wafer 100 over the first backbone layer 110 and spacer cap 108.

Figure 1E – Spacer Etching (D1D) Plus Ash: Etching and plasma ash processing is performed to form the first set of spacers 115.

5 Figure 1F – TiO/SILT Etch: Etching of the titanium oxide (TiO) spacer cap 108 and of the second backbone layer 106, exposing the first hard mask layer (HM1) 104 and creating second set of pillars 117 comprising material of the spacer cap 108 and a second backbone layer 106.

10 Figure 1G – TiO Spacer Deposition: Apply second spacer layer (such as titanium oxide) 116 over the second backbone layer 106 and the first hard mask layer 104, resulting in a set of channels 119 on the wafer.

15 Figure 1H – Trench Plug Lithography: To exclude one or more areas of the wafer from generation of trenches for metal material, applying a second hard mask (HM2) layer 118 and a second antireflective coating 120, and applying a trench plug mask 122 one or more areas of the ARC 120 as needed for areas that will not require lines of metal material.

Figure 1I – Tri-layer Etching: Etching through the second antireflective coating 120 and second hard mask layer 118 is performed, resulting in the exposure of the channels 119 in unmasked areas, with the remaining ARC 120 above the remaining hard mask 118 in the masked areas.

20 Figure 1J – HM1/Comp Trench Etching: Trench etching is performed in the first set of channels 119 through the first hard mask layer 104 and partially through the interlayer dielectric layer 102 to form first set of trenches 125.

25 Figure 1K – Ash and Clean: Plasma ash processing and cleaning is performed to remove the second antireflective coating 120 and second hard mask 118. This may result in, for example, channel 126 within the titanium oxide layer 116.

Figure 1L – Ferromagnetic Material Deposition: Ferromagnetic material (FM) 128 is deposited over the layers of the wafer 100.

Figure 1M – Polishing: Polishing is performed, resulting in the alternating FM material 128 and second backbone layer material 106 in the titanium oxide layer 116 in the wafer 100.

30 Figure 1N – Backbone, HM, ILD Etch, and Ash: Etching of the second backbone layer 106, first hard mask layer 104, and interlayer dielectric 102 is performed, with ash processing, to result in alternating finely pitched FM material 128 and etched second set of trenches 130 through the titanium oxide layer 116, first hard mask layer 104, and interlayer dielectric 102.

35 Figure 1O – MOS Metal Fill: Non-ferromagnetic conductive material, which may include metal-oxide semiconductor (MOS) metal fill 132, is applied to fill the finely pitched

etched channels between the FM material 128 through the titanium oxide layer 116, first hard mask layer 104, and interlayer dielectric 102.

Figure 1P – Polishing of MOS Metal Fill of Wafer: The wafer 100 is polished, resulting in finely pitched FM material 128 and MOS metal 132 (or more generally non-ferromagnetic conductive material) lines, the lines being alternating and laterally adjacent, and being formed through the first hard mask layer 104 and interlayer dielectric 102.

In some embodiments, the resulting wafer with finely pitched FM material 128 and MOS metal 132 elements is utilized in fabrication of magneto-electric spin orbit logic devices and connected transistor devices, including devices illustrated in Figures 4, 5 and 6.

Figure 2 is an illustration of spin polarized current in a magneto-electric spin orbit device according to an embodiment. As illustrated in Figure 2, a MESO logic device 200 includes first nanomagnet 210 and second nanomagnet 220 connected by channel 230. In operation of the MESO logic device 200, spin polarized current 240 is conducted between the nanomagnets 210-220 to switch magnetization by the spin torque effect.

In such spintronic devices, the signal is sent from one node to the other as a spin quantity (spin polarized current, a domain wall, or a spin wave). These signals are slow (~1000 m/s (meters per second)) and, more importantly, the signals exponentially attenuate over the length of ~1 μm (micrometers). In an embodiment of a spintronic device, the signal is instead sent over an electrical interconnect. In such device, the charge current does not attenuate and the communication is much faster (as limited by the RC delay).

In prior art, current induced injection of spin current from a magnet is used as the charge-to-spin conversion; spin torque is used to switch magnetization in the output magnet; and the effect of magnetoresistance detected by a sense amplifier is used as the spin-charge conversion.

In some embodiments, the input nanomagnet injects a spin polarized current into the high spin-orbit coupling (SOC) material stack. The spin polarization is determined by the magnetization of the input magnet. The injection stack comprises an interface with a high density 2D electron gas and with high SOC such as Ag/Bi, or a bulk material with high Spin Hall Effect (SHE) coefficient such as Tantalum (Ta), Tungsten (W), or Platinum (Pt). There further may be a Silver or Copper spacer between the nanomagnet and the injection stack.

In some embodiments, the spin-orbit mechanism responsible for spin to charge conversion is described by the Rashba effect in two-dimensional (2D) electron gases. The Hamiltonian (energy) of spin-orbit coupling electrons in a 2D electron gas is provided in Equation [1].

$$H_R = \alpha_R (k \times \hat{z}) \cdot \sigma \quad [1]$$

Spin polarized electrons with direction of polarization in-plane (in the xy-plane) experience an effective magnetic field dependent on the spin direction, according to Equation [2].

$$\vec{B}(k) = \frac{\alpha_R}{\mu_B} (k \times \hat{z}) \quad [2]$$

5 This results in the generation of a charge current in the interconnect proportional to the spin current. The spin-orbit interaction, such as at a silver/bismuth (Ag/Bi) interface (the Inverse Rashba-Edelstein Effect (IREE)), produces a charge current in the horizontal direction according to Equation [3].

$$I_c = \frac{\lambda_{IREE} I_s}{w_m} \quad [3]$$

10 Alternatively, the Inverse Spin Hall Effect (ISHE) in metals such as tantalum (Ta), tungsten (W), or platinum (Pt) produces the horizontal charge current according to Equation [4].

$$I_c = \frac{\Theta_{SHE} t_{she} I_s}{2w_m} \quad [4]$$

Both IREE and ISHE effects produce spin to charge current conversion around 0.1 with existing materials at 10 nm magnet width. For scaled nanomagnets (e.g., 5 nm (nanometers) width) and exploratory SHE materials such as Bi₂Se₃, the spin to charge conversion efficiency can be between 1 and 2.5. The net conversion of the drive charge current to magnetization dependent charge current is provided by Equation [5], where P is the spin polarization.

$$I_c = \pm \frac{\lambda_{IREE} P I_d}{w_m} \text{ For IREE and } I_c = \pm \frac{\Theta_{SHE} t_{she} P I_d}{2w_m} \text{ for ISHE} \quad [5]$$

For this estimate the drive current and the signal charge current are set according to Equation [6].

$$I_c = I_d = 100 \mu A \quad [6]$$

Estimating the resistance of the ISHE interface to be equal to R = 100 Ω, then the induced voltage is according to Equation (7).

$$V_{ISHE} = 10 mV \quad [7]$$

25 In an embodiment, detection mechanism and charge to spin conversion is achieved as described below. The charge current, as carried by an interconnect, produces a voltage on the capacitor including magnetoelectric material dielectric (such as bismuth ferric oxide (BFO) or

Cr₂O₃) in contact with an output nanomagnet. The output nanomagnet serves as one of the plates of a capacitor. In one embodiment, magnetoelectric materials are either intrinsic multi-ferroics or composite multi-ferroic structures.

As the charge accumulates on the magnetoelectric capacitor, a strong magnetoelectric interaction causes the switching of magnetization in the output nanomagnet. Using the following parameters of the magnetoelectric capacitor: thickness $t_{ME} = 5$ nm, dielectric constant = 500, and area $A = 60$ nm x 20 nm, then the capacitance is as provided in Equation (8).

$$C = \frac{\epsilon\epsilon_0 A}{t_{ME}} \approx 1 \text{ fF} \quad [8]$$

Demonstrated values of the magnetoelectric coefficient are as provided in Equation [9], where the speed of light is c .

$$B_{ME} = \alpha_{ME} E = \frac{\alpha_{ME} V_{ISHE}}{t_{ME}} \sim 0.06 T \quad [9]$$

This translates to the effective magnetic field exerted on the nanomagnet as provided in Equation [10], which is a strong field sufficient to switch magnetization.

$$E_{sw} \sim 100 \text{ mV} * 100 \mu\text{A} * 1 \text{ ps} \sim 10 \text{ aJ} \quad [10]$$

The charge on the capacitor Q is provided in Equation [11], and the time to fully charge it to the induced voltage is provided Equation [12] (with the account of decreased voltage difference as the capacitor charges).

$$Q = 1 \text{ fF} * 10 \text{ mV} = 10 \text{ aC} \quad [11]$$

$$t_d = 10Q / I_d \sim 1 \text{ ps} \quad [12]$$

If the driving voltage is as provided in Equation [13], then the energy switch is as provided in Equation [14], which is comparable to the switching energy of CMOS transistors.

$$V_d = 100 \text{ mV} \quad [13]$$

$$E_{sw} \sim 100 \text{ mV} * 100 \mu\text{A} * 1 \text{ ps} \sim 10 \text{ aJ} \quad [14]$$

It is noted that the time to switch magnetization remains much longer than the charging time and is determined by the magnetization precession rate. The micromagnetic simulations predict this time to be as provided in Equation [15].

$$t_{sw} \sim 100 \text{ ps} \quad [15]$$

Figures 3A and 3B illustrate operation of a spin-orbit logic device as a logic inverter or repeater according to an embodiment. In some embodiments, the energy to regenerate the logic

signal is derived from the power supply driving the charge current during the injector operation.

Referring to Figure 3A, a logic repeater operation works by injection of a spin current from a magnet 302 of a device 300. For $-V_{dd}$ supply voltage applied to the magnet 302 (e.g., an injector nanomagnet), a spin current having a direction of magnetization in the same direction as the nanomagnet is injected into a spin orbit effect stack 304. The spin orbit effect produces a charge current proportional to the injected spin current in a channel 306. The injected charge current charges a magnetoelectric stack 308 (negative on the top plate) producing a large effective magnetic field on a magnet 310 and magnetization the same as the input magnet.

Referring to Figure 3B, a logic inverter operation of a device 350 works by injection of a spin current from an input magnet 360 with a $+V_{dd}$ supply voltage. The injected spin current in a spin orbit effect stack 352 produces a charge current in a channel 354. The injected charge current charges a magnetoelectric stack 356 with opposite sign of voltage (positive on top plate), producing a large effective magnetic field on a detector free layer or magnet 358 and the opposite magnetization to that on the input magnet.

Referring again to Figures 3A and 3B, the energy to regenerate the logic signal is derived from the power supply driving the charge current during the injector operation. In an embodiment, the logic repeater operation works by injection of a spin current from the input magnet. For $-V_{dd}$ supply voltage applied to the injector nanomagnet, a spin current polarized in the same direction as the nanomagnet is injected into the high spin-orbit coupling (SOC) region. The SOC effects produce a charge current proportional to the injected spin current. The injected charge current charges a magneto-electric stack producing a large effective magnetic field on the output magnet. In an embodiment, the logic inverter operation works by injection of a spin current from the injector magnet with a $+V_{dd}$ supply voltage. The injected charge current charges a magnetoelectric stack with opposite polarity, producing a large effective magnetic field on the detector free layer.

In some embodiments, an SOL device provides logic cascability and unidirectional signal propagation (i.e., input-output isolation), unidirectionality of logic and cascability being as described below. The unidirectional nature of logic is ensured due large difference in impedance for injection path versus detection path. The injector is essentially a metallic spin valve with spin to charge transduction with resistance area (RA) products of approximately $10 \text{ m}\Omega \cdot \mu\text{m}^2$. The detection path is a low leakage capacitance with RA products significantly greater than $1 \text{ M}\Omega \cdot \mu\text{m}^2$ in series with the resistance of the ferromagnetic (FM) capacitor plate with estimated resistance greater than 500 Ohms.

In some embodiments, CMOS transistors are integrated with MESO logic for power delivery and clocked power supply. The MESO device provides high integration density with

CMOS drive and control transistors. As an exemplary integration for a logic inverter stage, **Figure 4** is an illustration of CMOS integration of a spin orbit logic device according to an embodiment. It is noted that CMOS drivers can be incorporated as power supplies as well as to provide clocked power to control logic.

Referring to Figure 4, an apparatus 400 includes a transistor 402 including a gate electrode 404 and a junction region 406 (e.g., source region) and a junction region 408 (e.g., drain region). Also illustrated is a transistor 410 including a gate electrode 412, a junction region 414, and a junction region 416. A metal interconnect line 418 is connected to junction region 408 of transistor 402, and a metal interconnect line 420 (representatively at the same level as interconnect line 418) is connected to junction region 408 and junction region 416. An interconnect line 422 and an interconnect line 424 (each representatively at a different level than interconnect line 418 and interconnect line 420) are connected to junction region 406 and junction region 408, respectively to provide power and ground.

Figure 4 illustrates the incorporation of a spin orbit logic (SOL) device into apparatus 400. As shown, the device includes two magnets each with two landing regions. Junction region 408 includes a magnet 426 connected at one end to a magnetoelectric material 428 and at an opposite end to a spin orbit effect stack 430 (including a material that will exhibit a spin orbit effect in a metallic system (an IREE or spin Hall effect material)). Apparatus 400 also includes a magnet 432 connected at one end to a magnetoelectric material 434 and at an opposite end to a spin orbit effect stack 436. Interconnect line 418 is connected to magnetoelectric material 428 (to form a capacitor), and interconnect line 420 is connected to spin orbit effect stack 430 and to magnetoelectric material 434. In operation, a charge current introduced on interconnect line 418 switches a direction of magnetization of magnet 426 and injects a spin current in magnet 426 that is converted to a charge current in interconnect line 420 that switches a direction of magnetization of magnet 432.

In an embodiment, relatively high logic density is achieved using the integration scheme of the device with CMOS drivers for power supply and clocking as illustrated in Figure 4. In one embodiment, the density of integration of the devices exceeds that of CMOS since an inverter operation can be achieved within 2.5PX2M0. In one embodiment, since the power transistor can be shared among all the devices at the same clock phases, vertical integration can also be used to increase the logic density.

In an embodiment, majority gate operation is as described below. A charge mediated majority gate is based on the spin orbit coupling and magneto-electric switching. As an example, **Figure 5** illustrates a charge mediated majority gate according to an embodiment.

Referring to Figure 5, an apparatus 500 includes a transistor 502, a transistor 504, and a

transistor 506 as inputs, and a transistor 508 as an output. Transistor 502 includes gate electrode 510, a source region 512, and a drain region 514. Disposed in (deposited on or otherwise connected to) drain region is a magnet 516 connected at one end to a magnetoelectric material 518 and at another end to a spin orbit effect stack 520. Transistor 504 similarly includes a source region and drain region with the drain region including a magnet 522 coupled at one end to a magnetoelectric material 524 and at another end to a spin orbit effect stack 526. Transistor 506 similarly includes a source region and drain region with the drain region including a magnet 528 coupled at one end to a magnetoelectric material 530 and at another end to a spin orbit effect stack 532. Transistor 508 includes a gate electrode 534 and source and drain regions with the drain region including a magnet connected at one end to a spin orbit effect stack 536 and at another end to a magnetoelectric material 538.

An interconnect line 540 (shown as three separate lines) is connected to each of magnetoelectric material 518, magnetoelectric material 524, and magnetoelectric material 530 of transistor 502, transistor 504, and transistor 506, respectively. An interconnect line 542 is shown connected to spin orbit effect stack 520 of transistor 502 and to spin orbit effect stack 536. In one embodiment, interconnect line 540 and interconnect line 542 are on a same level. An interconnect line 544 is perpendicular to interconnect line 540 and, in one embodiment, on another level than interconnect line 540 and interconnect line 542. Interconnect line 544 is connected to each of the spin orbit effect stacks 520, 526, and 532 of respective transistors 502, 504, and 506 and to spin orbit effect stack 536 of transistor 508. In one embodiment, a charge current carries the information of the magnet beneath it (the charge current will have a direction of current flow depending on a magnet orientation that is representative of a logic state). In the embodiment of Figure 5, the charge current into each of transistor 502, 504, and 506 (I_{ch}) will produce a charge current (I_{ch1} , I_{ch2} , and I_{ch3} , respectively) that represents an input to the transistor 508. For a logic operation, each of I_{ch1} , I_{ch2} , and I_{ch3} is 0 or 1 and transistor 508 will receive the majority output of the input transistors (either 0 or 1 depending on whether there are more 0's than 1's among I_{ch1} , I_{ch2} , and I_{ch3}).

Referring again to Figure 5, the three input stages share a common power/clock region. As such, the power/clock gating transistor can be shared among the three inputs of the majority gate. The input stages can also be stacked vertically to improve the logic density. Accordingly, a charge mediated majority gate can be formed using SOL devices. The input devices share a power/clock zone and can share the same power/clock transistor.

In an embodiment, a magnetic state element is as described below. State elements can be essential for clocked logic operation for synchronous and asynchronous (event driven) computing. In one embodiment, the unique nature of spin orbit logic where the interconnect is

charge based provides the ability to create state machines using the CMOS transistors. As an example, **Figure 6** illustrates a table and an apparatus for a state machine using spin orbit logic with CMOS integration according to an embodiment.

Table 602 of Figure 6 illustrates a representative truth table for a state element operation. If a control is 1, an output either follows the control (1) or is the inverse of the control (0). If a control is 0, the output will not respond to the control but will hold its previous state.

Referring again to Figure 6, an assembly 604 includes SOL device 606 and SOL device 608. SOL device 606, in this embodiment, is a control logic. SOL device 606 includes a magnet 610 and a magnet 612. Deposited on a surface of magnet 610 at one end is a magnetoelectric material 614 and, at another end, a spin orbit effect stack 616. Deposited on a surface of magnet 612 at one end is a magnetoelectric material 618 and, at another end, a spin orbit effect stack 620. An interconnect or channel 622 is connected between spin orbit effect stack 616 of magnet 610 and magnetoelectric material 620 of magnet 612. Interconnect 624 is connected to magnetoelectric material 614 on magnet 610, and interconnect 626 is connected to spin orbit effect stack 618 on magnet 612. Representatively, an input current (I_c) on interconnect 624 produces a voltage on magnetoelectric material 614 to control magnet 610, and then drive current (spin current) in magnet 610 that is converted to a charge current or control current (I_{control}) in interconnect 622.

In one embodiment, SOL device 608 is a repeater. SOL device 608 includes a magnet 628 and a magnet 630. Deposited on a surface of magnet 628 at one end is a magnetoelectric material 632 and, at another end, a spin orbit effect stack 634. Deposited on a surface of magnet 630 at one end is a spin orbit effect stack 636 and, at another end, a magnetoelectric material 638. An interconnect or channel 640 is connected between spin orbit effect stack 634 of magnet 628 and magnetoelectric material 638 of magnet 630. An interconnect 642 is connected to magnetoelectric material 632 on magnet 628, and an interconnect 644 is connected to spin orbit effect stack 636 on magnet 630. When SOL device 608 power is ON (i.e., drive current is flowing), the device functions as a repeater representatively receiving an input current on interconnect 642 and a charge current is repeated on interconnect 644. Such input current produces a drive current (spin current) in magnet 628 that is converted to a charge current in interconnect 640 that controls the direction of magnetization of magnet 630. The power to turn SOL device 608 ON is controlled with SOL device 606. SOL device 606 is connected to SOL device 608 and will produce a charge signal to turn power to device 608 ON or OFF.

Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital

signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the art. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

Figures 7A and 7B illustrate a methodology for fabrication of an apparatus including spin orbit logic devices according to an embodiment.

Referring to Figure 7A, in some embodiments a process 700 for fabrication of an apparatus includes:

702: Fabricate or obtain microelectronics wafer with multiple layers, wherein the layers include a first antireflective coating (ARC), a first backbone layer, a spacer cap (such as titanium oxide, TiO), a second backbone layer, a first hard mask layer, and an interlayer dielectric (ILD) layer.

704: Apply lithographic masking, and etch through non-masked layers through the first ARC and the first backbone layer to create first set of pillars comprising material of the first reflective layer and first backbone layer.

706: Remove the first antireflective coating from the first set of pillars.

708: Apply a first layer of spacer material to surface of the wafer.

710: Etch and process wafer to remove remaining first backbone and form a first set of spacers.

712: Utilizing the first set of spacers, etch spacer cap and second backbone to create second set of pillars comprising material of the spacer cap and second backbone layer.

714: Apply second layer of spacer material over the wafer.

716: Apply second hard mask layer and second ARC.

718: For areas of the wafer that will be not be etched and filled with FM or MOS metal material, apply trench plug mask.

720: Etch through second ARC and second hard mask to generate set of channels.

Referring to Figure 7B, in some embodiments a process 700 for fabrication of an apparatus further includes:

722: Trench etch through first hard mask layer and partially through the interlayer dielectric layer to form first set of trenches.

724: Process and clean to remove the second ARC and second hard mask.

726: Deposit FM material over the wafer, including depositing in the first set of trenches.

728: Polish surface of the wafer to provide in alternating FM material in the first set of trenches and second backbone material from the second set of pillars.

5 730: Etch through second backbone layer, first hard mask layer, and interlayer dielectric to form second set of trenches.

732: Apply non-magnetic metal material, such as metal material for connection of CMOS transistor elements, over the wafer, including filing of the second set of trenches.

10 734: Polish wafer to remove excess MOS metal material to generate alternating finely pitched lines of FM material and MOS metal material.

736: Fabrication of apparatus including MESO devices utilizing the finely pitched lines of FM material and MOS metal material.

Figure 8 is an illustration of a system on chip including spin orbit logic devices according to an embodiment. In this illustration, certain standard and well-known components that are not germane to the present description are not shown, and certain elements shown as
15 separate elements may be combined.

In some embodiments, the SoC 800 may further include, but is not limited to, the following:

(a) A central processing unit (CPU) or other processing element 810 for the processing
20 of data.

(b) A graphics processing unit (GPU) 820 to create images for output to a display.

(c) Memory 830, where memory may include random access memory (RAM) or other dynamic storage device or element as a main memory for storing information and instructions to be executed by the CPU 810 and the GPU 820. Main memory may include, but is not limited to,
25 dynamic random access memory (DRAM). Memory 830 may further include a non-volatile memory, such as flash memory, and a read only memory (ROM) or other static storage device for storing static information and instructions for the CPU 810 and GPU 820.

(d) A Northbridge 940 to handle communications between the CPU and other component of the SoC. In some embodiments, the SoC 800 may further include a Southbridge
30 850 to handle I/O functions.

(e) A transmitter, receiver, or both 860 for the transmission and reception of data via wireless communications, and one or more antennas for transmission or reception of wireless communication. Wireless communication includes, but is not limited to, Wi-Fi, Bluetooth™, near field communication, and other wireless communication standards. The one or more
35 antennas include one or more dipole, monopole, or other antennas.

(f) One or more interfaces 870, including USB (Universal Serial Bus), Firewire, Ethernet, or other interfaces.

(g) One or more active components 880, such as one or more transistors, wherein the transistors may include metal-oxide semiconductor devices.

5 In some embodiments, one or more components of the SoC 800, such as the CPU 810, GPU 820, and active components 880, include MESO devices in accordance with one or more embodiments described herein.

Figure 9 is an illustration of a computing system including spin logic devices according to an embodiment. In this illustration, certain standard and well-known components that are not
10 germane to the present description are not shown, and certain elements shown as separate elements may be combined.

In some embodiments, a computing system 900 may include a processing means such as one or more processors 910 coupled to one or more buses or interconnects, shown in general as bus 905. The processors 910 may comprise one or more physical processors and one or more
15 logical processors. In some embodiments, the processors may include one or more general-purpose processors or special-purpose processors.

The bus 905 is a communication means for transmission of data. The bus 905 is illustrated as a single bus for simplicity, but may represent multiple different interconnects or buses and the component connections to such interconnects or buses may vary. The bus 905
20 shown in Figure 9 is an abstraction that represents any one or more separate physical buses, point-to-point connections, or both connected by appropriate bridges, adapters, or controllers.

In some embodiments, the computing system 900 further comprises a random access memory (RAM) or other dynamic storage device or element as a main memory 915 for storing information and instructions to be executed by the processors 910. Main memory 915 may
25 include, but is not limited to, dynamic random access memory (DRAM). In some embodiments, the main memory 915 includes one or more memory devices having multiple memory dies, including stacked memory, the memory dies including multiple partitions.

The computing system 900 also may comprise a non-volatile memory 920; a storage device such as a solid-state drive (SSD) 930; and a read only memory (ROM) 935 or other static
30 storage device for storing static information and instructions for the processors 910.

In some embodiments, the computing system 900 includes one or more transmitters or receivers 940 coupled to the bus 905. In some embodiments, the computing system 900 may include one or more antennae 944, such as dipole or monopole antennae, for the transmission and reception of data via wireless communication using a wireless transmitter, receiver, or both,
35 and one or more ports 942 for the transmission and reception of data via wired communications.

Wireless communication includes, but is not limited to, Wi-Fi, Bluetooth™, near field communication, and other wireless communication standards.

In some embodiments, computing system 900 includes one or more input devices 950 for the input of data, including hard and soft buttons, a mouse or other pointing device, a keyboard, voice command system, or gesture recognition system.

In some embodiments, computing system 900 includes an output display 955, where the output display 955 may include a liquid crystal display (LCD), projection device, or any other display technology, for displaying information or content to a user. In some environments, the output display 955 may include a touch-screen that is also utilized as at least a part of an input device 950. Output display 955 may further include audio output, including one or more speakers, audio output jacks, or other audio, and other output to the user.

The computing system 900 may also comprise a battery or other power source 960, which may include a solar cell, a fuel cell, a charged capacitor, near field inductive coupling, or other system or device for providing or generating power in the computing system 900. The power provided by the power source 960 may be distributed as required to elements of the computing system 900.

In some embodiments, one or more components of the computing system 900, such as the processors 910, include MESO devices in accordance with one or more embodiments described herein.

In various implementations, the computing system 900 may be a laptop, a netbook, a notebook, an Ultrabook™, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing system 900 may be any other electronic device that processes data.

In some embodiments, an apparatus includes a first transistor and a second transistor, each including a gate electrode, a first junction region, and a second junction region; a plurality of lines including alternating ferromagnetic material lines and non-magnetic metal interconnect lines fabricated in a wafer, the plurality of lines including a metal interconnect line to provide connections for the junction regions of the first and second transistors, including connections to provide power and control; and a magneto-electric spin orbital (MESO) device including a first magnet and a second magnet, the plurality of lines including ferromagnetic material lines for fabrication of the MESO device magnets; wherein ferromagnetic material lines are contained in a first set of trenches and the non-magnetic material lines are contained in a second set of trenches, the first and second set of trenches being formed through a hard mask layer and partially through

an interlayer dielectric (ILD) layer of the wafer.

In some embodiments, the apparatus further includes an area excluding the alternating ferromagnetic material lines and non-magnetic metal interconnect lines.

5 In some embodiments, the non-magnetic metal material is a material selected from the group consisting of silver (Ag), aluminum (Al), gold (Au) and copper (Cu), and forming a material that exhibits a spin orbit effect, with an interface between the non-magnetic metal material and material that exhibits the spin orbit effect.

In some embodiments, the ferromagnetic material comprises a material selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), and Gadolinium (Gd).

10 In some embodiments, the ferromagnetic material comprises a Heusler alloy of the form X_2YZ or XYZ where X, Y, and Z are elements selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), Aluminum (Al), Germanium (Ge), Gallium (Ga), Gadolinium (Gd), and Manganese (Mn).

15 In some embodiments, a method of fabricating a microelectronic device includes applying lithographic masking to a wafer, the wafer including a plurality of layers, the plurality of layers including a first antireflective coating, a first backbone material layer, a spacer cap, a second backbone material layer, a first hard mask layer, and an interlayer dielectric (ILD) layer; performing a first etching of the wafer to generate a first set of pillars; applying a first layer of spacer material to the wafer; performing a second etching of the wafer to form a first set of
20 spacers from the first layer of spacer material; performing a third etching of the wafer to generate a second set of pillars; applying a second layer of spacer material to the wafer to generate a set of channels on the wafer; performing a first trench etching in the set of channels to form a first set of trenches; depositing ferromagnetic material on the wafer, including depositing ferromagnetic material in the first set of trenches; performing a second trench etching to form a second set of
25 trenches, the trenches of the second set of trenches alternating between the trenches of the first set of trenches; depositing non-magnetic metal material on the wafer, including depositing the MOS metal material in the second set of trenches; and polishing the wafer following deposition of the non-magnetic metal material to form alternating lines of ferromagnetic metal material and non-magnetic metal material.

30 In some embodiments, the method further includes forming an apparatus utilizing the alternating lines of ferromagnetic metal material and non-magnetic metal material, including forming interconnects to a transistor utilizing the lines of non-magnetic metal material and forming a spin logic device utilizing the lines of ferromagnetic material.

35 In some embodiments, the method further includes applying a second hard mask layer and a second antireflective layer to the wafer following application of the second set of spacer

material to the wafer; applying a trench plug mask to a first area of the wafer; and performing a fourth etching of the wafer to generate a set of channels, the set of channels excluding the first area of the wafer.

In some embodiments, the non-magnetic metal material includes metal for a metal-oxide semiconductor (MOS) transistor.

In some embodiments, the spacer cap comprises titanium oxide.

In some embodiments, the non-magnetic metal material is a material selected from the group consisting of silver (Ag), aluminum (Al), gold (Au), and copper (Cu), and the method further includes forming a material that exhibits a spin orbit effect, with an interface between the non-magnetic metal material and material that exhibits the spin orbit effect.

In some embodiments, the ferromagnetic material comprises a material selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), and Gadolinium (Gd).

In some embodiments, the ferromagnetic material comprises a Huesler alloy of the form X_2YZ or XYZ where X, Y, and Z are elements selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), Aluminum (Al), Germanium (Ge), Gallium (Ga), Gadolinium (Gd), and Manganese (Mn).

In some embodiments, a microelectronic device is fabricated by a process including applying lithographic masking to a wafer including a plurality of layers, the plurality of layers including a first antireflective coating, a first backbone material layer, a spacer cap, a second backbone material layer, a first hard mask layer, and an interlayer dielectric (ILD) layer; performing a first etching of the wafer to generate a first set of pillars; applying a first layer of spacer material to the wafer; performing a second etching of the wafer to form a first set of spacers from the first layer of spacer material; performing a third etching of the wafer to generate a second set of pillars; applying a second set of spacer material to the wafer to generate a set of channels on the wafer; performing a first trench etching in the set of channels to form a first set of trenches; depositing ferromagnetic material on the wafer, including depositing ferromagnetic material in the first set of trenches; performing a second trench etching to form a second set of trenches, the trenches of the second set of trenches alternating between the trenches of the first set of trenches; depositing non-magnetic metal material on the wafer, including depositing the MOS metal material in the second set of trenches; and polishing the wafer following deposition of the non-magnetic metal material to form alternating lines of ferromagnetic metal material and non-magnetic metal material.

In some embodiments, the process further includes forming interconnects to one or more transistors utilizing the lines of non-magnetic metal material.

In some embodiments, the microelectronic device forms a spin logic device utilizing the

lines of ferromagnetic material.

In some embodiments, the process further includes applying a second hard mask layer and a second antireflective layer to the wafer following application of the second set of spacer material to the wafer; applying a trench plug mask to a first area of the wafer; and performing a fourth etching of the wafer to generate a set of channels, the set of channels excluding the first area of the wafer.

In some embodiments, the non-magnetic metal material includes metals for a metal-oxide semiconductor (MOS) transistor.

In some embodiments, the spacer cap comprises titanium oxide.

In some embodiments, the non-magnetic metal material is a material selected from the group consisting of silver (Ag), aluminum (Al), gold (Au) and copper (Cu), and forming a material that exhibits a spin orbit effect, with an interface between the non-magnetic metal material and material that exhibits the spin orbit effect.

In some embodiments, the ferromagnetic material comprises a material selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), and Gadolinium (Gd).

In some embodiments, the ferromagnetic material comprises a Heusler alloy of the form X_2YZ or XYZ where X, Y, and Z are elements selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), Aluminum (Al), Germanium (Ge), Gallium (Ga), Gadolinium (Gd), and Manganese (Mn).

In the description above, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the described embodiments. It will be apparent, however, to one skilled in the art that embodiments may be practiced without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form. There may be intermediate structure between illustrated components. The components described or illustrated herein may have additional inputs or outputs that are not illustrated or described.

Various embodiments may include various processes. These processes may be performed by hardware components or may be embodied in computer program or machine-executable instructions, which may be used to cause a general-purpose or special-purpose processor or logic circuits programmed with the instructions to perform the processes. Alternatively, the processes may be performed by a combination of hardware and software.

Portions of various embodiments may be provided as a computer program product, which may include a computer-readable medium having stored thereon computer program instructions, which may be used to program a computer (or other electronic devices) for execution by one or more processors to perform a process according to certain embodiments.

The computer-readable medium may include, but is not limited to, magnetic disks, optical disks, read-only memory (ROM), random access memory (RAM), erasable programmable read-only memory (EPROM), electrically-erasable programmable read-only memory (EEPROM), magnetic or optical cards, flash memory, or other type of computer-readable medium suitable for storing electronic instructions. Moreover, embodiments may also be downloaded as a computer program product, wherein the program may be transferred from a remote computer to a requesting computer.

Many of the methods are described in their most basic form, but processes can be added to or deleted from any of the methods and information can be added or subtracted from any of the described messages without departing from the basic scope of the present embodiments. It will be apparent to those skilled in the art that many further modifications and adaptations can be made. The particular embodiments are not provided to limit the concept but to illustrate it. The scope of the embodiments is not to be determined by the specific examples provided above but only by the claims below.

If it is said that an element “A” is coupled to or with element “B,” element A may be directly coupled to element B or be indirectly coupled through, for example, element C. When the specification or claims state that a component, feature, structure, process, or characteristic A “causes” a component, feature, structure, process, or characteristic B, it means that “A” is at least a partial cause of “B” but that there may also be at least one other component, feature, structure, process, or characteristic that assists in causing “B.” If the specification indicates that a component, feature, structure, process, or characteristic “may”, “might”, or “could” be included, that particular component, feature, structure, process, or characteristic is not required to be included. If the specification or claim refers to “a” or “an” element, this does not mean there is only one of the described elements.

An embodiment is an implementation or example. Reference in the specification to “an embodiment,” “one embodiment,” “some embodiments,” or “other embodiments” means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of “an embodiment,” “one embodiment,” or “some embodiments” are not necessarily all referring to the same embodiments. It should be appreciated that in the foregoing description of exemplary embodiments, various features are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of one or more of the various novel aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed embodiments requires more features than are expressly recited in each claim. Rather, as the

following claims reflect, novel aspects lie in less than all features of a single foregoing disclosed embodiment. Thus, the claims are hereby expressly incorporated into this description, with each claim standing on its own as a separate embodiment.

CLAIMS

What is claimed is:

1. An apparatus comprising:
a first transistor and a second transistor, each including a gate electrode, a first junction
5 region, and a second junction region;
a plurality of lines including alternating ferromagnetic material lines and non-magnetic
metal interconnect lines fabricated in a wafer, the plurality of lines including a metal
interconnect line to provide connections for the junction regions of the first and second
transistors, including connections to provide power and control; and
10 a magneto-electric spin orbital (MESO) device including a first magnet and a second
magnet, the plurality of lines including ferromagnetic material lines for fabrication of the MESO
device magnets;
wherein ferromagnetic material lines are contained in a first set of trenches and the non-
magnetic material lines are contained in a second set of trenches, the first and second set of
15 trenches being formed through a hard mask layer and partially through an interlayer dielectric
(ILD) layer of the wafer.
2. The apparatus of claim 1, further comprising an area excluding the alternating
ferromagnetic material lines and non-magnetic metal interconnect lines.
3. The apparatus of claim 1, wherein the non-magnetic metal material is a material selected
20 from the group consisting of silver (Ag), aluminum (Al), gold (Au) and copper (Cu), and
forming a material that exhibits a spin orbit effect, with an interface between the non-magnetic
metal material and material that exhibits the spin orbit effect.
4. The apparatus of claim 1, wherein the ferromagnetic material comprises a material
selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), and Gadolinium (Gd).
- 25 5. The apparatus of claim 1, wherein the ferromagnetic material comprises a Heusler alloy
of the form X_2YZ or XYZ where X, Y, and Z are elements selected from the group consisting of
Cobalt (Co), Iron (Fe), Nickel (Ni), Aluminum (Al), Germanium (Ge), Gallium (Ga),
Gadolinium (Gd), and Manganese (Mn).
6. A method of fabricating a microelectronic device, the method comprising:
30 applying lithographic masking to a wafer, the wafer including a plurality of layers, the
plurality of layers including a first antireflective coating, a first backbone material layer, a spacer

cap, a second backbone material layer, a first hard mask layer, and an interlayer dielectric (ILD) layer;

performing a first etching of the wafer to generate a first set of pillars;

applying a first layer of spacer material to the wafer;

5 performing a second etching of the wafer to form a first set of spacers from the first layer of spacer material;

performing a third etching of the wafer to generate a second set of pillars;

applying a second layer of spacer material to the wafer to generate a set of channels on the wafer;

10 performing a first trench etching in the set of channels to form a first set of trenches;

depositing ferromagnetic material on the wafer, including depositing ferromagnetic material in the first set of trenches;

performing a second trench etching to form a second set of trenches, the trenches of the second set of trenches alternating between the trenches of the first set of trenches;

15 depositing non-magnetic metal material on the wafer, including depositing the MOS metal material in the second set of trenches; and

polishing the wafer following deposition of the non-magnetic metal material to form alternating lines of ferromagnetic metal material and non-magnetic metal material.

7. The method of claim 6, further comprising forming an apparatus utilizing the alternating
20 lines of ferromagnetic metal material and non-magnetic metal material, including forming interconnects to a transistor utilizing the lines of non-magnetic metal material and forming a spin logic device utilizing the lines of ferromagnetic material.

8. The method of claim 6, further comprising:

25 applying a second hard mask layer and a second antireflective layer to the wafer following application of the second set of spacer material to the wafer;

applying a trench plug mask to a first area of the wafer; and

performing a fourth etching of the wafer to generate a set of channels, the set of channels excluding the first area of the wafer.

9. The method of claim 6, wherein the non-magnetic metal material includes metal for a
30 metal-oxide semiconductor (MOS) transistor.

10. The method of claim 6, wherein the spacer cap comprises titanium oxide.

11. The method of claim 6, wherein the non-magnetic metal material is a material selected

from the group consisting of silver (Ag), aluminum (Al), gold (Au) and copper (Cu), and forming a material that exhibits a spin orbit effect, with an interface between the non-magnetic metal material and material that exhibits the spin orbit effect.

12. The method of claim 6, wherein the ferromagnetic material comprises a material selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), and Gadolinium (Gd).

13. The method of claim 6, wherein the ferromagnetic material comprises a Huesler alloy of the form X_2YZ or XYZ where X, Y, and Z are elements selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), Aluminum (Al), Germanium (Ge), Gallium (Ga), Gadolinium (Gd), and Manganese (Mn).

14. A microelectronic device fabricated by a process comprising:
applying lithographic masking to a wafer including a plurality of layers, the plurality of layers including a first antireflective coating, a first backbone material layer, a spacer cap, a second backbone material layer, a first hard mask layer, and an interlayer dielectric (ILD) layer;
performing a first etching of the wafer to generate a first set of pillars;
applying a first layer of spacer material to the wafer;
performing a second etching of the wafer to form a first set of spacers from the first layer of spacer material;
performing a third etching of the wafer to generate a second set of pillars;
applying a second set of spacer material to the wafer to generate a set of channels on the wafer;
performing a first trench etching in the set of channels to form a first set of trenches;
depositing ferromagnetic material on the wafer, including depositing ferromagnetic material in the first set of trenches;
performing a second trench etching to form a second set of trenches, the trenches of the second set of trenches alternating between the trenches of the first set of trenches;
depositing non-magnetic metal material on the wafer, including depositing the MOS metal material in the second set of trenches; and
polishing the wafer following deposition of the non-magnetic metal material to form alternating lines of ferromagnetic metal material and non-magnetic metal material.

15. The microelectronic device of claim 14, wherein the process further comprises:
forming interconnects to one or more transistors utilizing the lines of non-magnetic metal material.

16. The microelectronic device of claim 14, wherein the process further comprises:
forming a spin logic device utilizing the lines of ferromagnetic material.
17. The microelectronic device of claim 14, wherein the process further comprises:
applying a second hard mask layer and a second antireflective layer to the wafer
5 following application of the second set of spacer material to the wafer;
applying a trench plug mask to a first area of the wafer; and
performing a fourth etching of the wafer to generate a set of channels, the set of channels
excluding the first area of the wafer.
18. The microelectronic device of claim 14, wherein the non-magnetic metal material
10 includes metal for a metal-oxide semiconductor (MOS) transistor.
19. The microelectronic device of claim 14, wherein the spacer cap comprises titanium
oxide.
20. The microelectronic device of claim 14, wherein the non-magnetic metal material is a
material selected from the group consisting of silver (Ag), aluminum (Al), gold (Au) and copper
15 (Cu), and forming a material that exhibits a spin orbit effect, with an interface between the non-
magnetic metal material and material that exhibits the spin orbit effect.
21. The microelectronic device of claim 14, wherein the ferromagnetic material comprises a
material selected from the group consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), and
Gadolinium (Gd).
- 20 22. The microelectronic device of claim 14, wherein the ferromagnetic material comprises a
Heusler alloy of the form X_2YZ or XYZ where X, Y, and Z are elements selected from the group
consisting of Cobalt (Co), Iron (Fe), Nickel (Ni), Aluminum (Al), Germanium (Ge), Gallium
(Ga), Gadolinium (Gd), and Manganese (Mn).

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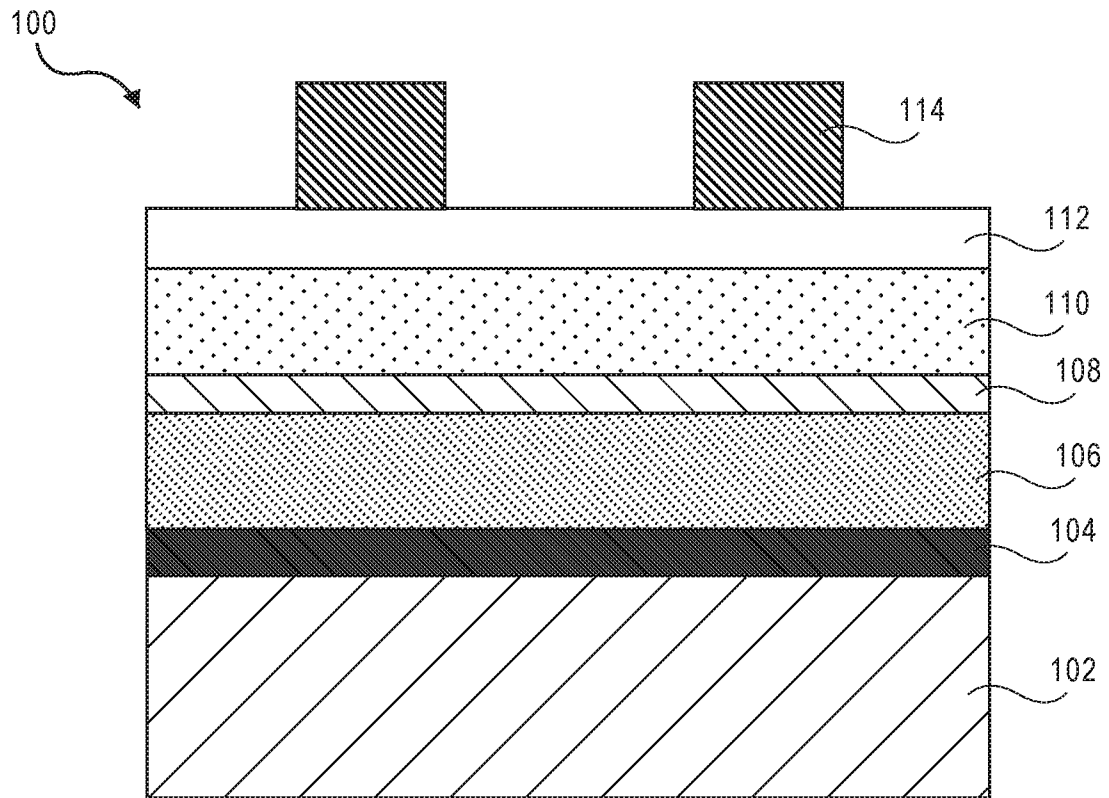


FIG. 1A

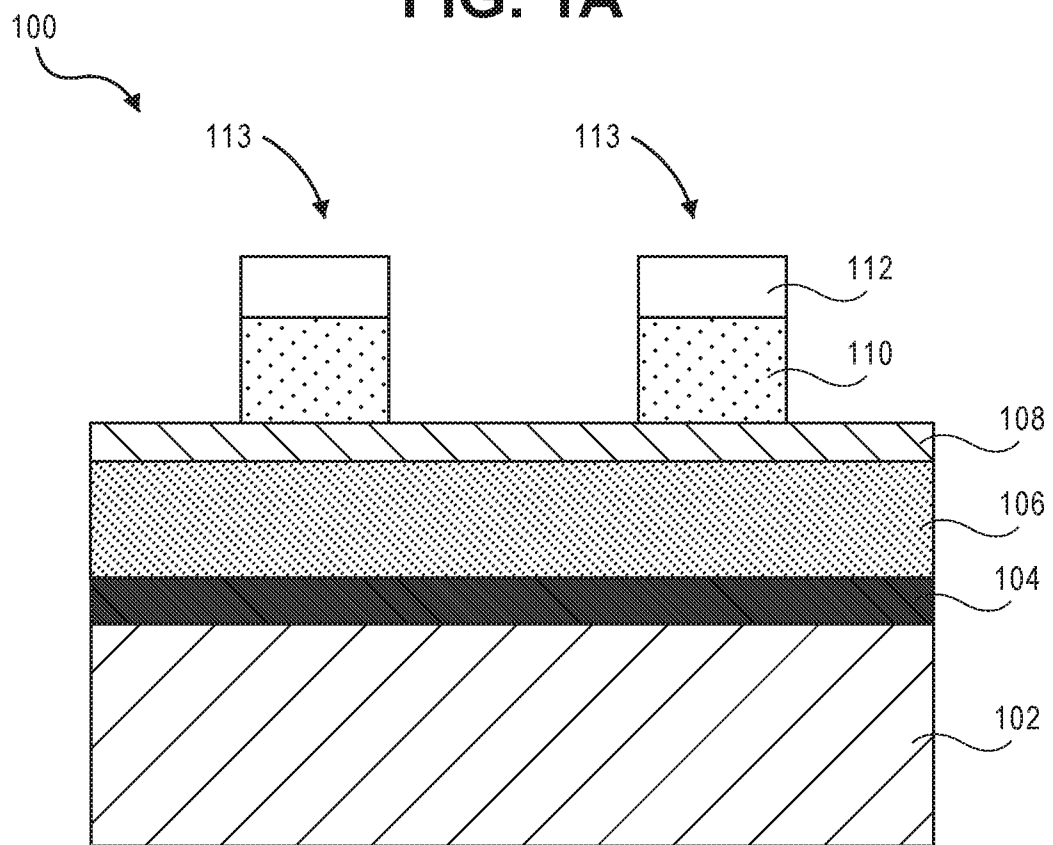


FIG. 1B

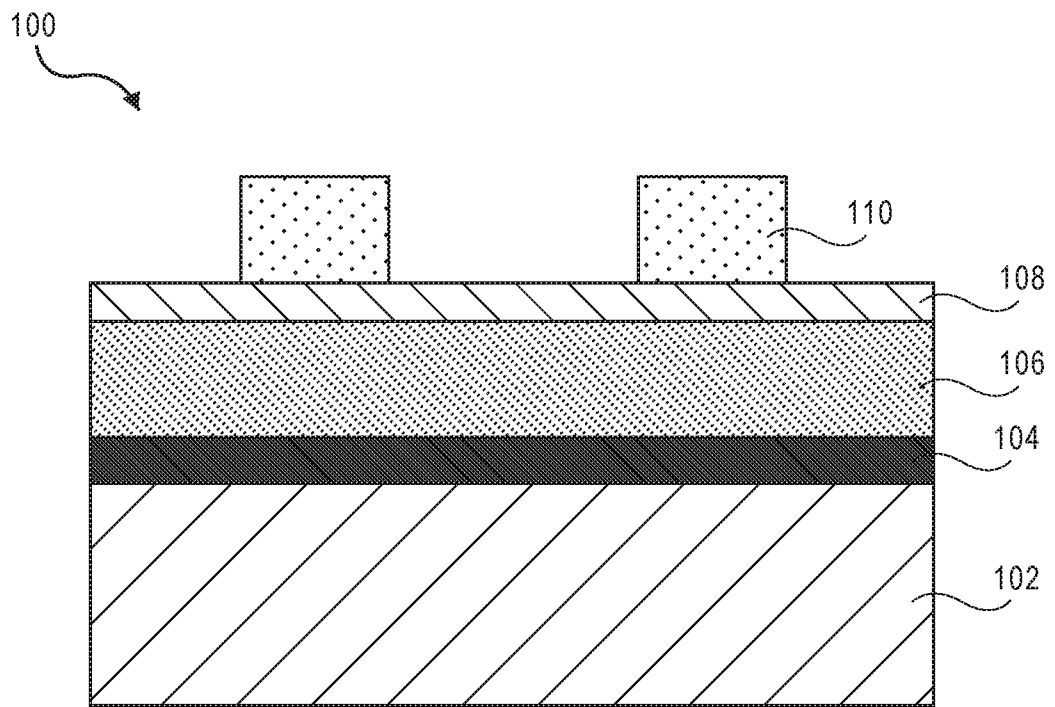


FIG. 1C

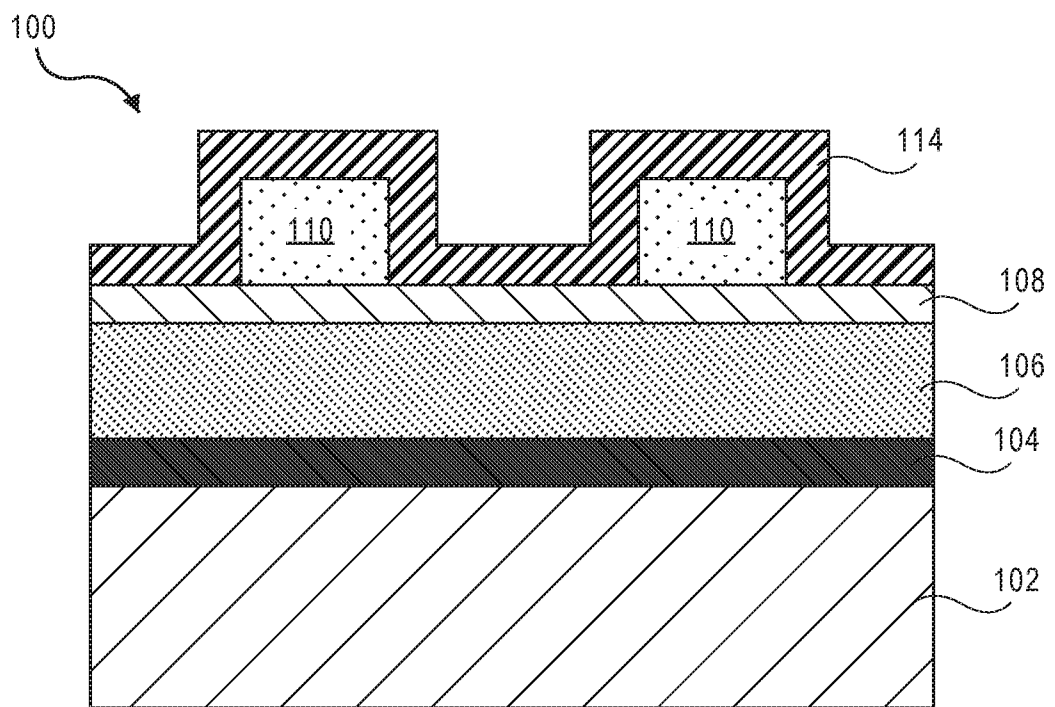


FIG. 1D

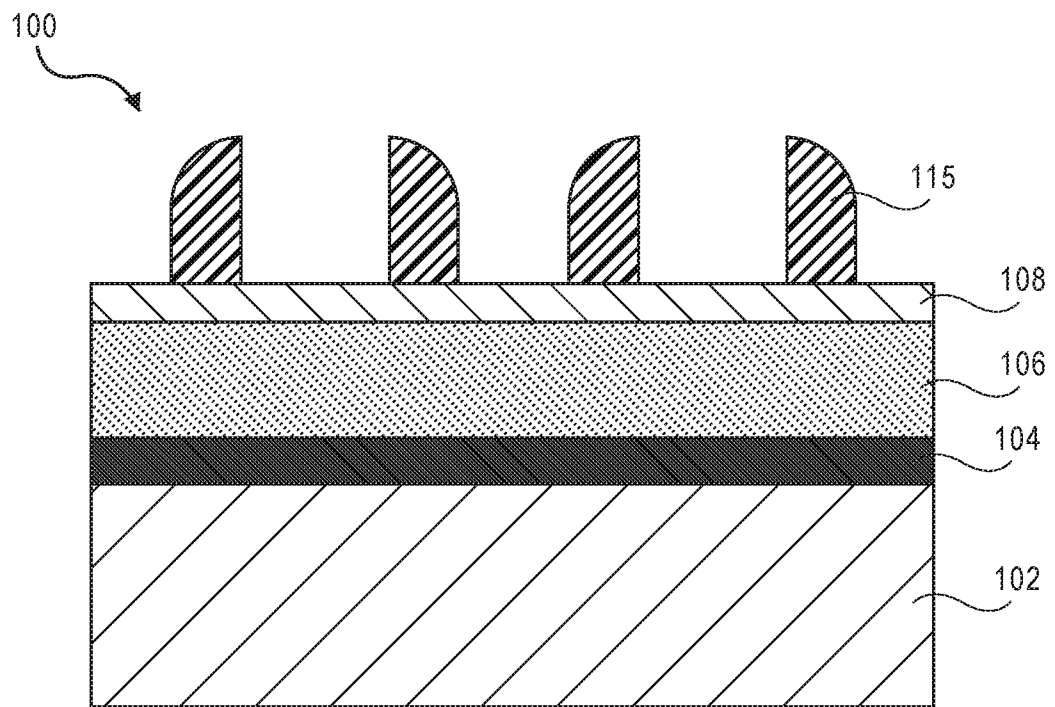


FIG. 1E

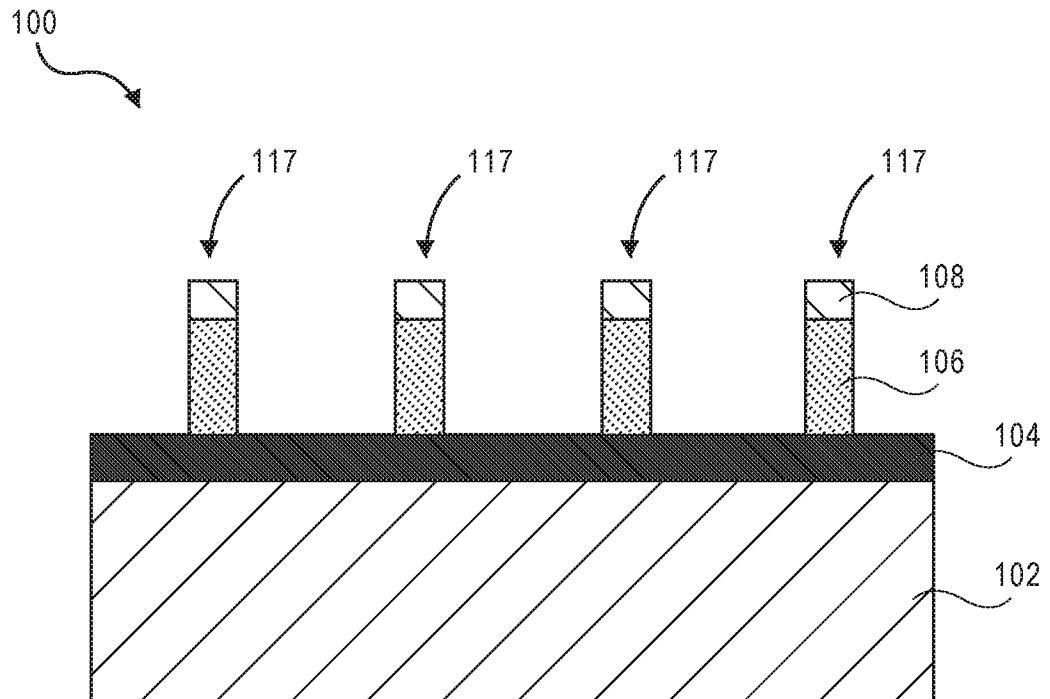


FIG. 1F

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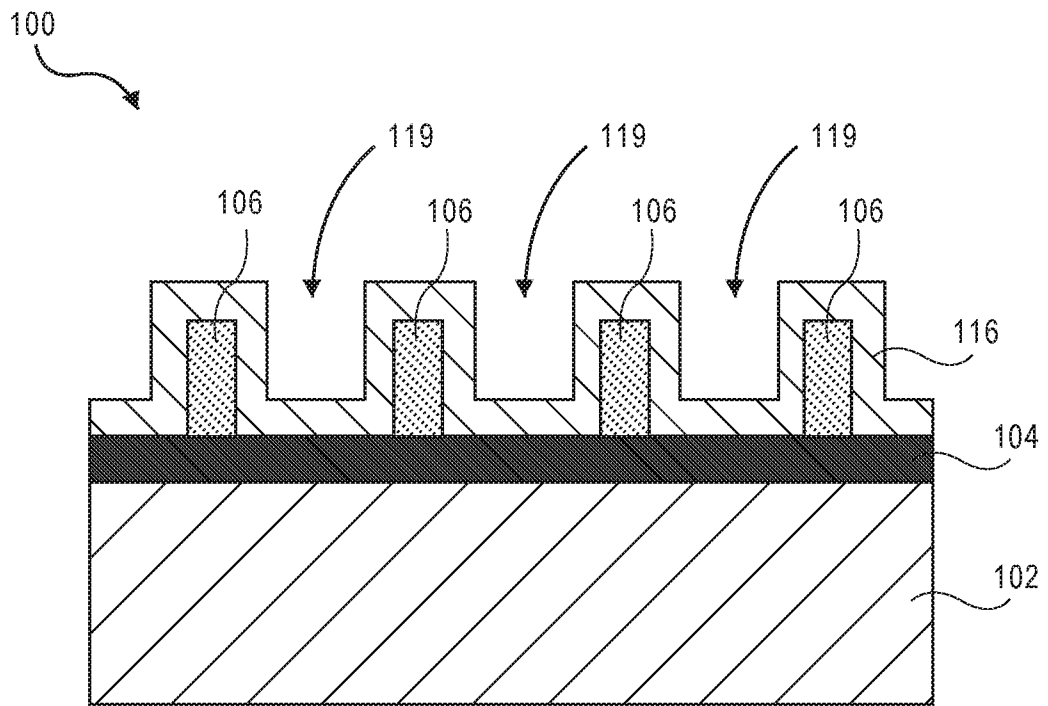


FIG. 1G

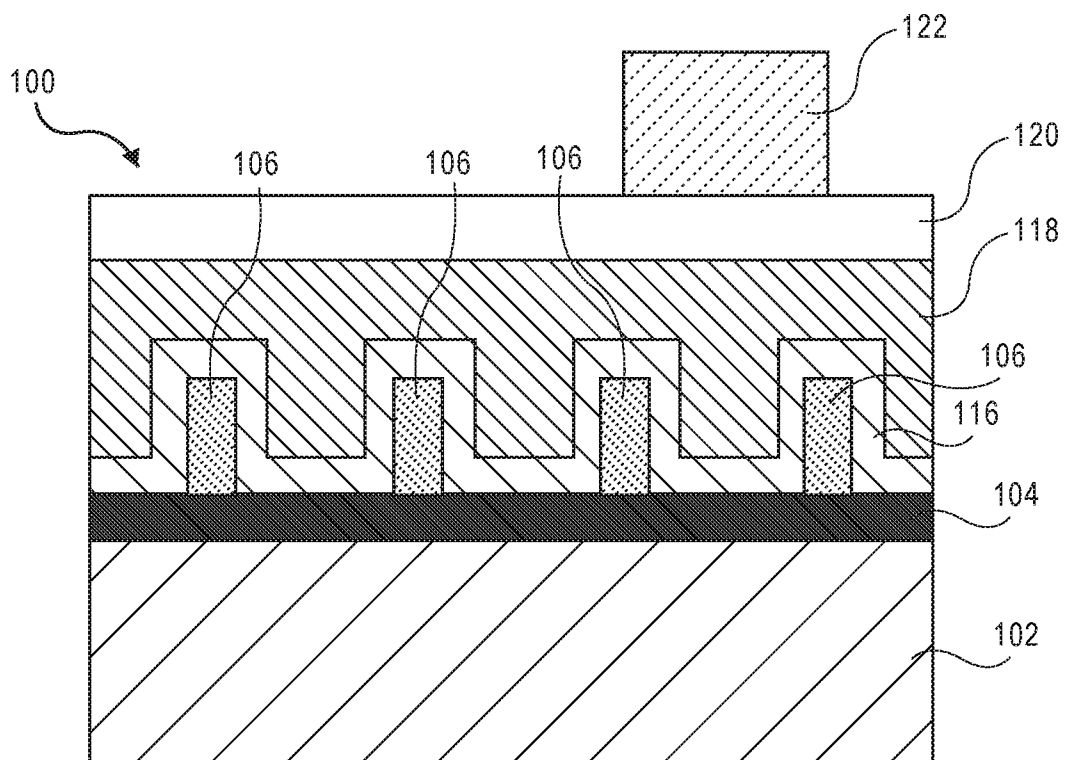


FIG. 1H

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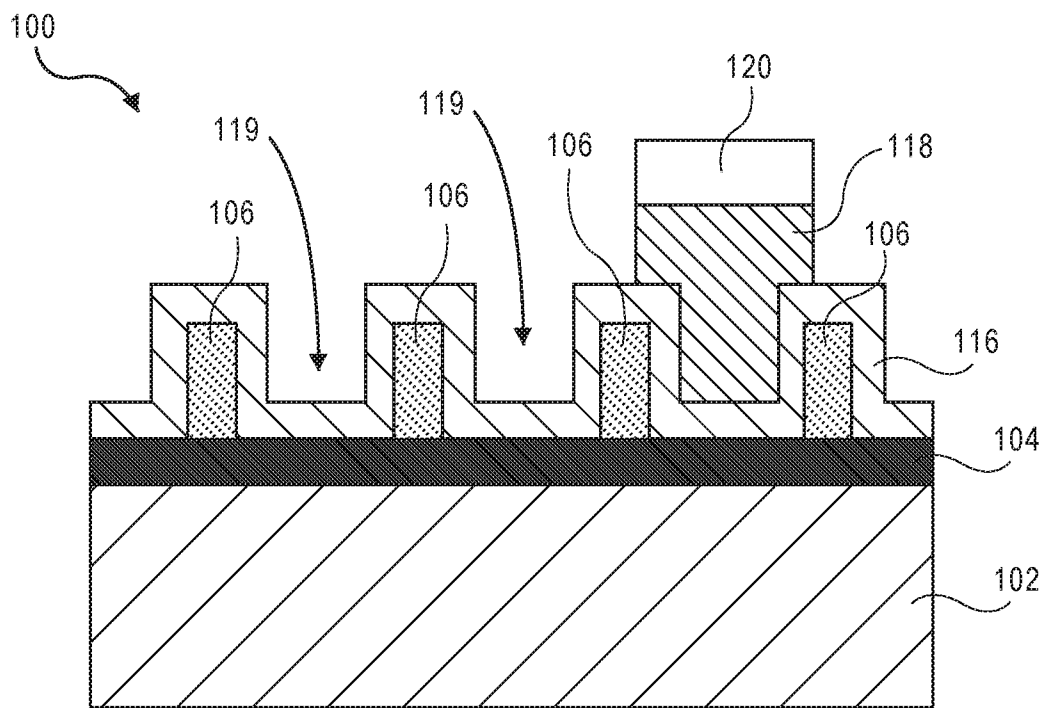


FIG. 1I

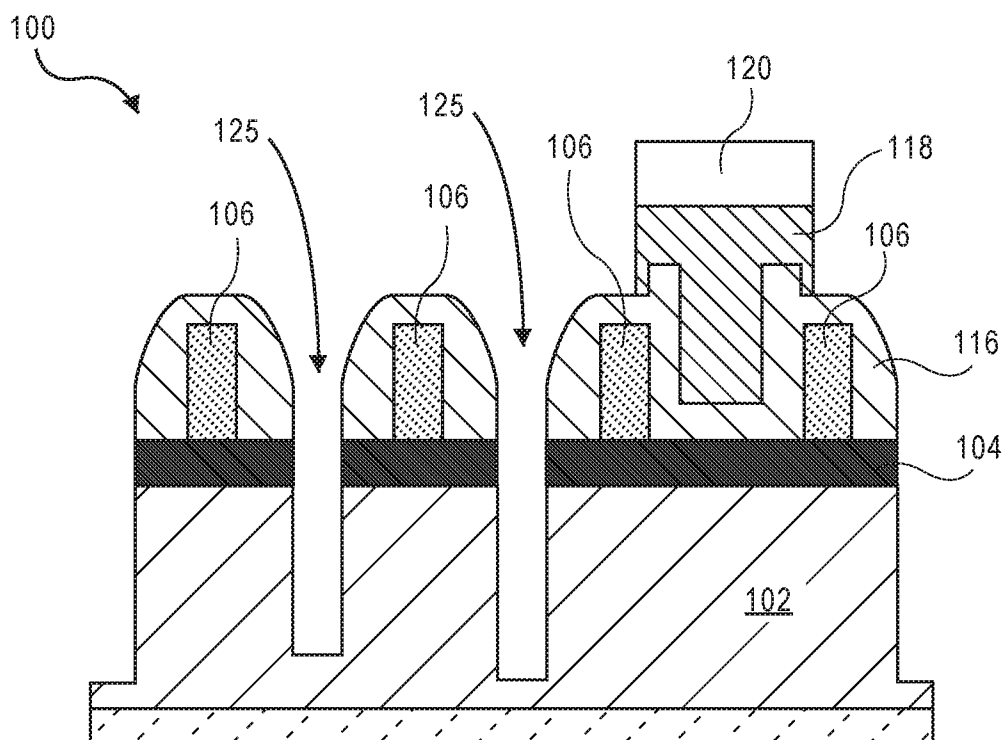


FIG. 1J

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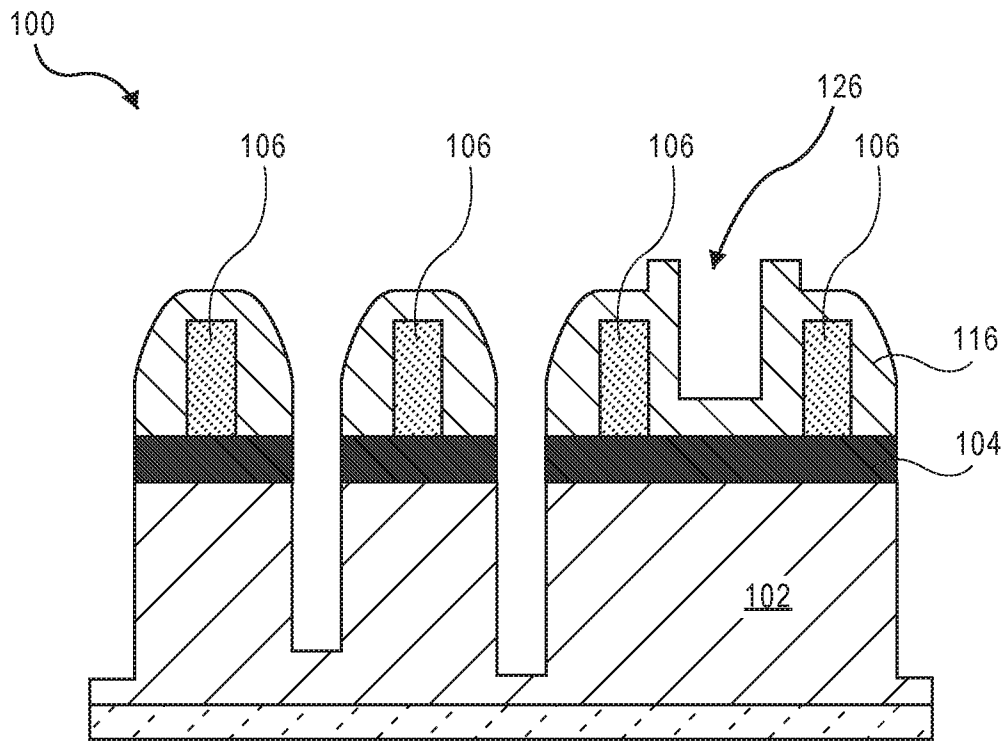


FIG. 1K

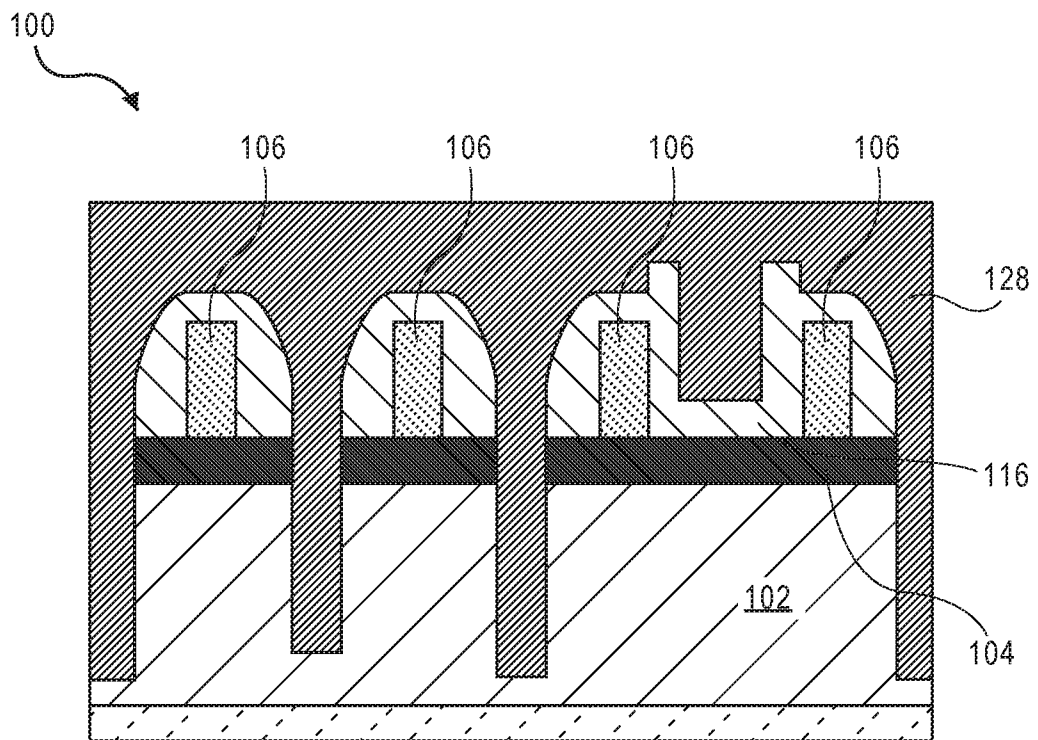


FIG. 1L

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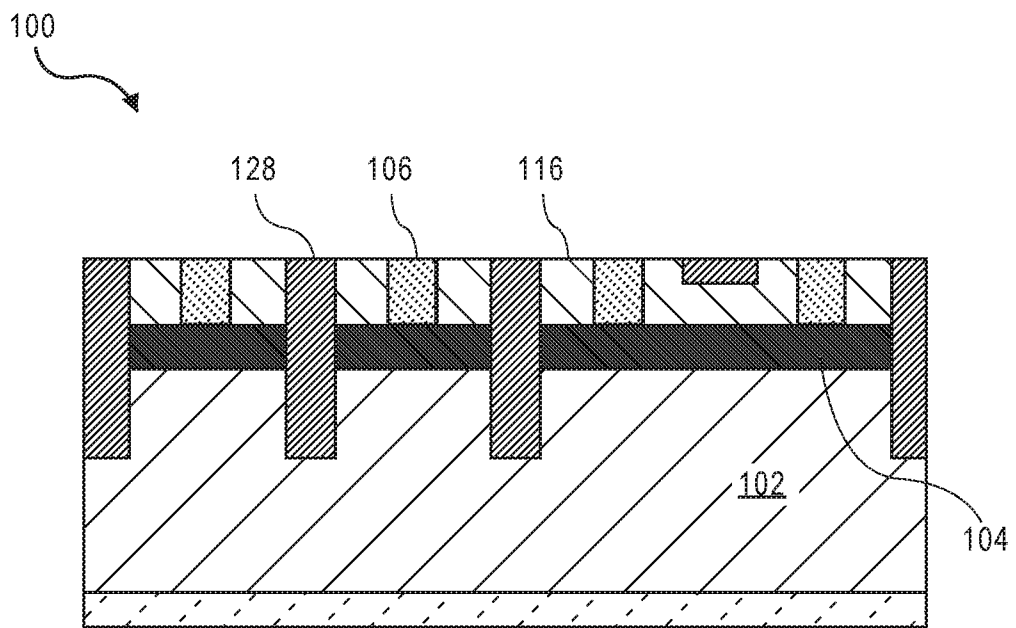


FIG. 1M

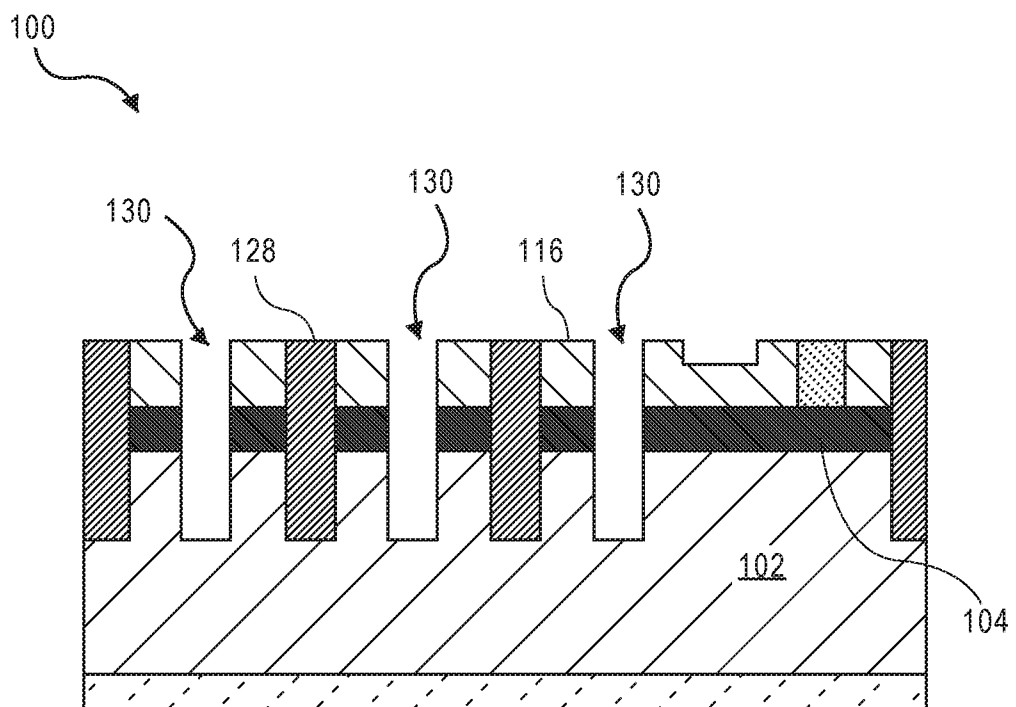
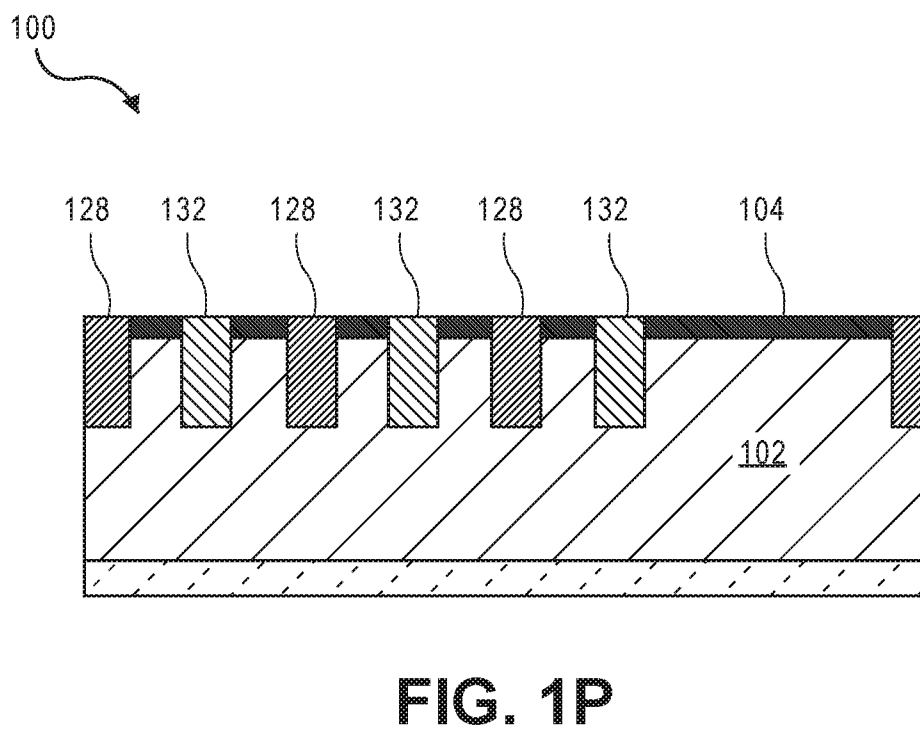
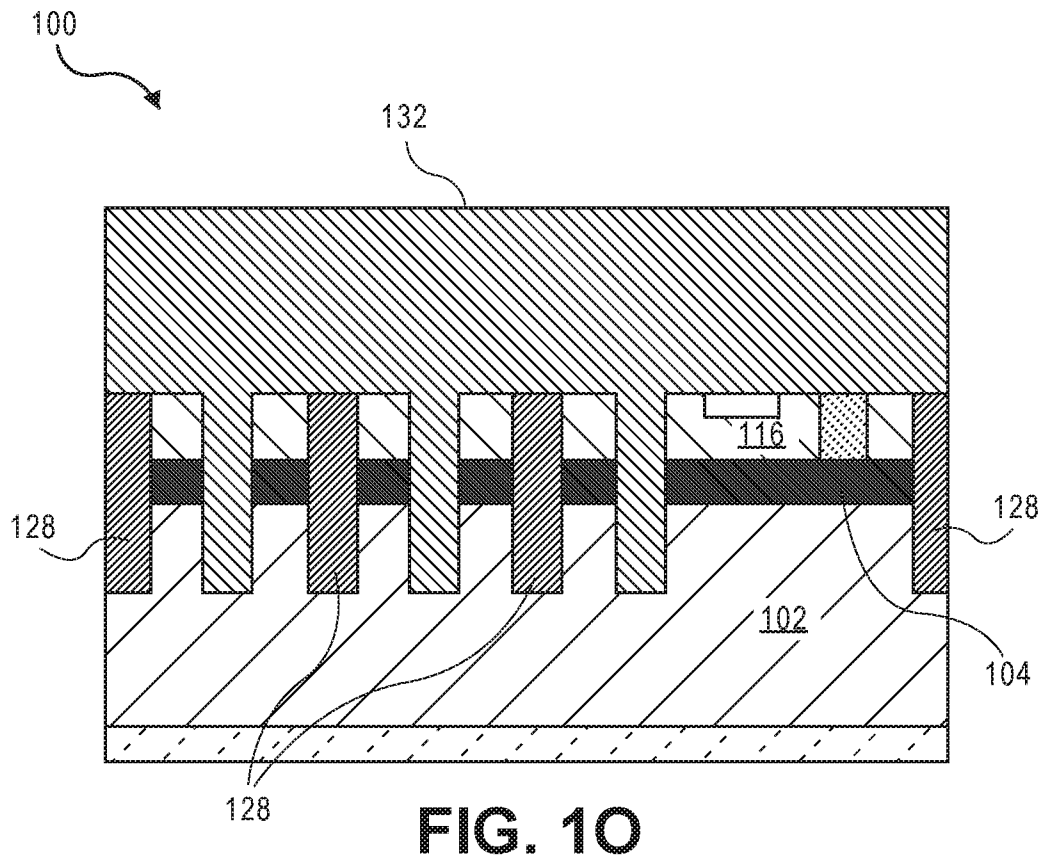
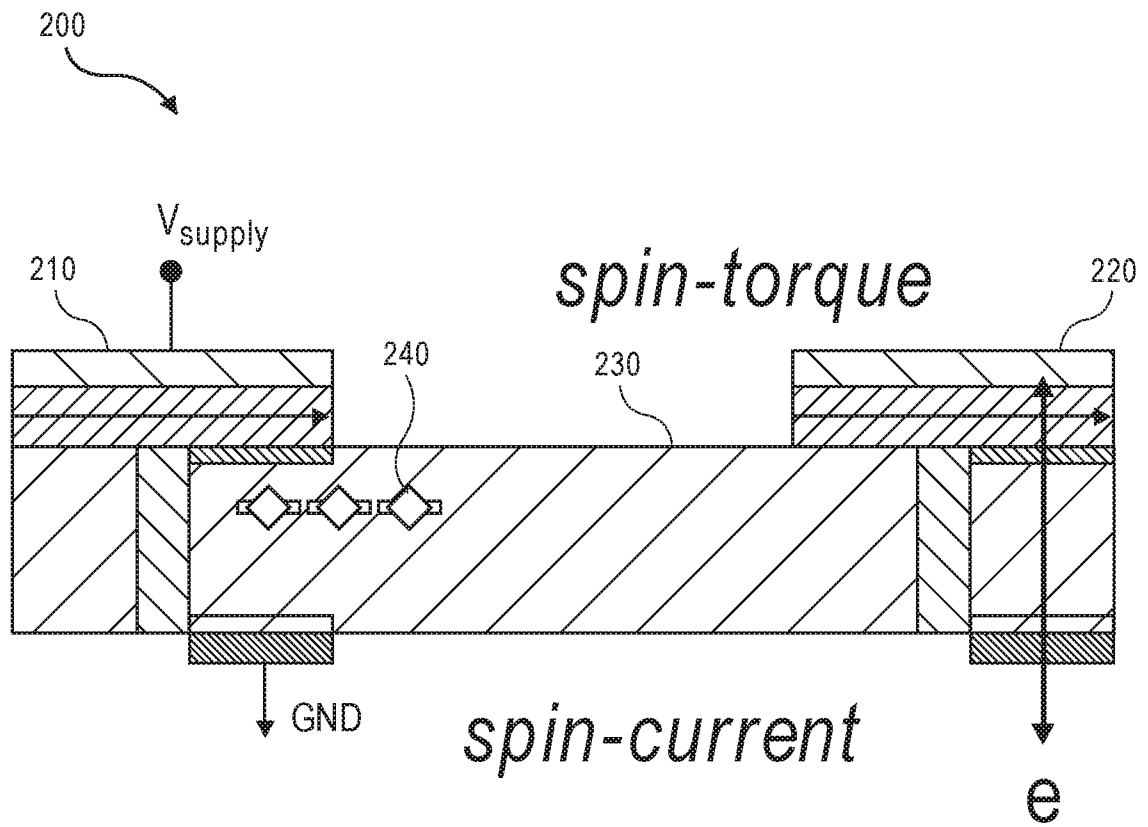


FIG. 1N

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**FIG. 2**

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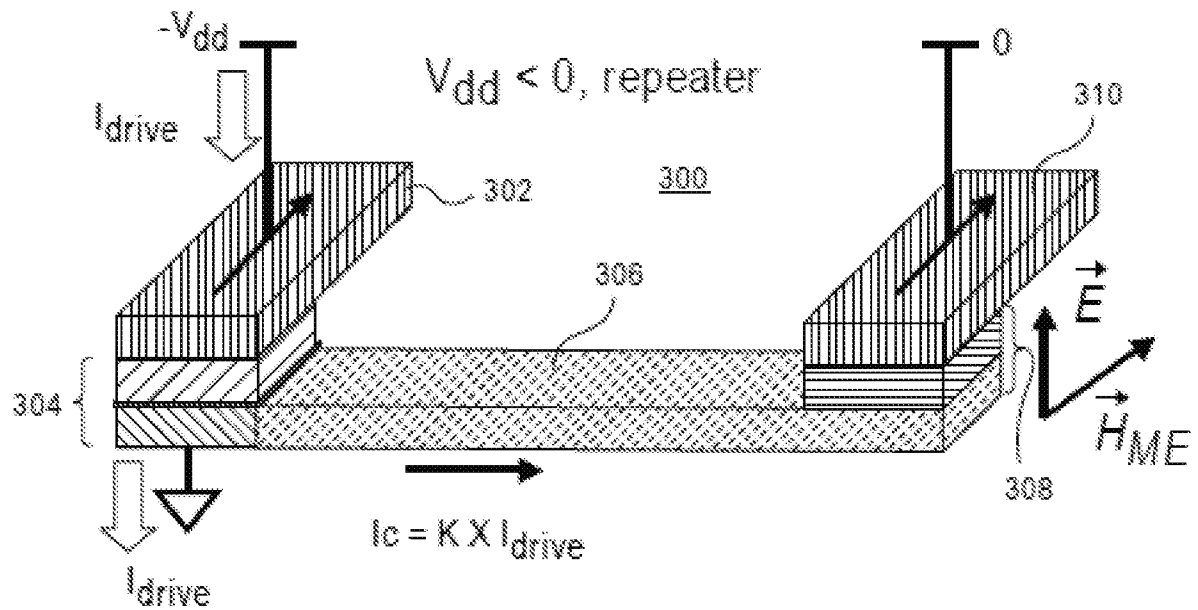


FIG. 3A

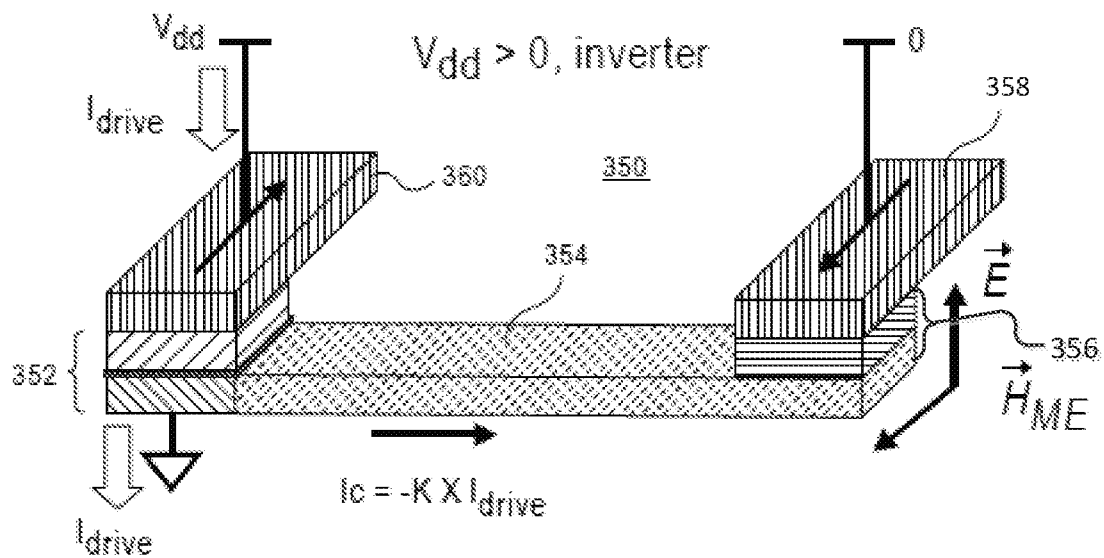


FIG. 3B

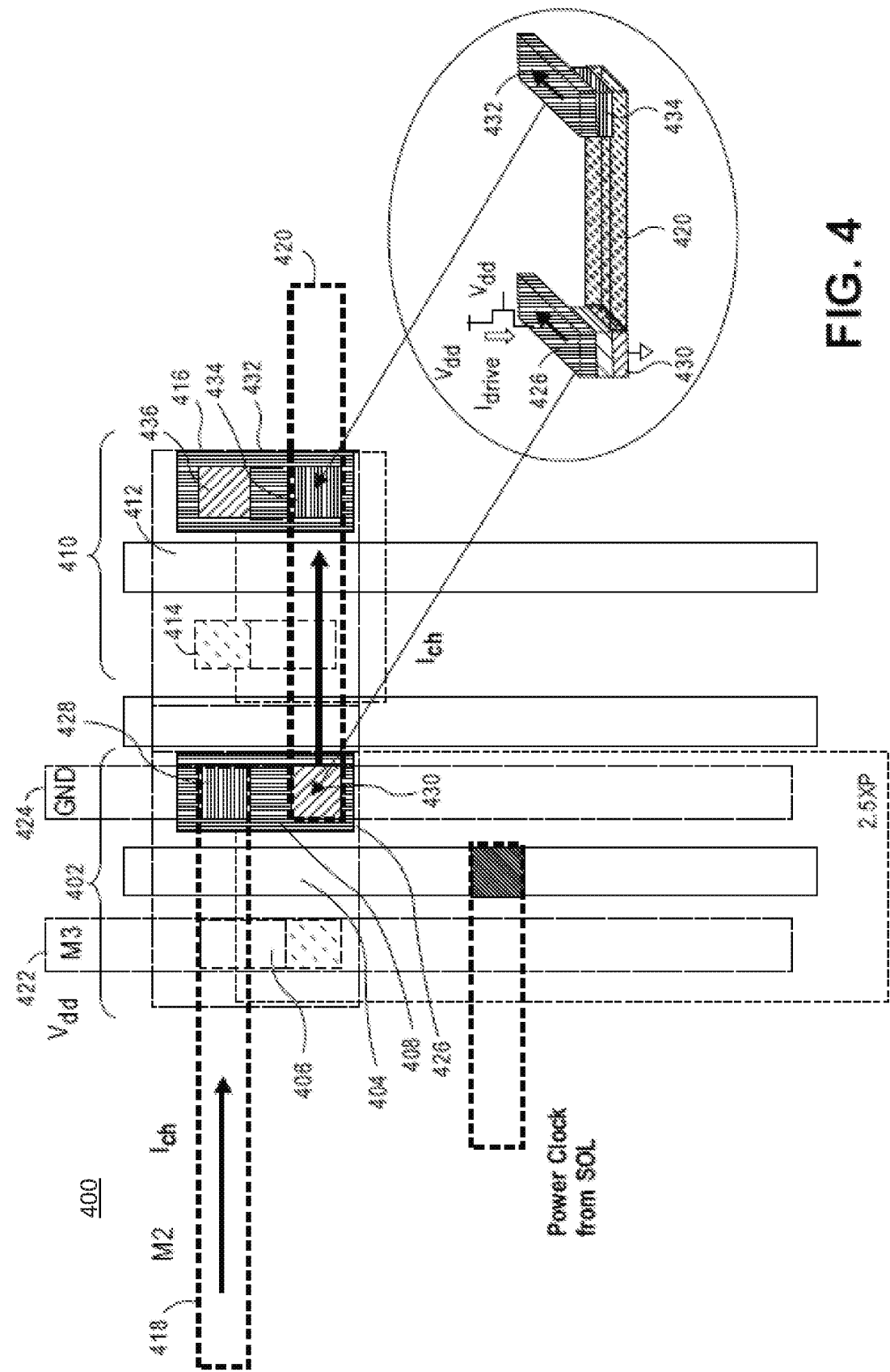


FIG. 4

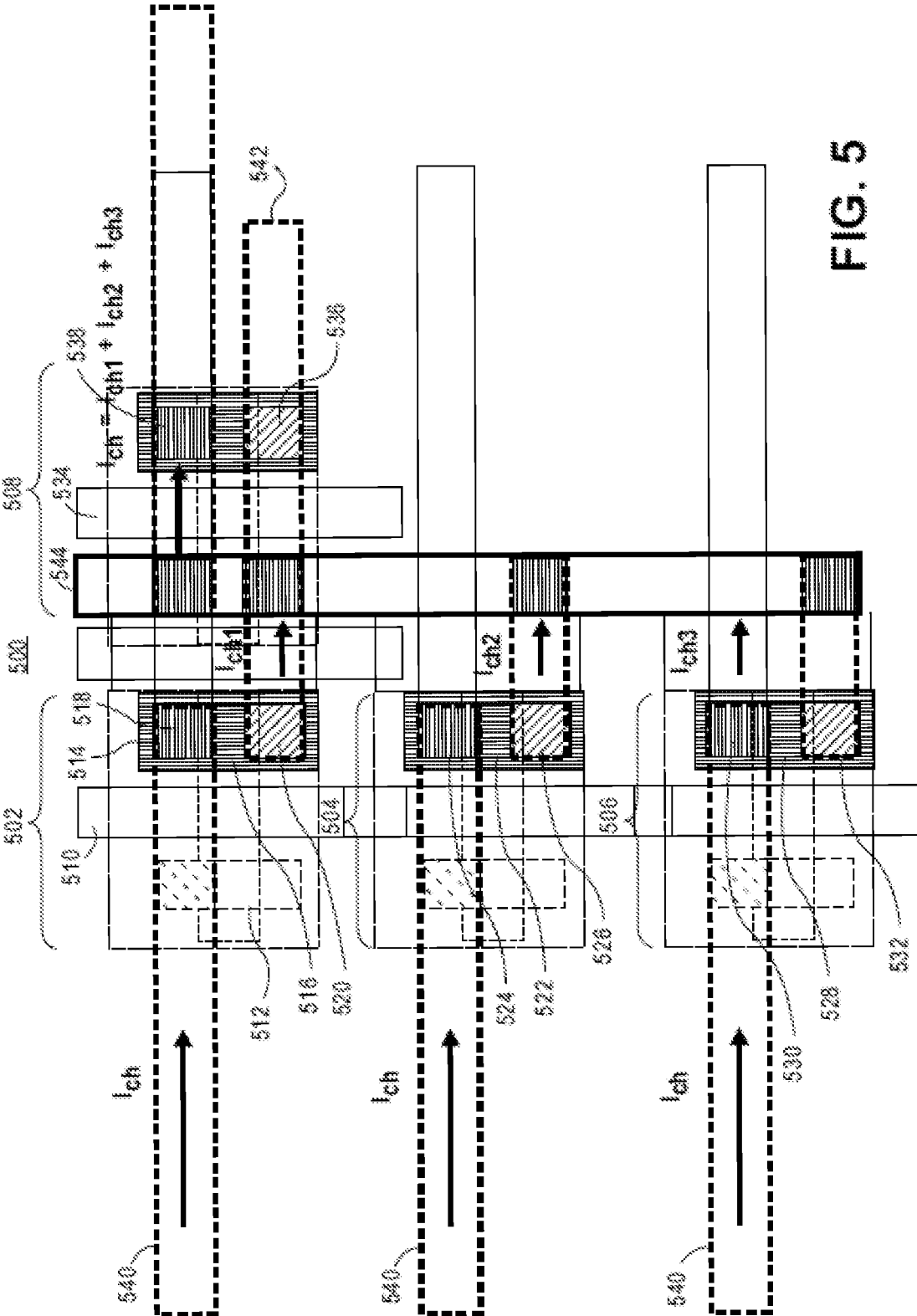


FIG. 5

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in_{i+1}	Control	$Out_{i+1} (V>0)$	$Out_{i+1} (V<0)$
1/0	1	1/0	0/1
1/0	0	Out_i	Out_i

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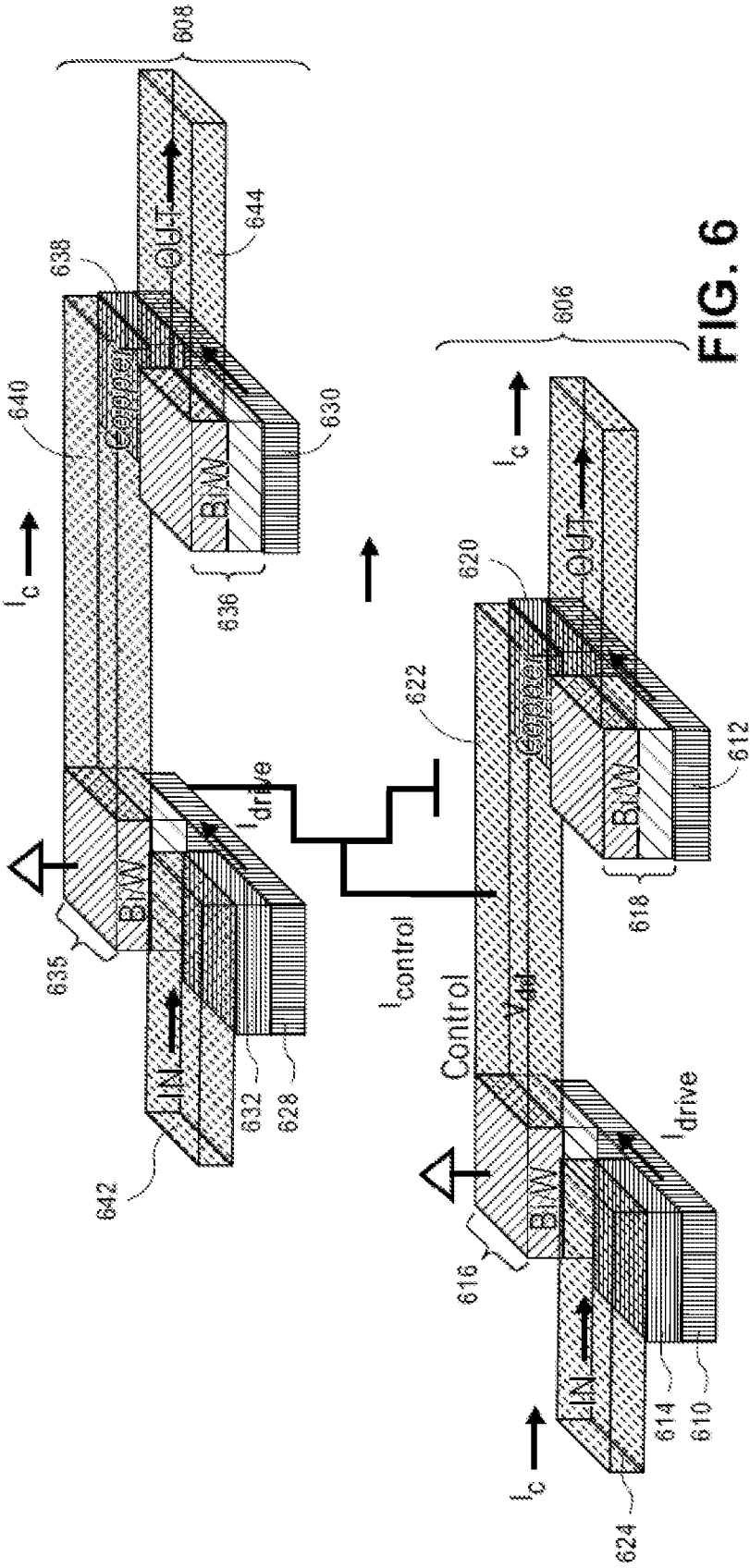


FIG. 6

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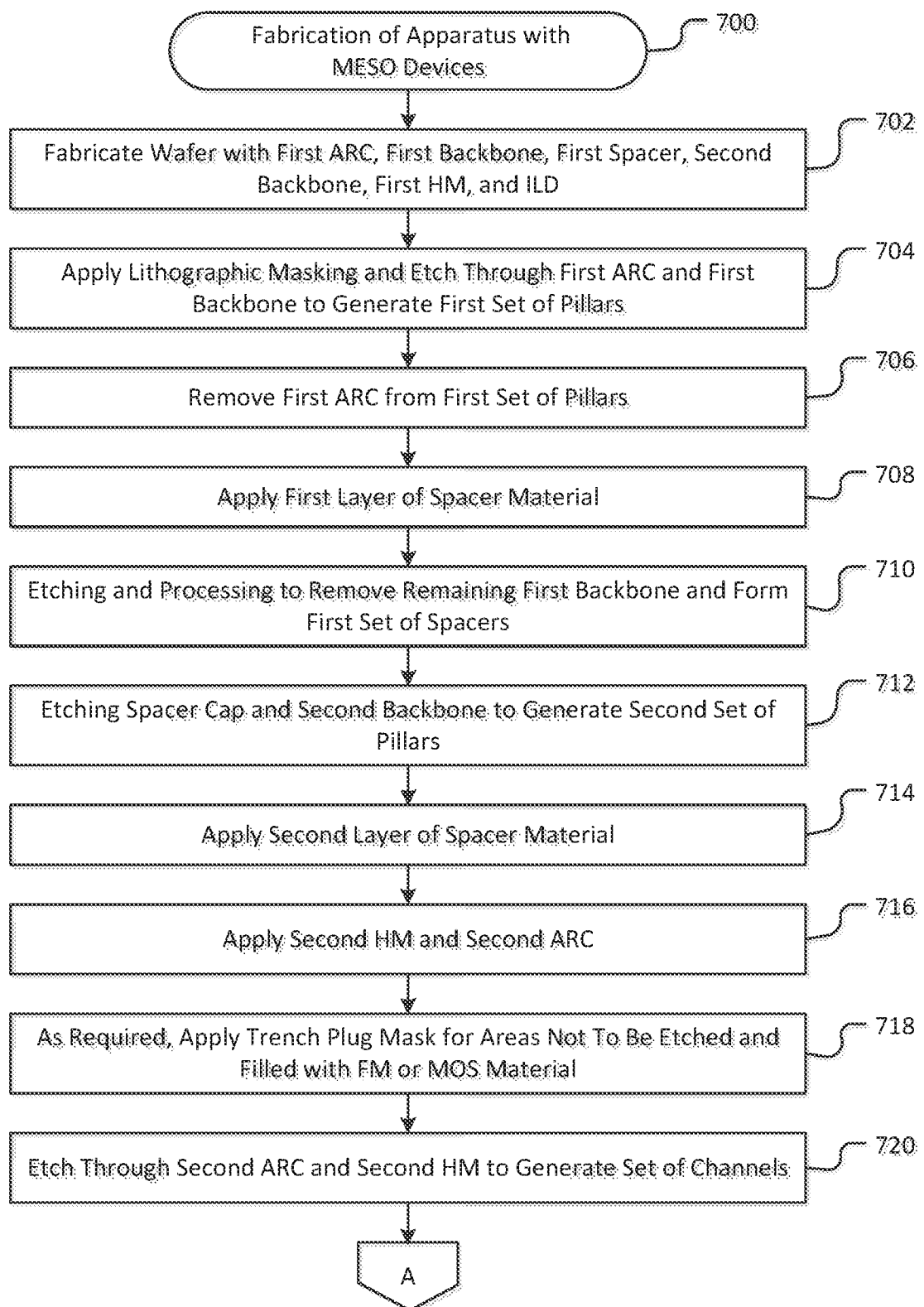


FIG. 7A

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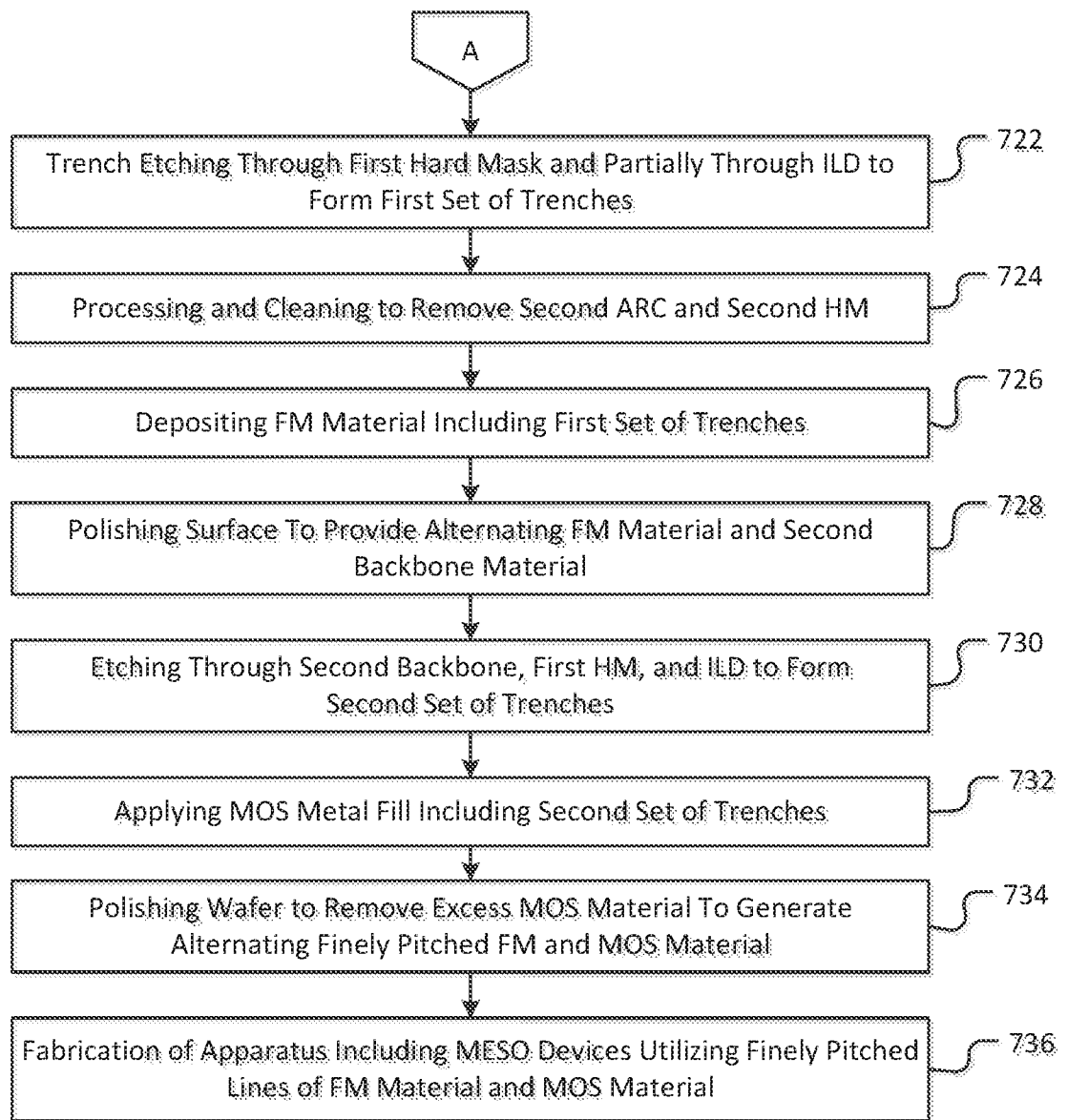


FIG. 7B

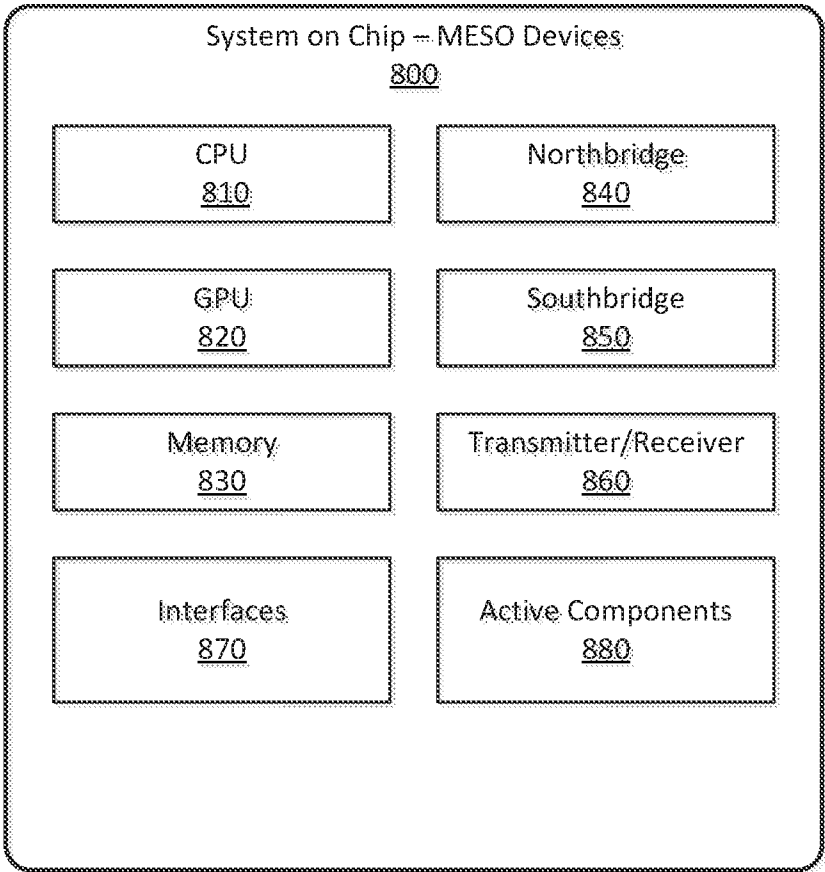


FIG. 8

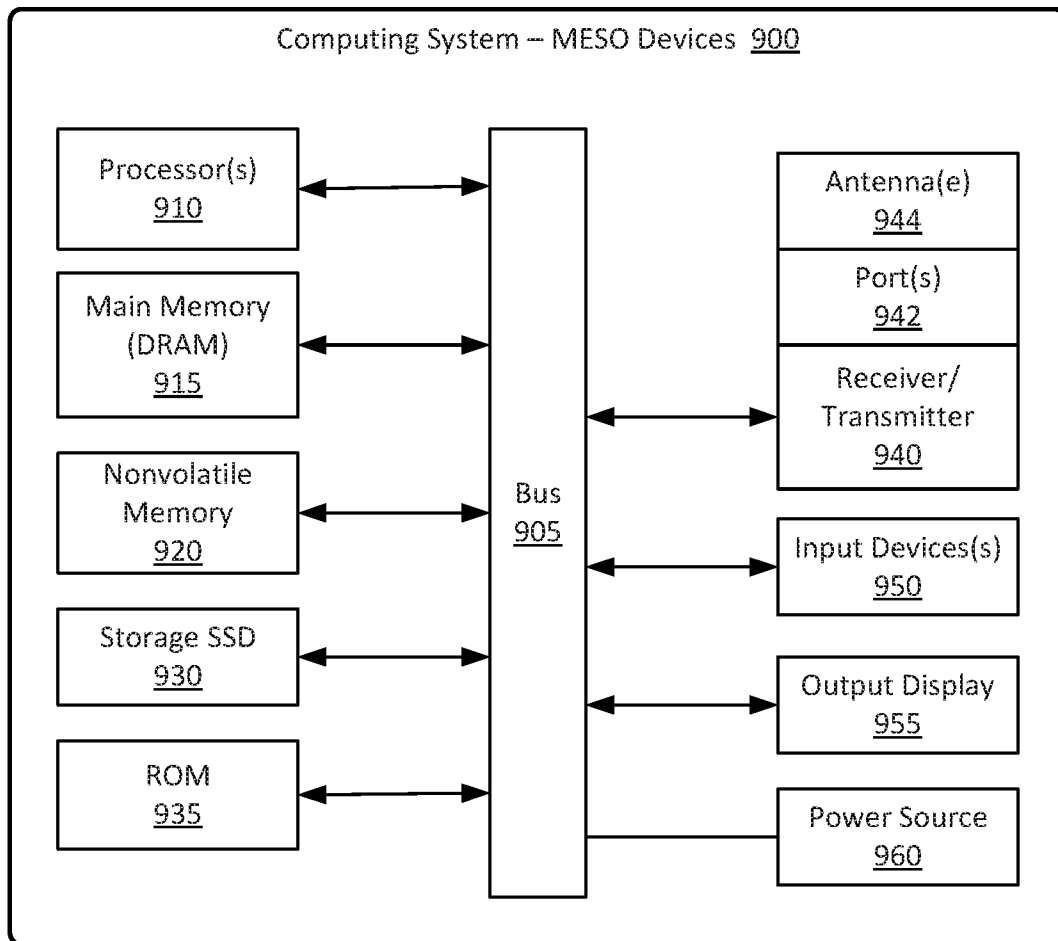


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/038507**A. CLASSIFICATION OF SUBJECT MATTER****H01L 43/02(2006.01)i, H01L 43/08(2006.01)i, H01L 43/10(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 43/02; H03K 19/20; H01L 23/528; H01L 29/82; H01L 29/78; H01L 21/02; H01L 29/66; H01L 43/08; H01L 43/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: spintronics, alternating, ferromagnetic, non-magnetic, interconnect

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 2016-105436 A1 (INTEL CORPORATION) 30 June 2016 See page 2, line 21 - page 7, line 10, claim 1 and figures 1-5.	1-22
A	US 2015-0243599 A1 (INTEL CORPORATION) 27 August 2015 See paragraphs [0025]-[0055], claim 8 and figures 4A-4Q.	1-22
A	JP 2012-049403 A (INSTITUTE OF PHYSICAL & CHEMICAL RESEARCH) 08 March 2012 See paragraphs [0020]-[0076], claims 3-4 and figure 1.	1-22
A	US 2014-0054685 A1 (STMICROELECTRONICS S.R.I.) 27 February 2014 See paragraphs [0047]-[0074], claim 1 and figure 3.	1-22
A	US 2008-0100345 A1 (ALEXANDRE M. BRATKOVSKI et al.) 01 May 2008 See paragraphs [0021]-[0028], claim 1 and figure 1.	1-22

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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Date of the actual completion of the international search

09 January 2018 (09.01.2018)

Date of mailing of the international search report

10 January 2018 (10.01.2018)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

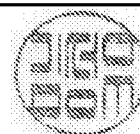


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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/038507

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