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(54) Title: INTERCONNECTS WITH TRENCHES

(57) Abstract: A conductor in a laminar structure, such as a printed circuit board or thin-film stack, is closely flanked by at least one open trench filled with an ambient medium (e.g., air, another gas, vacuum) of a lower dielectric loss than the conductor's surrounding dielectric. The trench may be made by any suitably precise method such as laser scribing, chemical etching or mechanical displacement. A thin layer of dielectric may be left on the sides of the conductor to prevent oxidation or other reactions that may reduce conductivity. When the conductor carries a signal, part of an electric and/or magnetic field that would ordinarily travel through the surrounding dielectric encounters the low-loss ambient medium (e.g. air) in the trench. The effective dielectric loss surrounding the conductor is lowered, reducing signal attenuation and crosstalk, particularly at high frequencies.



INTERCONNECTS WITH TRENCHES

FIELD

[0001] Related fields include circuits with laminar construction, and more particularly dielectric loss reduction in printed circuit board (PCB) and package interconnects formed from a conductive layer in a laminate structure, including without limitation masking, etching, sputter deposition, and electroplating.

BACKGROUND

[0002] Circuits fabricated as laminates (either printed circuit boards or thin-film stacks on semiconductor substrates) often include connective conductors formed from one or more patterned conductive layers. The conductors may carry signals, provide power, or act as ground or other reference lines. (In this document, “ground” will serve as a generic shorthand for any reference conductor). Conductors with different functions may be fabricated on different layers; the “signal plane,” the “power plane,” and the “ground plane” may sometimes be separate from each other. Alternatively, combinations of signal lines, power lines, and ground lines may be coplanar or formed in the same layer. Signal-carrying conductors may be single lines, differential pairs such as microstrip, or single or paired lines with coplanar parallel ground lines such as coplanar waveguides. Ground planes may be unpatterned conductive layers as in some printed circuit boards (PCBs).

[0003] Two ongoing trends in electronics manufacturing are (1) higher data rate, e.g., fabric or Peripheral Component Interconnect Express (PCIe) applications and (2) higher component density, which entails a corresponding increase in the density of signal lines and other interconnects. As data rates increase, the signaling performance degrades due to the frequency dependent loss of the presently used copper conductors and surrounding dielectrics. Thus, it becomes more and more important to control and reduce the dielectric loss in high speed digital

system designs. This is particularly critical for longer routing lengths in PCB or package. The dielectric loss becomes a dominant factor in high speed signaling since it dominates the total loss for frequency in GHz range. Through producing air-filled trenches along the conductor traces, the dielectric loss can be significantly reduced. Because air is lossless (dielectric constant = 1, loss tangent = 0), the total dielectric loss caused by the mixed medium (dielectric + air) surrounding the trace is reduced. Other approaches have included, without limitation, using a thicker layer of copper for the signal plane to reduce the conductor loss; using special low-loss dielectric as the substrate or as the fill layer around the signal conductors; or adding another conductive plane. All these add significant extra production cost, and/or are not effective in reducing the total PCB channel loss. For example, when there are only a few (e.g., the longest and thinnest) signal traces that do not easily meet the loss target, using a more expensive material or design throughout the entire package may not be cost-effective.

[0004] A need exists for a cost-effective solution to overcome the difficulty of meeting link loss targets and to improve the signal integrity performance of PCB microstrips. The present disclosure addresses these needs.

BRIEF DESCRIPTION OF DRAWINGS

[0005] FIGs. 1A-1C schematically illustrate an example of a microstrip fabricated on a printed circuit board (PCB) with open trenches.

[0006] FIGs. 2A-2C schematically illustrate two differential microstrip pairs with and without open trenches.

[0007] FIG. 3 is a flowchart of a process of making an interconnect layer with loss-reducing trenches in a laminate-type circuit.

[0008] FIGs. 4A-4D are data charts based on model results.

[0009] FIGs. 5A-5E are examples of single traces and the effects of trenches on the electromagnetic fields created by signals traveling along the traces.

[0010] FIGs. 6A-6E schematically illustrate planar waveguides with trenches.

[0011] FIGs. 7A-7D schematically illustrate trench formation on an interconnect layer of a laminate-type circuit after components are installed.

[0012] FIGs. 8A-8E schematically illustrate trench formation after applying a thick protective overcoating to the interconnect layer and installed components.

[0013] FIG. 9 schematically illustrates an approach to trenches in a double interconnect layer.

DETAILED DESCRIPTION

[0014] FIGs. 1A-1C schematically illustrate an example of a microstrip fabricated on a printed circuit board (PCB) with open trenches. FIG. 1A is a perspective view, FIG. 1B is a front view, and FIG. 1C is a top view of the section of the PCB. The following discussion refers to all three figures.

[0015] Substrate 101 of the PCB includes composite layer 104 and optionally ground backing layer 112. All the conductor embodiments described herein may be used with or without the ground backing layer 112. Composite layer 104 is an insulating material situated similarly to an interlayer dielectric (ILD) in thin-film circuits; that is, as a blanket insulating layer providing a base surface for the fabrication of components and/or their interconnections. On double-sided PCBs, the ground backing layer 112 may be positioned near the center of the stack, between two composite layers 104. Conductive traces 102 (hereinafter "conductors") are formed over the surface of composite layer 104. For example, the conductors may be fabricated by laminating a copper sheet onto a top surface of the composite layer, then etching away the parts of the copper sheet that are outside the paths of the conductors. In this example, conductors 102 are topped

with a plating layer 122. For instance, conductors 102 may be copper and plating 122 may be an alloy, such as copper with zinc. Plating 122 may be added before or after etching. Conductors 102 and plating 122 are buried in a surrounding dielectric 108. Surrounding dielectric 108 is analogous to the fill dielectric in thin-film circuits.

[0016] Open trenches 106 have been made beside conductors 102. A low-dielectric-loss ambient medium 150 is permitted to enter and fill trenches 106. For example, the ambient medium 150 may be air, another gas such as nitrogen or argon (e.g., for an application requiring a non-oxidizing atmosphere), or vacuum (e.g., for a space-based application). The trenches may be made by a laser scribe, mechanical action on dielectric layers that may be optionally softened by heating, or any other known etching procedure compatible with the materials.

[0017] In some embodiments, a thin layer of surrounding dielectric 108 is left to cover conductor 102 and, if present, plating 122. This thin layer shields conductor 102, plating 122, or both from exposure to a potentially corroding ambient medium 150; for example, to prevent copper from being oxidized by air. However, there may be embodiments where corrosion is not an issue; for example, if the ambient medium 150 is substantially free of oxygen (e.g., less than .01 ppm) or if conductor 102 and, if present, plating 122 are inert metals. In those embodiments, conductor 102 and, if present, plating 122 need not be sealed on all but the bottom side by surrounding dielectric 108. Plating 122 may be exposed on the top of conductor 102, or the sides of conductor 102 may be exposed. Preferably, if the surrounding dielectric 108 is to be removed from the sides of conductor 102, the scribing or etching procedure is sufficiently controllable that it does not take enough conductive material off the sides of conductor 102 to change conductor 102's impedance in an inconsistent or unpredictable way. Optionally, open trenches 106 may extend past the original top surface of the substrate 101 and into the bulk of composite layer 104 as illustrated.

[0018] Because only a thin layer, if any at all, of surrounding dielectric 108 still surrounds conductors 102, electric or magnetic fields created by signals traveling in conductors 102 experience the ambient medium 150 as part of a compound "surrounding dielectric." Air, nitrogen, argon, and vacuum produce vanishingly small dielectric losses. The compound-surrounding-dielectric effect may be expected to grow stronger as the frequency increases, as more of the electromagnetic energy generated by the signal propagates through low-loss medium 150 compared to the energy propagating through the etched or surrounding dielectric.

[0019] FIGs. 2A-2C schematically illustrate two differential microstrip pairs with and without open trenches.

[0020] FIG. 2A illustrates a first stage in constructing a conductor layer with trenches: namely, constructing a conventional, trenchless interconnect layer. A first differential microstrip pair 203.1 and a second differential microstrip pair 203.2 are fabricated on a surface 211 of a composite or ILD layer 204 on substrate 201. Ground backing layer 212 is optional. In addition, other layers and structures may be present under composite or ILD layer 204, but are not shown because they do not affect the loss-reducing properties of open trenches. Surrounding dielectric 208 completely covers differential microstrip pair 203.1 and 203.2. Some dimensional variables relevant to discussing modeling and test results are: inter-pair distance D between differential microstrip pair 203.1 and differential microstrip pair 203.2, conductor 202's width T_w , composite or ILD 204's thickness h , conductor 202's thickness y_c , surrounding dielectric 208's thickness y_d , and spacing T_s between two conductors 202 of the same differential microstrip pair 203.1 or 203.2.

[0021] FIG. 2B illustrates the second stage in constructing a conductor layer with trenches: namely, making the trenches. In this example, trenches 206 have created separated islands of both the surrounding dielectric 218 and the underlying composite or ILD layer 214. Ground backing

layer 212 acts as the support layer in this illustration, but any other suitable underlying layer could be substituted. Note that trenches 206 between the two isolated differential microstrip pair 213.1 and 213.2 are separated by a conductor-less dielectric island of the etched-away surrounding dielectric 218 and ILD 214. This may be convenient in some embodiments, e.g., using a scribe beam or mechanical scribe a fixed width.

[0022] FIG. 2C illustrates an alternative approach. After forming the conductors 202, surrounding dielectric 228 is applied as a thin conformal coating rather than a relatively thick blanket coating such as 208 in FIG. 2A. For example, a conformal coating may be applied by atomic layer deposition (ALD) or other forms of physical or chemical vapor deposition. Solder mask based on various materials is a common form of coating in PCBs. The extra process step of forming trenches is obviated because the existing "valleys" between conductors 202 are thinly lined, rather than filled, by the conformal coating. As with trenches formed by scribing or etching in a blanket coating, the end result is that conductors 202 have a thin solid dielectric coating 228 separating them from a space filled by ambient medium 250. Center valley 206 between the two differential microstrip pairs 223.1 and 223.2 spans the entire width D (see FIG. 2A) without requiring a scribe to adjust its "blade" width or make multiple passes. If the spacing between the two microstrips of the pair 223.1 and 223.2 is small, the thickness of the coating between the two microstrips in one pair may not be thin and may be similar to the blanket coating case. In this case, the trenches may still be made by laser scribing or other methods to reduce microstrip dielectric loss.

[0023] FIG. 3 is a flowchart of a process of making an interconnect layer with loss-reducing trenches in a laminate-type circuit. Initially, the substrate is prepared at step 302. Preparation 302 may include cleaning, degassing, or formation of layers or structures that may underlie the interconnect layer. At decision 310, if the top substrate layer is not a dielectric, a first dielectric

layer, such as a composite layer or an ILD, is formed over the top substrate layer by any suitable method before beginning step 312 of conductor formation. However, if the top layer is already dielectric, the process may immediately advance to step 312, formation of the conductors on the dielectric surface by an additive (e.g., spray-on or selective plating) or subtractive method (e.g., scribing or etching a homogeneously created conductive layer).

[0024] At step 314, a second, surrounding dielectric layer is formed over the conductors as well as over any exposed composite-layer / ILD surfaces. The surrounding dielectric layer may be either a blanket layer as in FIG. 2A or a conformal coating as in FIG. 2C. At decision 320, if the surrounding dielectric is a conformal layer, the existing thinly-lined valleys between the coated conductors may be used as trenches in step 323 and step 324 may be started. Alternatively, trenches may be formed at step 322 at any of a number of different points in the process.

[0025] Trench formation at step 322 may include laser ablation, photodisruption, laser/thermal cutting, mechanical displacement with or without heating the substrate to soften it, plasma or reactive-ion etching, or wet chemical etching. Those of ordinary skill in the art will be aware of which processes are suitable for the materials and scale of particular circuits of interest.

[0026] In some embodiments, trench formation 322 may be the very next step, before additional components are installed or formed during step 324. In step 324, components such as processors, transmitters, receivers, volatile or nonvolatile memory components, sensors, or input/output connectors are added to the board, or other laminated-circuit substrate. The components installed in step 324 may be connected by the conductors immediately below them. Alternatively, the components installed in step 324 may be connected by another interconnect layer to be installed above them, while the interconnect layer below them connects components located in an even lower layer. Combinations are also possible where the interconnect layer connect to one or more components below it with one or more components above it.

[0027] In some embodiments, trench formation 322 may follow component installation 324 and precedes an optional protective overcoating step 326. Some PCBs and other laminated circuits are given a thick overcoating, often of polymer or elastomer, to protect the fabricated circuit from damage during transport, storage, or operation. For example, if the protective overcoating is intended to be removed before the laminated circuit is operated or installed in a parent device, the trenches may be formed in step 322 and then covered with the overcoating, along with the components and conductors, in step 326. The trenches will then be exposed and filled with ambient medium (air, other gas, or vacuum) when the overcoating is removed for installation or operation of the circuit. Alternatively, the overcoating may be viscous and cohesive enough to cover the openings of the trenches but not sink into them, so air (or another gas) is trapped inside. Optionally, a few small vents may pierce the overcoating to equalize pressure or draw the gas out of the covered trenches.

[0028] In some embodiments, the trench formation 322 may follow protective overcoating step 326 and precede next process 399. For example, if the protective overcoating is intended to be permanent, the trenches may be formed through the in situ protective overcoating to allow ambient medium to circulate through it. If the materials exposed by trench formation step 322 are not likely to be harmed by contact with air during storage or shipping, the trenches may be left bare after formation in step 322. If the materials exposed in the trench walls or bottom still need further protection, a thin layer of low-viscosity, low-cohesion top-coating may be applied after trench formation step 322 through the thick protective layer applied in step 326. Next step 399 may be, for example, breaking apart multiple independent circuits on a large substrate, packaging the circuit, or connecting it to other circuits.

[0029] FIGs. 4A-4D are data charts based on model results. A theoretical model has been constructed to compare performance aspects of differential microstrip pairs on a conventional

trenchless PCB (e.g., as in FIG. 2A) with differential microstrip pairs on a PCB that is identical except for having trenches (e.g., as in FIG. 2B). As in FIGs. 2A and 2B, the model considered two neighboring differential microstrip pairs so that crosstalk could be included in the calculations. Referring to dimensions illustrated in FIGs. 2A and 2B, the parameters of the model included:

[0030] Thickness "h" of the composite core layer 204 = 0.101mm(0.004");

[0031] Thickness "y_d" of solder-mask = 0.086mm(0.0034"), thickness "y_c" of conductive traces = 0.079mm(0.0031");

[0032] Width "T_w" of individual traces = 0.152mm(0.006"), trace spacing "T_s" inside each differential pair = 0.14mm (0.0055");

[0033] Spacing "D" between one differential pair and the other = 0.622mm (0.0245") ~6h.

[0034] FIG. 4A compares the calculations of frequency-dependent differential insertion loss in 51mm (2") of microstrip length for a trenchless PCB with those of PCBs with various trench depths. Curve 402 is the conventional trenchless microstrip. Curve 404 shows the results for a trench depth of 0.051mm (0.002"). Curve 406 shows the results for a trench depth of 0.102mm (0.004"). Curve 408 shows the results for a trench depth of 0.178mm (0.007") trenches. The DC loss is negligible for all the PCBs but the trenchless microstrip (curve 402) has a slope of about -0.2 dB/GHz, while the 0.178mm deep trenches (curve 408) reduced the slope to about -0.12 dB/GHz, an improvement of about 40%.

[0035] Another notable feature of the graph is that a shallow trench has a significant effect, but the gains diminish for deeper trenches. Comparing the trench depths to the layer thicknesses, the shallowest 0.051mm trenches (curve 404) extend about 2/3 of the way through the solder-mask (surrounding dielectric), which for this model is also 2/3 of the way past the microstrip trace. The 0.102mm trenches (curve 406) extend all the way through the solder-mask (surrounding

dielectric) and into the composite layer to an additional 1/3 of the microstrip trace thickness.

The 0.178mm trenches (curve 408) go further into the composite layer. This suggests that most of the insertion-loss reduction benefit comes from the part of the trench right beside the side of the trace. Continuing to remove material below the level of the bottom of the trace may reduce the insertion loss a little more, but the improvement "tops out" and approaches a constant beyond a threshold distance past the bottom of the trace.

[0036] FIG. 4B compares the frequency-dependent differential far-end crosstalk (FEXT) of 50.8mm (2") lengths of the trenchless microstrip (curve 412) and the microstrip with 0.178mm trenches (curve 418). Up to about 25GHz, the trenches appear to cause no significant change in the differential FEXT.

[0037] FIG. 4C examines the time-domain pulse responses of 254mm (10") lengths of trenchless microstrip and microstrip with 0.178mm trenches. A single pulse (Unit Interval=62.5pS, Data Rate=16GTs) arrives earlier, and larger in magnitude, through the microstrip with trenches (curve 428) compared to the trenchless microstrip (curve 422). The trenches filled with low-loss air appear to increase the propagation speed of signals, in addition to reducing the dielectric loss and possibly reducing the dispersion (spreading) of short pulses.

[0038] FIG. 4D compares the impedance, measured by time-domain reflectometry (TDR) of 254mm sections of trenchless microstrip and microstrip with 0.178mm trenches. The TDR graph shows an impedance increase of 15Ω with the trenches. In some designs with target impedances, this impedance increase may need to be offset by an impedance-lowering measure such as widening the traces or narrowing the gap between differentially paired traces.

[0039] FIGs. 5A-5E are examples of single traces and the effects of trenches on the electromagnetic fields created by signals traveling along the traces. A single signal trace is the simplest implementation and provides a clear demonstration of the trenches' effect.

[0040] FIG. 5A schematically illustrates a conventional trenchless conductor layer. Conductor 502 of width w is laminated onto composite or ILD 504 and surrounded by dielectric 508 on the top and both sides. A DC current or very low-frequency signal in conductor 502 produces an electromagnetic field with envelope 510, approximately the same size as conductor 502. A high-frequency signal in conductor 502 produces an electromagnetic field with envelope 511, which extends further out from conductor 502; the higher the frequency, the larger the envelope.

[0041] In some embodiments, amplitudes of fields with envelopes 510 and 511 may drop exponentially outside the outer surface of conductor 502. For example, envelopes 510 and 511 may mark the full width as half-maximum (FWHM) of the fields, and the fields may extend at a decaying amplitude outside the illustrated envelopes. Any part of the field that travels through a lower-dielectric-loss medium than the surrounding dielectric will reduce the insertion loss of the conductor, but the effect may be more pronounced if a higher-amplitude part of the field (e.g., the part inside the envelope) is directed through the lower-loss medium.

[0042] Therefore, the inner boundary B_{in} of the trench is preferably as close to the surface of conductor 502 as possible. A lower limit on the distance of inner trench boundary B_{in} from the nearest edge of conductor 502 may be set to leave a thin layer of the surrounding dielectric 508 between conductor 502 and the ambient medium in the trench if the ambient medium is likely to react with the conductor. Additionally or alternatively, such a limit may be imposed by manufacturing tolerances to avoid inadvertently cutting into conductor 502. A lower limit on outer trench boundary B_{out} may be placed by calculating the expected exponential decay of the amplitude of electromagnetic field envelope 511 at the maximum frequency of interest. For example, B_{out} may be placed where the field at a maximum frequency of interest drops to, for example, 10%, 5%, or 1% of its amplitude at B_{in} . A trench spanning a width from the B_{in} of a first conductor to the B_{in} of a second conductor, where the exponential decay sections of the field

envelopes of both conductors are fully contained in the trench, may produce the same loss reduction as two separate trenches that each contain the decay portion of the field envelope of one of the conductors.

[0043] FIG. 5B schematically illustrates the effect of a trench from B_{in} to B_{out} and completely through the dielectric in the interconnect layer shown in FIG. 5A. Trench 506 in dielectric 508, which as illustrated reaches the upper surface of composite or ILD 504, is filled with air or another low-loss ambient medium 550. Part of high-frequency envelope 511 is captured by trench 506, but DC/low-frequency envelope 510 is not. Part of the decaying “tail” of the DC/low-frequency field outside envelope 510 may travel through ambient medium 550, but the effect on loss may not be significant.

[0044] FIG. 5C schematically illustrates the effect of a trench from B_{in} to B_{out} but only about one-third of the depth of dielectric 508 in the interconnect layer shown in FIG. 5A. Trench 506 may cut into high-frequency envelope 511, reducing some of the dielectric loss but not as much as the deeper trench in FIG. 5B. DC/low-frequency effects may be small because trench 506 does not intersect envelope 510.

[0045] FIG. 5D schematically illustrates the effect of a round-bottomed trench from B_{in} to B_{out} , at its lowest point extending about halfway past the conductor 502 through the dielectric 508 in the interconnect layer shown in FIG. 5A. In some types of laminated circuits, flat bottoms and sharp corners on trenches are preferred. However, such features may be difficult to achieve; many etching methods produce round-bottomed trenches. The loss-reducing open trenches described herein are not very sensitive to differences in bottom profile. Trench 506 filled with low-loss ambient medium 550 is round-bottomed. The shape has little effect on the dielectric loss reduction. Trench 506 may intersect high-frequency field envelope 511, reducing more of the dielectric loss than the shallow flat-bottomed trench 506 in FIG. 5C, but less than the deep flat-

bottomed trench in FIG. 5B. DC/low-frequency effects may be small because trench 506 does not intersect envelope 510.

[0046] FIG. 5E schematically illustrates the interconnect layer of FIG. 5A with two trenches 506.1 and 506.2, one on each side of conductor 502. Trenches 506.1 and 506.2 intersect opposing portions of high-frequency field envelope 511, so the overall high-frequency insertion loss is reduced more than it would be with only a single trench, all other variables being equal. The same applies to DC/low-frequency envelope 510, though the effects of each of the trenches 506.1 and 506.2 may be small.

[0047] FIGs. 6A-6E schematically illustrate planar waveguides with trenches. The following contextual elements are alike in FIGs. 6A-6E: Composite core 604 and optional ground backing layer 612 constitute a substrate 601. One or more conductors 602 are configured to carry signals and are flanked by one or more coplanar ground lines 642. Conductor 602 and coplanar ground lines 642 are buried under dielectric fill layer 608.

[0048] FIG. 6A schematically illustrates a single-ended (i.e., single-trace) planar waveguide on a PCB with trenches added around the signal-carrying conductor. As illustrated, two open trenches 606.1 and 606.2 extend from just outside conductor 602 to just outside the nearest coplanar ground line 642. A thin layer of surrounding dielectric layer 608 protects the sides of conductor 602 and the top surface of composite core 604 in this example. This may be preferable, for example, if the material of composite core 604, as well as that of conductor 602 and coplanar ground line 642, may be vulnerable to an external environment. Alternatively, the trenches 606.1 and 606.2 may have some other depth between zero and the entire thickness of substrate 601 and surrounding dielectric 608. Another independent alternative is to have one wall of each trench 606.1 and 606.2 close to conductor 602 as illustrated, but narrower so is not to reach all the way to coplanar ground line 642.

[0049] FIG. 6B schematically illustrates a differential-pair-based planar waveguide on a PCB with a single central trench added. Open trench 606.3 reaches from just beyond an inward-facing side one of the conductors 602 to just beyond in inter-facing side of the other conductor 602. This will reduce the loss by about the same amount in each member of the differential pair, maintaining a balance between the two signals.

[0050] FIG. 6C schematically illustrates a differential-pair-based planar waveguide on a PCB with a pair of central trenches added to the differential pair. Trenches 606.4 and 606.5 closely flank their neighboring conductors 602, but leave some intact dielectric 608 between them.

[0051] FIG. 6D schematically illustrates a differential-pair-based planar waveguide on a PCB with a pair of outer-edge trenches added to the differential pair. In essence, this differential pair of conductor 602 is flanked by outer trenches just like 606.1 and 606.2 in FIG. 6A. Any of the same options available to a single-trace waveguide may readily adapt to use with the differential pair: Trenches 606.1 and 606.2 may have some other depth between zero and the entire thickness of substrate 601 and surrounding dielectric 608. Another independent alternative is to have one wall of each trench 606.1 and 606.2 close to conductor 602 as illustrated, but narrower so is not to reach all the way to coplanar ground line 642.

[0052] FIG. 6E schematically illustrates a differential-pair-based planar waveguide on a PCB with the combination the trenches from FIG.6D and the trenches from FIG. 6B or 6C. The combination may provide the greatest dielectric loss reduction among the differential-pair options. However, a manufacturing tool may have multiple parallel scribing-laser beams, mechanical blades, mask slits, or other trench-making means so that all the trenches may be made in a single pass.

[0053] As additional alternatives to the configurations illustrated in FIGs. 1A-1C, 2A-2C, 5A-5E and 6A-6E, there may be other types of signal lines using only a single coplanar ground line 642 along with the signal conductor or differential pair 602.

[0054] FIGs. 7A-7D schematically illustrate trench formation on an interconnect layer of a laminate-type circuit after components are installed. While the preceding discussion has centered on forming trenches around conductors immediately after filling the interconnect layer with dielectric, embodiments are also feasible in which the trenches are formed after components are added above the interconnect layer.

[0055] FIG. 7A is a top view of the PCB with components installed. Signal conductors 702 are embedded in surrounding dielectric 708; a thin layer of dielectric 708 may optionally cover conductors 702 to protect them from corrosion. First component 707 and second component 717 are communicatively coupled by conductors 702, which are presently trenchless. Conductors 702 may be two single-ended signal traces, a differential pair, two differential pairs, planar waveguides, or any other suitable type of interconnect.

[0056] FIGs. 7B and 7C are cross-sectional views through section A-A of FIG. 7A, showing composite layer 704 and optional ground backing layer 712. Component 707 and its mounts 705 are also visible, but do not actually intersect with sectioning line A-A. In FIG. 7B, conductors 702 are still trenchless. In FIG. 7C, trenches 706 have been formed around and between conductors 702. As illustrated, trenches 706 are round-bottomed and extend into composite 704, but any other suitable trench configuration may be used.

[0057] FIG. 7D is a top view corresponding to the cross-section of FIG. 7C, showing the trenches 706 through dielectric 708 and exposing the composite 704 between and around the conductors 702.

[0058] FIGs. 8A-8E schematically illustrate trench formation after applying a thick protective overcoating to the interconnect layer and installed components. Some PCBs or other laminate-type circuits may be given a thick protective overcoating after the components are installed. The overcoating may protect the circuit from damage during transport, storage, or operation.

[0059] FIG. 8A is a top view of the trenchless overcoated PCB with components installed. Signal conductors 802, first component 807, and second component 817 are buried under overcoating 809. Conductors 802 may be two single-ended signal traces, a differential pair, two differential pairs, planar waveguides, or any other suitable type of interconnect.

[0060] FIGs. 8B and 8C are cross-sectional views through section A-A of FIG. 8A, showing composite layer 804 and optional ground backing layer 812. In FIG. 8B, conductors 802 are still trenchless. In FIG. 8C, trenches 806 have been formed around and between conductors 802 through overcoating 809 and surrounding dielectric layer 808. As illustrated, trenches 806 are round-bottomed and extend into composite 804, but any other suitable trench configuration may be used.

[0061] FIG. 8D is a top view corresponding to the cross-section of FIG. 8C, showing the trenches 806 penetrating through overcoating 809 and intervening layers to the composite 804 between and around the conductors 802.

[0062] FIG. 8E is a cross-sectional view of an alternative approach to trenches in circuits that use thick protective overcoating. Trenches 806 were fabricated through surrounding dielectric layer 808 and part of composite layer 804 sometime before overcoating 809 was applied. Overcoating 809, when applied, is sufficiently viscous and cohesive that it does not flow into trenches 806, so that air or other ambient medium is trapped inside trenches 806. If the application indicates that the circuit may perform better if the trenches are at equilibrium with the environment outside the circuit, a small vent 846 may be made through overcoating 809.

[0063] FIG. 9 schematically illustrates an approach to trenches in a double interconnect layer.

Occasionally, a second interconnect layer is added to a laminate-type circuit (e.g., to meet routing demands in the allotted space).

[0064] In FIG. 9, composite layer 904 underlies a lower interconnect layer 908, an ILD layer 954, and an upper interconnect layer 958. Upper interconnect layer 958 includes conductors 952.1 and 952.2. Lower interconnect layer 908 includes conductors 902.1 and 902.2. Optionally, a via 951 may connect upper conductor 952.1 to lower conductor 902.1.

[0065] Open trenches may be implemented in the upper layer using the same approaches as for a single interconnect layer. For example, trench 906.1 only needs to penetrate upper layer 958 to reduce dielectric loss in conductor 952.2. Conductors crossing under conductor 952.2 on lower level 908 will not be disturbed by the shallow upper trenches.

[0066] As for the lower layer, the trenches may extend from a top surface of the circuit down through the lower layer like narrow trenches 956.1 and wide trench 956.2. Where a lower-layer conductor crosses under an upper-layer conductor, the deep trench for the lower-layer conductor can stop on one side of the crossing and re-start on the other side to avoid cutting into the upper-layer conductor.

[0067] The proposed approach may be implemented with existing manufacturing equipment and processes. It is potentially a cost-effective alternative to expensive low-dielectric-loss substrates for reducing link loss at high data rates.

[0068] The preceding Description and accompanying Drawings describe examples of embodiments in some detail to aid understanding. However, the scope of protection may also include equivalents, permutations, and combinations that are not explicitly described herein. Only the claims appended here (along with those of parent, child, or divisional patents, if any) define the limits of the protected intellectual-property rights.

We claim:

1. A device, comprising:
 - a substrate;
 - a conductor laminated onto the substrate;
 - a first dielectric layer disposed on the top surface and sides of the conductor;
 - a second dielectric layer disposed on the substrate; and
 - a first open trench disposed in a second dielectric layer and filled with a low-loss ambient medium,wherein the first open trench is disposed between the second dielectric layer and the conductor, and
 - wherein the first open trench intersects an electromagnetic field induced in the dielectric layer by a signal traveling in the conductor.
2. The device of claim 1, further comprising a second open trench disposed in the second dielectric layer on an opposite side of the conductor from the first open trench,
 - wherein the second open trench is filled with the low-loss ambient medium, and
 - wherein the second open trench intersects an envelope of the electromagnetic field induced in the dielectric layer by the signal traveling in the conductor.
3. The device of claim 1, wherein the first open trench does not contact a conductive material of the conductor.
4. The device of claim 1, wherein the conductor is a single-ended signal trace.
5. The device of claim 1, wherein the conductor is a pair of traces carrying a differential signal.

6. The device of claim 5, further comprising a third open trench disposed in the second dielectric layer between the pair of traces;
wherein the third open trench is filled with the low-loss ambient medium, and
wherein the third open trench intersects an envelope of the electromagnetic field induced in the second dielectric layer by the signal traveling in the conductor.
7. The device of claim 1, wherein the conductor comprises a plurality of traces,
wherein the conductor has a first impedance, and
wherein an actual spacing between the traces is narrower than a calculated spacing predicted to produce the first impedance in a trenchless but otherwise identical conductor.
8. The device of claim 1, further comprising a first ground line on a first side of the conductor.
9. The device of claim 8, further comprising a second ground line on a second side of the conductor, wherein the second side of the conductor is opposite the first side of the conductor.
10. The device of claim 8, wherein the conductor comprises a microstrip or a planar waveguide.
11. A printed circuit board, comprising:
a first dielectric layer;
a conductor adjacent to the first dielectric layer, a portion of the first dielectric layer disposed on a top surface of the conductor,
wherein the conductor is disposed in a signal plane on the first dielectric layer; and
one or more open trenches adjacent to the conductor on the opposite side of the first dielectric layer,
wherein the one or more open trenches are parallel to the conductor, intersect an

electromagnetic field induced in the first dielectric layer by a signal traveling in the conductor, and are filled with a low-loss ambient medium.

12. The printed circuit board of claim 11, wherein the first dielectric layer comprises an epoxy.

13. The printed circuit board of claim 11, wherein the first dielectric layer comprises resin-impregnated cloth.

14. The printed circuit board of claim 11, wherein the conductor is plated.

15. The printed circuit board of claim 11, further comprising a ground backing layer under the first dielectric layer.

16. A method, comprising:

upon a substrate that has a composite dielectric layer,

forming a pair of conductive microstrips on the composite dielectric layer;

forming a plurality of trenches adjacent to the conductive microstrips wherein the

plurality of trenches extend through the composite dielectric layer;

assembling a mount on a top surface of each conductive microstrip; and

assembling at least one electrical component on a top surface of the pair of

conductive microstrips.

17. The method of claim 16 further comprising forming a plating layer on a top surface of the pair of conductive microstrips.

18. The method of claim 16, wherein the plurality of trenches are round-bottomed.

19. The method of claim 16, wherein the plurality of trenches are formed by at least one of laser ablation, photodisruption, laser cutting, thermal cutting, mechanical displacement, reactive-ion etching, or wet chemical etching.
20. The method of claim 16, wherein the pair of conductive microstrips are laminated on the composite dielectric layer.

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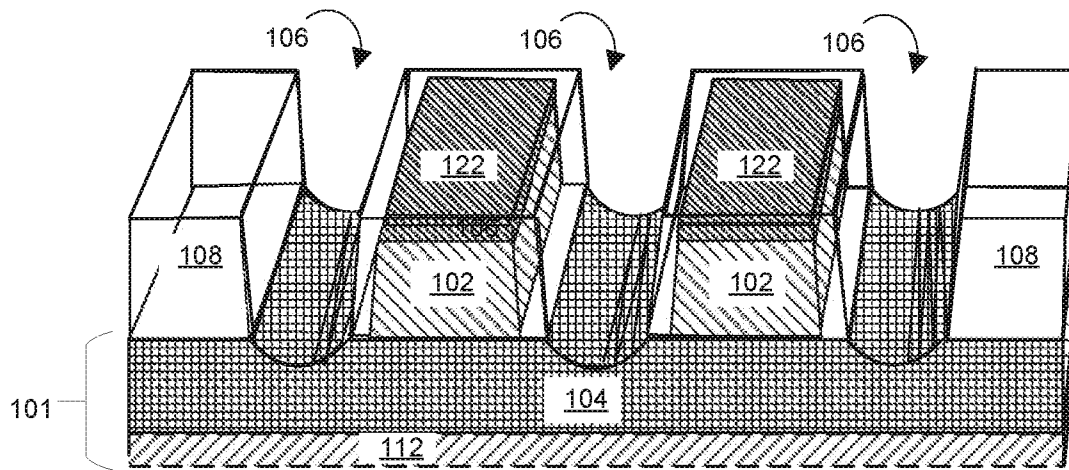


FIG. 1A

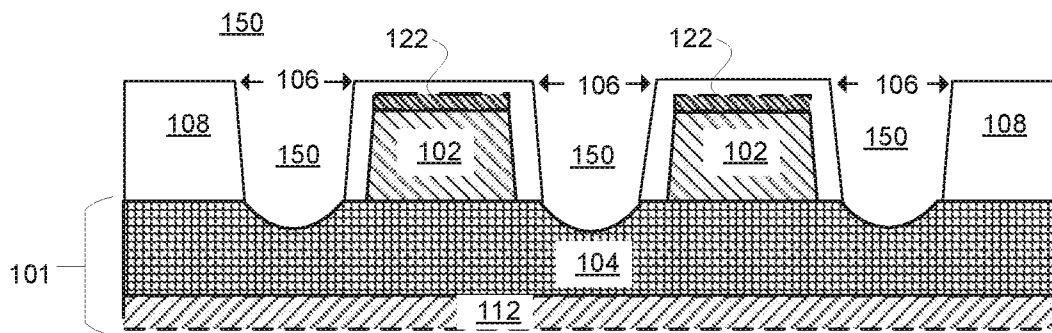


FIG. 1B

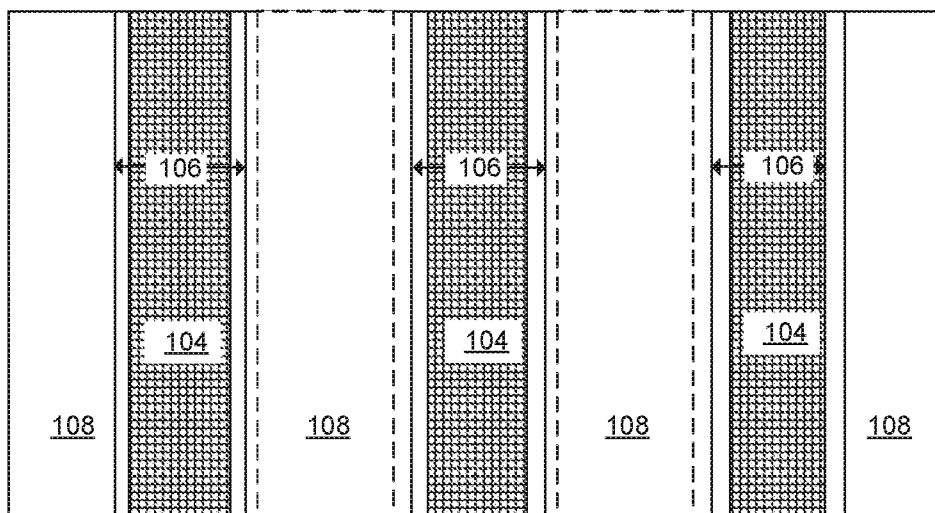


FIG. 1C

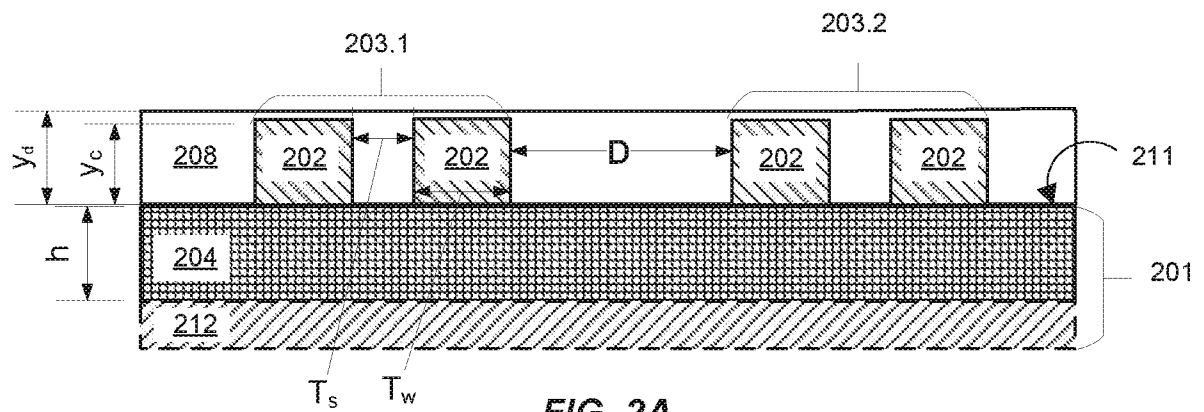


FIG. 2A

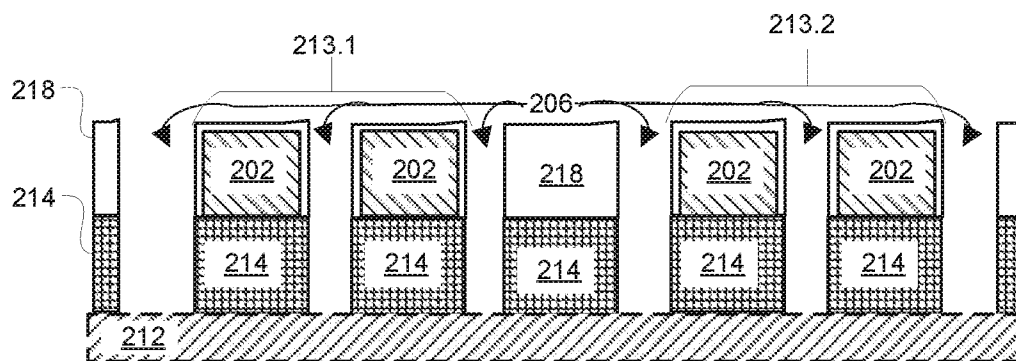


FIG. 2B

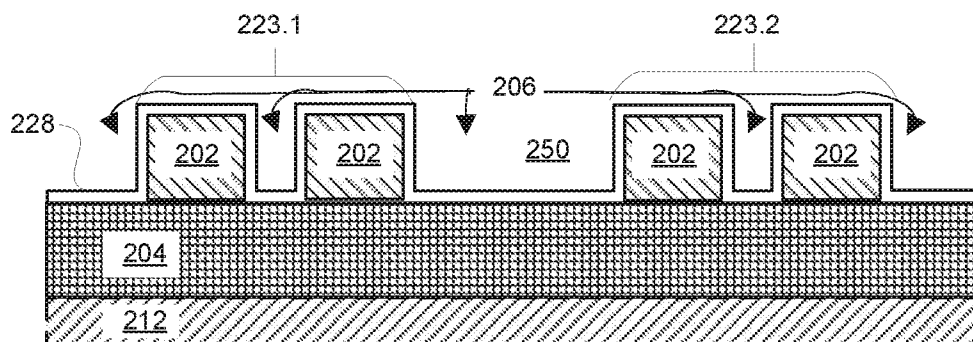


FIG. 2C

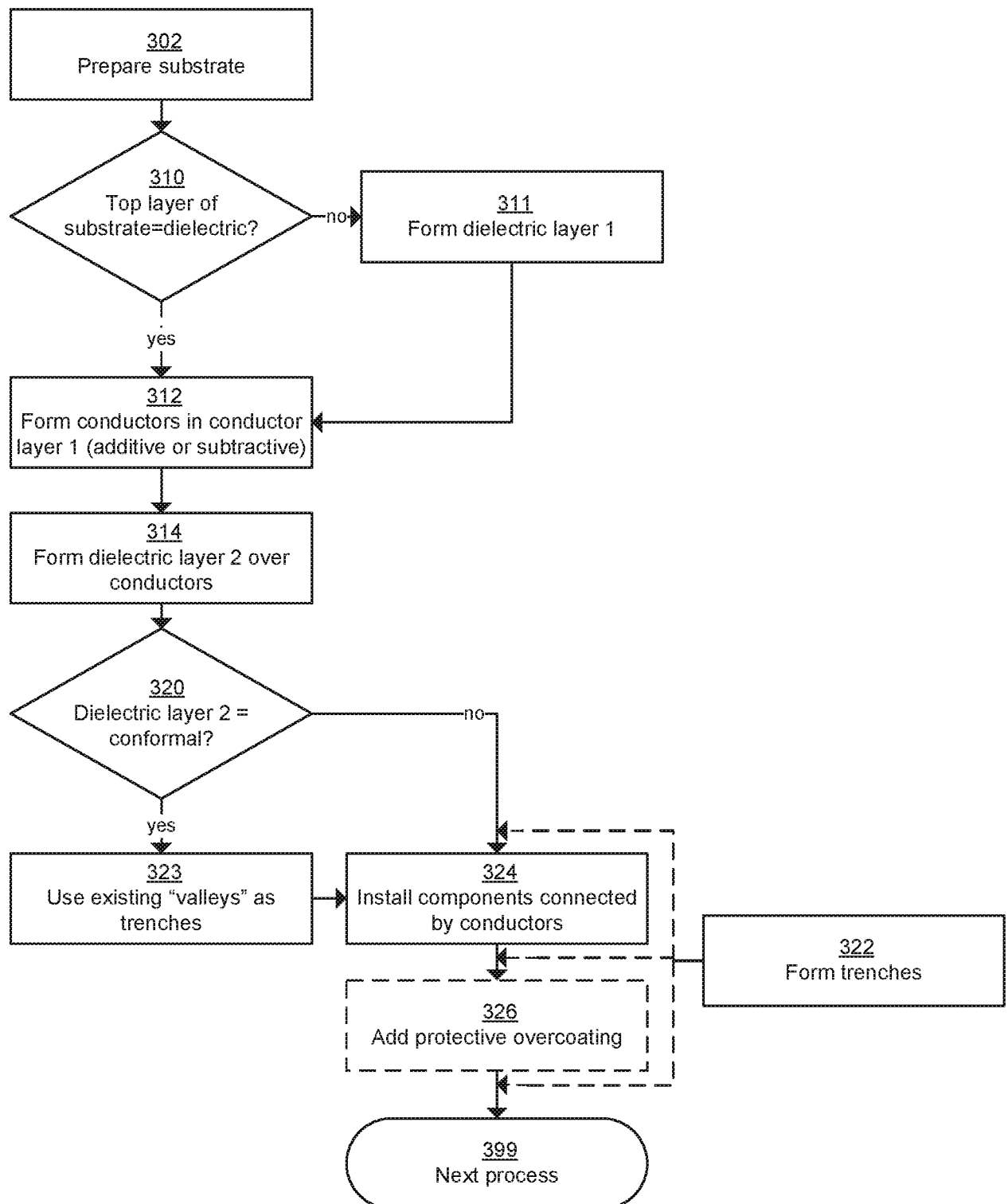


FIG. 3

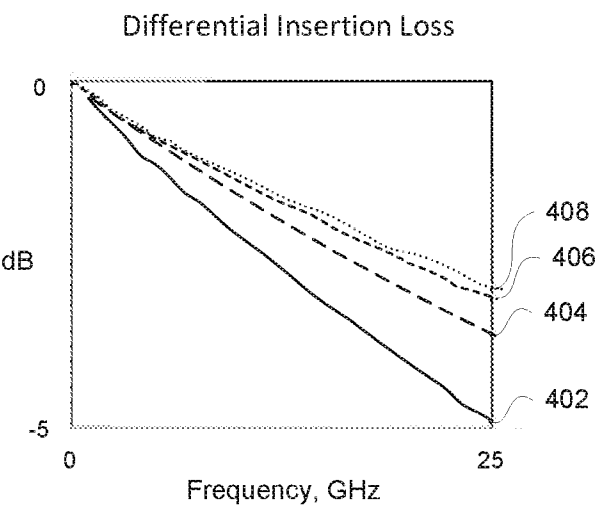


FIG. 4A

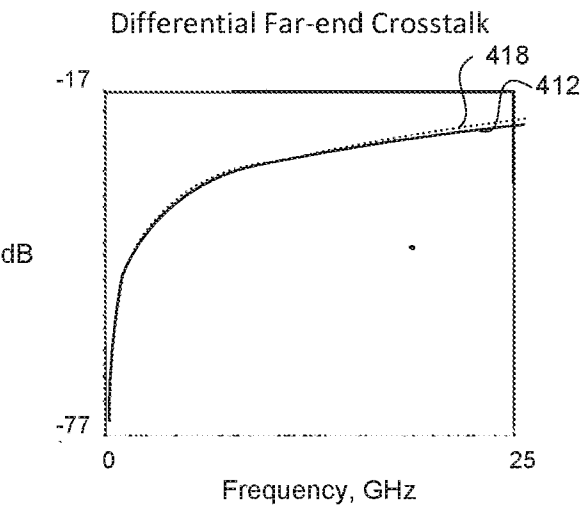


FIG. 4B

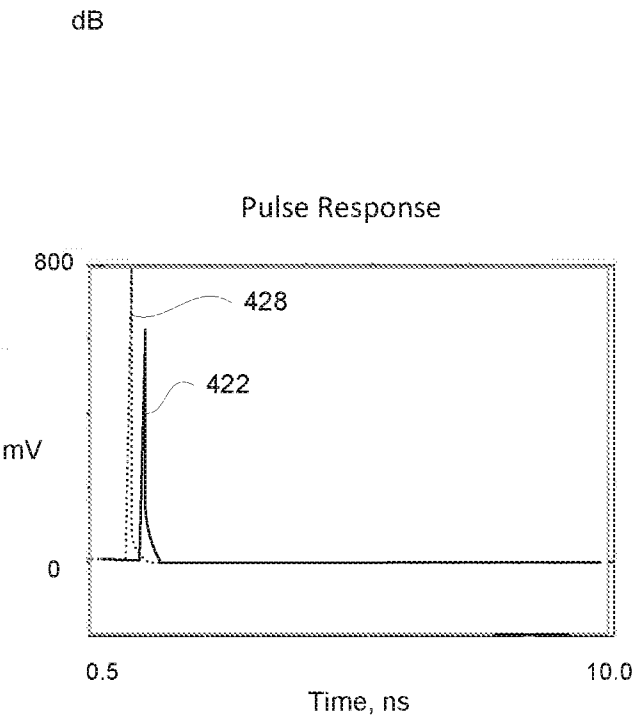


FIG. 4C

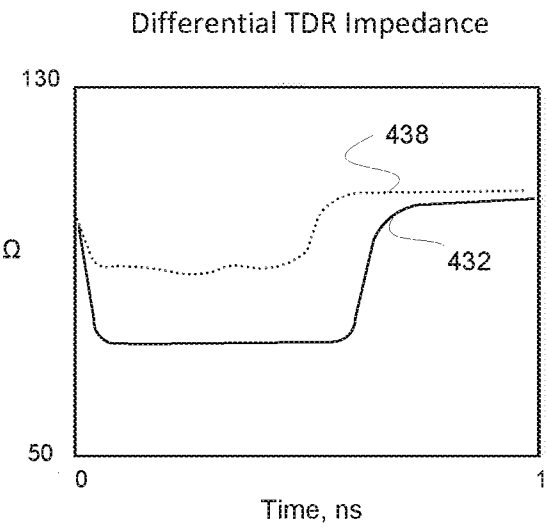


FIG. 4D

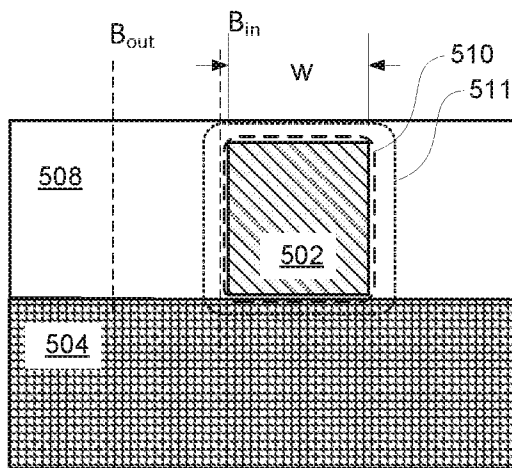


FIG. 5A

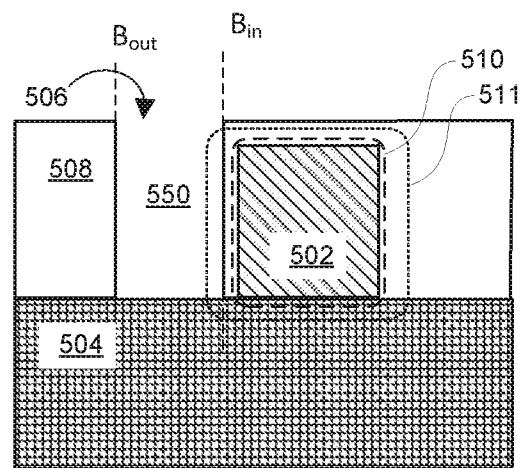


FIG. 5B

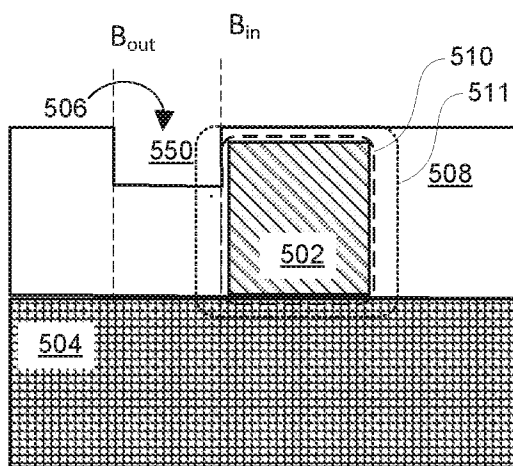


FIG. 5C

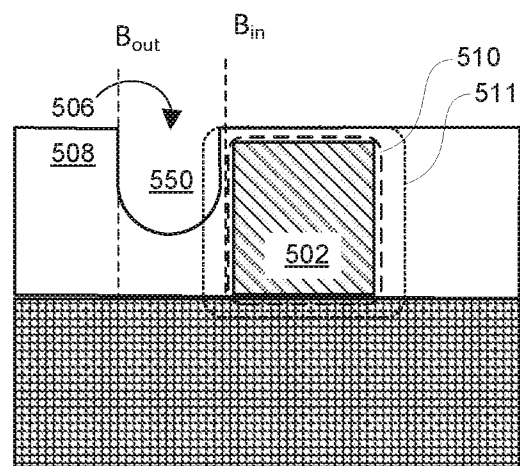


FIG. 5D

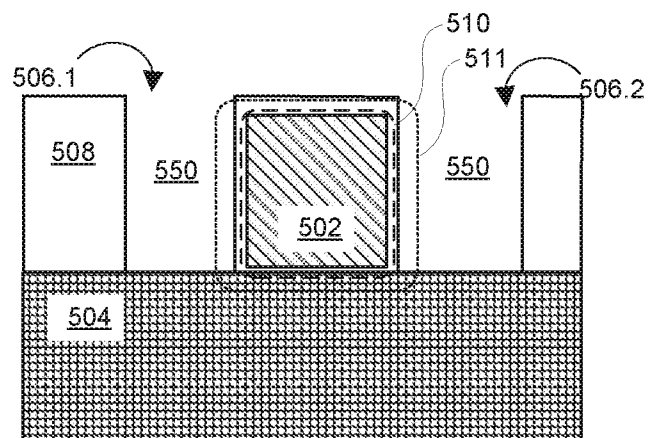


FIG. 5E

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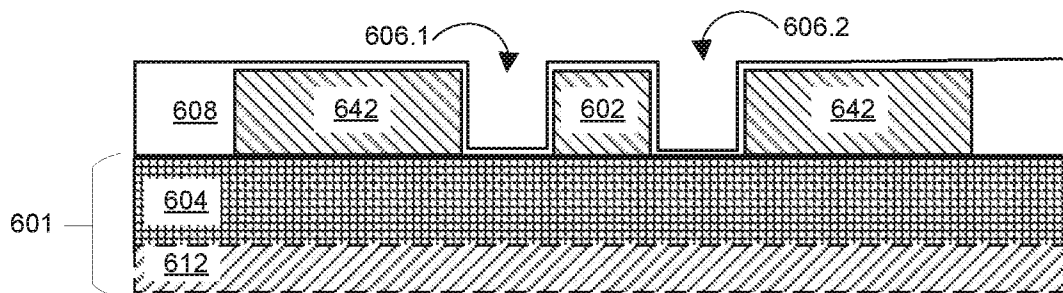


FIG. 6A

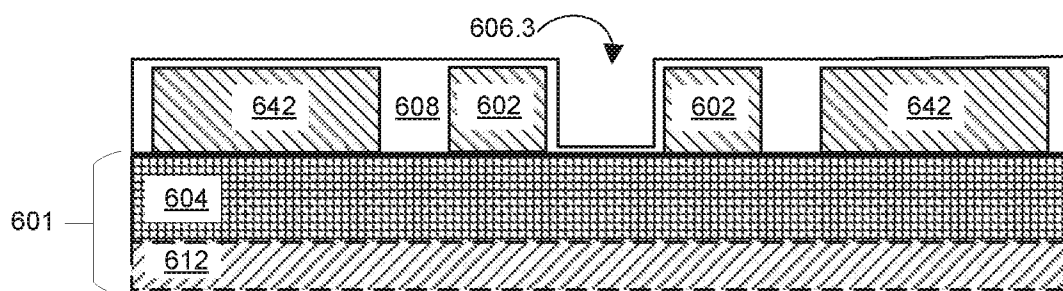


FIG. 6B

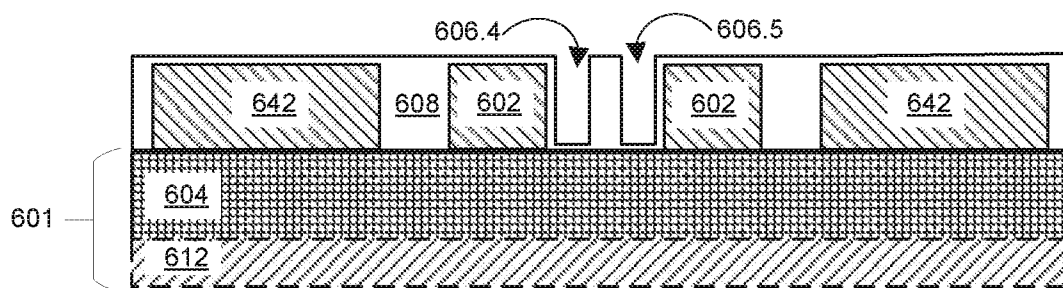


FIG. 6C

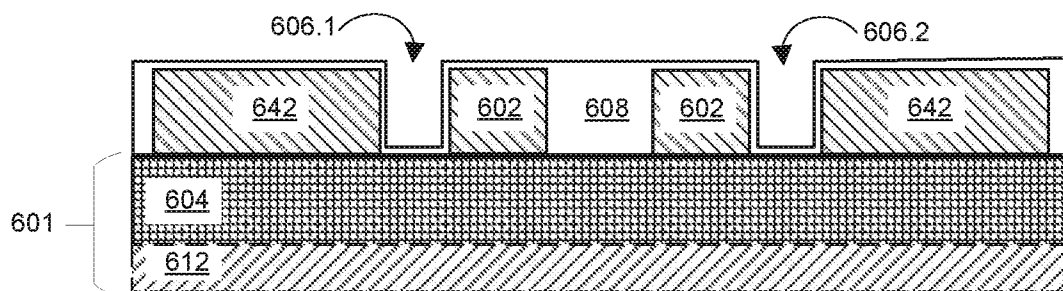


FIG. 6D

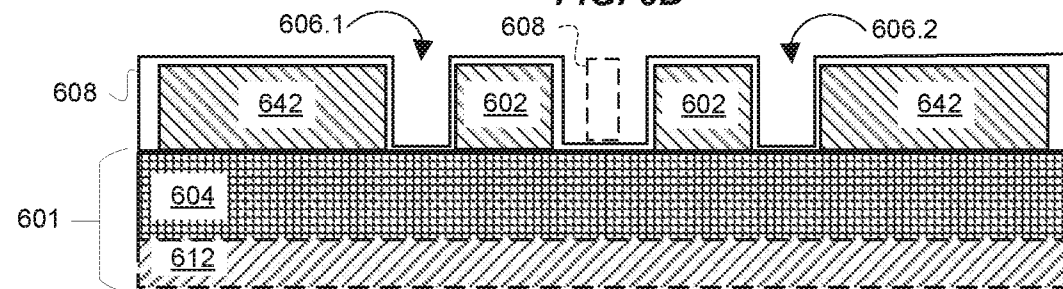


FIG. 6E

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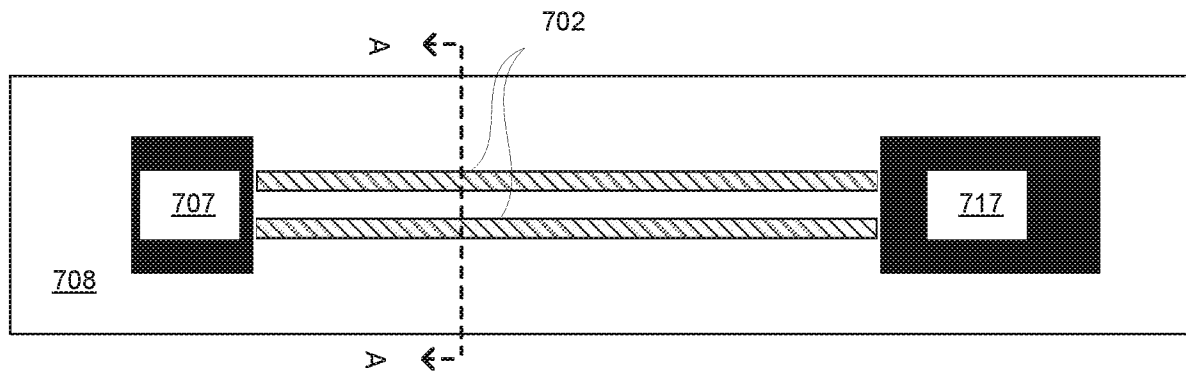


FIG. 7A

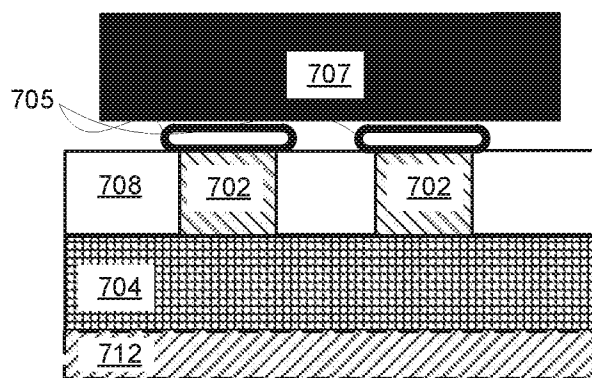


FIG. 7B

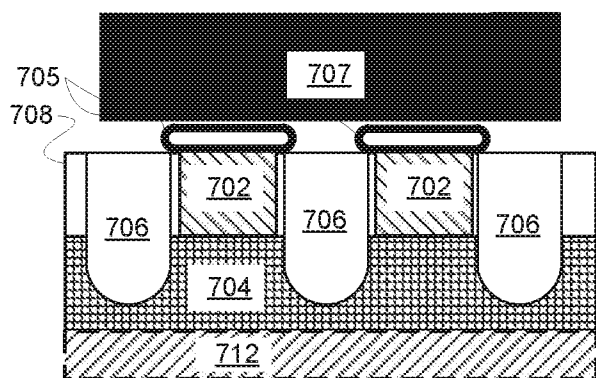


FIG. 7C

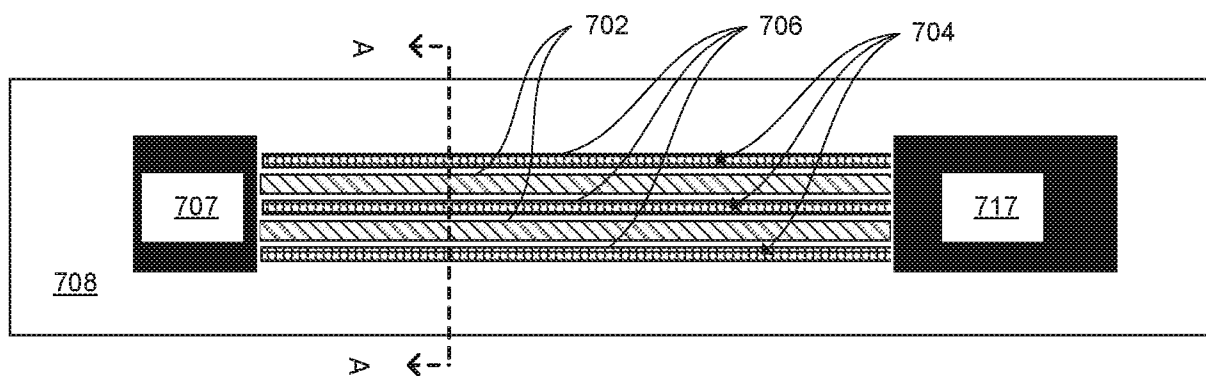


FIG. 7D

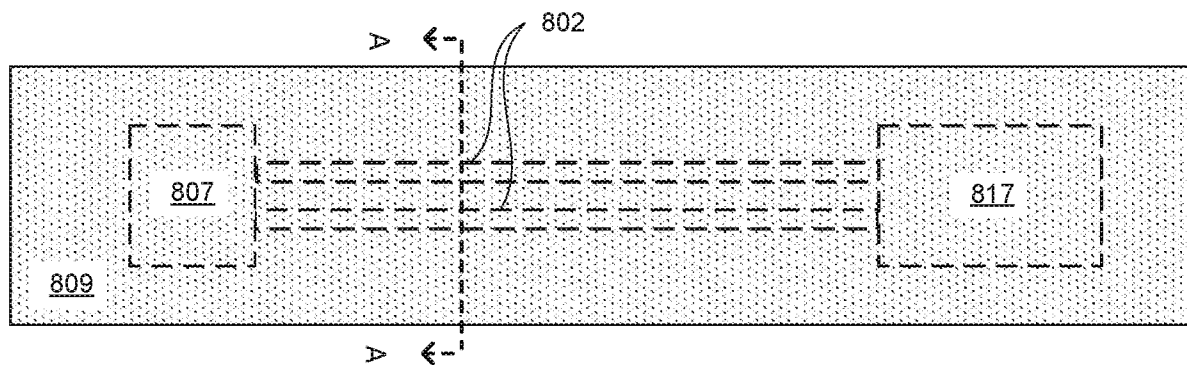


FIG. 8A

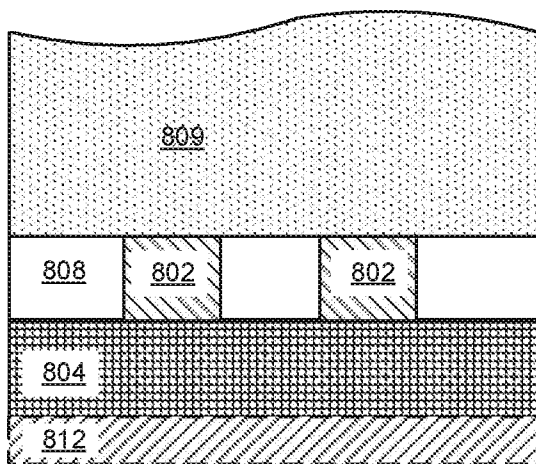


FIG. 8B

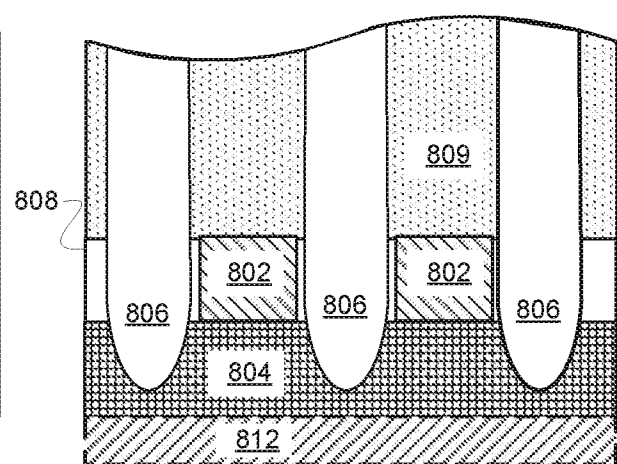


FIG. 8C

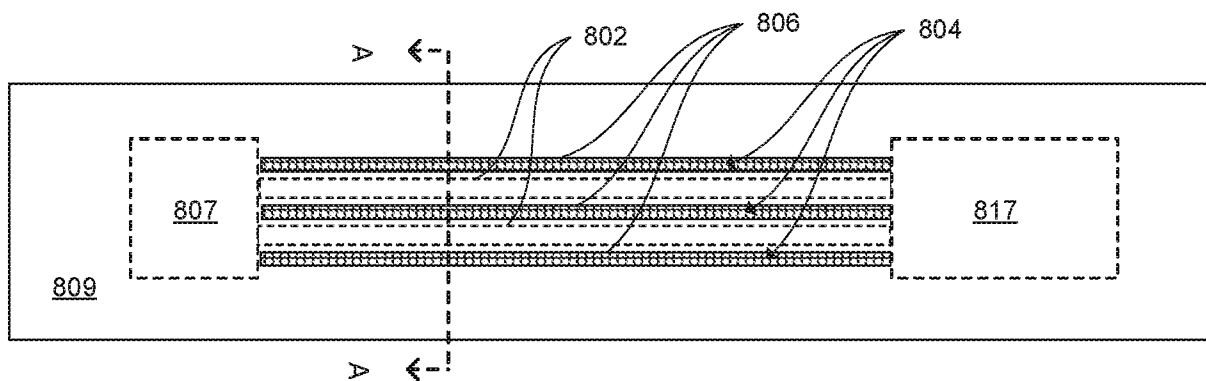


FIG. 8D

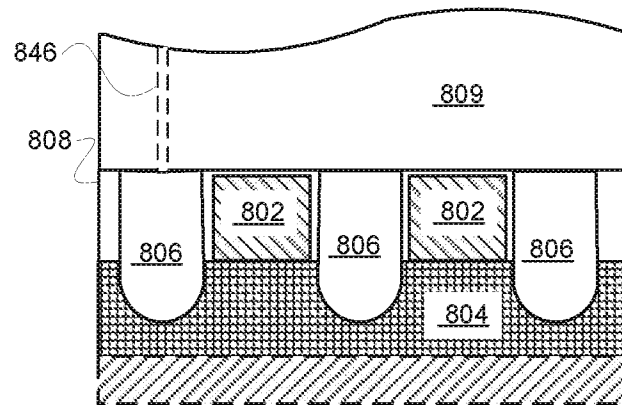


FIG. 8E

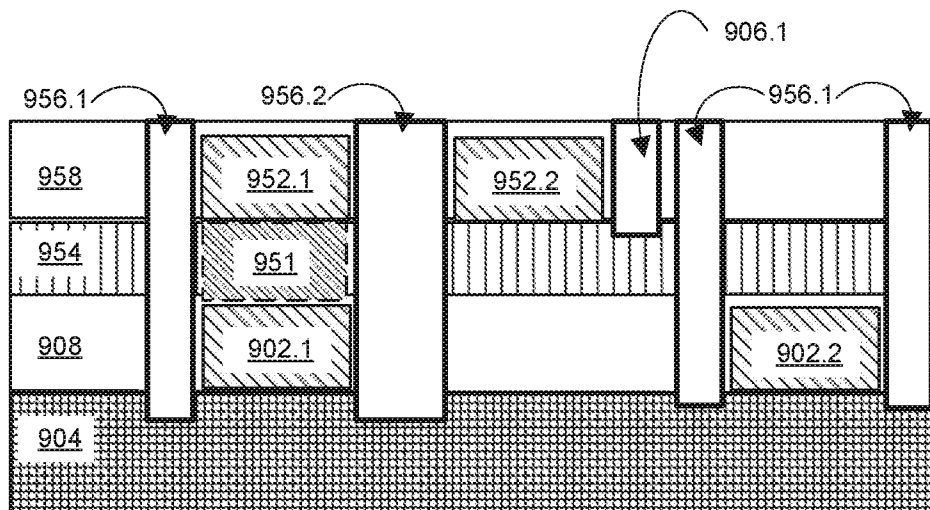


FIG. 9

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 16/50324

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I: Claims 1-15, drawn to a device and a printed circuit board.

Group II: Claims 16-20, drawn to a method of forming microstrip.

-- Please See Supplemental Box --

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-15

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 16/50324

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01G 4/33, H01L 21/31, H01L 21/765, H01L 21/8224, H01L 27/10 (2016.01)

CPC - H01G 4/33, H01L 21/31, H01L 21/765, H01L 21/76205, H01L 21/8224, H01L 27/10, H01L 27/10841

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC(8)- H01G 4/33, H01L 21/31, H01L 21/765, H01L 21/8224, H01L 27/10 (2016.01);

CPC- H01G 4/33, H01L 21/31, H01L 21/765, H01L 21/76205, H01L 21/8224, H01L 27/10, H01L 27/10841

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC- 257/296-306, 257/622, 257/E21.652, 257/E21.653, 438/239-256, 438/618-642;

Patents and NPL (classification, keyword; search terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Pub West (US EP JP WO), Pat Base (AU BE BR CA CH CN DE DK EP ES FI FR GB IN JP KR SE TH TW US WO), Google Patent, Google Scholar, Google Web, FPO; search terms: interconnect, trench, trough, groove, trace, fill, single, end, signal, laminate, low, loss, air, nitrogen, inert, argon, vacuum, suction, printed, circuit, board, cloth, impregnated, plate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2002/0050606 A1 (BUERGER JR.) 02 May 2002 (02.05.2002), Figs. 5, 23c, 31, 33c; para [0008] [0041], [0056], [0065], [0068], [0099], [0102], [0104], [0106], [0127], [0131]-[0133], [0135], [0138], [0140], [0146], [0149], [0153]	1-15
Y	US 6,444,922 B1 (KWONG) 03 September 2002 (03.09.2002), col 1, ln 56-65; col 2, ln 48-62; col 3, ln 17-33, col 4, ln 0-29, col 5, ln 38-61, col 7, ln 19-34.	1-15
Y, P	US 2015/0303177 A1 (BLANCHARD et al.) 22 October 2015 (22.10.2015), para [0018]-[0126]	1-15
Y	US 2014/0264573 A1 (KOCON et al.) 18 September 2014 (18.09.2014), para [0009]-[0222]	1-15
Y	US 2007/0164438 A1 (SIR et al.) 19 July 2007 (19.07.2007), para [0016]-[0094]	1-15

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

06 January 2017

Date of mailing of the international search report

19 JAN 2017

Name and mailing address of the ISA/US

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P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-8300

Authorized officer:

Lee W. Young

PCT Helpdesk: 571-272-4300

PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 16/50324

Continued from Box No. III, Observations where unity of invention is lacking,

The inventions listed as Groups I and II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special Technical Features

Group II do not require a device, comprising: a substrate; a conductor laminated onto the substrate; a first dielectric layer disposed on the top surface and sides of the conductor; a second dielectric layer disposed on the substrate; and a first open trench disposed in a second dielectric layer and filled with a low-loss ambient medium, wherein the first open trench is disposed between the second dielectric layer and the conductor, and wherein the first open trench intersects an electromagnetic field induced in the dielectric layer by a signal traveling in the conductor (as in Claim 1); or printed circuit board, comprising: a first dielectric layer; a conductor adjacent to the first dielectric layer, a portion of the first dielectric layer disposed on a top surface of the conductor, wherein the conductor is disposed in a signal plane on the first dielectric layer; and one or more open trenches adjacent to the conductor on the opposite side of the first dielectric layer, wherein the one or more open trenches are parallel to the conductor, intersect an electromagnetic field induced in the first dielectric layer by a signal traveling in the conductor, and are filled with a low-loss ambient medium (as in Claim 11), as required by Group I.

Group I do not require a method, comprising: upon a substrate that has a composite dielectric layer, forming a pair of conductive microstrips on the composite dielectric layer; forming a plurality of trenches adjacent to the conductive microstrips wherein the plurality of trenches extend through the composite dielectric layer; assembling a mount on a top surface of each conductive microstrip; and assembling at least one electrical component on a top surface of the pair of conductive microstrips (as in Claim 16), as required by Group II.

Shared Common Features

The only feature shared by Groups I and II that would otherwise unify the groups is a substrate, a dielectric layer, a conductor, trenches, and a top surface. However, this shared technical feature does not represent a contribution over prior art, because the shared technical feature is anticipated by US 1 to Chudzik, et al. (hereinafter 'Chudzik'). Chudzik discloses a substrate (para [0005]), a dielectric layer (para [0005]), a conductor (para [0013]), trenches (para [0008]), and a top surface (Fig. 1; para [0007], pad layer, 110.).

As the technical features were known in the art at the time of the invention, this cannot be considered a special technical feature that would otherwise unify the groups.

Groups I and II therefore lack unity under PCT Rule 13 because they do not share a same or corresponding special technical feature.