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SPRUSON & FERGUSON

- 7 APR 1986

APPLICATION ACCEPTED AND AMENDMENTS ALLOWED 13 - 11 - 87

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

CONVENTION APPLICATION FOR A STANDARD PATENT

We, NEC Corporation, of 33-1, Shiba 5-chome, Minato-ku, Tokyo, Japan hereby apply for the grant of a standard patent for an invention entitled:

"RADIO PAGER HAVING LOCAL- AND WIDE-AREA RECEPTION MODES"

which is described in the accompanying complete specification.

DETAILS OF BASIC APPLICATION

Number of Basic Application:-
60-73239

Name of Convention Country in which Basic Application was filed:-
Japan

Date of Basic application:-
6 April, 1985

Our address for service is:-

C/- Spruson & Ferguson
Patent Attorneys
Level 33 St Martins Tower
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Sydney New South Wales Australia

DATED this SEVENTH day of APRIL 1986

NEC Corporation

By: M.J. Anderson

Registered Patent Attorney.

TO: THE COMMISSIONER OF PATENTS
AUSTRALIA

FEE STAMP TO VALUE OF $ 165 ATTACHED
MAIL OFFICER

SBR/JS/0087M

Spruson & Ferguson

AUSTRALIA
CONVENTION
STANDARD
& PETTY PATENT
DECLARATION
SFP4

COMMONWEALTH OF AUSTRALIA

THE PATENTS ACT 1952

DECLARATION IN SUPPORT OF A CONVENTION APPLICATION FOR A PATENT

In support of the Convention Application made for a patent for an invention entitled:

of Invention "Radio Paper Having Local- and Wide-Area Reception Modes"

Full name(s) and address(es) of Declarant(s)

I/~~We~~ Susumu Uchihara

~~of~~ c/o NEC Corporation of 33-1, Shiba 5-chome, Minato-ku, Tokyo, Japan

do solemnly and sincerely declare as follows:–

Full name(s) of Applicant(s)

~~1. I am/We are the applicant(s) for the patent~~

(or, in the case of an application by a body corporate)

1. I am/~~We are~~ authorised by NEC Corporation

the applicant(~~s~~) for the patent to make this declaration on its/~~their~~ behalf.

2. The basic application(~~s~~) as defined by Section 141 of the Act was/~~were~~ made

Basic Country(ies) in Japan

Priority Date(s) on the 6th April, 1985

Basic Applicant(s) by NEC Corporation

~~3. I am/We are the actual inventor(s) of the invention referred to in the basic application(s)~~

Full name(s) and address(es) of inventor(s)

(or where a person other than the inventor is the applicant)

3. Koichi NAGATA and Yohichiro MINAMI

both ~~of~~ c/o NEC Corporation of 33-1, Shiba 5-chome, Minato-ku, Tokyo, Japan

~~(respectively)~~

~~is~~/are the actual inventor(s) of the invention and the facts upon which the applicant(~~s~~) is/~~are~~ entitled to make the application are as follows:

Set out how Applicant(s) derive title from actual inventor(s) e.g. The Applicant(s) is/are the assignee(s) of the invention from the inventor(s)

The said applicant is the assignee of the actual inventors.

4. The basic application(~~s~~) referred to in paragraph 2 of this Declaration was/~~were~~ the first application(~~s~~) made in a Convention country in respect of the invention(~~s~~) the subject of the application.

Declared at Tokyo, Japan this 31st day of March, 1986

NEC Corporation

Susumu Uchihara
Signature of Declarant(s)

Susumu Uchihara
General Manager, Patents Division

To: The Commissioner of Patents

(12) PATENT ABRIDGMENT (11) Document No. AU-B-55698/86
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 592783

(54) Title
RADIO PAGER BI-CHANNEL RECEIVE ALERT

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58091/86 G06F 9/06; H04B 5/04, 7/26
31757/84 574379 G08B 7/06; H03J 9/02; H04B 1/04, 1/16,
75840/81 553165 G06F 9/06; H04B 5/04, 7/26

(57) Claim

1. A radio pager comprising:

manually controlled channel selecting means for selecting a first channel to operate the pager in a local area reception mode and a for selecting a second channel to operate the pager in a wide area reception mode;

receiving means responsive to said channel selecting means for receiving a first paging signal which is transmitted on the first channel and for receiving a second pageing signal transmitted on the second channel, said first paging signal containing an address in a Bose-Chaudhuri-Hocquenghem ("BCH")(L,M) code format and said second paging signal containing an address in a BCH(L,N) code format, where L>N>M;

a shift register having L-bit positions in which the address of either the received first or second paging signal is sequentially stored;

first and second memories respectively operable during said local area reception mode and wide area reception mode, said first and second memories having L-bit memory elements coupled respectively to the L-bit positions of said shift register and memorizing a user's first identification number in said BCH (L,M) code format and a user's second

identification number in said BCH (L,N) code format, respectively, and for generating a coincidence signal as an indication of reception of said first or second paging signal when the address stored in said shift register coincides with one of said user's identification numbers in said first and second memories; and

means responsive to said coincidence signal for producing a paging signal.

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PATENTS ACT 1952

COMPLETE SPECIFICATION

(ORIGINAL)

FOR OFFICE USE:

55698/86

Class Int. Class

Complete Specification Lodged:

Accepted:

Published:

Priority:

Related Art:

Name of Applicant: NEC Corporation

Address of Applicant: 33-1, Shiba 5-chome, Minato-ku, Tokyo, Japan

Actual Inventor(s): KOICHI NAGATA and YOHICHIRO MINAMI

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Complete Specification for the invention entitled:

"RADIO PAGER HAVING LOCAL- AND WIDE-AREA RECEPTION MODES"

The following statement is a full description of this invention, including the best method of performing it known us

SBR/JS/0087M

"Radio Pager Having Local- and Wide-Area Reception Modes"

APSTRACT OF THE DISCLOSURE

Disclosed is a radio pager wherein a manually controlled channel selector selects a first channel to operate the pager in a local area reception mode and selects a second channel to operate it in a wide area reception mode. A receiving circuit is responsive to the selector for receiving a first paging signal transmitted on the first channel and receiving a second paging signal transmitted on the second channel, the first and second paging signals containing address signals in first and second code formats, respectively. A decoder is responsive to the manual selector for comparing the address signal of the first paging signal with a first identification signal representing a user's identification number in the first code format and comparing the address signal of the second paging signal with a second identification signal representing the same user's identification number in the second code format. The decoder produces a coincidence signal when the address signal of each paging signal coincides with the identification signal of the corresponding code format to generate an audible tone.

The present invention relates to a radio pager which is capable of operation in a local-area reception mode and in a wide-area reception mode.

Conventional radio pagesr are assigned with an identification code representing the user's identification number. Theidentification code is in the Bose-Chaudhuri-Hocquenghem (31, 16) format for a given local area and transmitted on a specified radio frequency channel. The total number of subscribers available with the BCH (31, 16) code format is 65,536. Therefore, if the number of subscribers exceeds the limit, an extra radio frequency channel is required to accommodate new subscribers and this procedure must be repeated in units of 65,625 new subscribers.

It is therefore an object of the present invention to provide a radio pager which permits efficient utilization of radio frequency channels.

According to one aspect of the present invention there is disclosed a radio pager comprising:

manually controlled channel selecting means for selecting a first channel to operate the pager in a local area reception mode and a for selecting a second channel to operate the pager in a wide area reception mode;

receiving means responsive to said channel selecting means for receiving a first paging signal which is transmitted on the first channel and for receiving a second pageing signal transmitted on the second channel, said first paging signal containing an address in a Bose-Chaudhuri-Hocquenghem ("BCH")(L,M) code format and said second paging signal containing an address in a BCH(L,N) code format, where L>N>M;

a shift register having L-bit positions in which the address of either the received first or second paging signal is sequentially stored;

first and second memories respectively operable during said local area reception mode and wide area reception mode, said first and second memories having L-bit memory elements coupled respectively to the L-bit positions of said shift register and memorizing a user's first identification number in said BCH (L,M) code format and a user's second identification number in said BCH (L,N) code format, respectively, and for generating a coincidence signal as an indication of reception of said first or second paging signal when the address stored in said shift register coincides with one of said user's identification numbers in said first and second memories; and

means responsive to said coincidence signal for producing a paging signal.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described in further detail with reference to the accompanying drawings, in which:

Figure 1 is a block diagram of a radio pager according to a preferred embodiment of the invention;

Figure 2 is a block diagram of the decoder of Figure 1; and

Fig. 3 is a block diagram of a modified embodiment of the invention.

DETAILED DESCRIPTION

Referring to Fig. 1, there is shown a multi-channel radio paging receiver, or pager according to the present invention. In Fig. 1, first and second paging signals are frequency-modulated respectively upon first and second channels and transmitted from a transmitting station for local and wide area services, respectively. Each paging signal comprises a selective calling address signal and a message signal. The address signal of the first paging signal is in the Bose-Chaudhuri-Hocquenghem (31, 16) code format for local area service and the address signal of the second paging signal is in the BCH (31, 21) code format for wide area service. The total capacity of codes that can be transmitted on the first channel for local area is 65,536, whereas the total capacity of codes that can be transmitted on the second channel for wide area is 2,097,152, a value 32 times greater than that available for local-area service. This is best understood by analyzing the BCH (31, 21) code and BCH (31, 16) code as follows. Let it be assumed that generator polynominals are represented by:

$$M_1(x) = x^5 + x^2 + 1$$

$$M_3(x) = x^5 + x^4 + x^3 + x^2 + 1$$

$$M_5(x) = x^5 + x^4 + x^2 + x + 1$$

then the generator polynomial of the BCH (31, 21) code is given by:

$$M_1(x) * M_3(x) = x^{10} + x^9 + x^8 + x^6 + x^5 + x^3 + 1$$

and the generator polynomial of the BCH (31, 16) code is given by:

$$M_1(x) * M_3(x) * M_5(x) = x^{15} + x^{11} + x^{10} + x^9 + x^8 + x^7 + x^5 + x^3 + x^2 + x + 1$$

Since $M_1(x) * M_3(x)$ is a common term of the two generator polynomials, the BCH (31, 16) code is a part of the BCH (31, 21) code.

The paging signal is intercepted by an antenna 1, filtered through a band-pass amplifier 2 and fed to a frequency converter 3 to which is also applied the output of a variable frequency local oscillator 4. The radio-frequency signal is transposed to an intermediate-frequency signal by the frequency converter 3 and fed to a frequency demodulator 5 and thence to a waveshaper 6. Waveshaper 6 comprises a low-pass filter for eliminating undesirable high frequency components of the demodulated signal and a comparator for comparing the output of the low-pass filter with a threshold to generate a dignal signal which is a replica of the original signal comprising a message signal preceded by a selective calling signal. The output of waveshaper 6 is connected to a display unit 7 and to a decoder 8 which decodes the address signal by

comparing it with an identification code and activates an audio-frequency oscillator 9 to generate an audible tone by a loudspeaker 10 when the address signal coincides with the identification code. Display unit 7 essentially comprises a message decoder and a liquid-crystal display to provide a visual display of a message following an address signal. A user carrying the pager is thus alerted of the reception of a page from a caller.

Variable frequency local oscillator 4 includes a crystal-controlled Colpitts circuit which is formed by a transformer 402 in parallel with a capacitor 403, the transformer being coupled by a parallel circuit of a bypass capacitor 406 and a biasing resistor 407 to the emitter of transistor 408. The emitter of transistor 408 is further coupled to its base by a capacitor 409 and the collector of transistor 408 is connected by a bypass capacitor 411 to ground, by a biasing resistor 410 to its base and directly to a DC voltage source 11. The base of transistor 408 is connected through a local-area selecting circuit to a series of a quartz crystal 414 and a variable capacitor 415 and through a wide-area selecting circuit to a series of a quartz crystal 412 and a variable capacitor 413.

A high-frequency tuning circuit is formed by a transformer 404 and a capacitor 405 connected in parallel therewith. The high-frequency tuning transformer 404 has

one end connected through a coupling capacitor 401 to the frequency converter 3. Transformer 402 is connected through an intermediate tap of transformer 404 to ground.

The operating parameters of the local oscillator are determined so that the combined impedance of the two tuning circuits as seen from across the emitter of transistor 408 and ground is capacitive in the variable range of frequencies generated by quartz crystals 412 and 414. In a practical embodiment, each of the quartz cyrstals has an oscillating frequency which is 1/3 of the difference in frequency between the frequency of the respective channel and the intermediate frequency.

The local-area selecting circuit is established when a first area-selecting switch 12 couples the quartz crystal 414 through contacts 106 and 105 to the base of transistor 408 and the wide-area selecting circuit is established when the switch 12 is moved to a position connecting the quartz crystal 412 through contacts 105 and 104 to the base of the transistor.

Decoder 8 comprises a shift register 80 having 31 bit positions into which the address code is sequentially stored, and a local-area memory 84 and a wide-area memory 83. Local-area memory 84 is enabled by DC voltage source 11 when a second area-selecting switch 13, which is ganged to switch 12, couples the DC source thereto through contacts

102 and 103 and memory 83 is enabled by DC voltage source 11 when the second switch 13 is moved to a position connecting the source voltage thereto through contacts 102 and 101. Each of the memories 83 and 84 has memory cells corresponding in number to the bit positions of shift register 80.

As shown in Fig. 2, each memory cell of memories 83 and 84 is formed by a Zener diode 810, a transistor 820, and a protection resistor 830. Each Zener diode has its cathode connected to an associated input bit line 81 and its anode connected to the base of the associated transistor. Each of the transistors 820 has its collector coupled to a common output line 82 and to contact 101 or 103 through a common resistor 840 and has its emitter connected through the respective resistor 830 to ground.

The user's identification code bits are stored into memory cells by destroying particular Zener diodes to transform them into mere resistance elements. This is accomplished by applying a high positive DC potential to associated input bit lines 81 and a negative DC potential to an output line 82. Resistors 830 serve as a means for protecting the associated transistor from being damaged by the high DC potential. An identification number assigned to the user in the BCH (31,16) code format is stored in local-area memory 84 and the same identification number in

the BCH (31,21) code format is stored in wide-area memory 83.

When a logical "1" input is applied, the memory cell having a destroyed Zener diode develops a logical "0" output at the collector of the associated transistor and the memory cell having a non-destroyed Zener diode develops a logical "1" output, and when a logical "0" input is applied, the memory cell having a destroyed Zener diode develops a logical "1" output and the cell having a non-destroyed Zener diode develops a logical "0" output. Since the transistors 820 of all cells of each memory are connected in parallel, they establish an AND gate to produce a logical "1" output at the output line 82 when there is a one-to-one coincidence between the address code and identification code. The coincidence output from each memory is coupled by an OR gate 85 to oscillator 9 to activate the speaker 10 and to a control terminal of the display unit 7 to provide a display of a message signal following the address signal.

From the transmitting station, two paging signals respectively having BCH (31,16) and BCH (31,21) formatted address signals are respectively transmitted on the local-area channel and wide-area channel. When the user is in his own local service area, switches 12 and 13 are positioned so that quartz crystal 414 and memory 84 are enabled. Oscillator 4 is tuned to the local-area channel to

check the BCH (31,16) address signal transmitted on the local-area channel against the BCH (31,16) identification code stored in memory 84. When the user enters the wide service area, switches 12 and 13 are moved to wide-area service positions so that quartz crystal 412 and memory 83 are enabled. Oscillator 4 is tuned to receive the wide-area channel to decode the BCH (31,21) address signal transmitted on the wide-area channel by comparing it with the BCH (31,21) identification code stored in memory 83.

It is preferred that error correction circuits be provided respectively for correcting errors in the address signals of the BCH (31, 21) and BCH (31,16) code formats. In Fig. 3, a 1-bit error correction circuit 86 and a 2-bit error correction circuit 87 are provided to receive the output of waveshaper 6. Each error correction circuit includes a buffer, or shift register into which the received address signal is sequentially loaded in a manner as it is loaded into the shift register of Fig. 2. The address bits stored in the shift register undergo an error correction process known in the art. The 1-bit error correction circuit 86 is connected to the contact 101 so that it is enabled simultaneously with memory 83 during wide-area reception mode and the 2-bit error correction circuit 87 is connected to the contact 103 to be enabled with memory 84 during local-area reception mode. During local-area

reception mode, 2-bit error correction is performed by circuit 87 on the address signal of the BCH (31, 16) code format and during wide-area reception mode, 1-bit error correction is performed by circuit 86 on the address signal of the BCH (31, 21) code format. The error-corrected 31-bit address signals are applied from error correction circuits 86 and 87 are respectively applied to memories 83 and 84 on input lines 81.

The claims defining the invention are as follows:

1. A radio pager comprising:

manually controlled channel selecting means for selecting a first channel to operate the pager in a local area reception mode and a for selecting a second channel to operate the pager in a wide area recention mode;

receiving means responsive to said channel selecting means for receiving a first paging signal which is transmitted on the first channel and for receiving a second pageing signal transmitted on the second channel, said first paging signal containing an address in a Bose-Chaudhuri-Hocquenghem ("BCH")(L,M) code format and said second paging signal containing an address in a BCH(L,N) code format, where L>N>M;

a shift register having L-bit positions in which the address of either the received first or second paging signal is sequentially stored;

first and second memories respectively operable during said local area reception mode and wide area reception mode, said first and second memories having L-bit memory elements coupled respectively to the L-bit positions of said shift register and memorizing a user's first identification number in said BCH (L,M) code format and a user's second identification number in said BCH (L,N) code format, respectively, and for generating a coincidence signal as an indication of reception of said first or second paging signal when the address stored in said shift register coincides with one of said user's identification numbers in said first and second memories; and

means responsive to said coincidence signal for producing a paging signal.

2. A radio pager as claimed in claim 1, wherein said user's first identification number is the same as said user's second identification number.

3. A radio pager as claimed in claim 1, further comprising a first error correction circuit operable during said local-area receiption mode and a second error correction circuit operable during the wide-area reception mode, said first error correction circuit providing two-bit error correction on the address signal of the BCH (L,M) code format and said second error correction circuit providing 1-bit error correction on the address signal of the BCH (L,N) code format.

4. A radio pager as claimed in claim 3, wherein L, M and N are 31, 16 and 21 respectively.

5. A radio pager as claimed in claim 1, further comprising means for decoding said first and second paging signals into corresponding display signals in response to said coincidence signal from said first and second memories and means for displaying said display signals.

6. A radio pager as claimed in claim 1, wherein the memory elements of each of said first and second memories comprise a plurality of breakdown diodes and a plurality of transistors forming a plurality of sets with said breakdown diodes, wherein a certain of said breakdown diodes is destroyed in accordance with one of said user's identification numbers, a first electrode of the breakdown diode of each of the sets being connected to a corresponding one of the L-bit positions of the shift register, and the transistor of the set having a control electrode connected to a second electrode of the breakdown diode of the set and having controlled electrodes biased to produce an output signal when coincidence cocurs between a binary state of the breakdown diode of the set and a binary state of the corresponding bit position of the shift register.

7. A radio pager substantially as described with reference to Figures 1 and 2 or Figure 3 of the accompanying drawings.

DATED this SECOND day of NOVEMBER 1989
NEC Corporation

Patent Attorneys for the Applicant
SPRUSON & FERGUSON

HRF/0193y

FIG. 1

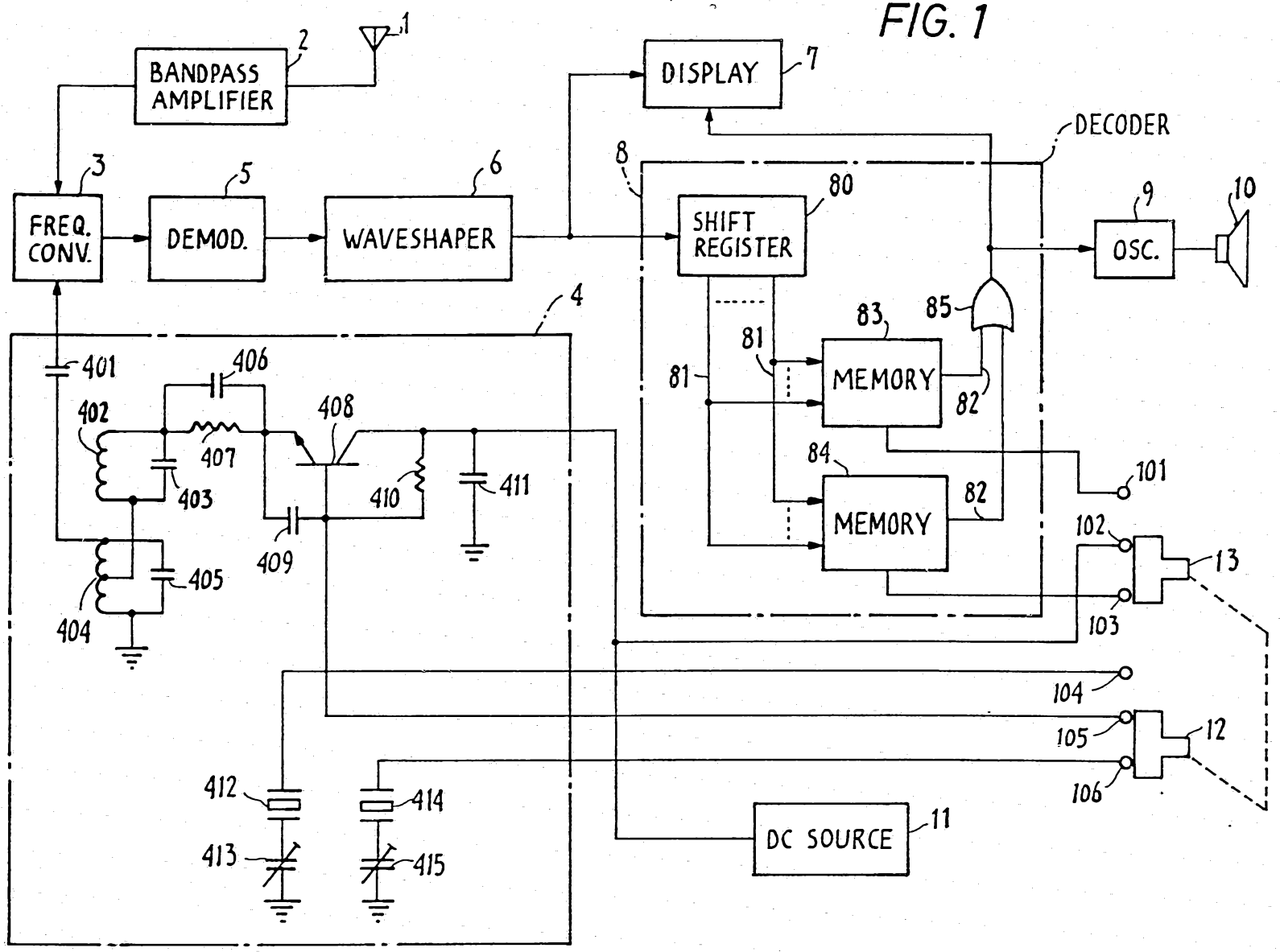


FIG. 2

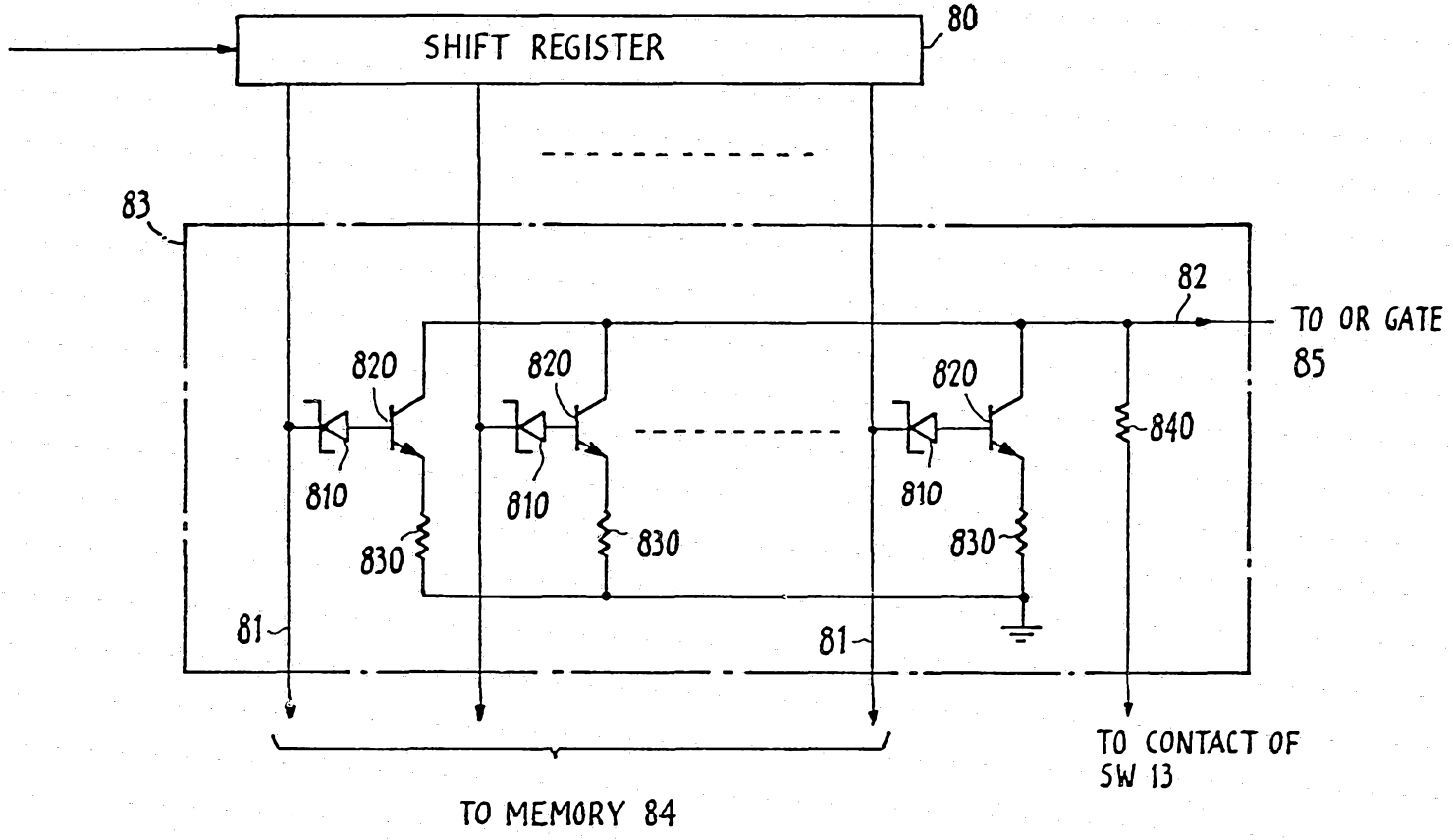
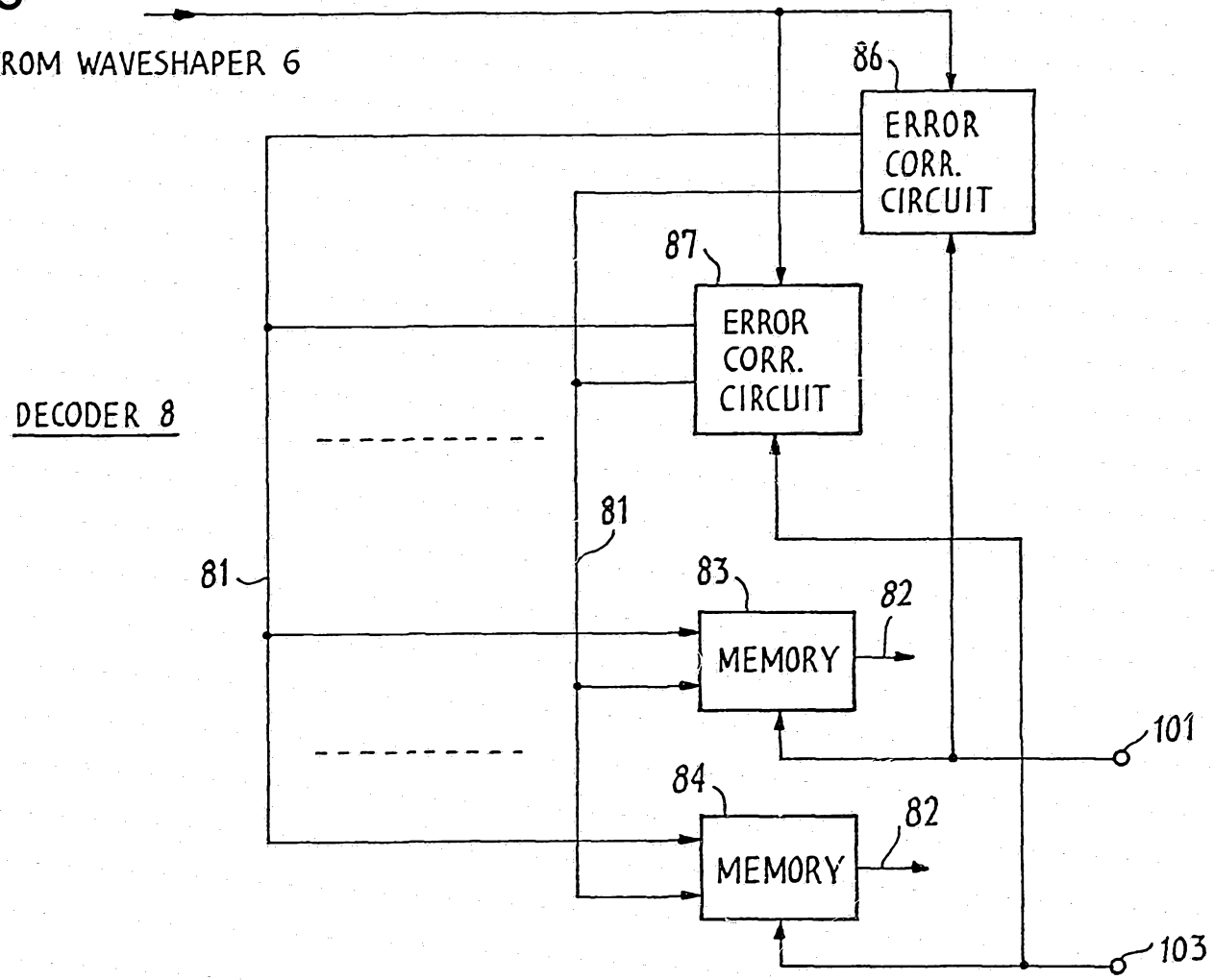

SHIFT REGISTER
80
83
82
TO OR GATE
85
820
820
820
810
810
810
830
830
830
840
81
81
TO CONTACT OF
SW 13
TO MEMORY 84

FIG. 3


FROM WAVESHAPER 6
86
ERROR CORR. CIRCUIT
87
ERROR CORR. CIRCUIT
DECODER 8
81
81
83
82
MEMORY
101
84
82
MEMORY
103