

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
16 October 2008 (16.10.2008)

PCT

(10) International Publication Number
WO 2008/123766 A2

- (51) International Patent Classification:
H05K 1/05 (2006.01)
- (21) International Application Number:
PCT/MY2008/000028
- (22) International Filing Date: 4 April 2008 (04.04.2008)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
PI 20070532 5 April 2007 (05.04.2007) MY
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- (81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KH, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— without international search report and to be republished upon receipt of that report

(54) Title: HIGH THERMAL-EFFICIENT METAL CORE PRINTED CIRCUIT BOARD WITH SELECTIVE ELECTRICAL AND THERMAL CIRCUITRY CONNECTIVITY

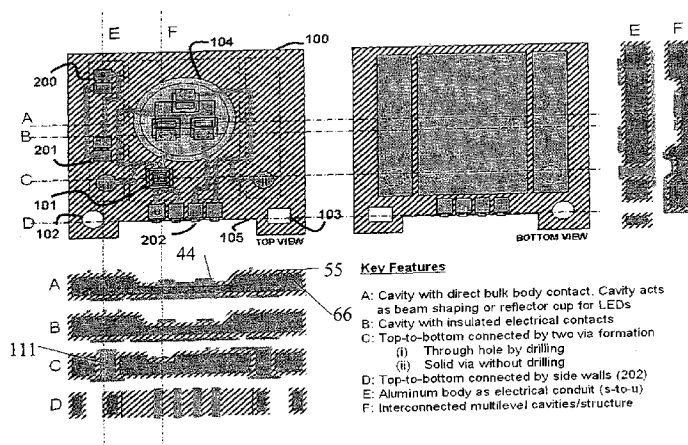


FIG. 2a

(57) Abstract: In accordance with the present invention, a thermally-efficient metal core printed circuit board comprises a metal base (66) including opposing first face and a second face, and the said faces with a plurality of dispersed dielectric (55) or insulating layer selectively fabricated overlying the metal base (66) resulting in a planar surface for the overlying circuitries, a plurality of dispersed thermal metallization layer connected directly to the metal base (66) for optimum thermal performance and a plurality of electrical circuitries connected accordingly to the profile of the metal body for the multi-layer electrical circuit connectivity. The selective dielectric (55) or insulation layer configuration allows direct thermal pad contact to the bulk metal base (66) and insulation for the electrical terminals resulting in high thermal-efficient circuit board for single, matrix, multi-chip device assembly and motherboard applications. The selective dielectric and metallization topology is also applicable to 3D heat sink structure.

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**HIGH THERMAL-EFFICIENT METAL CORE PRINTED CIRCUIT BOARD
WITH SELECTIVE ELECTRICAL AND THERMAL CIRCUITRY
CONNECTIVITY**

FIELD OF THE INVENTION

- 5 The present invention relates to a high thermal-efficient metal core printed circuit board with selective electrical and thermal circuitry connectivity.

BACKGROUND OF THE INVENTION

The need for high thermal performance substrates or printed circuit board is well known in the electronic industry. Although the metal core printed circuit board or substrate have
10 been in used for many years, these known prior art substrates or metal core printed circuit board or more commonly known as insulated metal substrates have known deficiencies.

This invention relates to a thermally-efficient metal core printed circuit board with enhanced in-plane and through-plane thermal conductivity performance for high power
15 or heat sensitive electronic device applications. More particularly, this invention relates to the manufacture of aluminum metal core substrate using selective fabrication methodology resulting in close to bulk metal thermal conductivity for the thermal path and programmable high breakdown voltage protection for the electrical circuitries. The electrical insulation is provided by the aluminum oxide. The selective anodization, metal
20 sputtering and additive copper plating methodology allows selective surface insulation, selective embedded insulation and vertical via isolations. Since there is no adhesive system in the process, the resulted substrate can withstand high temperature operation with no thermo-mechanical failures like delamination or inner-layer blistering. In summary, this invention relates to a cost effective high-thermal efficient and robust
25 printed circuit board or substrates for the electronic industry.

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A circuit board is usually comprised of a base material with opposing first and second face with electrical interconnects for electronic device assembly. The electronic devices mounted on a circuit board can be of any number of devices such as packaged integrated circuits, multi-chip modules, transistors, resistors, capacitors, Light Emitting Diodes (LED), and the like. When operated the active devices dissipate energy in the form of heat.

For discussion purposes, LED will be used to illustrate the related art printed circuit board application. LED has very high heat density because of the tiny light source. About 85% of the power into the LED is converted to heat. The drive to increase brightness in the tiny light source requires higher power resulting in rapid increase in device junction temperature. The increase in temperature translates to poor light extraction efficiency and high device failure rate. In general the device failure rate doubles for every 10C rise in junction temperature. Secondary heat sink is being use to help dissipate the generated heat. Heat sink adds to the overall product cost. In the case of LED, light is emitted from the top.

Generally, a high percentage of the heat is conducted downwards from the device to the circuit board suggesting lowest vertical thermal resistance will result in optimum thermal conduction path for the heat source.

The through-plane thermal resistance increases with the number of stacked up layers for the multi-layer circuit board. With the device miniaturization trend, heat density increases many folds. In-plane circuit board heat spreading will help distribute heat away from the hot spots. The efficiency of heat spreading and heat conduction vertically through the circuit board is an important factor in how well heat can be transferred from an electronic device to the ambient air. The traditional fiber glass or epoxy based printed circuit is not a good thermal conductor vertically and laterally. This is mainly due the thin interspersed and discontinuous metal and non-metal layers.

Thermal via, multi-layer copper planes and metal core with dielectric layer are used as alternative solution to alleviate the heat problem. FIG. 1 is a typical Prior Art metal core

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printed circuit board embodiment. It comprises of a resin-base dielectric layer laminated onto the metal base and another layer of copper foil laminated on to the dielectric layer. The adhesive system used has relatively low Glass Transition temperature, T_g , which may result in low copper peel strength and other thermo-mechanical related failures over
5 high temperature exposure. Other similar embodiment uses anodic coating as the dielectric layer. The dielectric layer provides the electrical isolation between the copper circuit layer and the metal core. A thick dielectric layer provides good electrical breakdown performance. On the contrary, a thicker dielectric layer adds thermal resistance to the stacked up structure.

10 One commonality of the Prior Art circuit design as referenced in FIG. 1, attempts to work around these conflicting properties by trying to isolate the electrical connections from the bulk metal base with a very thin layer of thermally conductive dielectric which if too thin will result in lower breakdown voltage. If too thick, the thermal resistance will increase accordingly.

15 Typical FIG. 1 Option A solution has dielectric at about 75-100um thick and a very thick copper of 70 – 105 um for heat spreading purposes. Option A shows the copper layer (11 and 13) to be on the same plane as thermal pad (12).

Other enhanced Prior Art implementation as depicted in FIG. 1. Option B has a via (51) for the heat source region; however, since the dielectric is about, say 75 um thick, the
20 thermal interface material has to be at least 75 um thick as well to fill the via (51). Contradictory as shown in FIG. 6, the thicker the thermal interface material, the higher the thermal resistance at the heat source path. With reference to FIG. 6, assuming a 75um thick thermal interface material for embodiment (700) and a 1 um thick interface for embodiment (800); the R_{800} is about 75 times better as compared R_{700} for flat surface
25 mountable devices.

The present invention also aims to reduce the thermal interface gap by providing a planar surface for device assembly.

SUMMARY OF THE INVENTION

The design challenge is to create a cost effective thermally efficient metal core circuit board with a planar surface for electrical and thermal circuitries. The goal is a thermally-efficient metal core printed circuit board with enhanced in-plane and through-plane
5 thermal conductivity performance for high power or heat sensitive electronic device applications:

More particularly, this invention relates to the manufacture of aluminum metal core substrate using selective fabrication methodology resulting in close to bulk metal thermal conductivity for the thermal path and programmable high breakdown voltage
10 protection for the electrical circuitries. The electrical insulation is provided by the aluminum oxide or any dielectric layer formed by known art methods, for instances, surface resin coating, Plasma Electrolytic Oxidation, to name a few. The selective anodization or coating, metal sputtering and additive copper plating methodology allows selective surface insulation, selective embedded insulation and vertical via isolations.

15 In accordance with the present invention, a thermally-efficient metal core printed circuit board comprises an Aluminum base including opposing first face and a second face, and the said faces with a plurality of dispersed dielectric layer embedded within the metal base resulting in a planar surface for the overlying circuitries, a plurality of dispersed thermal metallization layer connected directly to the metal base for optimum thermal
20 performance and a plurality of electrical circuitries connected accordingly to the profile of the metal body for the multi-layer electrical circuit connectivity. The planar surface is paramount for flat surface mounting technology and flip-chip devices assembly. The selective dielectric layer configuration allows direct thermal pad contact to the bulk metal base and insulation for the electrical terminals resulting in high thermally-efficient
25 circuit board for single or matrix device assembly or mother-board applications. The selective dielectric and metallization topology is also applicable 3D heat sink structure.

In accordance to the present invention, the dielectric layer is selectively formed using known art photo-lithography masking steps and anodic coating processes.

Additional planarization steps either by etching, deburring or plating-up metallization step are added to the anodized metal base to create the planar surface critical for surface mounting device application as depicted in FIG. 8. The subsequent metallization steps are the same known art copper plating or silver printing or sputtering processes.

- 5 In the present invention, the dielectric is selectively grown on top the metal base for electrical isolation purposes. Electrical circuits are then plated on top of the dielectric area for electrical isolation and breakdown voltage capability.

In the present invention, the thermal pad is directly plated on the metal surface of the metal base resulting in negligible thermal resistance or close to bulk metal thermal
10 conductivity per unit area.

In the present invention, the novel selective isolation methodology on the circuit board produces best thermal performance and highest breakdown voltage capability as opposed to prior art composite material methodology whereby both the electrical and thermal pads sit on the same dielectric insulation layer.

- 15 The basic planar metal Circuit Board structure can be extended to 3-D heat sink structure whereby the planar face comprises a plurality of selectively insulated electrical circuitries from the metal base and a plurality of thermal pads connected directly to the metal base.

The same invention is applicable to a copper base whereby dielectric layer can be
20 selectively printed onto the copper base. The dielectric and can be sputtered on a etched surface so that the finished dielectric layer is in the same plane as the rest of the copper base surface or the direct thermal pad area is copper plated up to achieve the same planar

surface. The process steps can be repeated resulting in a thicker substrate with vertically connected via.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of the Prior Art laminated Insulated Metal Core Board.

5 It has a copper layer laminated on to a dielectric layer covering the whole surface of the metal base;

FIG. 1 Option A is the schematic cross section view of the dielectric layer 50 overlying the whole metal base;

FIG. 1 Option B is the schematic cross section view of the enhanced version with via 51
10 for the thermal pads. Since there is no copper in the via area, the connection is done using thermal interface material;

FIG. 2a is the schematic cross section of a generic embodiment of the present invention. The substrate consists of cavity 101 and 104. Both cavity bases are on a different level as depicted in cross section view F. Cavity 104 has the whole cavity coated with a
15 reflective coating for light beam shaping purposes. The smaller cavity 101 can be used for embedded chips or as a base for tall chips which can create shadow for light emitting diode applications.

The same substrate can have anodized round hole 102 or square hole 103 for metal screws or connectors. Cutout 105 allow top-to-bottom circuit connections by the
20 insulated wall. The two protruding arm is to prevent side wall circuit shorting.

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The top layer copper can be connected to the bottom layer copper by three different approaches.

(1) With the selective metallization, pads 's' is connected to 'u' via the metal body.

(2) Side wall connects using vertical insulation/metallization.

5 Plated-through-hole via (i) by drilling and chemical etched via (ii) by vertical selective isolation creating vertical via without drilling. Figure 2a embodiment summarizes all the key novelty features for this invention. They are as follows:

A: Cavity with direct bulk body contact. Cavity acts as beam shaping or reflector cup for LEDs.

10 B: Cavity with insulated electrical contacts to all multi-levels component assembly.

C: Top-to-bottom connected by two via formation approach, for example, (i) plated through hole via by drilling and (ii) Solid via by vertical chemical isolation.

D: Top-to-bottom layer connected by side walls

E: Aluminum core as electrical conduits

15 F: Interconnected multilevel cavity structure allowing circuits to be connected via the cavity walls.

FIG. 2b is the schematic cross section of another embodiment of the present invention. The top view is without circuitries for easy referencing;

FIG. 3 is the schematic cross section of yet another embodiment of the present
20 invention;

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FIG. 4a illustrates the Prior Art embodiment and a Flip-Chip Power Device shown separately;

FIG. 4b illustrates the Prior Art embodiment and a Power Device for Wire-Bonding;

FIG. 4c illustrates the Power Device flip-chip Assembly on the Prior Art Metal Core
5 Substrate;

FIG. 4d illustrates the Power Device wire-bonding Assembly on the Prior Art Metal
Core Substrate;

FIG. 4e illustrates the Packaged Power Device Assembly on the Prior Art Metal Core
Substrate;

10 FIG. 4f illustrates the Power Device Assembly with Thermal Interface Material directly
to the Metal Core Substrate;

FIG. 5 illustrates the Power Device Assembly using the present invention embodiment;

FIG. 6 illustrates the thermal resistances of the various embodiments;

FIG. 7 illustrates the many variations of power device packages with over-mold
15 protection, lens system and surface mountable external heat-sink devices for enhanced

thermal dissipations;

FIG. 7A is the present invention substrate embodiment;

FIG. 7B is the present invention package design embodiment with over-mold compound, a cavity and a clear protection material for the dice;

- 5 FIG. 7C is the present invention package design embodiment with a pre-stamped metal base, a cavity and a clear protection material for the dice;

FIG. 7D is the present invention package design with a colored over-molded epoxy. The over-mold compound can be replaced with green ceramic;

- 10 FIG. 7E is the present invention package design with an over-molded lens shaping system;

FIG. 7F is the present invention package design with an packaged device and a separate dielectric layer at the bottom of the substrate;

FIG. 7G is the present invention package design with a packaged device and no dielectric at the bottom of the substrate;

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FIG. 7H illustrates the embodiment with multiple devices on the metal core board for motherboard application and/or on a 3D metal structure and/or prefabricated heat sink with a planar top surface;

FIG. 7I shows the copper plated second face of the board can be directly solder mounted
5 to another plated aluminum heat sink or a copper heat sink without thermal grease or thermal adhesive;

FIG. 8 shows the present invention basic process steps to produce embedded dielectric and planar surface by etching, deburring or plating-up;

FIG. 9 shows the present invention implementation on a copper base;

10 It is to be understood that these drawings are for illustrating the concepts of the invention and are not to scale.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In accordance to the present invention, the product goal is to bring the thermal contact surface to be the same level as the electrical contact. Known art anodization process is
15 described; however, the basic innovation of selective electrical insulation for electrical path and thermal path is application to all known art surface treatment technology, for instance resin coating, Plasma Electrolytic Oxidation, to name a few.

FIG. 8 shows the various steps to create the dispersed dielectric layers within the aluminum base. Depending on anodization time, the dielectric layer thickness and

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porosity can be controlled to suit breakdown voltage level requirement. At the end of the anodization process, the anodic coating will protrude slightly above the surface. The surface planarization can be accomplished by controlled oxide etching or by mechanical deburring the top of the oxide layer or by plating-up around the oxide layer. The planar
5 surface with embedded dielectric layer is ready for subsequent circuit fabrication processes.

FIG. 2a depicts the schematic of the various connectivity possibilities of the present invention. The start material can be a flat plate or multi-tier 3-dimension metal base. The metal substrate can have pre-drilled through holes, for examples, (102, 103) and pre-
10 stamped cut-out, (105).

FIG. 2a is the schematic cross section of a generic embodiment of the present invention. The substrate consists of cavity (101 and 104). Both cavity bases are on a different level as depicted in cross section view F. Cavity (104) has the whole cavity coated with a reflective coating for light beam shaping purposes. The smaller cavity (101) can be used
15 for embedded chips or as a base for tall chips which can create shadow for light emitting diode applications.

The same substrate can have anodized round hole (102) or square hole (103) for metal screws or connectors. Cut out (105) allow top-to-bottom circuit connections by the insulated wall. The two protruding arm is to prevent side wall circuit shorting.

20 The top layer copper can be connected to the bottom layer copper by three different approaches.

- (1) With the selective metallization, pads 's' is connected to 'u' via the metal body.
- (2) Side wall connects using vertical insulation/metallization.

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Plated-through-hole via (i) by drilling and chemical etched via (ii) by vertical selective isolation creating vertical via without drilling. Figure 2a embodiment summarizes all the key novelty features for this invention. They are as follows:

5 A: Cavity with direct bulk body contact. Cavity acts as beam shaping or reflector cup for LED.

B: Cavity with insulated electrical contacts to all multi-levels component assembly.

C: Top-to-bottom connected by two via formation approach, for example, (i) plated through hole via by drilling and (ii) Solid via by vertical chemical isolation.

D: Top-to-bottom layer connected by side walls

10 E: Aluminum core as electrical conduits

F: Interconnected multilevel cavity structure allowing circuits to be connected via the cavity walls.

The following describes the implementation details in various embodiments.

Referring to the drawings, FIG. 2b is a schematic of the top view of the start aluminum
15 metal material (30) with optional different shape vertical holes (31 and 32); and the A-A cross sectional view of the preferred embodiment (500) with the selective insulation layers (40C, 40D and 40E).

The metal circuit board (500) has opposing first face and second face. Formed on the surfaces of base (30) are dielectric layer (40C, 40D and 40E) shaped according to the
20 insulation layer requirement. Optionally, vertical oxide layer (40A and 40B) can be formed in pre-stamped holes.

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Copper circuitry is then plated on top of the insulation layer. As depicted in the preferred embodiment, the copper layer can selectively be plated on top of the insulation layer and the metal surface without any insulation. Copper layer (15) sits directly on top of an insulation layer. One part copper layer (16) sits on the insulation layer and another part
5 sitting on the metal layer; thus forming the basis of direct thermal connection to the bulk metal and optionally acting as an electrical connection for the opposing faces.

Copper layer (18) is plated directly on the metal surface. Solder mask (60A, 60B) is applied per IPC standard requirements and for lateral breakdown protection.

Copper layer (25) of FIG. 2b provides the vertical circuit connection of the two opposing
10 faces. Effectively, a multi-layer circuit is created. FIG. 3 shows another preferred embodiment (600) with a three-dimension metal base material. Metal trace (26) is plated on the first face connected to the second and third face. Vertical walls (33, 34 and 35) can be selectively insulated. Wall (33) is then metallized with metal trace (26). The two walls (34 and 35) will protect electrical contact to wall (33) mechanically. The same
15 approach is applicable for through-hole via.

FIG. 4c shows the prior art power device assembly to a metal core substrate or printed circuit board. The prior art metal core board is fabricated using the traditional laminated technology. Both the dielectric and the copper foil are physically laminated together with adhesive which has varying degree of Glass Transition temperatures. The adhesive
20 absorbs moistures and it is sensitive to high temperature exposure which may result in lower copper to dielectric peel strength. Structurally, the typical dielectric has thickness varying from 75um to 150um depending on the breakdown voltage requirement. Thermally, the thermal resistance increases with the dielectric thickness. Other Prior Art metal core board has no dielectric at the heat source area as depicted in FIG. 4f. This
25 provides best thermal path with minimum thermal resistance. Since the copper plane is overlying the dielectric, the thermal contact will be about the same height away from the

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metal core base. This topology requires very thick thermal interface material 16. Since thermal resistance is also pressure dependent; this topology is not suitable for surface mountable devices.

FIG. 5 shows our preferred embodiment according to the current invention. The dielectric layers, (17 and 18), are on the same plane as the metal core surface resulting in planar copper metallization (11, 12 and 13). The selective dielectric allows copper layer (12) to be plated directly on to the metal base; thus, providing best thermal path with close to bulk material thermal conductivity.

FIG. 6 shows the three power device assembly on metal core board. (6a and 6b) are the prior art assemblies and (6c) is the preferred embodiment according to the current invention.

Advantageously, (6c) has power device (112) directly connected to the bulk metal base. Since there is no dielectric between the plated copper and the metal base, the through-plane thermal resistance of thermal path is close to the bulk thermal resistance, $R_{\text{substrate}}$ estimated at

$$R_{\text{substrate}} \sim (t/kA) \text{ C/W} \quad \text{Equation 1}$$

where t is the substrate thickness in meter, k is the material thermal conductivity in W/m-K and A is the area of the heat source in m^2 . The thermal conductivity for aluminum alloy ranges from 170W/m-K to 230W/m-K versus the more expensive ceramic at ~ 30 W/m-K and about 0.3 W/m-K for FR4.

Comparatively, the thermal resistance $R_{600} > R_{700} > R_{800}$.

Besides the selective copper plating, other type of electrically conductive material like silver ink may also be used for the metallization interconnects.

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The present invention is specifically adapted to and has been described in connection with a flat plate metal base substrate but is not so limited; the invention can, in fact, be applied to substantially any substrate made of different material particularly hybrid metal substrate or metal finned heat sink with a flat interface for electrical connectivity.

- 5 FIG. 7H shows the base material is a normal aluminum base heat sink with prefabrication fins. FIG. 7I shows an alternative embodiment of FIG 7H. Heat sink (819) in FIG. 7I can be made of copper instead of a plated aluminum heat sink.

As shown in FIG. 9, the present invention can be implemented on a copper base. Copper has better thermal conductivity performance as compared to Aluminum.

- 10 Specific to some LEDs whereby the LED heat slug under the packaged emitter is not electrically isolated, another layer of oxide can be formed on the second face. Structurally, this configuration will allow negligible thermal resistance between the heat slug and the bulk metal resulting in better heat spreading. The second face electrical insulation layer as shown in FIG. 7F will provide unit level isolation when connected
15 together in a matrix format.

- It is understood that the above-described embodiments are illustrative of only a few of the many possible specific embodiments, which can represent applications of the invention. The same metal core substrate or metal core printed circuit board can be used for power electronic devices; multi-chip module and system level motherboard
20 applications. Numerous and other varied arrangements can be made by those skilled in the art without departing from the spirit and scope of the invention.

CLAIMS

1. A circuit board comprising:
a base metal layer (66) having first and second opposed surfaces and optional (102, 103), through-holes (111), cut-outs (105) and three-dimensional cavity (101, 104) structures;
5 a plurality of dielectric layers (55) selectively embedded into the base metal layer (66), the dielectric layers (55) forming the electrical isolation layer and being co-planar with the surface of the base metal layer (66) for subsequent steps;
a plurality of electrical circuit layers (44) overlying the first and second surfaces of said
10 base metal layer (66) including at least a portion of the said optional (102, 103), through-holes, cut-out (105) and three-dimensional cavity (101, 104) structures insulated and the rest of non-insulated regions remain as bulk metal;
a plurality of thermal and electrical conductive layers selectively overlying the insulated and non-insulated regions of the base metal layer including the walls of the optional
15 (102), through-holes (111), cut-out and three-dimensional cavity (101, 104) structures;
an optional solder-masking protective co-planar layer selectively applied to the said first and second surfaces of the base metal layer (66).
2. A circuit board of claim 1, wherein the material of the base metal layer (66) is aluminum.
- 20 3. A circuit board of claim 1, wherein the thermal and electrical conductive layers are provided in material selected from the group consisting of copper, silver and conductive ink.
4. A circuit board of claim 1, wherein electrical circuitries of the electrical circuit layers (44) are selectively connected according to the profile of the walls by the thermal and electrical conductive layer and the bulk metal of the base metal layer (66).
25
5. A circuit board of claim 1, wherein a heat source is mounted directly to the base metal layer (66) without any dielectric layer (55) in between the heat source and the base metal layer (66).

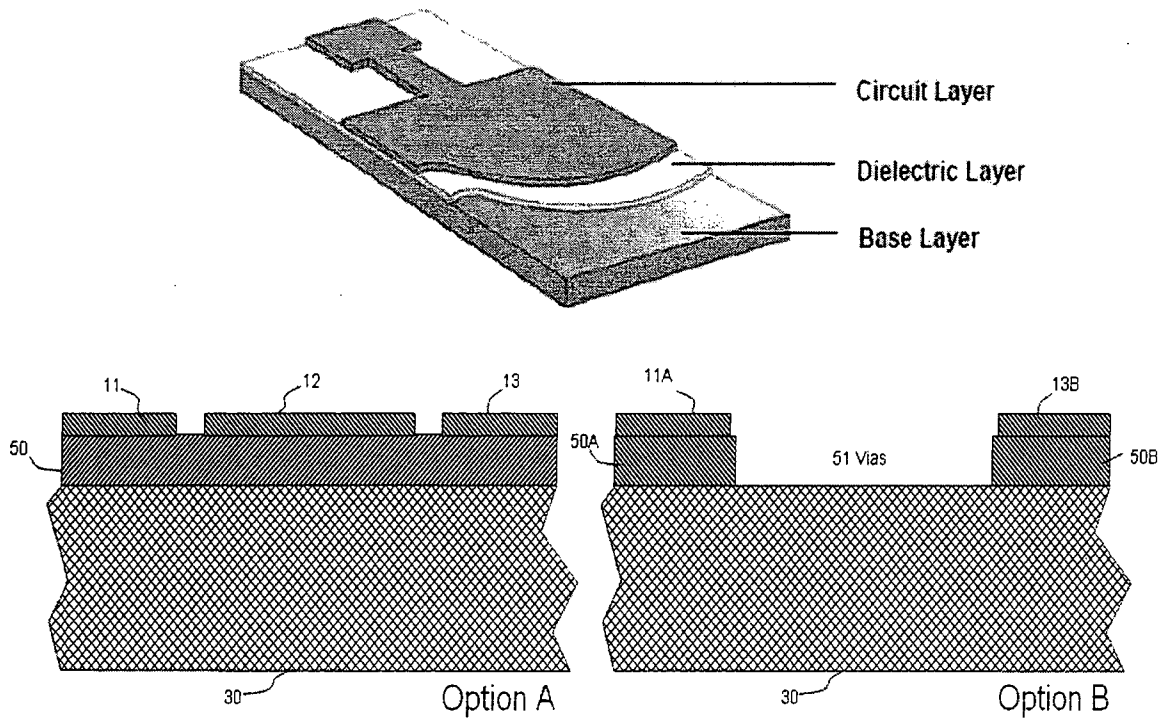
- 17 -

6. A circuit board of claim 1, wherein the flat surfaces of the three-dimensional cavity (101, 104) structures having a plurality of selective electrically isolated circuits and a plurality of direct thermal pads for device-mounting inside the three-dimensional cavity (101, 104) structures.
- 5 7. A circuit board according to claim 6, wherein the said flat surfaces of the three-dimensional cavity (101, 104) structures are sprayed or plated with reflective material for LED light shaping purposes.
8. A circuit board according to claim 6, wherein the three-dimensional cavity (101, 104) structures are filled with epoxy.
- 10 9. A circuit board according to claim 6, wherein the three-dimensional cavity (101, 104) structures are laminated with material selected from the group consisting of ceramic material, protective material and clear material.
10. A circuit board according to any one of the claims 1 to 8, wherein a multi-level and multi-layer circuitries are built on planar surface of the base metal layer (66)
15 wherein the base metal layer (66) is fabricated as a base heat sink.
11. A three dimension circuit board according to claim 10, further comprising thermal pad layer overlying the planar surface of the base heat sink or any surface thereof mounted with component.
12. A circuit board of claim 1, wherein the circuit board is applicable for single
20 device-mounting or multiple-device mounting suitable for multi-chip module configuration and replacement technology for printed circuit board for large system implementation.
13. A circuit board of claim 1, wherein the dielectric layers (66) under the electrical circuit layers 44 having high thermal resistance to facilitate lower temperature soldering.

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14. A circuit board of claim 1, wherein the material of the base metal layer (66) is further selected from the group consisting of copper, magnesium, titanium, beryllium, nickel and alloys.
15. A circuit board of claim 1, wherein the dielectric layers (55) for electrical and thermal circuitries is formed by surface treatment technologies selected from the group consisting of resin coating, Plasma Electrolytic Oxidation and selective printing technologies.

FIG 1. PRIOR ART METAL CORE SUBSTRATE



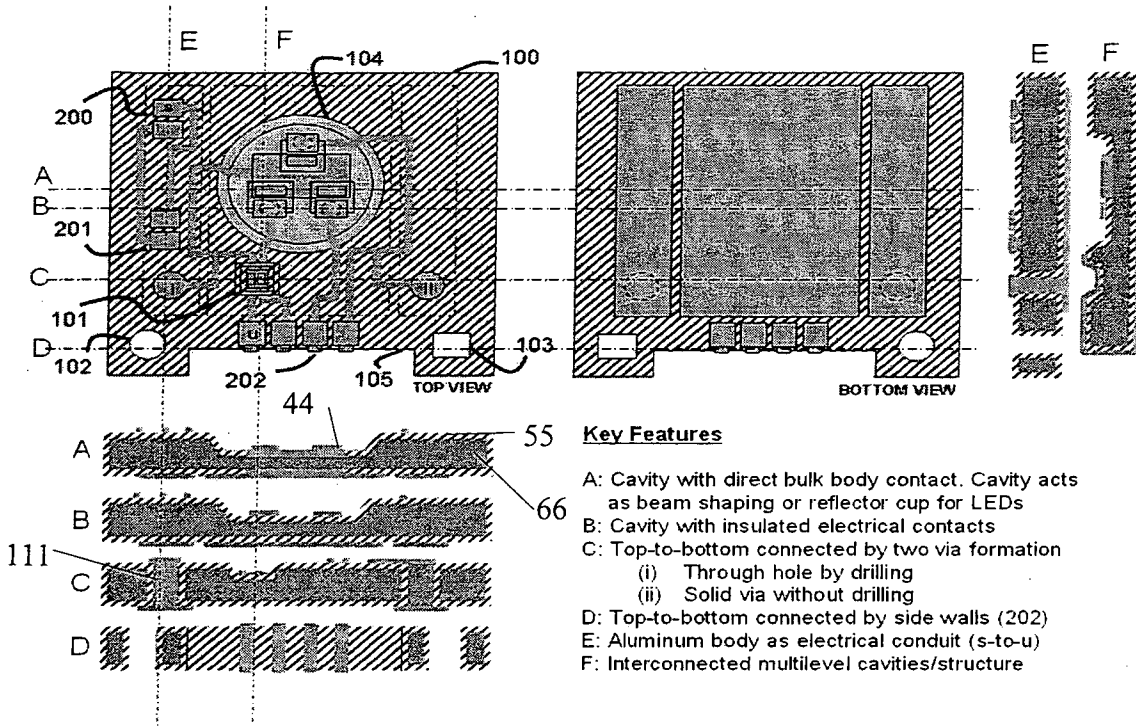


FIG. 2a

FIG. 2b

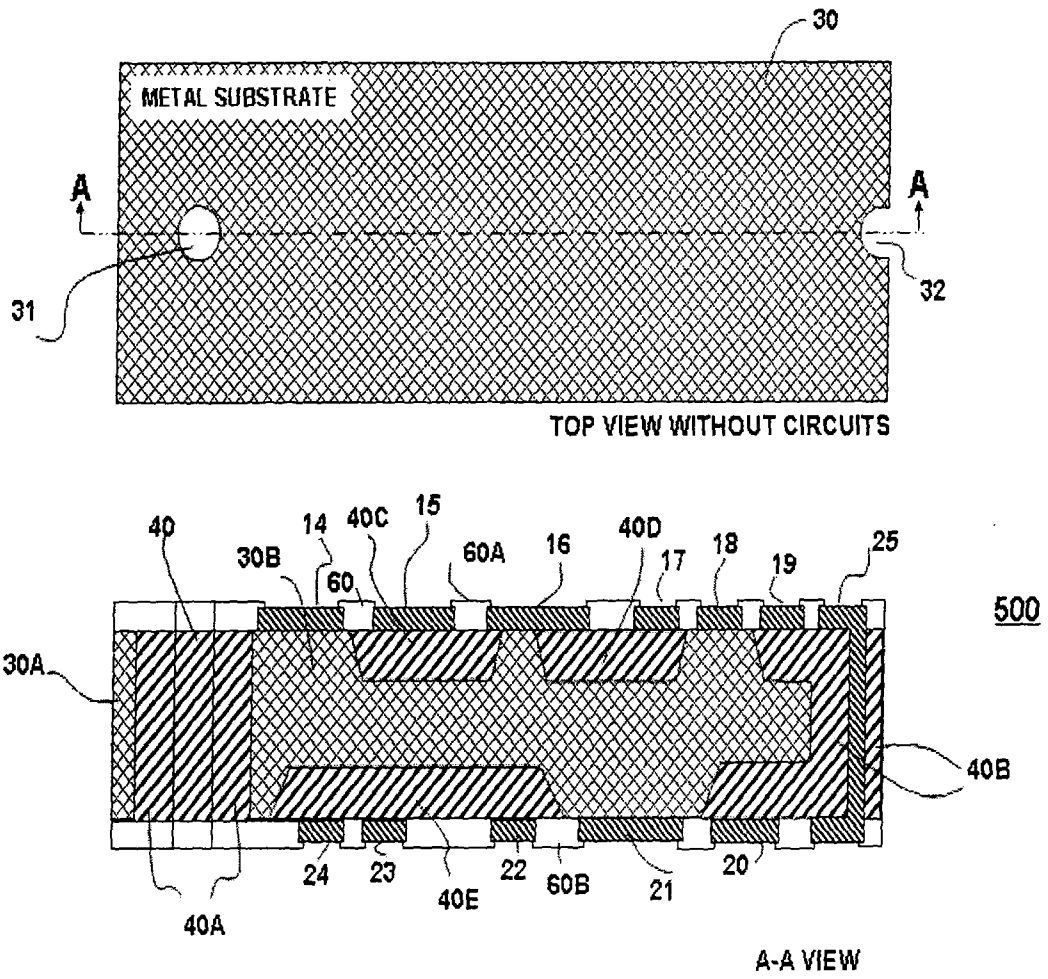


FIG. 3

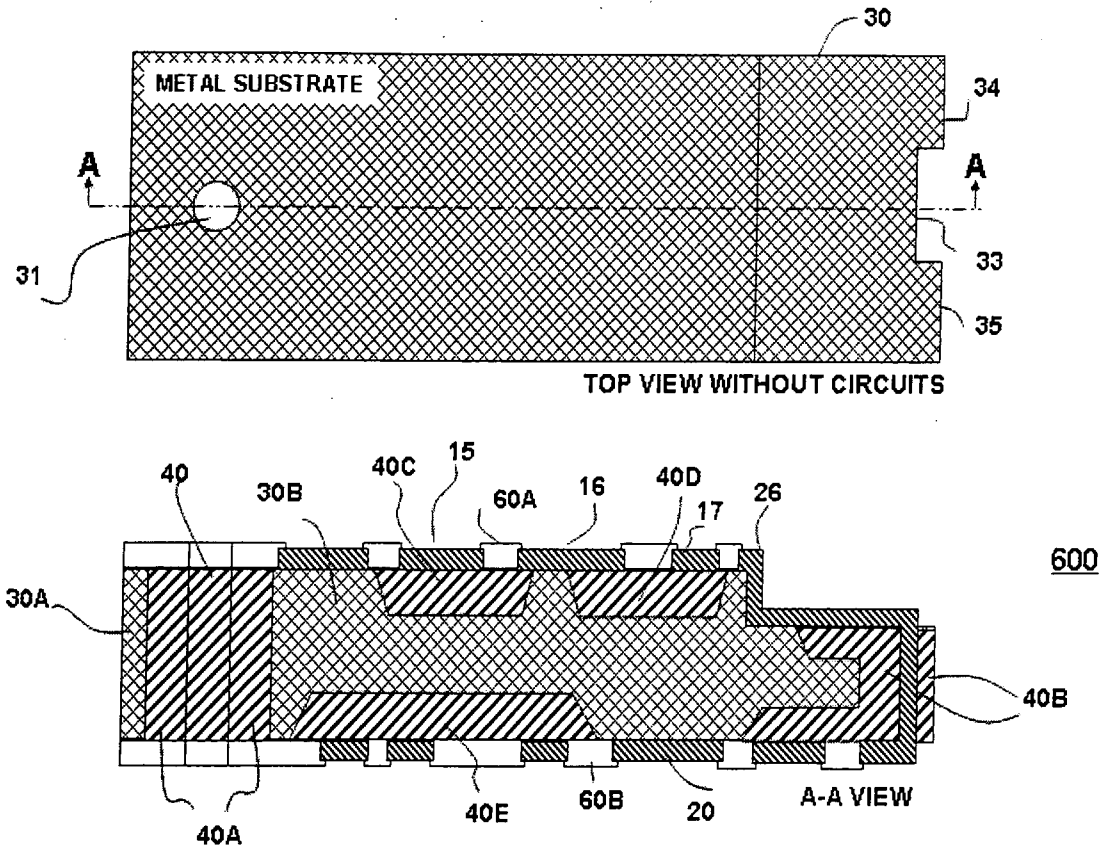


FIG 4a. PRIOR ART HIGH POWER DEVICE AND METAL CORE SUBSTRATE (FLIP CHIP)

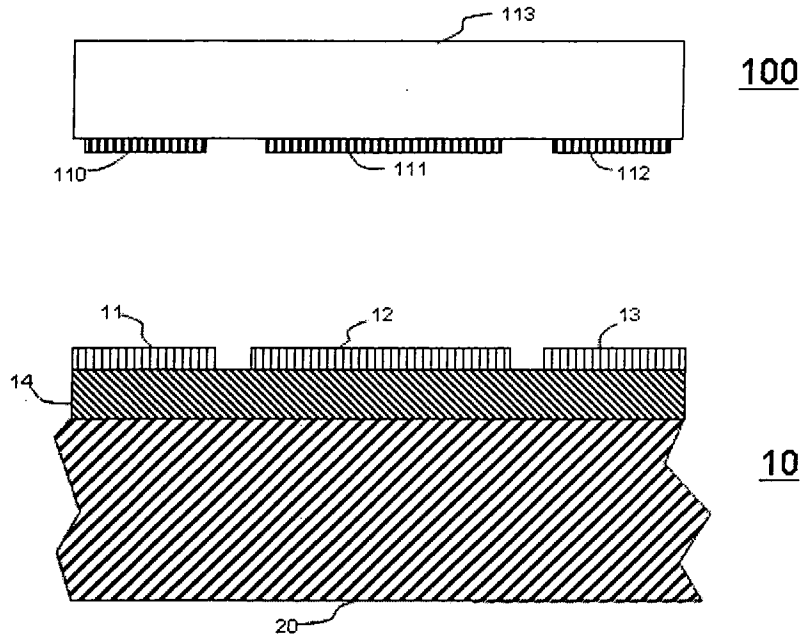


FIG 4b. PRIOR ART HIGH POWER DEVICE AND METAL CORE SUBSTRATE (WIRE-BONDING)

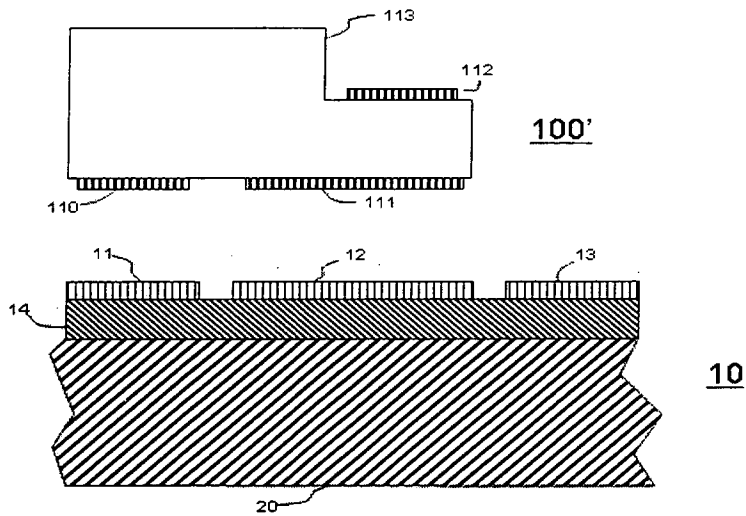


FIG 4c. PRIOR ART HIGH POWER DEVICE ASSEMBLY ON METAL CORE SUBSTRATE (FLIP CHIP)

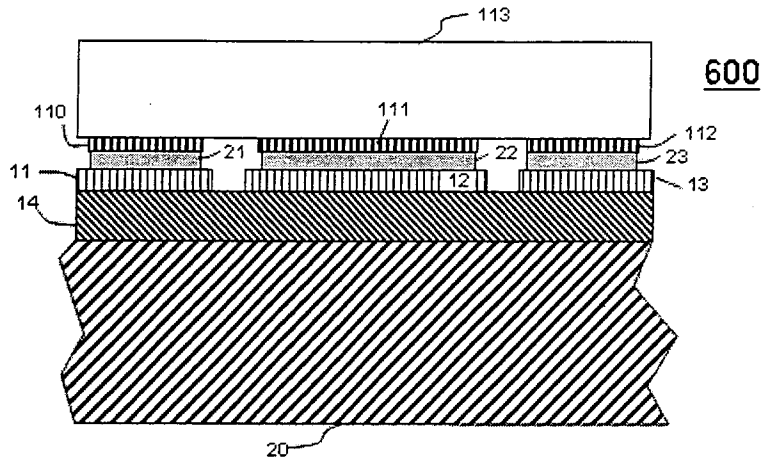


FIG 4d. PRIOR ART HIGH POWER DEVICE ASSEMBLY ON METAL CORE SUBSTRATE (WITH WIRE BONDING)

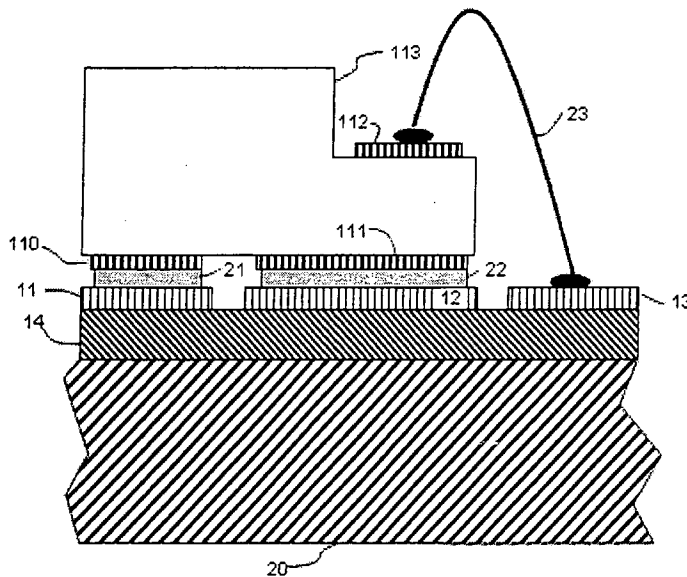


FIG 4e. PRIOR ART HIGH POWER DEVICE ASSEMBLY ON METAL CORE SUBSTRATE (WITH PACKAGED DEVICE)

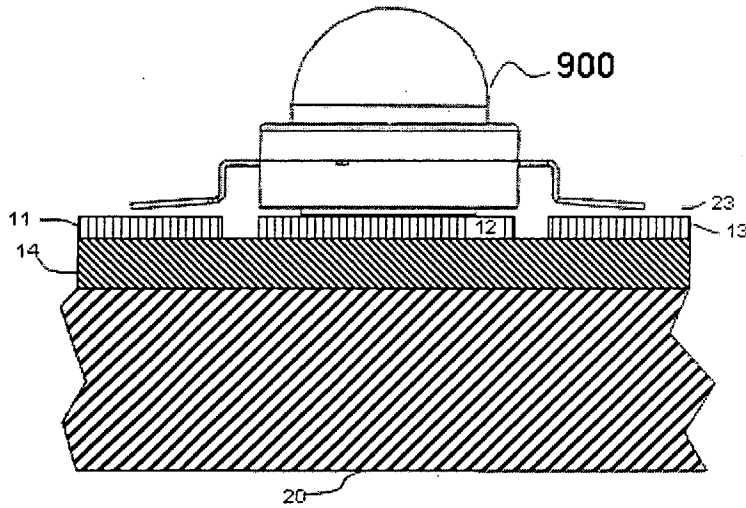
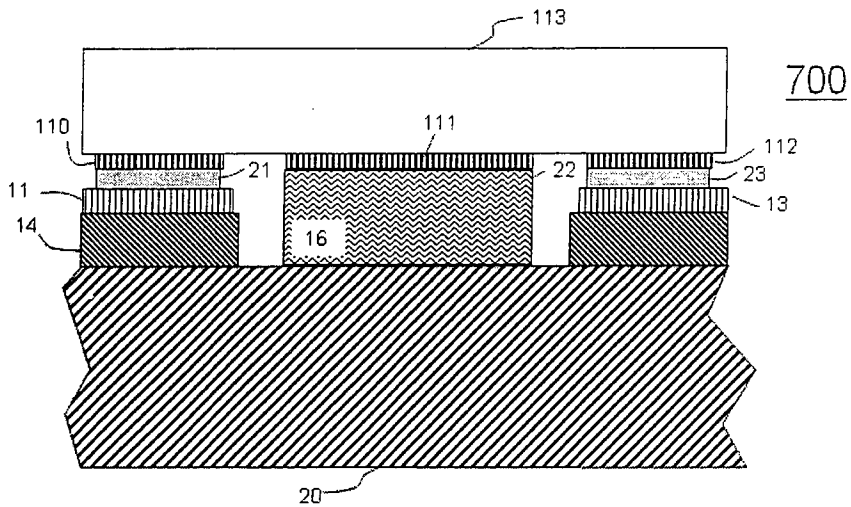


FIG 4f. PRIOR ART HIGH POWER DEVICE ASSEMBLY WITH DIRECT THERMAL CONTACT TO METAL CORE SUBSTRATE



**FIG 5. HIGH POWER DEVICE ASSEMBLY
TO INTEGRATED METAL CORE SUBSTRATE**

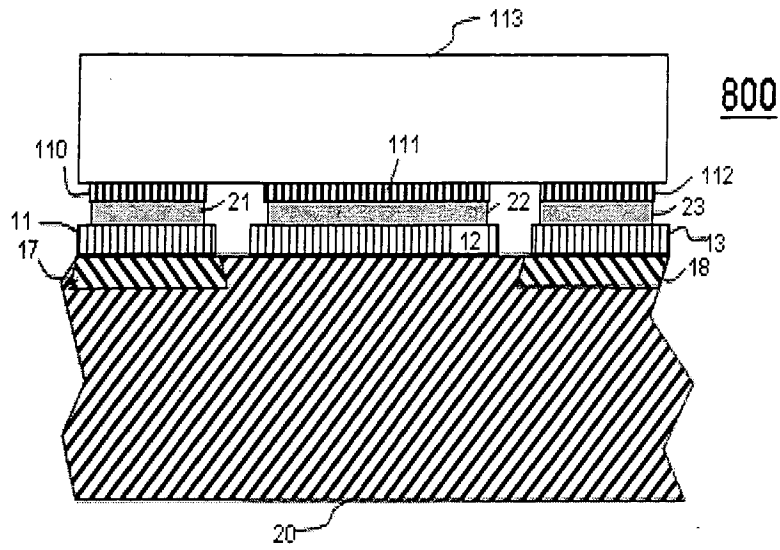


FIG 6. HIGH POWER DEVICE ASSEMBLY ON METAL CORE SUBSTRATE COMPARISON

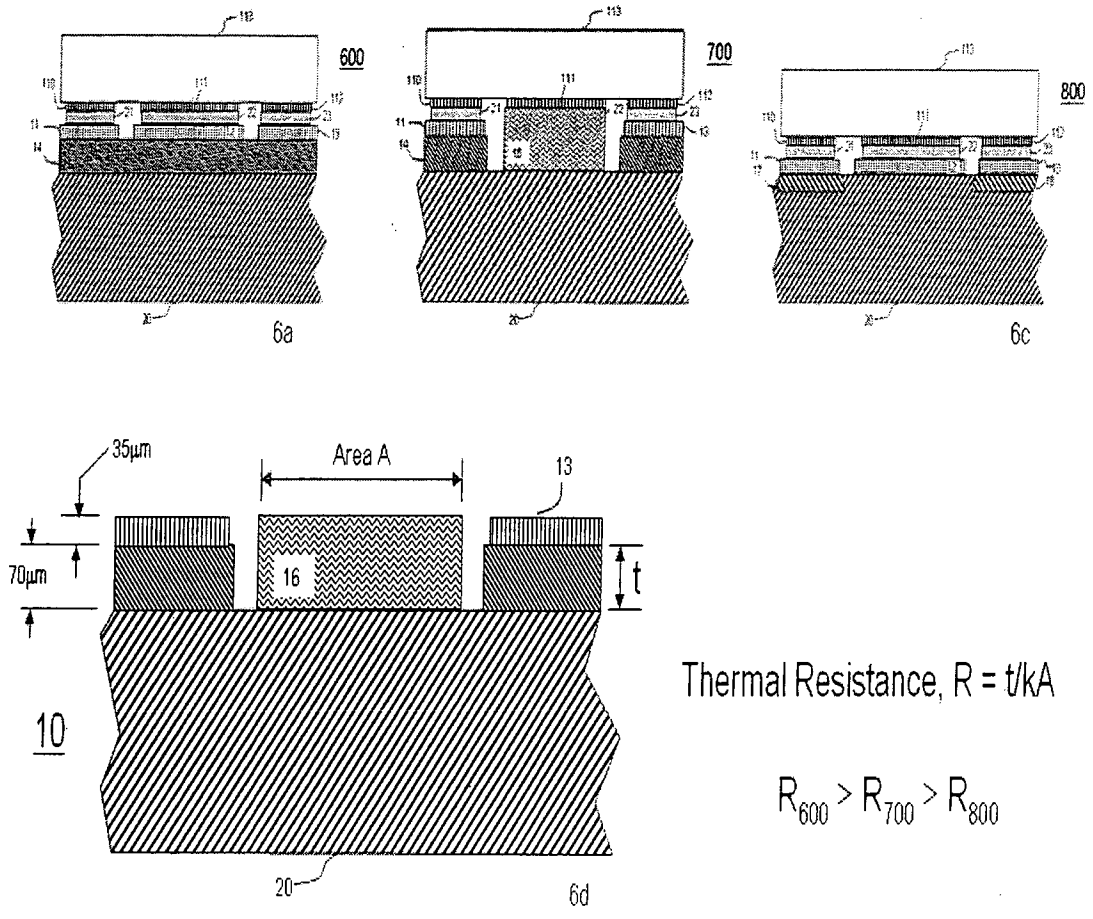


FIG. 7

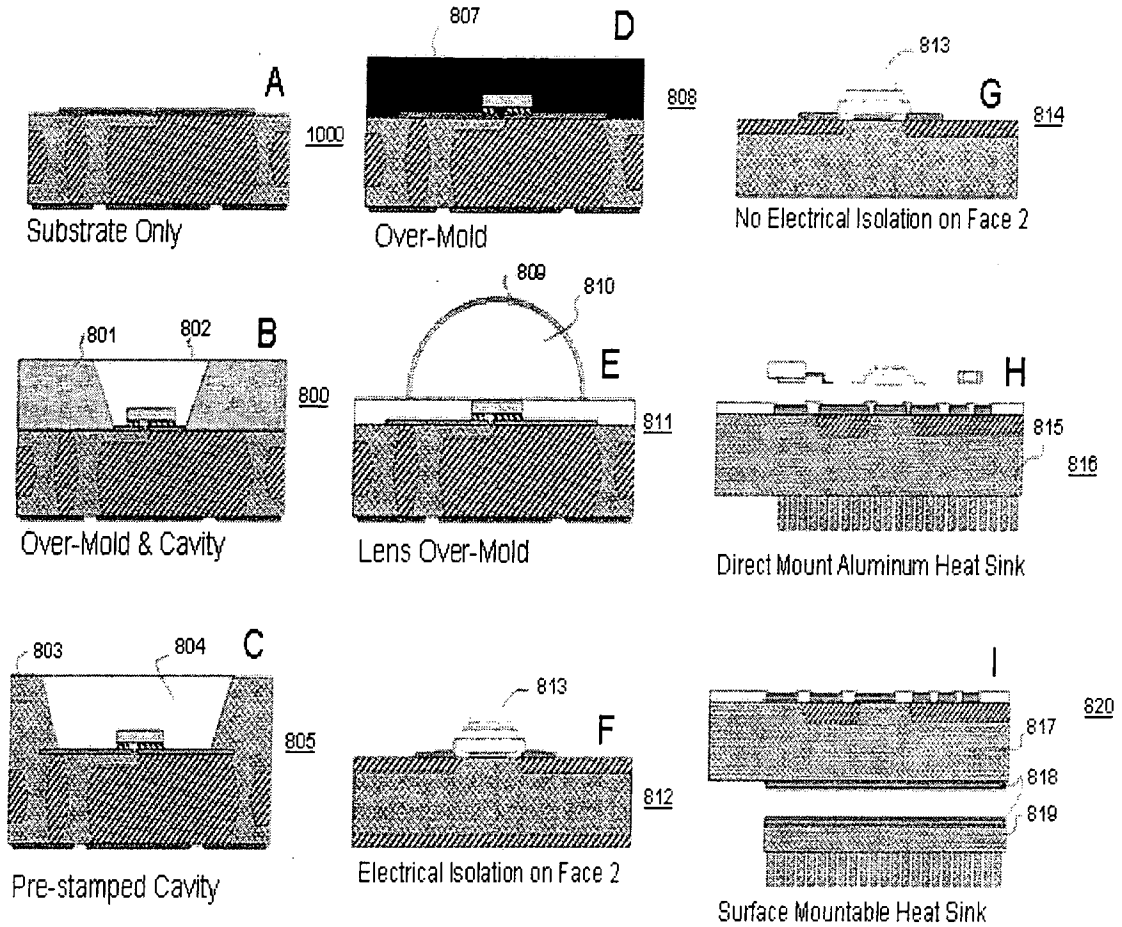


FIG. 8

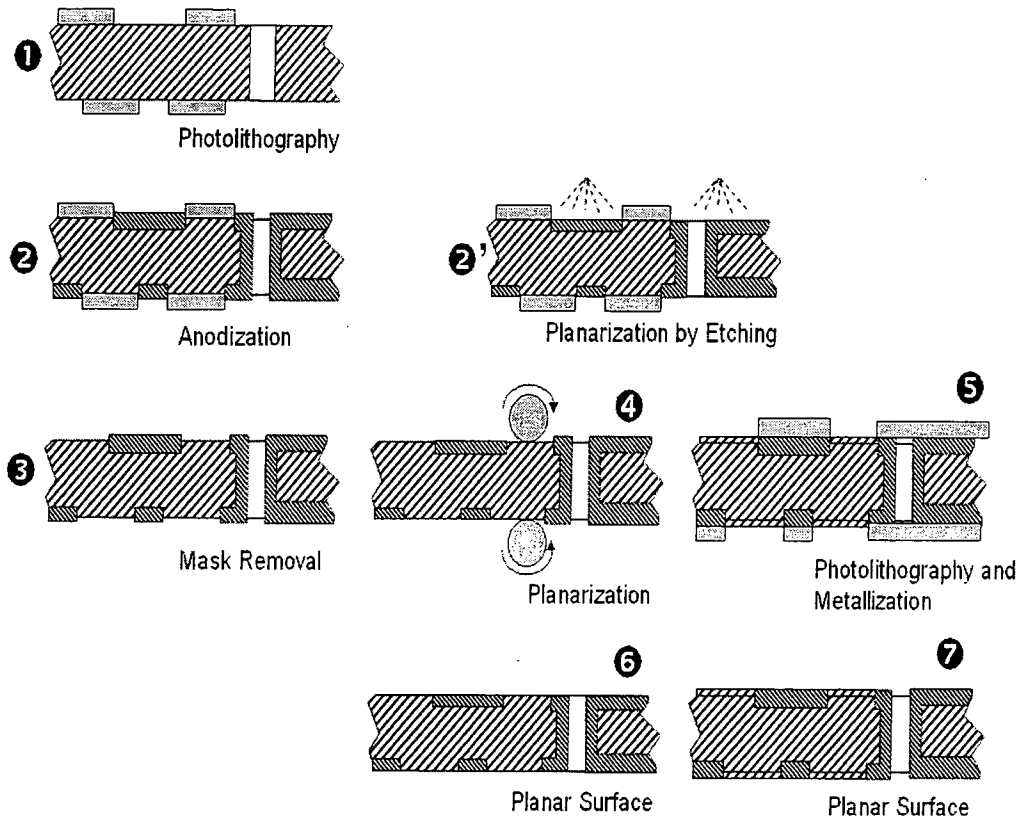


FIG. 9

