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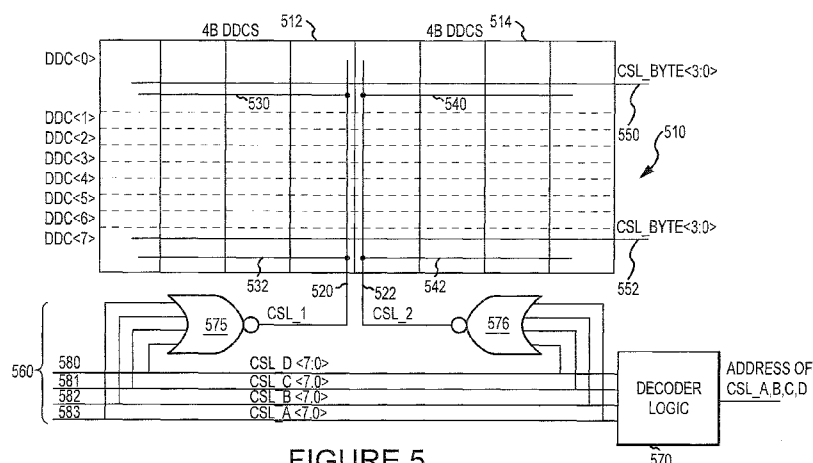


FIGURE 5

(57) Abstract: Examples described include dynamic data caches (DDCs), decoders and decoding methods that may fit into a smaller width area.. The DDCs, decoders and decoding method may be used in flash memory devices. A single column select line may be provided to select a plurality of cached bytes, while a second select line selects a byte of the selected plurality. The column select line may be routed parallel to bit lines carrying data, while the second select line may be routed perpendicular to the bit lines.

DYNAMIC DATA CACHES, DECODERS AND DECODING METHODS**TECHNICAL FIELD**

[001] Embodiments of the invention relate generally to semiconductor memory, and particularly, to dynamic data caches, decoders, and decoding methods.

BACKGROUND

[002] With increasing popularity of electronic devices, such as laptop computers, portable digital assistants, digital cameras, mobile phones, digital audio players, video game consoles and the like, demand for nonvolatile memories are on the rise. Nonvolatile memories come in various types, including flash memories. Flash memories are widely used nowadays for fast information storage in electronic devices such as those mentioned above. A flash memory cell is generally programmed by storing charge on a charge storage structure, such as a charge trap or a floating gate. The charge may thereafter remain on the charge storage structure for an indefinite period even after power has been removed from the flash memory device. Flash memory devices are therefore non-volatile.

[003] Charge is stored on the charge storage structure (referred to hereinafter by example as a “floating gate”) by applying appropriate voltages to the control gate and the drain or source. For example, negative charge can be placed on the floating gate by grounding the source while applying a sufficiently large positive voltage to the control gate to attract electrons, which tunnel through the gate oxide to the floating gate from the channel region.

[004] A flash memory cell can be read by applying a voltage to the control gate that is positive with respect to the source. The amount of charge stored on the flash memory cell determines the magnitude of the voltage that must be applied to the control gate to allow the flash memory cell to conduct current between the source and the drain. As negative charge is added to the floating gate, the threshold voltage of the flash memory cell increases thus increasing the magnitude of the voltage that must be applied to the control gate to allow the flash memory cell to conduct current. During a read operation, a read voltage is applied to the control gate that is large enough to render the cell conductive if insufficient charge is stored on the floating gate, but not large enough to

render the cell conductive if sufficient charge is stored on the floating gate. During the read operation, the drain, which is used as the output terminal of the cell, is precharged to a positive voltage, and the source is coupled to ground. Therefore, if the floating gate of the flash memory cell is sufficiently charged, the drain will remain at the positive voltage. If the floating gate of the flash memory cell is not sufficiently charged, the cell will ground the drain.

[005] Before a flash memory cell can be programmed, it may be erased by removing charge from the floating gate. The cell can be erased by applying a gate-to-source voltage to the cell that has a polarity opposite that used for programming. For example, the control gate can be grounded, and a large positive voltage applied to the source to cause the electrons to tunnel through the gate oxide and deplete charge from the floating gate. In another approach, a relatively large negative voltage is applied to the control gate, and a positive voltage, such as a supply voltage, is applied to the source region.

[006] A typical flash memory device includes a memory array containing a large number of flash memory cells arranged in rows and columns. Two common types of flash memory array architectures are the "NAND" and "NOR" architectures, so called for the logical form in which the basic flash memory cell configuration of each is arranged. A typical flash memory array may include a large number of flash memory cells divided into a number of blocks. Each block may include a number of rows, with the cells in the same row having their control gates coupled to a common word line. Cells in the same column may have their sources and drains connected to each other in series. Thus all of the memory cells in the same column of each block are typically connected in series with each other. The drain of the upper flash memory cell in the block is coupled to a bit line through a select gate transistor. Each of the bit lines output a respective bit line signal BL1-BLN indicative of the data bit stored in the respective column of the array. The bit lines may extend through multiple blocks to respective sense amplifiers.

[007] The storage capacity of a flash memory array can be increased by storing multiple bits of data in each flash memory cell. This can be accomplished by storing multiple levels of charge on the floating gate of each cell. These memory devices are commonly referred to as multi-bit or multi-level flash memory cells, known as "MLC memory cells." In MLC cells, multiple bits of binary data corresponding to distinct threshold voltage levels defined over respective voltage ranges are stored within a single

cell. Each distinct threshold voltage level corresponds to a respective combination of data bits. Specifically, the number N of bits requires 2^N distinct threshold voltage levels. For example, for a flash memory cell to store 2 bits of data, 4 distinct threshold voltage levels corresponding to bit states 00, 01, 10, and 11 are needed. When reading the state of the memory cell, the threshold voltage level for which the memory cell conducts current corresponds to a combination of bits representing data programmed into the cell. The two or more bits stored in each flash memory cell may be adjacent bits in the same page of data. However, more frequently, one bit is treated as a bit in one page of data, and the other bit is treated as the corresponding bit in an adjacent page of data. The bit states assigned to respective charge levels are normally the same for all rows of memory cells in an array. The bit states assigned to the flash memory cells in the array are usually implemented in hardware and thus cannot be changed during operation of the flash memory device.

[008] Figure 1 is a schematic illustration of a memory layout 100 including two memory arrays 102, 104 according to the prior art. The memory arrays 102, 104 may include any number and arrangement of memory cells. Each memory array 102, 104 is connected to a corresponding multiplexor region 106, 108. The multiplexor regions 106, 108 include circuitry for coupling selected blocks of the memory arrays 102, 104 to other components of the memory 100. High voltage isolation regions 110, 112 are provided which include circuitry for isolating the higher voltages which may be used in the memory arrays 102, 104 and/or the multiplexor regions 106, 108 from other components.

[009] A dynamic data cache (DDC) region 114 is included which contains circuitry for dynamic data caches. The dynamic data caches may temporarily store data sensed from the memory arrays 102 and 104 or data that will be programmed into the memory arrays 102 and 104. As shown in Figure 1, the dynamic data cache region 114 includes, for example, sixteen dynamic data caches. The sixteen dynamic data caches may be shared between the top and bottom memory arrays 102, 104. In other examples, eight dynamic data caches may be used. Region 116 includes circuitry for interacting with the memory arrays 102, 104 and/or DDCs 114, including a data detector, column knock-out latch, and a column select (csl) decoder. The column select decoder may provide appropriate signals to the DDCs in the DDC region 114 to select a particular DDC and allow sensed data to be stored therein, or allow the data stored therein to be programmed into the connected memory array.

[010] Figure 2 is a schematic illustration of portions of the memory of Figure 1 showing additional detail. The memory array 102 includes sixteen pairs of even and odd bit lines, labeled ble0/blo0 through ble15/blo15. The multiplexer region 106 includes corresponding pairs of bias transistors 206(1) through 206(32). The bias transistors are configured to receive a bias signal at one source/drain terminal while the bit line is connected to the other source/drain terminal. The bias transistors receive either an even bias signal, blbiase, or an odd bias signal, blbiaso, at their gate terminal. The bit lines are further coupled to a source/drain terminal of a respective select transistor, 207(1) through 207(32). The select transistors 207(1-32) each receive either an odd select signal, blso, or an even select signal, blse, at their gate terminal. The blse/blso signals will select whether an even or odd bit line will be coupled to the isolation transistor. Each pair of select transistors is coupled to a respective isolation transistor within the isolation region 110. The isolation transistors 210(1)-210(16) receive an isolation signal, hviso, at their gate terminal. Accordingly, the isolation transistors 210(1)-210(16), when on, couple a selected even or odd bit line through to a DDC.

[011] The DDC region 114 includes sixteen DDCs, labeled DDC<0> through DDC<15>. Each pair of bit lines of the memory array 102 is coupled to one of the DDCs. Each pair of bit lines of the memory array 104 is also coupled to one of the DDCs. Accordingly, the data lines 250, dw<0>, extending from the transistor 210(1) and serving the bit lines ble0 and blo0 traverses the entire length of the DDC region 114 to connect to bit lines in the memory array 104. Similarly, the data line 252, dw<15> extending from the transistor 210(16) traverses the entire length of the DDC region 114 to connect to bit lines in the memory array 104.

[012] Column select lines, such as the csl line 260, and data verify lines, such as the dvrify line 262 are provided for each byte of data lines to couple data stored in the DDCs to and from the two sets of data output lines dataio<0>-dataio<7> as shown. That is, for each eight data lines, one csl line and one dvrify line are provided in the embodiment of Figure 2. Accordingly, for each byte of data, eight data lines dw<0> through dw<7>, one csl line, and one dvrify line are required, for a total of 10 lines per byte of data.

[013] The dvrify line is used to check a fail bit during programming and verify operations of the memory device. A primary data cache in the dynamic data caches may store the pass or fail bit information during the operation. In this manner, data may be verified and, if the data has failed, a fail bit may indicate that the data is not good.

BRIEF DESCRIPTION OF THE DRAWINGS

- [014] Figure 1 is a schematic illustration of a memory layout according to the prior art.
- [015] Figure 2 is a schematic illustration of portions of the memory of Figure 1 showing additional detail.
- [016] Figure 3 is a schematic illustration of a layout for a DDC region in accordance with an embodiment of the present invention.
- [017] Figure 4 is a schematic illustration of a secondary data cache accessing circuit in accordance with an embodiment of the present invention.
- [018] Figure 5 is a schematic illustration of a DDC region including a CSL decoder in accordance with an embodiment of the present invention.
- [019] Figure 6 is a schematic illustration of a flash memory that includes dynamic data caches in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

- [020] Embodiments of the present invention include shared dynamic data caches for use with memory arrays. Examples of dynamic data caches described herein include an arrangement of components such that shared dynamic data caches are feasible in a reduced area relative to prior designs. Certain details are set forth below to provide a sufficient understanding of embodiments of the invention. However, it will be clear to one skilled in the art that embodiments of the invention may be practiced without various of these particular details. In some instances, well-known circuits, control signals, timing protocols, and software operations have not been shown in detail in order to avoid unnecessarily obscuring the described embodiments of the invention.
- [021] As described above, shared DDCs have used data lines for each pair of bit lines which traverse an entire DDC layout region. Moreover, csl and vrfy lines have been provided for each byte, and the csl and vrfy lines also traverse the entire region, that is, they run parallel to the data lines as they cross the region 114. As technology has become smaller, the area allowed for DDC layouts has decreased. Accordingly, it may no longer be feasible to route as many lines as needed for the layout shown in Figures 1 and 2 within the space allotted for a DDC region. Embodiments of the present invention advantageously provide dynamic data caches (DDCs) and decoding methods that may fit into a smaller width area.

[022] Figure 3 is a schematic illustration of a layout for a DDC region in accordance with an embodiment of the present invention. The DDC region 300 includes, for example, eight DDCs, although for clarity only two DDCs 305, 306 (ddc<0>, ddc<1>) are shown in Figure 3. Thirty-two data lines may traverse the DDC region 300 according to one embodiment. Eight data lines dw0-dw7 are shown in Figure 3. In contrast with Figure 2, the dvrify lines are routed horizontally to verify data stored in each DDC. The dvrify lines 310 and 312 are shown, labeled dvrify<0> and dvrify <1>. Orienting the dvrify lines horizontally increases the amount of width available to route the data lines across the DDC region 300.

[023] Rather than having a single csl line for each byte, as was the case in Figure 2, in the embodiment of Figure 3, one csl line is provided for a plurality of bytes of data lines, such as one every four bytes of data lines. In some embodiments, one csl line may be provided every eight bytes of data lines. Other frequencies may also be used. Accordingly, the csl line 320 may be used to select four bytes of data lines. To include a particular byte of data lines out of the four bytes of data lines, horizontal csl_byte select lines 322, 324 are provided. A selected csl line in combination with a csl_byte signal accordingly selects a particular byte of data lines. By removing three of the vertical csl lines for each four byte grouping, the spacing available for data lines traversing the region 300 may also be increased. In this manner, there may be sufficient width to route the thirty-two data lines across the region 300 from one memory to another.

[024] For example, the dw0 line arrives at the DDC region 300 from a first memory. The dw0 line is coupled to a transistor 330. The dw0 line electrically continues as line 332 on to the second memory. In this manner, the dw0 line is coupled from the first memory, through the DDC region, to the second memory. Data read from or data to be programmed into either the first or second memory may be stored in the DDCs present in the DDC region 300.

[025] Figure 4 is a schematic illustration of a secondary data cache accessing circuit in accordance with an embodiment of the present invention. As known in the art, each dynamic data cache may include a primary and a secondary data cache. Data may be read out or into the secondary data cache using data i/o lines. One data i/o line 410 including complementary dataio signals dataio and dataio_ is shown in Figure 4. Each DDC used in a memory, including ddc<0> and ddc<1> of Figure 3 may output stored

data to a respective data i/o line, and may also receive data to be programmed from the respective data i/o line.

[026] In previous systems, one csl line may have been provided for each byte of DDC storage. However, in the embodiment of Figure 3 one csl line is provided for every four bytes of DDC storage and a csl_byte signal selects the particular byte to be output or input to or from the respective data i/o line. The cache access circuit 400 receives both the csl and csl_byte signals. The csl signal is provided to the gates of the transistors 412 and 414. When the transistors 412 and 414 are on, the data i/o line 410 is coupled to the source/drain terminals of the transistors 422 and 424. The transistors 422 and 424 are provided with the csl_byte signal at their gate terminals. If the transistors 422 and 424 are not turned on, the data i/o line will remain isolated from the secondary data cache line 450. If the transistors 422 and 424 have been turned on by the csl_byte signal and the transistors 412 and 414 have been turned on by the csl signal, the data i/o line 410 will be coupled to the sdc line 450. In this manner, both the csl signal and the csl_byte signal must be sufficient to turn on their respective transistors before the secondary data cache is coupled to the data i/o line.

[027] The sdc line 450 is coupled to two cross-coupled inverters 460, 462. While the cross-coupled inverters 460, 462 may be implemented in any suitable manner, as shown in Figure 4, each of the inverters 460, 462 includes two transistors. A first transistor of each pair 462 and 464 receive a read signal at their respective gates. A second transistor of each pair 466 and 468 receive a signal from the sdc line 450 at their respective gates. In this manner, the cross-coupled inverters 460, 462 may serve as a latch.

[028] Figure 5 is a schematic illustration of a DDC region including a CSL decoder in accordance with an embodiment of the present invention. The DDC region 510 includes eight DDCs, ddc<0> through ddc<7>. The DDCs are each eight byte DDCs. The DDC region 510 is divided into two four byte regions 512 and 514 by way of illustration. One csl line traverses the DDC region 510 for each of the four byte regions 512 and 514. The csl line 520 traverses across the layout regions for each of the DDCs ddc<0> through ddc<7> in the first four byte region 512. The csl line 522 traverses across the layout regions for each of the DDCs ddc<0> through ddc<7> in the second four byte region 514. Although the csl lines 520 and 522 are shown positioned at an edge of the respective four-byte DDC regions 512 and 514, the csl lines 520 and 522 may be positioned anywhere laterally along the four-byte regions in other embodiments.

[029] Each csl line also includes horizontal branches extending across each byte of the respective four-byte region. For example, the csl line 520 is electrically connected to a branch 530. The branch 530 provides the csl_1 signal from the csl line 520 to access circuits in each byte of ddc<0> in the region 512. Although not shown in Figure 5, similar branches connected to the csl line 520 are provided for each of the DDCs ddc<0> through ddc<7>, including the branch 532 shown in ddc<7>. The csl line 522 similarly connects to multiple branches that may provide the csl_2 signal from the csl line 522 to each byte of the DDCs in the region 514. The branch 540 provides the csl_2 signal from the csl line 522 to each byte of the ddc<0> in the region 514, for example, while the branch 542 provides the csl_2 signal from the csl line 522 to each byte of the ddc<7> in the region 514. In this manner, the csl_1 signal may be provided to each byte of the four byte DDCs in the region 512 using only a single line traversing the DDC region in parallel with the bit lines. The branches run perpendicular to the bit lines. The csl_2 signal may be provided to each byte of the four byte DDC in the region 514 using only a single line traversing the DDC region in parallel with the bit lines.

[030] As was generally described above with reference to Figure 4, a csl_byte signal may be provided to the DDCs to select one of the four bytes served by the csl lines. Accordingly, the csl_byte lines 550 and 552 are shown in Figure 5. The csl_byte line 550 provides the csl_byte signal to each byte of ddc<0>, both in the region 512 and the region 514. The csl_byte line 552 provides the csl_byte signal to each byte of the ddc<7>, both in the region 512 and in the region 514. Although not shown, additional csl_byte lines are provided for each of the other DDCs in Figure 5. A particular byte of the DDCs may be selected by providing a csl signal corresponding to the four-byte region in which the particular byte is located, and providing one or more csl_byte signals to select which byte of the four-byte region should be selected.

[031] A csl decoder 560 is also shown in Figure 5. The csl decoder 560 may provide (e.g. generate) the csl_1 and csl_2 signals. Decoder logic 570 may generate four csl signals – labeled csl a,b,c,d, in Figure 5, corresponding to an address received by the decoder logic 570. The decoder logic 570 may also generate the csl_byte signal based on the address. The csl a,b,c,d signals may each be carried on multiple bus lines – with eight bus lines shown for each signal in Figure 5. The number of bus lines may be selected based on a density of the memory array. One NOR gate is provided for each csl line to generate the corresponding csl signal. For example, the NOR gate 575 is coupled

to the csl line 520. The NOR gate 575 is coupled to the lines 580-583 to receive the csl a,b,c,d signals. If the csl a,b,c,d signals provided select the four-byte region 512, the csl_1 signal may transition high, selecting the region 512. Similarly, the NOR gate 576 is also coupled to the lines 580-583 to receive the csl a,b,c,d signals. If the csl a,b,c,d signals provided select the four-byte region 514, the csl_2 signal may transition high, selecting the region 514. In other examples, a NAND gate followed by an inverter may be used in place of one or both of the NOR gates 575, 576. Note that only one NOR gate is used in this example for each csl line, corresponding to each four byte region in the example of Figure 5. Prior systems required one NOR gate decoder for each byte when a csl line was provided for each byte. Accordingly, embodiment of the present invention may advantageously reduce the number of NOR gates required for csl decoding and may also reduce the area required to implement the csl decoders.

[032] A flash memory 600 that includes dynamic data caches in accordance with an embodiment of the invention is shown in Figure 6. The flash memory 600 includes two arrays of flash memory cells 130 and 135. The arrays of flash memory cells may be arranged in banks of rows and columns, as has generally been described above.

[033] Most command signals, address signals and write data signals may be applied to the memory 600 as sets of sequential input/output ("I/O") signals transmitted through an I/O bus 634. Similarly, read data signals may be output from the memory 600 through the I/O bus 634. The I/O bus may be connected to an I/O control unit 640 that may route the signals between the I/O bus 634 and an internal data bus 642, an internal address bus 644, and an internal command bus 646. The memory 600 may also include a control logic unit 650 that may receive a number of control signals either externally or through the command bus 646 to control the operation of the memory 600. The control logic unit 150 may, for example, generate the csl and/or csl_byte signals described above. The address bus 644 may apply row address signals to row decoders 660, 661 and column address signals to column decoders 664, 665. The row decoders 660, 661 may each include a word line driver system, which drives the word lines of the respective arrays with appropriate voltages corresponding to the decoded row address signals and the type of memory operation. Similarly, the column decoders 664, 665 may enable write data signals to be applied to bit lines for columns corresponding to the column address signals and allow read data signals to be coupled from bit lines for columns corresponding to the column address signals.

- [034] In response to the memory commands decoded by the control logic unit 150, the flash memory cells in the arrays 630 and 635 may be erased, programmed, and/or read. The memory arrays 630, 635 may be programmed on a row-by-row or page-by-page basis. After the row address signals have been applied to the address bus 644, the I/O control unit 640 may route write data signals to the dynamic data caches 680. The dynamic data caches 680 may be laid out and csl signals decoded in accordance with Figures 3-5 described above. That is, the DDC region 510 and csl decoder 560 of Figure 5 may be used to implement the DDCs 680 shown in Figure 6. Embodiments described above may advantageously allow the two memory arrays 630, 635 to operate with a shared stack of eight DDCs within a predetermined width.
- [035] Referring again to Figure 6, write data signals may be stored in the DDCs 680 in successive sets each having a size corresponding to the width of the I/O bus 634. The DDCs 680 may sequentially store sets of write data signals for an entire row or page of flash memory cells in the arrays 630, 635. All of the stored write data signals may then be used to program a row or page of memory cells in one or both of the arrays 630, 635 selected by the row address coupled through the address bus 644. In a similar manner, during a read operation, data signals from a row or page of memory cells selected by the row address coupled through the address bus 644 may be stored in the dynamic data caches 680. Sets of data signals corresponding in size to the width of the I/O bus 634 may then be sequentially transferred through the I/O control unit 640 from the dynamic data caches 680 to the I/O bus 634.
- [036] The memory device shown in Figure 6 may be implemented in any of a variety of products employing processors and memory including for example cameras, phones, wireless devices, displays, chip sets, set top boxes, gaming systems, vehicles, and appliances. Resulting devices employing the memory system may benefit from the embodiments of dynamic data caches and/or decoders described above to perform their ultimate user function.
- [037] From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. A dynamic data cache region comprising:
a plurality of dynamic data caches, each configured to store a plurality of bytes of data;
a plurality of bit lines, wherein the plurality of bit lines are configured to provide the plurality of bytes of data to the plurality of dynamic data caches;
a first select line configured to select a group of the plurality of bytes of data; and
a second select line configured to select a byte within the group.
2. The dynamic data cache region of claim 1, wherein the first select line is parallel to the plurality of bit lines.
3. The dynamic data cache region of claim 2, wherein the second select line is perpendicular to the plurality of bit lines.
4. The dynamic data cache region of claim 1, further comprising a plurality of second select lines, wherein each of the plurality of second select lines is associated with a respective one of the bytes within the group.
5. The dynamic data cache region of claim 1, wherein the plurality of bit lines are configured to couple to at least two memory arrays.
6. A dynamic data cache system comprising:
a plurality of dynamic data caches, wherein each of the dynamic data caches includes storage for a first plurality of bytes and a second plurality of bytes;
a first select line configured to select the first plurality of bytes of the plurality of dynamic data caches;
a second select line configured to select the second plurality of bytes of the plurality of dynamic data caches;

12

a first decoder coupled to the first select line and configured to decode a select signal and provide the decoded select signal to the first select line; and

a second decoder coupled to the second select line and configured to decode the select signal and provide the decoded select signal to the second select line.

7. The dynamic data cache system of claim 6, wherein the first plurality of bytes and the second plurality of bytes each are four bytes.

8. The dynamic data cache system of claim 6, wherein the first decoder comprises a NOR gate.

9. The dynamic data cache system of claim 6, further comprising a plurality of additional select lines configured to select one byte from among the first and second plurality of bytes.

10. The dynamic data cache system of claim 9, further comprising a plurality of bit lines configured to provide the first and second plurality of bytes to the plurality of dynamic data caches, wherein the first and second select lines are routed parallel to the bit lines and wherein the plurality of additional select lines are routed perpendicular to the bit lines.

11. A cache access circuit comprising:

a data input/output line;

a cache line;

a first transistor having a source/drain terminal coupled to the data input/output line, wherein the first transistor is configured to receive a first select signal at its gate terminal;

a second transistor having a first source/drain terminal coupled to the source/drain terminal of the first transistor and a second source/drain terminal coupled to the cache line, wherein the second transistor is configured to receive a second select signal at its gate terminal;

13

wherein the first select signal is configured to select a group of bytes, and the second select signal is configured to select a particular byte within the group of bytes.

12. The cache access circuit of claim 11, wherein the data input/output line and the cache line are differential lines.

13. The cache access circuit of claim 11, wherein the first and second transistors are configured to couple the data input/output line to the cache line responsive to a combination of the first and second select signals.

14. The cache access circuit of claim 11, further comprising a pair of cross coupled inverters coupled to the cache line.

15. The cache access circuit of claim 11, wherein the cache line is coupled to a secondary data cache.

16. A method for accessing a dynamic data cache, the method comprising:
providing a first signal configured to select a plurality of bytes of the dynamic data cache to an access circuit;
providing a second signal configured to select one of the bytes of the plurality of bytes to the access circuit;
wherein a data input/output line is coupled to a data cache responsive to both the first and second signals.

17. The method of claim 16, further comprising decoding the first signal from a plurality of column select signals, wherein the act of decoding comprises providing the plurality of column select signals to a NOR gate.

18. The method of claim 16, wherein said providing a first signal comprises applying the first signal to a first select line, and wherein said providing a second signal comprises applying the second signal to a second select line.

19. The method of claim 18, wherein the first and second select lines are perpendicular to each other.

20. The method of claim 16, wherein the data cache is a dynamic data cache of a flash memory device.

21. A memory device having a dynamic data cache (DDC) region including a DDC, the memory device comprising:

a plurality of data lines, wherein each of the plurality of data lines traverses the DDC region, wherein the plurality of data lines comprises a plurality of bytes of data lines;

a single column select line configured to select the plurality of bytes of data lines; and

a single verify line corresponding to the DDC, wherein the verify line does not run parallel to the data lines as it traverses the DDC region.

22. The memory device of claim 21, wherein the verify line is perpendicular to the plurality of data lines.

23. The memory device of claim 21, wherein the verify line is configured to verify data stored in the DDC.

24. The memory device of claim 23, further comprising a plurality of byte select lines, wherein each of the byte select lines is configured to select a respective one of the plurality of bytes of data lines.

25. The memory device of claim 24, wherein the plurality of byte select lines do not run parallel to the data lines as they traverse the DDC region.

26. The memory device of claim 25, wherein each of the plurality of byte select lines are perpendicular to the plurality of bytes of data lines.

27. A memory device having a dynamic data cache (DDC) region including a DDC, the memory device comprising:

a plurality of bytes of data lines, wherein each of the plurality of data lines traverses the DDC region;

a single column select line configured to select the plurality of bytes of data lines;
and

a plurality of byte select lines, wherein each of the byte select lines is configured to select a respective one of the plurality of bytes of data lines.

28. The memory device of claim 27, wherein each of the plurality of byte select lines do not run parallel to the plurality of bytes of data lines as they traverse the DDC region.

29. The memory device of claim 28, wherein each of the plurality of byte select lines are perpendicular to the plurality of bytes of data lines.

30. The memory device of claim 27, further comprising a single verify line corresponding to the DDC.

31. The memory device of claim 30, wherein the single verify line does not run parallel to the plurality of bytes of data lines as it traverses the DDC region.

32. The memory device of claim 31, wherein the verify line is perpendicular to the plurality of bytes of data lines.

1/6

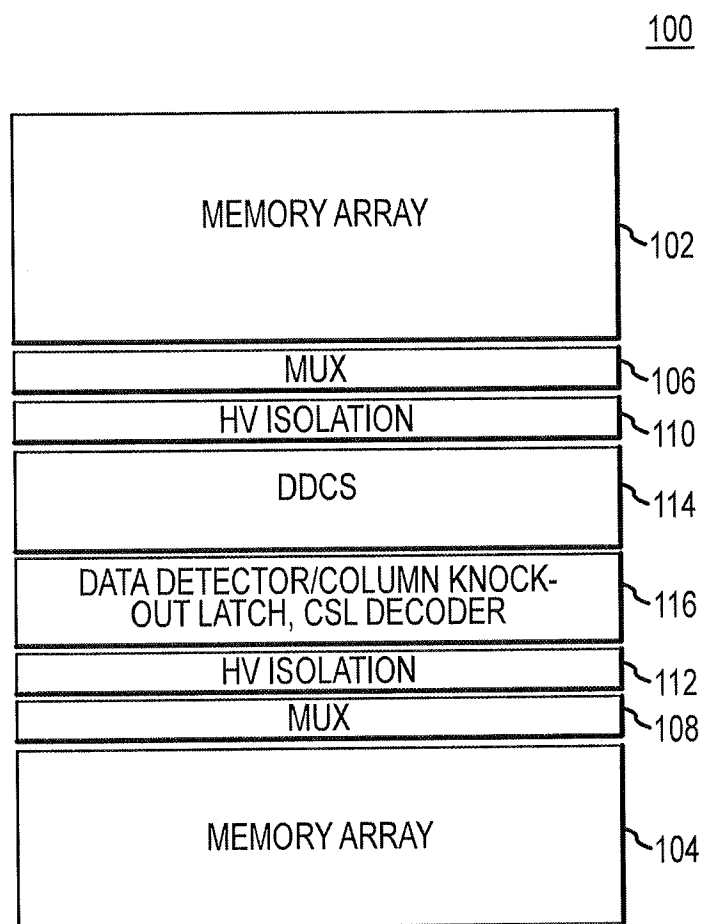


FIGURE 1

2/6

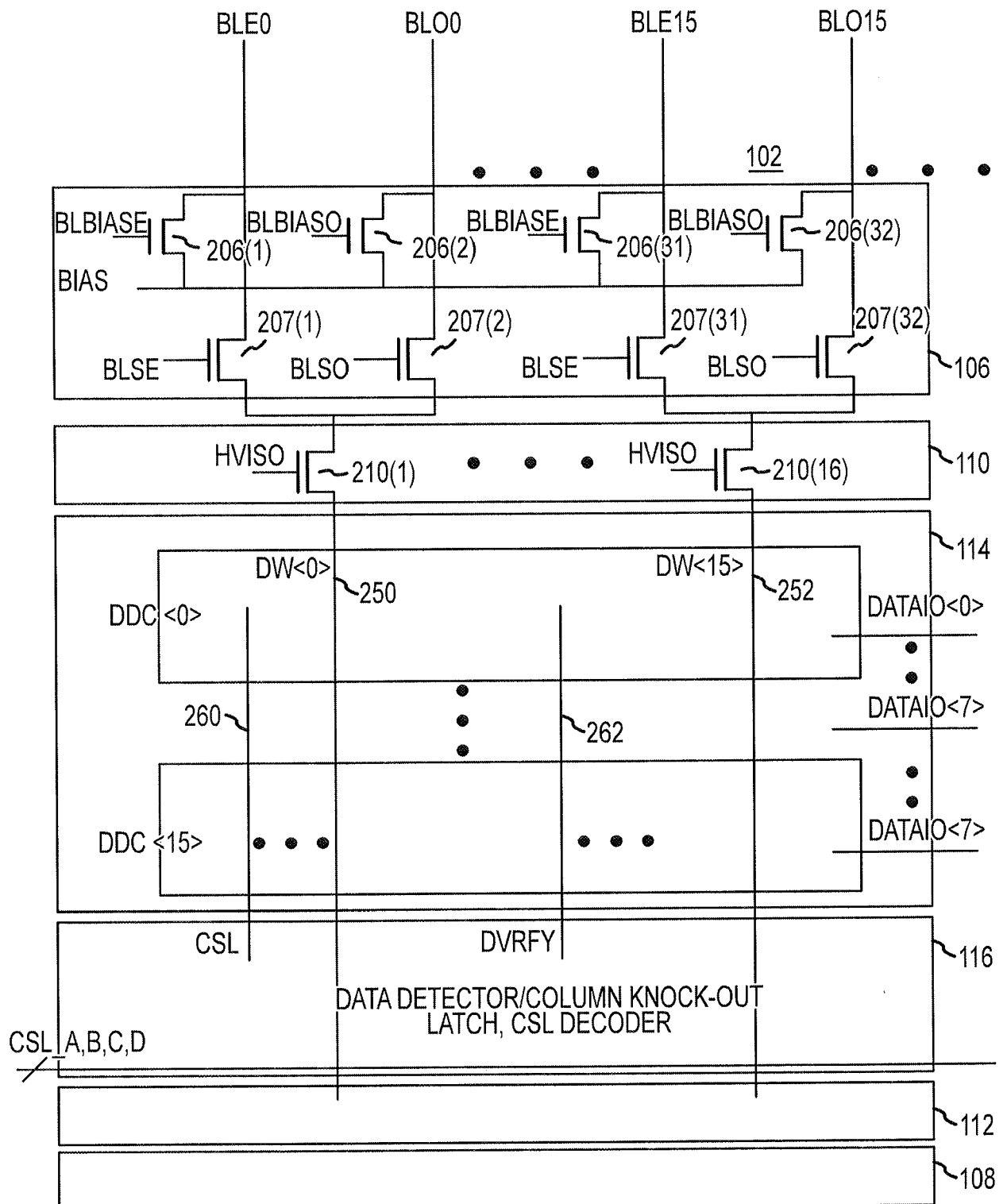


FIGURE 2

104

3/6

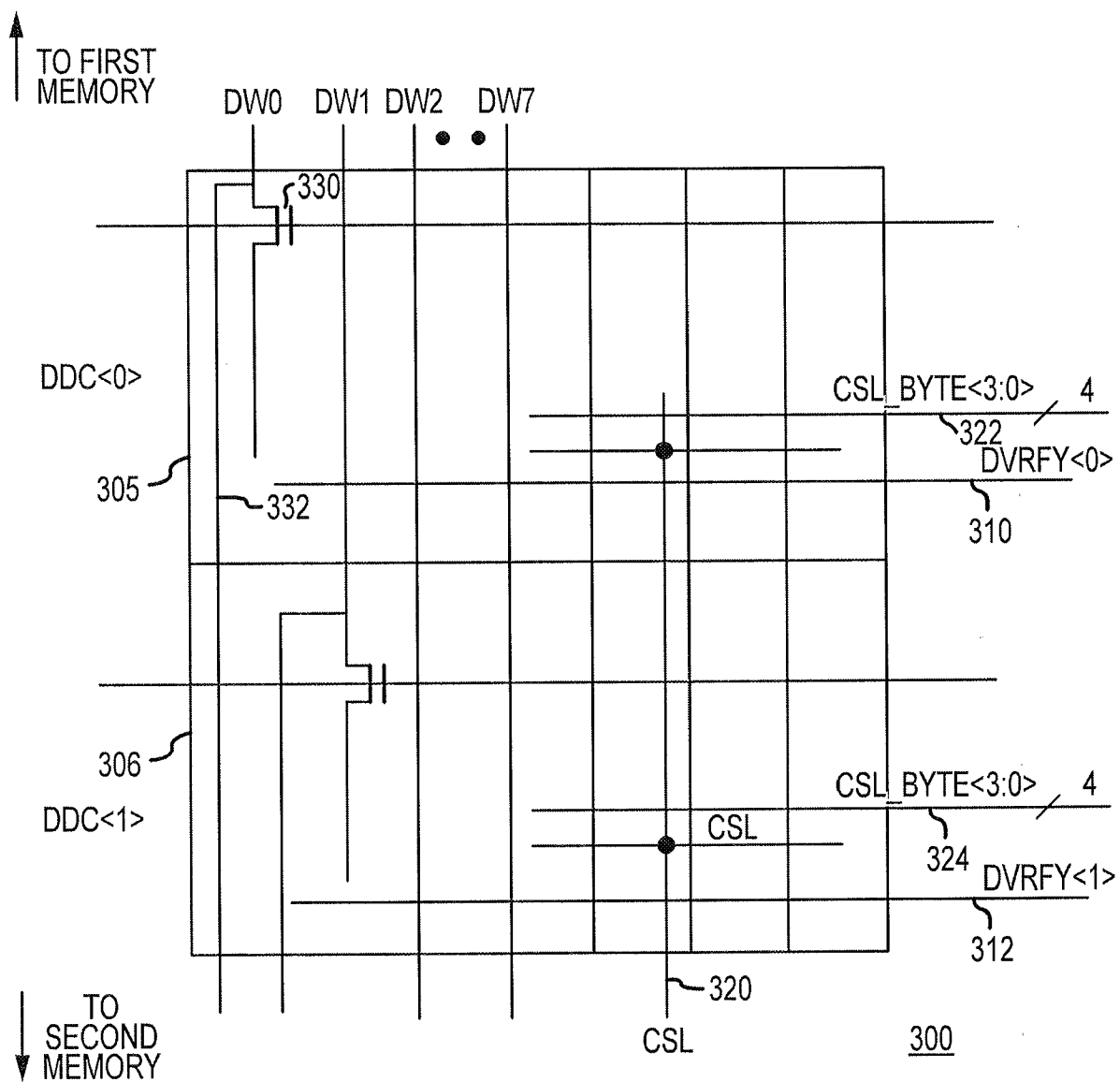


FIGURE 3

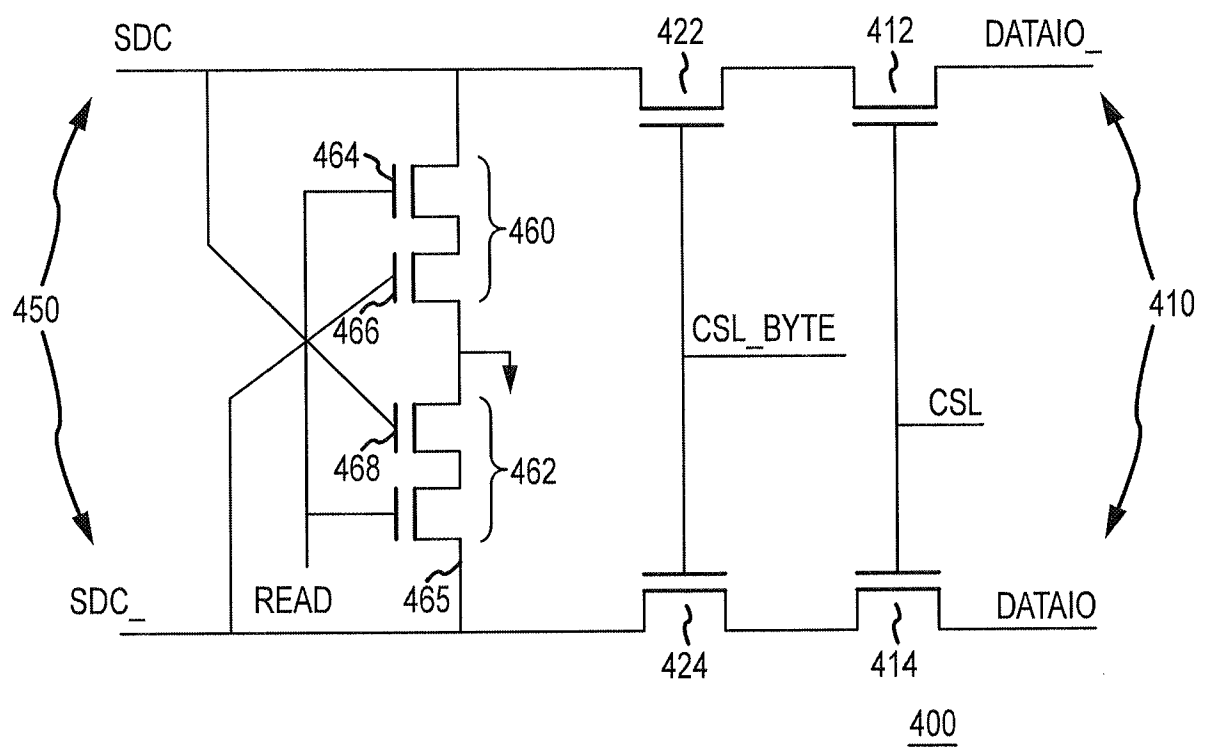


FIGURE 4

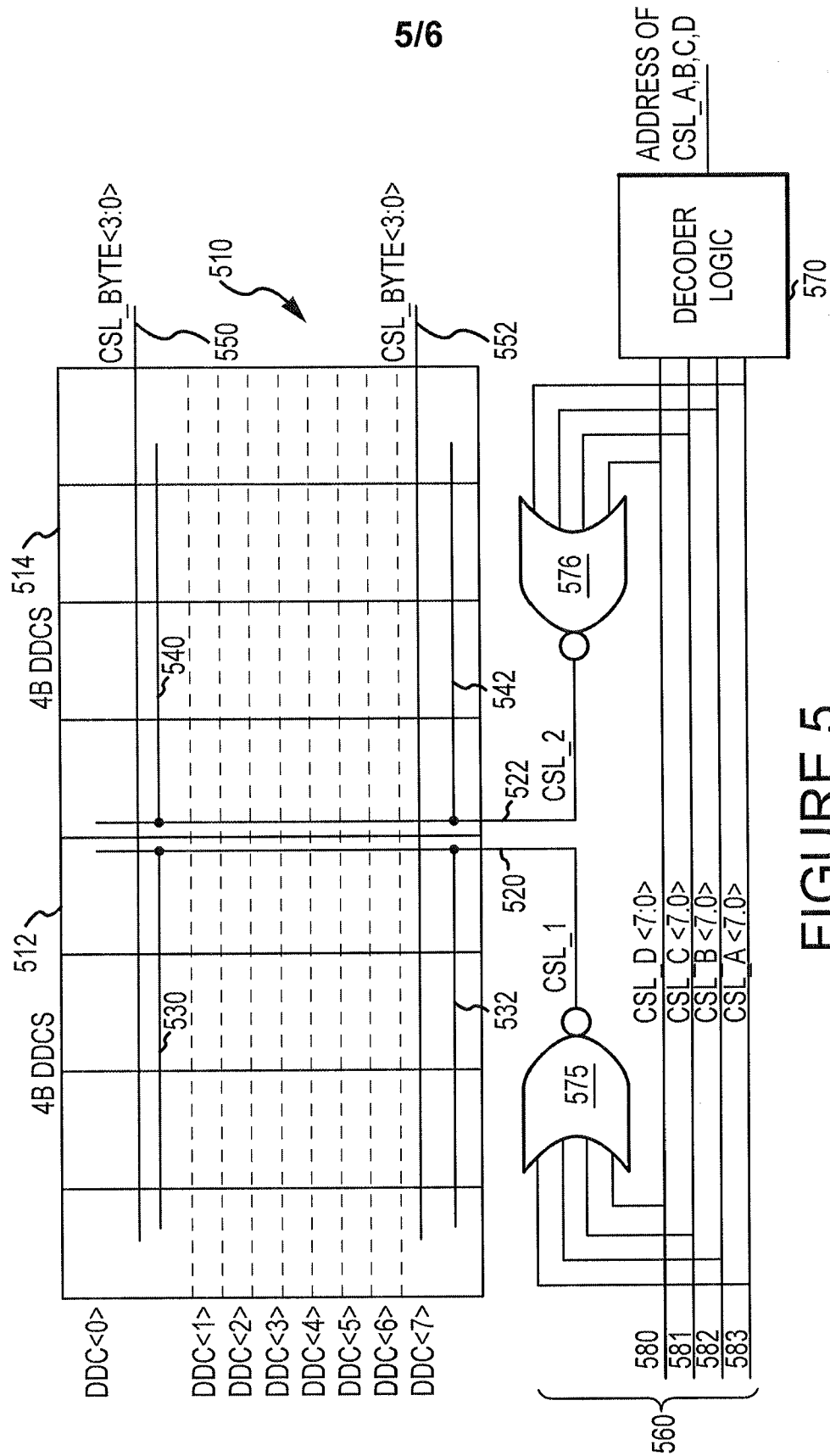


FIGURE 5

6/6

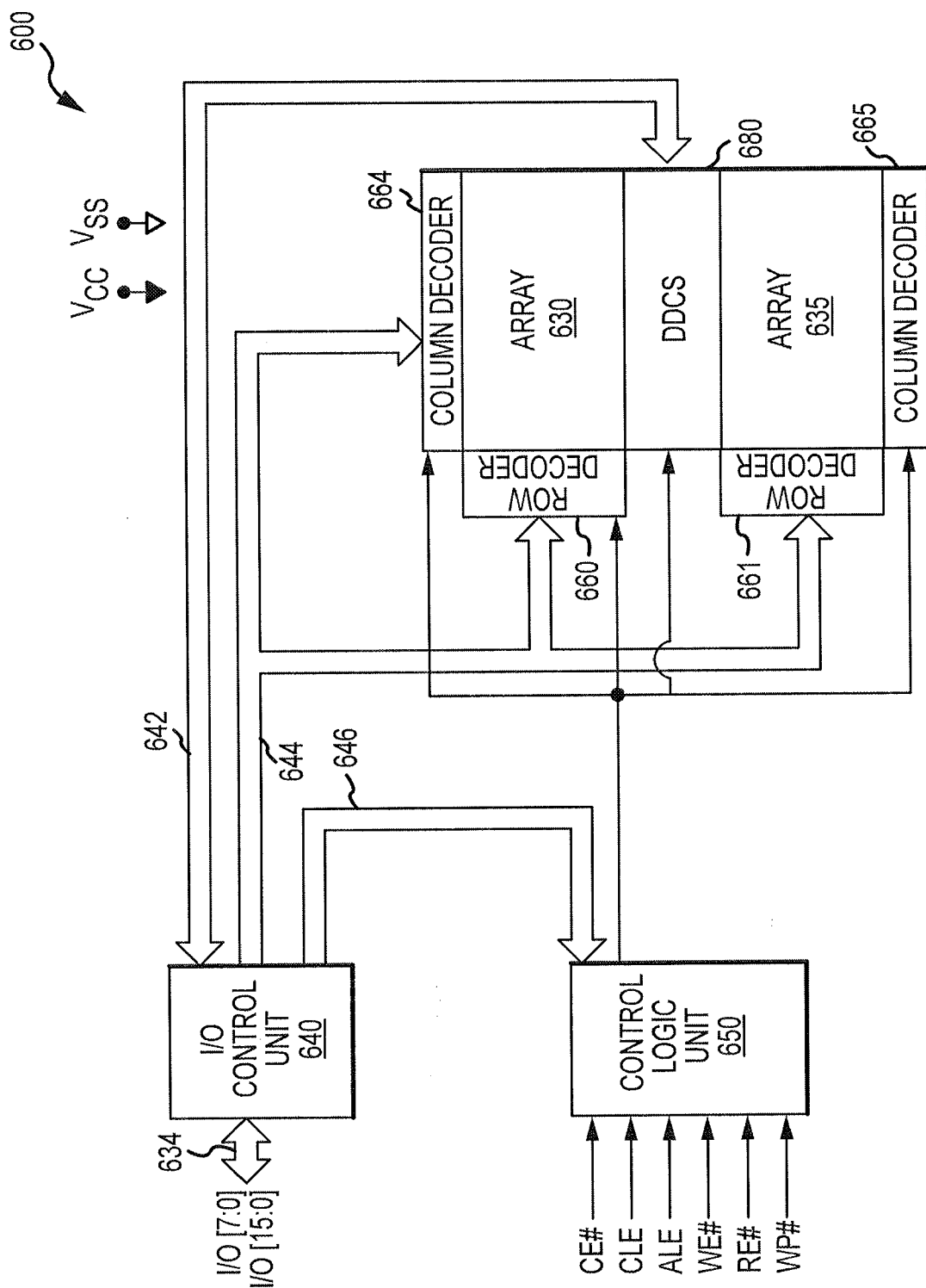


FIGURE 6