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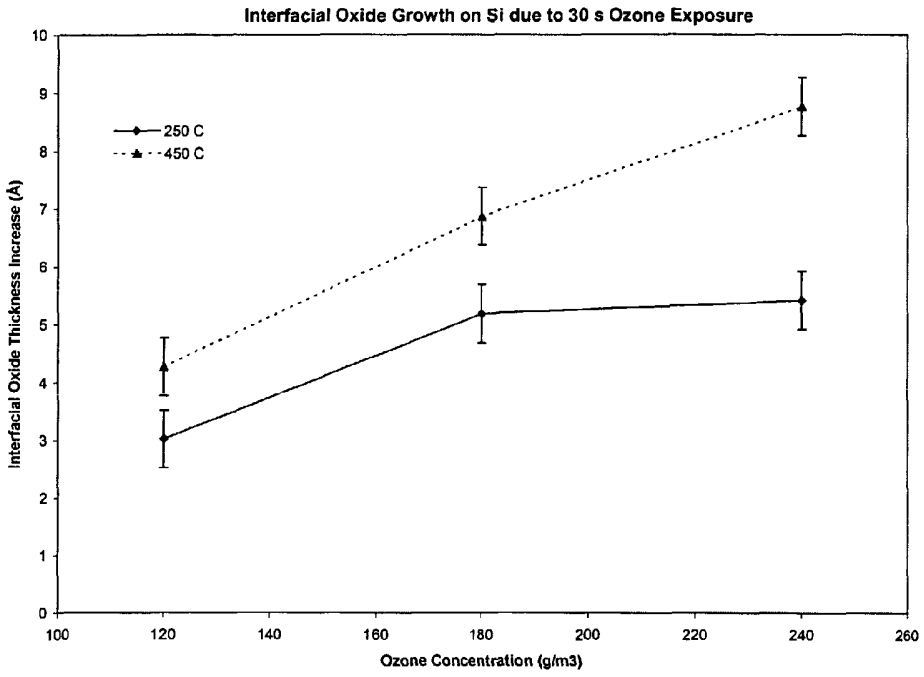
(54) Title: OZONE OXIDATION OF SILICON SUBSTRATES FOR FOR FORMATION OF AN INTERFACIAL LAYER FOR HIGH-K GATE STACKS




(57) Abstract: A new method of forming an interfacial oxide layer for gate structures is provided. The method comprises ozone oxidation of a silicon substrate at low temperatures to form an interfacial oxide layer. A method of making gate stacks is also provided which includes forming an interfacial oxide layer on the top surface of a silicon substrate by ozone oxidation at a low temperature, and depositing dielectric layers on the top of the interfacial oxide layer.

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# OZONE OXIDATION OF SILICON SUBSTRATES FOR FORMATION OF AN INTERFACIAL LAYER FOR HIGH-K GATE STACKS

## CROSS REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of and priority to U.S. Provisional Patent Application Serial No. 60/399,463 filed July 29, 2002, entitled "Ozone Oxidation of Silicon Substrates for Formation of an Interfacial Layer for High-K Gate Stacks," the entire disclosure of which is hereby incorporated by reference. This application is related to U.S. Provisional Patent Application Serial No. 60/396,733 filed July 19, 2002, entitled "Steam Oxidation for the Formation of Thin Gate and Capacitor Dielectrics with Improved Electrical Properties;" and U.S. Provisional Patent Application Serial No. 60/396,742 filed July 19, 2002, entitled "Low Temperature Ozone of Gate and Capacitor Dielectrics," the disclosures of both or which are hereby incorporated by reference in their entirety.

## FIELD OF THE INVENTION

The present invention relates generally to the field of semiconductors. More specifically, the present invention relates to methods of forming interfacial layers for high dielectric constant (high-k) gate stacks by ozone oxidation of silicon substrates at low temperatures.

## BACKGROUND OF THE INVENTION

Oxidation processes are often an important step in the fabrication of semiconductor devices. Various equipment is known in the art for conducting oxidation of semiconductor

devices.

In a batch furnace, or in a single wafer system using a Rapid Thermal Oxidation (RTO) process, silicon wafers are generally ramped up to an elevated temperature (circa 900 C) in an ambient atmosphere of inert gas (such as nitrogen and/or argon) that contains a small percentage of dry oxygen (typically 1-10%). After the wafer is heat stabilized at an oxidation process temperature, a higher concentration of oxygen is introduced, followed by the introduction of steam. A final step may involve purging the steam and ramping down the temperature in an ambient atmosphere of inert gas. This dry/wet oxidation process is used to endow the silicon oxide with better electrical properties, such as lower leakage, higher breakdown voltage, and lower interface trap density, compared to a dry process where silicon oxide is prepared using oxygen without steam.

However, the quality of the resulting silicon oxide in the dry/wet process is an average between the properties of dry and wet silicon oxide, depending upon the amount of dry silicon oxide growth during the ramp up and stabilization steps (the first dry step) in the process. As device geometries are reduced and oxide films become thinner, a greater percentage of the oxide thickness is the oxide grown in the first dry step. This results in an oxide film with poor properties. Therefore, new methods for growing high quality oxides are needed.

As the future device scale aggressively reduces, alternative high-k dielectrics to conventional silicon dioxide dielectrics ($SiO_2$) are actively sought. Semiconductor devices of future generation require thin dielectric films for metal-oxide-silicon (MOS) transistor gates and capacitor dielectrics. As oxides are scaled down, the tunneling leakage current becomes significant and limits the useful range for gate oxides to about 1.8 nm or more.

To address this problem, different dielectric materials are being evaluated, particularly materials exhibiting a dielectric constant (k) greater than silicon oxides (which have a k of about 3.9). Silicon nitride (having a k of about 8), and higher dielectric constant metal oxides such as hafnium oxide $HfO_2$ (having a k of about 20-25), zirconium oxide $ZrO_2$ (having a k of about 20-25), and hafnium (Hf) and zirconium (Zr) silicates are considered alternative materials to silicon oxide to provide gate dielectrics with high capacitance without compromising the leakage current.

For advanced high-k or oxide/nitride (ON) gate stacks, high quality thin interfacial oxide layers are needed for better electrical properties, such as mobility. In the prior art, interfacial oxide layers for gate stacks are conventionally produced by high temperature

thermal or steam oxidation, or wet chemical oxidation. With these conventional techniques it is difficult to control oxide thickness and quality, and as stated above, such control is becoming increasing critical. There exists a need for fabrication of improved interfacial oxide layers, particularly interfacial oxide layers formed with better control in thickness, uniformity, and quality.

## SUMMARY OF THE INVENTION

In general, the present invention provides an improved oxidation method in the fabrication of semiconductors. More specifically, the present invention provides a method of producing interfacial oxide layers for high k gate stacks by ozone oxidation at a low temperature. Of particular advantage, the present invention promotes the formation of improved interfacial oxide layers as compared to conventional fabrication methods using high temperature thermal or steam oxidation and wet chemical oxidation. The present invention further provides a method of producing high dielectric constant (k) gate stacks which includes an interfacial oxide layer formed by the ozone oxidation method of the present invention.

In one aspect of the present invention, an interfacial oxide layer is formed by ozone oxidation at a low temperature on the top surface of a substrate such as a silicon wafer. The ozone oxidation can be performed at a low temperature either thermally or photochemically. The interfacial oxide layer formed by the present ozone oxidation method has controlled thickness, uniformity, and quality.

In another aspect of the present invention a method of producing a gate structure including an interfacial oxide layer formed by ozone oxidation at a low temperature is provided. In accordance with this embodiment, an interfacial oxide layer is formed by ozone oxidation at a low temperature on the top surface of a silicon substrate. A dielectric material is then deposited on the top surface of the interfacial oxide layer. Preferably the top surface of the interfacial oxide layer is nitrided prior to the deposition of the dielectric material. The deposition of dielectric materials can be performed by chemical vapor deposition, physical vapor deposition, jet vapor deposition, aerosol decomposition, or atomic layer deposition.

## BRIEF DESCRIPTION OF THE FIGURES

The foregoing and other objects of the invention will be more clearly understood from the following description when read in conjunction with the accompanying drawings in

which:

FIGS. 1A and 1B are simplified cross-sectional schematic diagrams of two different apparatus suitable for carrying out the method of the present invention.

FIG. 2 is a cross-sectional view of a gate stack structure including an interfacial oxide layer formed by ozone oxidation according to one embodiment of the present invention.

FIG. 3 is graph illustrating interfacial oxide growth on a silicon substrate according to two embodiments of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

In general, the present invention provides a method of producing an interfacial oxide layer for gate structures. In one aspect of the present invention, an interfacial oxide layer is formed by ozone oxidation at a low temperature on the top surface of a substrate such as a silicon wafer. The ozone oxidation can be performed at a low temperature either thermally or photochemically. The interfacial oxide layer formed by the present ozone oxidation method has controlled thickness, uniformity, and quality.

In particular, the present method comprises a step of forming an interfacial oxide layer by ozone oxidation at a low temperature of a silicon substrate. The ozone oxidation can be performed thermally or photochemically. The ozone oxidation is carried out at a temperature in the range of approximately 25°C to 600°C. In another embodiment the ozone oxidation is carried out at a temperature in the range of approximately 250°C to 450°C. These temperature ranges are significantly less than conventional oxidation treatment methods. In one exemplary embodiment, oxidation is carried out with ozone at a concentration in the range of approximately 120 $g/m^3$ to 240 $g/m^3$, with an ozone exposure time of approximately 30 seconds.

The ozone oxidation reaction can be summarized in the following equations:

$$O_3 \rightarrow O_2 + O \quad (1)$$

$$Si + 2O \rightarrow SiO_2 \quad (2)$$

Ozone is disassociated into oxygen molecules and atomic oxygen under thermal or photochemical conditions. When the oxidation method is carried out with photochemical excitation, the temperature of the method is carried out at the lower end of the recited range.

The atomic oxygen reacts with silicon on the top surface of the silicon substrate to form an interfacial oxide layer.

The method of the present invention may be carried out in any suitable equipment known in the art. Oxidation systems are well known in the industry. Examples of suitable systems include that described in U.S. Patent No. 6,300,600, entitled Hot Wall Rapid Thermal Processor, and U.S. Provisional Patent Application Serial No. 60/428,526, filed November 22, 2002, entitled Thermal Processing System and Method for Using the Same, both of which are incorporated herein by reference in their entirety. The oxidation method may also be carried out in an atomic layer deposition system.

As such systems are well known, they are not described in detail herein but two examples are shown in a simplified manner in FIGS. 1A and 1B. Referring to FIG. 1A, a hot wall chamber type system 101 is partially shown in a cross sectional view. This type of system processes a batch of wafers. In this embodiment, a plurality of wafers 100 are stacked vertically in the chamber. Heater elements (not shown) are provided to heat the environment of the wafer 100. Gases are conveyed to and from the chamber 101 via inlet 104 and outlet 105, respectively.

Referring to FIG. 1B, a cold wall chamber type system 102 is partially shown in a cross sectional view. In this embodiment, a single wafer 100 is processes in the chamber. The wafer is supported and heated by a heated support or chuck 103. Gases are conveyed to and from the chamber 102 via inlet 104 and outlet 105, respectively. Those skilled in the art will recognize that other system may be used to carry out the method of the present invention.

The present invention of forming an interfacial oxide layer is advantageous in preparing high k gate structures. In preparing such gate structures, an interfacial oxide layer is first formed on the top surface of a substrate by ozone oxidation at a low temperature. In one example the temperature is in the range of approximately 25°C to 600°C. In another example the temperature is in the range of approximately 250°C to 450°C. Dielectric materials are then deposited on the top of the interfacial oxide layer by a variety of deposition methods.

One embodiment of the present invention of making gate stacks is now described in more detail with reference to FIG. 2. A silicon substrate or wafer 200 is provided as the substrate of a gate structure. The substrate is placed in a chamber and exposed to ozone to oxidize the top surface of the substrate. In one example, the substrate is exposed to ozone at a

concentration in the range of approximately 120 g/m3 to 240 g/m3, for an exposure time of about 30 seconds. Oxygen gas may also be conveyed to the chamber. In one example oxygen is conveyed to the chamber at a total flow rate of about 200 sccm. Ozone oxidation is performed either thermally or photochemically at a temperature in the range of approximately 25°C to 600°C, more usually in a range of approximately 250°C to 450°C, to form an interfacial oxide layer 202 on the top surface of the silicon substrate. In this example the interfacial oxide layer is comprised of $SiO_2$. The thickness of the interfacial oxide layer may vary as desired, and in one example interfacial oxide layers having a thickness in the range of approximately 3Å to 9 Å are grown.

After the interfacial layer 202 is formed by ozone oxidation, layers of dielectric materials are deposited sequentially on the top of the interfacial oxide layer 202. In one embodiment, one or more dielectric layers 204 (such as a metal oxide layer and the like ) are formed atop the interfacial layer 202. The dielectric layer 204 may be comprised of a mid-k dielectric material such as silicon nitride, or alternatively may be comprised of a high-k dielectric material such as $HfO_2$, $ZrO_2$, hafnium silicate, zirconium silicate and the like. The dielectric layer 204 may be comprised of a plurality of layers.

For preparing high-k gate stacks, it is preferred that the top surface of the interfacial oxide layer be thermally nitrided in $NH_3$ to form a nitrided oxide (SiON) layer 206 prior to deposition of mid- and/or high-k dielectric layers. Forming the nitrided oxide layer 206 avoids additional oxide growth in contact with the high-k metal oxide during the mid- or high dielectric deposition, or a post-gate stack deposition thermal treatment.

To form a gate device, a gate electrode 208 is formed on the top of the dielectric layers 204. The gate electrode may be formed of polysilicon, polySi-Ge, a metal gate material and the like, and is formed by well known conventional techniques.

The dielectric layers 204 on the top surface of the interfacial layer 202 can be formed by a variety of methods well known in the art, and typically are formed by conventional deposition techniques including but not limited to chemical vapor deposition (CVD) such as thermal CVD, plasma CVD, laser CVD, and photo assisted CVD, physical vapor deposition (PVD), jet vapor deposition, aerosol decomposition, or atomic layer deposition (ALD) such as thermal ALD and photo-assisted ALD.

Experimental

Several experiments were performed with the method of the present invention. Silicon substrates were placed in an oxidation chamber and exposed to ozone to oxidize the surface of the silicon substrate, forming an interfacial oxide layer thereon. The silicon substrates were exposed to ozone for a total ozone exposure time of 30 seconds. Oxygen was also conveyed to the chamber at a total oxygen flow rate of 200 sccm. The silicon substrate temperature was varied from 250 °C to 450 °C and the ozone concentration was varied from 120 g/m$^3$ to 240 g/m$^3$. The resultant interfacial oxide growth thickness (Å) is summarized in Table 1 below, and is graphically depicted in FIG. 3.

Table 1

| Wafer | $SiO_2$ Thickness Increase (Å) at | | |
|---|---|---|---|
| Temp | Ozone Concentration = | | |
| (C) | 120 g/m$^3$ | 180 g/m$^3$ | 240 g/m$^3$ |
| 250 C | 3.02 | 5.19 | 5.41 |
| 350 C | 4.52 | 7.56 | 7.51 |
| 450 C | 4.27 | 6.87 | 8.76 |

As illustrated in Table 1 and FIG. 3, the interfacial oxide thickness increased with the ozone concentration and temperature.

While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than limiting sense, as it is contemplated that modifications and combinations will readily occur to those skilled in the art, which modifications and combinations will be within the scope of the invention and the scope of the appended claims.

# CLAIMS

What is claimed:

1. A method of producing an interfacial oxide layer on a semiconductor substrate, comprising:

forming an interfacial oxide layer on top of the substrate by ozone oxidation at a temperature in the range of approximately 25°C to 600 °C .

2. The method of claim 1 wherein the ozone oxidation is carried out with photochemical excitation .

3. The method of claim 1 further comprising the step of:

exposing the surface of the interfacial oxide layer to $NH_3$ to form a nitrided oxide layer on top of the interfacial oxide layer.

4. A method of forming a gate structure on a substrate, comprising:

forming an interfacial oxide layer by ozone oxidation at a low temperature on a top surface of the substrate; and

depositing one or more dielectric layers on the top surface of the interfacial oxide layer.

5. The method of claim 4 further comprising:

nitriding the top surface of the interfacial oxide layer prior to depositing the one or more dielectric layers.

6. The method of claim 4 wherein the step of forming the interfacial oxide layer is carried out at a temperature ranging from approximately 250°C to 450°C.

7. The method of claim 4 wherein the step of depositing one or more dielectric layers is performed by chemical vapor deposition, physical vapor deposition, jet vapor deposition, aerosol decomposition, or atomic layer deposition.

8. The method of claim 4 further comprising:
depositing a gate electrode atop the one or more dielectric layers.

9. The method of claim 4 where said one or more dielectric layers are comprised of any of the following materials: silicon nitride, $HfO_2$, $ZrO_2$, hafnium silicate and zirconium silicate.

10. The method of claim 4 wherein the step of forming the interfacial oxide layer is carried out with photochemical excitation.

FIG. 1A

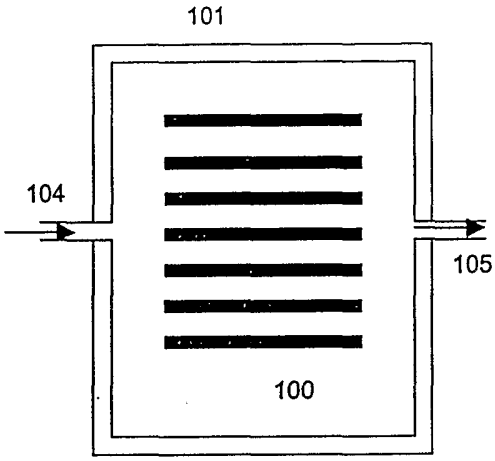
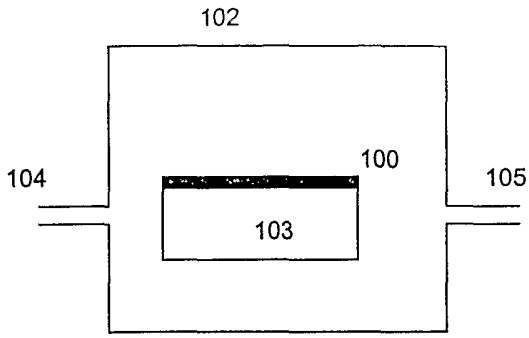



FIG. 1B.



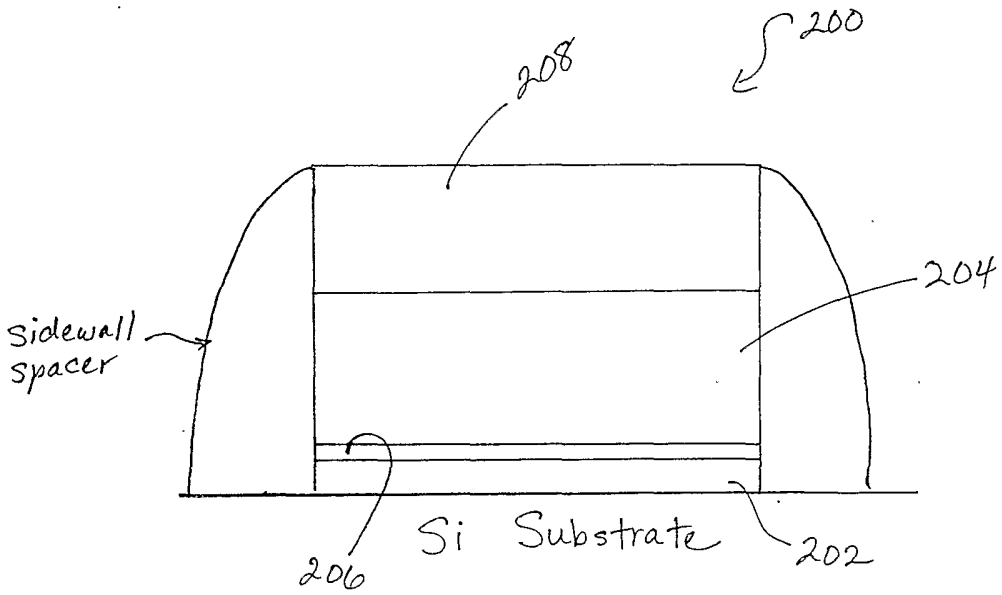
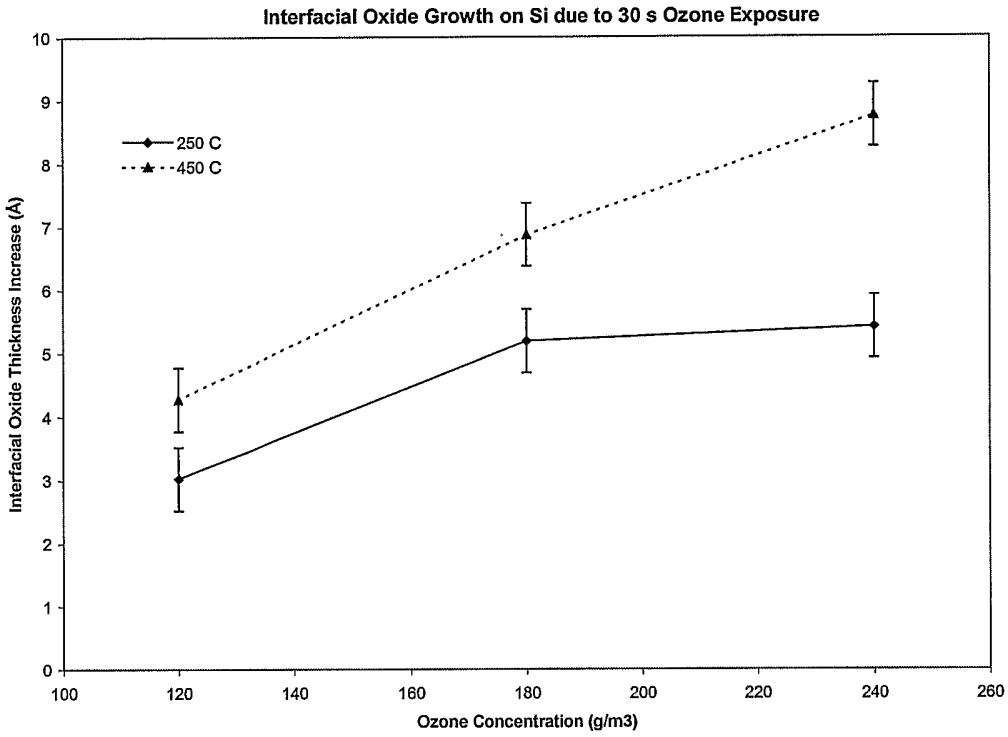




FIG. 2

FIG. 3


Interfacial Oxide Growth on Si due to 30 s Ozone Exposure
Interfacial Oxide Thickness Increase (Å)
Ozone Concentration (g/m3)
250 C
450 C
0
1
2
3
4
5
6
7
8
9
10
100
120
140
160
180
200
220
240
260