(19) DANMARK

(10) **DK/EP 2449782 T3**

Patent- og Varemærkestyrelsen

(12) # Oversættelse af europæisk patentskrift

(51) Int.Cl.: *H 04 N 19/70 (2014.01)* *H 04 N 19/11 (2014.01)* *H 04 N 19/136 (2014.01)* *H 04 N 19/147 (2014.01)* *H 04 N 19/176 (2014.01)* *H 04 N 19/196 (2014.01)* *H 04 N 19/463 (2014.01)* *H 04 N 19/96 (2014.01)*

(45) Oversættelsen bekendtgjort den: **2018-02-05**

(80) Dato for Den Europæiske Patentmyndigheds bekendtgørelse om meddelelse af patentet: **2017-12-06**

(86) Europæisk ansøgning nr.: **10743254.4**

(86) Europæisk indleveringsdag: **2010-06-29**

(87) Den europæiske ansøgnings publiceringsdag: **2012-05-09**

(86) International ansøgning nr.: **US2010001862**

(87) Internationalt publikationsnr.: **WO2011002504**

(30) Prioritet: **2009-07-01 US 222177 P**

(84) Designerede stater: **AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR**

(73) Patenthaver: **Thomson Licensing, 1-5, rue Jeanne d'Arc, 92130 Issy-les-Moulineaux, Frankrig**

(72) Opfinder: **ZHENG, Yunfei, 123 Quail Ridge Drive, Plainsboro, New Jersey 08536, USA**
XU, Qian, 206 Deer Creek Drive, Plainsboro, New Jersey 08536, USA
LU, Xiaoan, 30 Kennedy Court, Princeton, New Jersey 08540, USA
YIN, Peng, 6 John Street, Ithaca, New York 14850, USA
SOLE, Joel, 94 1/2 Leigh Avenue, Princeton, New Jersey 08542, USA
ABBAS, Adeel, 2608 Pheasant Hollow Drive, Plainsboro, New Jersey 08536, USA

(74) Fuldmægtig i Danmark: **Plougmann Vingtoft A/S, Rued Langgaards Vej 8, 2300 København S, Danmark**

(54) Benævnelse: **FREMGANGSMÅDER OG APPARATER TIL SIGNALERING AF INTRAPRÆDIKTION AF STORE BLOKKE TIL VIDEOKODERE OG -AFKODERE**

(56) Fremdragne publikationer:
WO-A2-2008/027192
WO-A2-2010/039731
US-A1- 2008 123 977
S-C LIM ET AL: "Intra coding using extended block size" 38. VCEG MEETING; 89. MPEG MEETING; 1-7-2009 - 8-7-2009; LONDON, GENEVA; (VIDEO CODING EXPERTS GROUP OF ITU-T SG.16),, 29 June 2009 (2009-06-29), XP030003709
WIEN M: "Variable block-size transforms for H.264/AVC" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS FOR VIDEO TECHNOLOGY, IEEE SERVICE CENTER, PISCATAWAY, NJ, US LNKD-DOI:10.1109/TCSVT.2003.815380, vol. 13, no. 7, 1 July 2003 (2003-07-01), pages 604-613, XP011099253 ISSN: 1051-8215
KIM J ET AL: "Enlarging MB size for high fidelity video coding beyond HD" 36. VCEG MEETING; 8-10-2008 - 10-

Fortsættes ...

10-2008; SAN DIEGO, US; (VIDEO CODING EXPERTS GROUP OF ITU-T SG.16),, 5 October 2008 (2008-10-05), XP030003643
Anonymous: "ITU-T Video Coding Experts Group (VCEG) - Yahoo Groups", , 1 July 2009 (2009-07-01), XP055180483, Retrieved from the Internet: URL:https://groups.yahoo.com/neo/groups/vc eg-experts/conversations/messages/511 [retrieved on 2015-03-31]

DESCRIPTION

TECHNICAL FIELD

[0001] The present principles relate generally to video encoding and decoding and, more particularly, to methods and apparatus for signaling intra prediction for large blocks for video encoders and decoders.

BACKGROUND

[0002] Most modern video coding standards employ various coding modes to efficiently reduce the correlations in the spatial and temporal domains. For example, in the International Organization for Standardization/International Electrotechnical Commission (ISO/IEC) Moving Picture Experts Group-4 (MPEG-4) Part 10 Advanced Video Coding (AVC) standard/International Telecommunication Union, Telecommunication Sector (ITU-T) H.264 Recommendation (hereinafter the "MPEG-4 AVC Standard"), a picture can be intra or inter coded. In intra pictures, all macroblocks are coded in intra modes, thus exploiting spatial correlations within the picture. Intra modes can be classified into the following three types: INTRA4x4; INTRA8x8; and INTRA16x16. INTRA4x4 and INTRA8x8 support 9 intra prediction modes and INTRA16x16 supports 4 intra prediction modes.

[0003] INTRA4x4 and INTRA8x8 support the following 9 intra prediction modes: vertical; horizontal; DC; diagonal-down/left; diagonal-down/right; vertical-left; horizontal-down; vertical-right; and horizontal-up prediction. INTRA16x16 supports the following 4 intra prediction modes: vertical; horizontal; DC; and plane prediction. Turning to FIG. 1, INTRA4x4 and INTRA8x8 prediction modes are indicated generally by the reference numeral 100. In FIG. 1, the reference numeral 0 indicates a vertical prediction mode, the reference numeral 1 indicates a horizontal prediction mode, the reference numeral 3 indicates a diagonal-down/left prediction mode, the reference numeral 4 indicates a diagonal-down/right prediction mode, the reference numeral 5 indicates a vertical-right prediction mode, the reference numeral 6 indicates a horizontal-down prediction mode, the reference numeral 7 indicates a vertical-left prediction mode, and the reference numeral 8 indicates a horizontal-up prediction mode. DC mode, which is part of the INTRA4x4 and INTRA8x8 prediction modes, is not shown. Turning to FIG. 2, INTRA16x16 prediction modes are indicated generally by the reference numeral 200. In FIG. 2, the reference numeral 0 indicates a vertical prediction mode, the reference numeral 1 indicates a horizontal prediction mode, and the reference numeral 3 indicates a plane prediction mode. DC mode, which is part of the INTRA16x16 prediction modes, is not shown.

[0004] INTRA4x4 uses a 4x4 discrete cosine transform (DCT). INTRA8x8 uses 8x8 transforms. INTRA16x16 uses cascaded 4x4 transforms. For the signaling, INTRA4x4 and INTRA8x8 share the same macroblock type (mb_type) 0 and are differentiated by a transform size flag (transform_8x8_size_flag). Then the choice of intra prediction mode in INTRA4x4 or INTRA8x8 is signaled by the most probable mode possibly with a remaining mode if necessary. For INTRA16x16, all the intra prediction modes along with a coded block pattern (cbp) type are signaled in mb_type, which uses an mb_type value from 1 to 24. TABLE 1 shows the detailed signaling for macroblock types for Intra coded slices (I slices). If a larger block size than 16x16 is used for intra prediction, then several possible issues are faced, as follows.

1. (1) If INTRA32x32 or INTRA64x64 prediction are added, by simply extending the mb_type in the MPEG-4 AVC Standard, it will cause too much overhead for those two new modes and, in addition, will not allow a hierarchical type of intra prediction. An example of a hierarchical type of intra prediction is explained as follows. If a 32x32 block is used as a large block and we allow sub-partitions to be 16x16 then, for each 16x16 sub-partition, INTRA4x4, INTRA8x8, INTRA16x16 should be allowed.
2. (2) If a larger transform (such as a 16x16 transform) instead of a cascaded transform is used for INTRA16x16, then the current signaling cannot be applied.
3. (3) We should give different priority for intra prediction modes inside one intra partition type.

TABLE 1

mb_type	Name of mb_type	transform_size_8x8_flag	MbPartPredMode (mb_type, 0)	Intra16x16-PredMode	CodedBlock-PatternChroma	CodedBlock-PatternLuma
0	I_NxN	0	Intra_4x4	na	Equation 7-33	Equation 7-33
0	I_NxN	1	Intra_8x8	na	Equation 7-33	Equation 7-33
1	I_16x16_0_0_0	na	Intra_16x16	0	0	0
2	I_16x16_1_0_0	na	Intra_16x16	1	0	0
3	I_16x16_2_0_0	na	Intra_16x16	2	0	0
4	I_16x16_3_0_0	na	Intra_16x16	3	0	0
5	I_16x16_0_1_0	na	Intra_16x16	0	1	0
6	I_16x16_1_1_0	na	Intra_16x16	1	1	0
7	I_16x16_2_1_0	na	Intra_16x16	2	1	0
8	I_16x16_3_1_0	na	Intra_16x16	3	1	0
9	I_16x16_0_2_0	na	Intra_16x16	0	2	0
10	I_16x16_1_2_0	na	Intra_16x16	1	2	0
11	I_16x16_2_2_0	na	Intra_16x16	2	2	0
12	I_16x16_3_2_0	na	Intra_16x16	3	2	0
13	I_16x16_0_0_1	na	Intra_16x16	0	0	15
14	I_16x16_1_0_1	na	Intra_16x16	1	0	15
15	I_16x16_2_0_1	na	Intra_16x16	2	0	15
16	I_16x16_3_0_1	na	Intra_16x16	3	0	15
17	I_16x16_0_1_1	na	Intra_16x16	0	1	15
18	I_16x16_1_1_1	na	Intra_16x16	1	1	15
19	I_16x16_2_1_1	na	Intra_16x16	2	1	15
20	I_16x16_3_1_1	na	Intra_16x16	3	1	15
21	I_16x16_0_2_1	na	Intra_16x16	0	2	15
22	I_16x16_1_2_1	na	Intra_16x16	1	2	15
23	I_16x16_2_2_1	na	Intra_16x16	2	2	15
24	I_16x16_3_2_1	na	Intra_16x16	3	2	15
25	I_PCM	na	na	na	na	na

[0005] Some prior art approaches exist relating to signaling large motion (inter) partitions in extensions of the MPEG-4 AVC Standard. One example of how large motion (Inter) partitions are signaled in extensions of the MPEG-4 AVC Standard is described with respect to a first prior art approach. The first prior art approach describes how signaling is done for 32x32 blocks or 64x64 blocks using a hierarchical coding structure.

[0006] Moreover, in addition to the existing motion partition sizes (16x16, 16x8, 8x16, 8x8, 8x4, 4x8 and 4x4) in the MPEG-4 AVC Standard, inter coding has also been proposed for an extension of the MPEG-4 AVC Standard using 32x32, 32x16, and 16x32 partitions. Turning to FIG. 3, motion partitions for use in 32x32 blocks are indicated generally by the reference numeral 300. The partitions include 32x32, 32x16, 16x32, and 16x16. 16x16 partitions can be further partitioned into partitions of sizes 16x16, 16x8, 8x16, and 8x8. Moreover, 8x8 partitions can be further partitioned into partitions of sizes 8x8, 8x4, 4x8, and 4x4.

[0007] For each 32x32 block, SKIP mode or DIRECT mode is signaled using an mb32_skip_flag in a way similar to that performed for other modes of the MPEG-4 AVC Standard. In addition, the original mb_type for an MxN (M=8, or 16 and N =8, or 16) partition in the MPEG-4 AVC Standard is also used to signal a 2Mx2N partition in a 32x32 block. If the mb32_type of a 32x32 indicates that a 16x16 partition is used, then the four 16x16 blocks are signaled in raster scan order by using the same syntax elements as macroblock_layer() in the MPEG-4 AVC Standard. Each 16x16 block may be partitioned further in the quadtree manner, from size 16x16 down to size 4x4.

[0008] For macroblock size 64x64, the following partitions are added above the partitions used in 32x32 blocks: 64x64; 64x32; and 32x64. Thus, one more hierarchical layer is added in the macroblock partition above block size 32x32. The original mb_type for an MxN (M =8, or 16 and N =8, or 16) macroblock partition in the MPEG-4 AVC Standard is used to signal a 4Mx4N macroblock partition in 64x64 macroblocks. If a 32x32 macroblock partition is used for a 64x64 block, then each 32x32 block will be handled in the same manner as described above.

[0009] However, the existing literature does not address how large intra mode is signaled, where large intra mode is defined to mean intra prediction involving partition blocks having a size equal to or larger than 32x32.

[0010] Document US 2008/123977 A1 discloses an image encoder including a predicted-image generating unit that generates a predicted image in accordance with a plurality of prediction modes. In tabulated rules of a predicted value setting conventional rules of intra prediction modes are not complied with and a better predicted value is judged from continuity of an image pattern.

[0011] Furthermore, the article Kim J. et al.: "Enlarging MB size for high fidelity vido coding beyond HD", 36. VCEG Meeting; 8-10-2008 - 10-10-2008; San Diego, US; (Video Coding Experts Group Of ITU-T SG. 16), October 5, 2008 (2008-10-05), XP030003643 discloses a method comprising encoding picture data for at least a large block in a picture by signaling prediction for the at least a large block, wherein the prediction is signaled by selecting a basic coding unit size and assigning a single partition type for the basic coding unit size, the single partition type being selected from among a plurality of spatial intra partition types. The extended architecture with the enlarged MB structure are first proposed for ME&MC but new designs of transform kernels, intra prediction, luma/chroma DC transforms, CABAC context models and de-blocking filters for the enlarged MB are not yet addressed.

SUMMARY

[0012] These and other drawbacks and disadvantages of the prior art are addressed by the present principles, which are directed to methods and apparatus for signaling intra prediction for large blocks for video encoders and decoders.

[0013] According to an aspect of the present principles, a method is provided as defined in claim 1.

[0014] These and other aspects, features and advantages of the present principles will become apparent from the following detailed description of exemplary embodiments, which is to be read in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The present principles may be better understood in accordance with the following exemplary figures, in which:

FIG. 1 is a diagram showing INTRA4x4 and INTRA8x8 prediction modes to which the present principles may be applied;

FIG. 2 is a diagram showing INTRA16x16 prediction modes to which the present principles may be applied;

FIG. 3 is a diagram showing motion partitions for use in 32x32 blocks to which the present principles may be applied;

FIG. 4 is a block diagram for an exemplary video encoder to which the present principles may be applied in accordance with an embodiment of the present principles;

FIG. 5 is a block diagram for an exemplary video decoder to which the present principles may be applied in accordance with an embodiment of the present principles;

FIG. 6 is a block diagram for exemplary hierarchical partitions to which the present principles may be applied in accordance with an embodiment of the present principles;

FIGS. 7A and 7B represent a flow diagram for an exemplary method for encoding picture data for large blocks by signaling intra prediction for the large blocks in accordance with an embodiment of the present principles; and

FIGS. 8A and 8B represent a flow diagram showing an exemplary method for decoding picture data for large blocks by determining that intra prediction is to be applied to the large blocks in accordance with an embodiment of the present principles.

DETAILED DESCRIPTION

[0016] The present principles are directed to methods and apparatus for signaling intra prediction for large blocks for video encoders and decoders.

[0017] The present description illustrates the present principles. It will thus be appreciated that those skilled in the art will be able to devise various arrangements that, although not explicitly described or shown herein, embody the present principles and are included within its spirit and scope.

[0018] All examples and conditional language recited herein are intended for pedagogical purposes to aid the reader in understanding the present principles and the concepts contributed by the inventor(s) to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions.

[0019] Moreover, all statements herein reciting principles, aspects, and embodiments of the present principles, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents as well as equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

[0020] Thus, for example, it will be appreciated by those skilled in the art that the block diagrams presented herein represent conceptual views of illustrative circuitry embodying the present principles. Similarly, it will be appreciated that any flow charts, flow diagrams, state transition diagrams, pseudocode, and the like represent various processes which may be substantially represented in computer readable media and so executed by a computer or processor, whether or not such computer or processor is explicitly shown.

[0021] The functions of the various elements shown in the figures may be provided through the use of dedicated hardware as well as hardware capable of executing software in association with appropriate software. When provided by a processor, the functions may be provided by a single dedicated processor, by a single shared processor, or by a plurality of individual processors, some of which may be shared. Moreover, explicit use of the term "processor" or "controller" should not be construed to refer exclusively to hardware capable of executing software, and may implicitly include, without limitation, digital signal processor ("DSP") hardware, read-only memory ("ROM") for storing software, random access memory ("RAM"), and non-volatile storage.

[0022] Other hardware, conventional and/or custom, may also be included. Similarly, any switches shown in the figures are conceptual only. Their function may be carried out through the operation of program logic, through dedicated logic, through the interaction of program control and dedicated logic, or even manually, the particular technique being selectable by the implementer as more specifically understood from the context.

[0023] In the claims hereof, any element expressed as a means for performing a specified function is intended to encompass any way of performing that function including, for example, a) a combination of circuit elements that performs that function or b) software in any form, including, therefore, firmware, microcode or the like, combined with appropriate circuitry for executing that software to perform the function. The present principles as defined by such claims reside in the fact that the functionalities provided by the various recited means are combined and brought together in the manner which the claims call for. It is thus regarded that any means that can provide those functionalities are equivalent to those shown herein.

[0024] Reference in the specification to "one embodiment" or "an embodiment" of the present principles, as well as other variations thereof, means that a particular feature, structure, characteristic, and so forth described in connection with the embodiment is included in at least one embodiment of the present principles. Thus, the appearances of the phrase "in one embodiment" or "in an embodiment", as well any other variations, appearing in various places throughout the specification are not necessarily all referring to the same embodiment.

[0025] It is to be appreciated that the use of any of the following "/", "and/or", and "at least one of", for example, in the cases of "A/B", "A and/or B" and "at least one of A and B", is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of both options (A and B). As a further example, in the cases of "A, B, and/or C" and "at least one of A, B, and C", such phrasing is intended to encompass the selection of the first listed option (A) only, or the selection of the second listed option (B) only, or the selection of the third listed option (C) only, or the selection of the first and the second listed options (A and B) only, or the selection of the first and third listed options (A and C) only, or the selection of the second and third listed options (B and C) only, or the selection of all three options (A and B and C). This may be extended, as readily apparent by one of ordinary skill in this and related arts, for as many items listed.

[0026] Moreover, it is to be appreciated that while one or more embodiments of the present principles are described herein with respect to an extension of the MPEG-4 AVC standard, the present principles are not limited to solely this extension and/or this standard and, thus, may be utilized with respect to other video coding standards, recommendations, and extensions thereof, while maintaining the spirit of the present principles.

[0027] As used herein, "high level syntax" refers to syntax present in the bitstream that resides hierarchically above the macroblock layer. For example, high level syntax, as used herein, may refer to, but is not limited to, syntax at the slice header level, Supplemental Enhancement Information (SEI) level, Picture Parameter Set (PPS) level, Sequence Parameter Set (SPS) level and Network Abstraction Layer (NAL) unit header level.

[0028] Also, as used herein, the words "picture" and "image" are used interchangeably and refer to a still image or a picture from a video sequence. As is known, a picture may be a frame or a field.

[0029] Additionally, as used herein, the word "signal" refers to indicating something to a corresponding decoder. For example, the encoder may signal that intra prediction is designated to be used for a particular large block (as defined herein) in order to make the decoder aware of which particular prediction type (e.g., intra or inter) was used on the encoder side. In this way, the same prediction type may be used at both the encoder side and the decoder side. Thus, for example, an encoder may transmit an indication (i.e., signal) for a particular large block that intra prediction is to be performed on that large block to simply allow the decoder to know and select the same prediction type for that large block. It is to be appreciated that signaling may be accomplished in a variety of ways. For example, one or more syntax elements, flags, and so forth may be used to signal information to a corresponding decoder.

[0030] Turning to FIG. 4, an exemplary video encoder to which the present principles may be applied in accordance with an embodiment of the present principles is indicated generally by the reference numeral 400.

[0031] The video encoder 400 includes a frame ordering buffer 410 having an output in signal communication with a non-inverting input of a combiner 485. An output of the combiner 485 is connected in signal communication with a first input of a transformer and quantizer 425. An output of the transformer and quantizer 425 is connected in signal communication with a first input of an entropy coder 445 and a first input of an inverse transformer and inverse quantizer 450. An output of the entropy coder 445 is connected in signal communication with a first non-inverting input of a combiner 490. An output of the combiner 490 is connected in signal communication with a first input of an output buffer 435.

[0032] A first output of an encoder controller 405 is connected in signal communication with a second input of the frame ordering buffer 410, a second input of the inverse transformer and inverse quantizer 450, an input of a picture-type decision module 415, an input of a macroblock-type (MB-type) decision module 420, a second input of a super intra prediction module 460, a second input of a deblocking filter 465, a first input of a motion compensator 470, a first input of a motion estimator 475, and a second input of a reference picture buffer 480.

[0033] A second output of the encoder controller 405 is connected in signal communication with a first input of a Supplemental Enhancement Information (SEI) inserter 430, a second input of the transformer and quantizer 425, a second input of the entropy coder 445, a second input of the output buffer 435, and an input of the Sequence Parameter Set (SPS) and Picture Parameter Set (PPS) inserter 440.

[0034] A first output of the picture-type decision module 415 is connected in signal communication with a third input of a frame ordering buffer 410. A second output of the picture-type decision module 415 is connected in signal communication with a second input of a macroblock-type decision module 420.

[0035] An output of the Sequence Parameter Set (SPS) and Picture Parameter Set (PPS) inserter 440 is connected in signal communication with a third non-inverting input of the combiner 490.

[0036] An output of the inverse quantizer and inverse transformer 450 is connected in signal communication with a first non-inverting input of a combiner 419. An output of the combiner 419 is connected in signal communication with a first input of the super intra prediction module 460 and a first input of the deblocking filter 465. An output of the deblocking filter 465 is connected in signal communication with a first input of a reference picture buffer 480. An output of the reference picture buffer 480 is connected in signal communication with a second input of the motion estimator 475. A first output of the motion estimator 475 is connected in signal communication with a second input of the motion compensator 470. A second output of the motion estimator 475 is connected in signal communication with a third input of the entropy coder 445.

[0037] An output of the motion compensator 470 is connected in signal communication with a first input of a switch 497. An output of the super intra prediction module 460 is connected in signal communication with a second input of the switch 497. An output of the macroblock-type decision module 420 is connected in signal communication with a third input of the switch 497. The third input of the switch 497 determines whether or not the "data" input of the switch (as compared to the control input, i.e., the third input) is to be provided by the motion compensator 470 or the super intra prediction module 460. The output of the switch 497 is connected in signal communication with a second non-inverting input of the combiner 419 and with an inverting input of the combiner 485.

[0038] Inputs of the frame ordering buffer 410 and the encoder controller 405 are available as input of the encoder 400, for receiving an input picture 401. Moreover, an input of the Supplemental Enhancement Information (SEI) inserter 430 is available as an input of the encoder 400, for receiving metadata. An output of the output buffer 435 is available as an output of the encoder 400, for outputting a bitstream.

[0039] Turning to FIG. 5, an exemplary video decoder to which the present principles may be applied in accordance with an embodiment of the present principles is indicated generally by the reference numeral 500.

[0040] The video decoder 500 includes an input buffer 510 having an output connected in signal communication with a first input of the entropy decoder 545. A first output of the entropy decoder 545 is connected in signal communication with a first input of an inverse transformer and inverse quantizer 550. An output of the inverse transformer and inverse quantizer 550 is connected in signal communication with a second non-inverting input of a combiner 525. An output of the combiner 525 is connected in signal communication with a second input of a deblocking filter 565 and a first input of a super intra prediction module 560. A second output of the deblocking filter 565 is connected in signal communication with a first input of a reference picture buffer 580. An output of the reference picture buffer 580 is connected in signal communication with a second input of a motion compensator 570.

[0041] A second output of the entropy decoder 545 is connected in signal communication with a third input of the motion compensator 570 and a first input of the deblocking filter 565. A third output of the entropy decoder 545 is connected in signal communication with an input of a decoder controller 505. A first output of the decoder controller 505 is connected in signal communication with a second input of the entropy decoder 545. A second output of the decoder controller 505 is connected in signal communication with a second input of the inverse transformer and inverse quantizer 550. A third output of the decoder controller 505 is connected in signal communication with a third input of the deblocking filter 565. A fourth output of the decoder controller 505 is connected in signal communication with a second input of the super intra prediction module 560, with a first input of the motion compensator 570, and with a second input of the reference picture buffer 580.

[0042] An output of the motion compensator 570 is connected in signal communication with a first input of a switch 597. An output of the super intra prediction module 560 is connected in signal communication with a second input of the switch 597. An output of the switch 597 is connected in signal communication with a first non-inverting input of the combiner 525.

[0043] An input of the input buffer 510 is available as an input of the decoder 500, for receiving an input bitstream. A first output of the deblocking filter 565 is available as an output of the decoder 500, for outputting an output picture.

[0044] As noted above, the present principles are directed to methods and apparatus for signaling intra prediction for large blocks for video encoders and decoders. Moreover, as noted above, large blocks, to which the present principles may be applied, are defined to means blocks having a size equal to or larger than 32x32.

[0045] In an embodiment, for ease of notation, we split the signaling of intra prediction into the following two parts: sip_type (spatial intra partition type, which can be INTRA4x4, INTRA8x8, INTRA16x16, and so forth); and intra_pred_mode (such as, e.g., the 9 Intra Prediction Modes within INTRA4x4 and INTRA8x8) within each sip_type. In further detail with respect to a particular embodiment, we propose the following three rules for the present principles: (1) select a basic coding unit; (2) allow hierarchical layer intra prediction by either splitting from a largest intra prediction type or merging from the basic coding unit; and (3) for each sip_type, assign a higher priority to the intra_pred_mode which is most frequently used. With respect to Rule (1), we allow several sip_types for the basic coding unit.

An Embodiment

[0046] In an embodiment, we set the basic coding unit to be 16x16. In this coding unit, we allow sip_type to be INTRA4x4, INTRA8x8 and INTRA16x16. We also allow hierarchical layer intra prediction as shown in FIG. 6.

[0047] Turning to FIG. 6, exemplary hierarchical partitions to which the present principles may be applied are indicated generally by the reference numeral 600. In this embodiment, if the largest block size is set to 64x64, then we use "split signaling" to allow hierarchical layer intra prediction. That is, in an embodiment, we add intra64_flag. If intra64_flag is equal to 1, then INTRA64x64 is used. Otherwise, if intra64_flag is equal to 0, then we split a 64x64 block 611 into four 32x32 blocks 621. For each of the 32x32 blocks 621, we add intra32_flag. If intra32_flag is equal to 1, then INTRA32x32 is used. Otherwise, if intra32_flag is equal to 0, then all sip types allowed in the 16x16 basic coding unit are allowed here (i.e., for the 32x32 blocks 621) as well. For intra_pred_mode in INTRA16x16, we have DC mode and the directional modes, the latter allowing different types of directional predictions by sending the mode information. Thus, a 32x32 intra prediction block 621 may be further split into 4 16x16 intra prediction blocks 631. One or more of the 4 16x16 intra prediction blocks 631 may be further split to DC mode (not shown), a 16x16 mode 641, an 8x8 mode 651, and a 4x4 mode 661. In this embodiment, we presume having the following four 16x16 intra prediction modes: DC; horizontal (HOR); vertical (VER); and multi-directional (Multi-DIR). The intra_pred_mode is signaled by considering the priority of each mode. In INTRA16x16, since the DC mode is used more often than other modes, we add INTRA16x16_DC in the sip_type table before INTRA16x16. Then we remove the most_probable_mode indication in intra_pred_mode for INTRA16x16. Instead, the other 3 modes (16x16, 8x8, and 4x4) are absolutely indicated.

Syntax

[0048] We illustrate an example of syntax for this embodiment in TABLE 2 and TABLE 3. In particular, TABLE 2 shows an exemplary specification of sip types for a 16x16 coding unit in accordance with an embodiment of the present principles, and TABLE 3 shows exemplary INTRA16x16 prediction modes in accordance with an embodiment of the present principles. For INTRA32x32/INTRA64x64, the same modes as INTRA16x16 are used. For signaling, we replace the most_probable_mode indication with intra32_DC_flag and intra64_DC flag since DC is mostly used. Then we absolutely code other intra_pred_mode.

[0049] intra_pred_mode signaling for INTRA4x4 and INTRA8x8 may be performed exactly the same as in the MPEG-4 AVC Standard, so we will not list these modes in any of the tables.

TABLE 2

Sip_type	Index	Binarization bits
SIP8x8	0	0
SIP16x16DC	1	10
SIP16x16	2	110
SIP4x4	3	1110

TABLE 3

Intra Prediction Mode	Index	Binarization bits
VER	0	0
HOR	1	10
Multi-DIR	2	11

[0050] TABLE 4 shows exemplary macroblock layer syntax, in accordance with an embodiment of the present principles.

TABLE 4

macroblock_layer( ) {	**C**	**Descriptor**
...		
intra64_flag	2	u(1)
if (intra64_flag==1) {		
intra64_DC_flag	2	u(1)
if (intra64_DC_flag==0) {		
intra_pred_mode_64	2	ue(v)/se(v)
if (intra_pred_mode_64==Multi-DIR) {		
intra64_multidir_index	2	ue(v)/se(v)
}		
}		
}		
else {		
for (i32=0; i32<4; i32++) {		
intra32_flag[i32]	2	u(1)
if (intra32_flag[i32]==1) {		
intra32_DC_flag[i32]	2	u(1)
if (intra32_DC_flag[i32]==0) {		
intra_pred_mode_32[i32]	2	ue(v)/se(v)
if (intra_pred_mode_32[i32]==Multi-DIR) {		
intra32_multidir_index[i32]	2	ue(v)/se(v)
}		
}		

}		
else {		
for (i16=0; i16<4; i16++) {		
sip_type[i16]	2	ue(v)/se(v)
if (sip_type[i16]==SIP16x16) {		
intra_pred_mode_16[i16]	2	ue(v)/se(v)
if (intra_pred_mode_16[i16]==Multi-DIR) {		
intra16_multidir_index[i16]	2	ue(v)/se(v)
}		
}		
else if (sip_type[i16]!=SIP16x16_DC) {		
mb_intra_prediction_syntax(); /*this is same as H.264*/		
}		
}		
}		
...		
}		

[0051] The semantics of some of the syntax elements of TABLE 4 are as follows:

Intra64_flag equal to 1 specifies that INTRA64x64 is used. Intra64_flag equal to 0 specifies that a 64x64 large block is further split into 32x32 partitions.

Intra64_DC_flag equal to 1 specifies that the intra_pred_mode is DC mode for INTRA64x64. Intra64_DC_flag equal to 0 specifies that the intra_pred_mode is not DC mode for INTRA64x64.

intra_pred_mode_64 specifies intra prediction mode (not including DC mode) for INTRA64x64.

intra64_multidir_index specifies the index of the angle for Multi_Dir mode in INTRA64x64.

Intra32_flag [i] equal to 1 specifies that INTRA32x32 is used for the ith 32x32 large block. Intra32_flag [i] equal to 0 specifies that the ith 32x32 large block is further split into 16x16 partitions.

intra32_DC_flag [i] equal to 1 specifies that the intra_pred_mode is DC mode for INTRA32x32 for the ith 32x32 block. intra32_DC_flag[i] equal to 0 specifies that the intra_pred_mode is not DC mode for INTRA32x32 for the ith 32x32 block.

intra_pred_mode_32 [i] specifies the intra prediction mode (not including DC mode) for INTRA32x32 for the ith 32x32 large block.

intra32_multidir_index specifies the index of the angle for Multi_Dir mode in INTRA32x32.

sip_type [i] specifies the spatial intra partition type for the basic block coding unit in the ith 16x16 block.

intra_pred_mode_16 [i] specifies the intra prediction mode (not including DC mode) for INTRA16x16 for the ith 16x16 block.

Intra16_multidir_index specifies the index of the angle for Multi_Dir mode in INTRA16x16 for the ith 16x16 block.

Another Embodiment

[0052] In another embodiment, we adaptively select the large block unit to be 32x32 or 64x64. The selection may be signaled using one or more high level syntax elements. In an embodiment, if 32x32 is selected, then we just remove all the syntax related to 64x64.

[0053] In another embodiment, hierarchical intra layer prediction can involve merging from basic coding unit. For example, if the largest block unit is 64x64 and the basic coding unit is 16x16, then we use one flag (is_all_16x16_coding) to indicate if all of the 16x16 blocks inside one 64x64 block are of the 16x16 coding type. If is_all_16x16_coding is equal to 1, then this indicates that 16x16 coding type is used and we stop signaling. Otherwise, we use one flag (is_all_32x32_coding) to indicate if all of the 32x32 blocks inside one 64x64 block are of the 32x32 coding type. If is_all_32x32_coding is equal to 1, then this indicates that all of the 32x32 blocks inside one 64x64 block are of the 32x32 coding type. Otherwise, if is_all_32x32_coding and is_all_16x16_coding are equal to 0, then this indicates that INTRA64x64 is used.

[0054] In another embodiment, we introduce a SIP type for a block unit (large_sip_type) having a size not less than 16x16. The three types are referred to as follows: large_intra_16x16; large_intra_32x32; and large_intra_64x64. large_intra_16x16 means that all 16x16 blocks inside one large block are of the 16x16 coding type. large_intra_32x32 means that all 32x32 blocks inside one large block are of the 32x32 coding type. In an embodiment, large_intra_32x32 can be combined with the embodiment described above with intra32_flag to allow hierarchical intra prediction. large_intra_64x64 means that all 64x64 blocks inside one large block are coded as INTRA64x64.

[0055] In another embodiment, we can introduce several sip/mode tables. The tables can be pre-stored at both an encoder and a decoder, or the tables can be user specified and transmitted using one or more high level syntax elements. TABLE 5 shows exemplary macroblock layer syntax, in accordance with an embodiment of the present principles.

TABLE 5

macroblock_layer( ) {	**C**	**Descriptor**
...		
is_all_16x16_coding	2	u(1)
if (is_all_16x16_coding == 0) {		
is_all_32x32_coding	2	u(1)
if (is_all_32x32_coding == 0) {		
decode_with_64x64_coding_type()		
}		
else{		
decode_with_32x32_coding_type()		
}		
}		
else {		
decode_with_16x16_coding_type()		
}		
...		
}		

[0056] The semantics of the some of the syntax elements of TABLE 5 are as follows:

is_all_16x16_coding equal to 1 specifies that all 16x16 blocks inside a large block are coded by a 16x16 coding type. is_all_16x16_coding equal to 0 specifies that the large block is not coded by a 16x16 coding type.

is_all_32x32_coding equal to 1 specifies that all 32x32 blocks inside a large block are coded by a 32x32 coding type. is_all_32x32_coding equal to 0 specifies that the large block is not coded by a 32x32 coding type.

[0057] Turning to FIGS. 7A and 7B, which together represent an exemplary method for encoding picture data for large blocks by signaling intra prediction for the large blocks, indicated generally by the reference numeral 700. The method 700 includes a start block 705 that passes control to a function block 710. The function block 710 performs an initialization, and passes control to a loop limit block 715. The loop limit block 715 performs a loop (hereinafter also loop 1) over 64x64 blocks (i.e., blocks having a block size of 64x64), and passes control to a function block 785 and a loop limit block 720.

[0058] The function block 785 performs an Intra 64x64 mode decision, sets Intra64_DC flag based on RD64 (i.e., the rate distortion resulting from the Intra 64x64 mode decision), and passes control to a decision block 770.

[0059] The loop limit block 720 performs a loop (hereinafter also loop 2) over four 32x32 blocks (i.e., the four blocks having a block size of 32x32 and obtained from the current 64x64 block being processed by loop 1), and passes control to a function block 790 and a loop limit block 725.

[0060] The function block 790 performs an Intra 32x32 mode decision, sets Intra32_DC flag based on RD32 (i.e., the rate distortion resulting from the Intra 32x32 mode decision), and passes control to a decision block 750.

[0061] The loop limit block 725 performs a loop (hereinafter also loop 3) over four 16x16 blocks (i.e., the four blocks having a block size of 16x16 and obtained from the current 32x32 block being processed by loop 2), and passes control to a function block 730 and a function block 735.

[0062] The function block 730 evaluates Intra16x16_DC mode, and passes control to a function block 740. The function block 735 evaluates other 16x16 modes (i.e., other than Intra16x16_DC) and below (e.g., 8x8, 4x4, etc.), and passes control to the function block 740.

[0063] The function block 740 performs a 16x16 mode decision based on RD16 (i.e., the rate distortion resulting from the intra 16x16 mode decision), then accumulates the RD16 of each 16x16 block to obtain TotRD16 (which indicates the total rate distortion of the whole 32x32 block when coded by four 16x16 blocks), and passes control to a loop limit block 745. The loop limit block 745 ends the loop (i.e., loop 3) over the 16x16 blocks, and passes control to the decision block 750.

[0064] The decision block 750 determines whether or not RD32 < TotRD16 (i.e., whether the rate distortion cost for a current 32x32 block is less than the total rate distortion cost for the four 16x16 blocks obtained from the current 32x32 block). If so, then control is passed to a function block 755. Otherwise, control is passed to a function block 742.

[0065] The function block 755 sets Intra32_flag equal to one, and passes control to a function block 760. The function block 742 sets Intra32_flag equal to zero, and passes control to the function block 760.

[0066] The function block 760 sets an accumulation of the RD32 of each 32x32 block to TotRD32 to indicate the total rate distortion of the whole 64x64 block when coded by four 32x32 blocks, and passes control to a loop limit block 765. The loop limit block 765 ends the loop (i.e., loop 2) over the 32x32 blocks, and passes control to a decision block 770.

[0067] The decision block 770 determines whether or not RD64 < TotRD32 (i.e., whether the rate distortion cost for a current 64x64 block is less than the total rate distortion cost for the four 32x32 blocks obtained from the current 64x64 block). If so, then control is passed to a function block 775. Otherwise, control is passed to a function block 780.

[0068] The function block 775 sets Intra64_flag equal to one, and passes control to a loop limit block 795. The function block 780 sets Intra64_flag equal to zero, and passes control to the function block 795.

[0069] The function block 795 ends the loop (i.e., loop 1) over the 64x64 blocks, and passes control to a function block 797. The function block 797 entropy codes flags, intra_pred_mode, and a residue, and passes control to an end block 799.

[0070] Turning to FIGS. 8A and 8B, which together represent an exemplary method for decoding picture data for large blocks by determining that intra prediction is to be applied to the large blocks, indicated generally by the reference numeral 800. The method 800 includes a start block 805 that passes control to a function block 808. The function block 808 initializes the decoder and then passes the control to a function block 810. The function block 810 parses the bitstream, and passes control to a loop limit block 815. The loop limit block 815 performs a loop (hereinafter loop 1) over 64x64 blocks, and passes control to a decision block 820. The decision block 820 determines whether or not Intra64_flag is set equal to one. If so, then control is passed to a function block 885. Otherwise, control is passed to a loop limit block 825.

[0071] The function block 885 determines whether or not intra64_DC_flag is set equal to one. If so, then control is passed to a function block 887. Otherwise, control is passed to a function block 888. The function block 887 performs intra 64x64 DC prediction, and then passes control to a function block 890. The function block 888 performs intra 64x64 predictions other than intra 64x64 DC mode and then passes control to a function block 890. The function block 890 decodes a current 64x64 block, and passes control to a loop limit block 880. The loop limit block 880 ends the loop (i.e., loop 1) over the 64x64 blocks, and passes control to an end block 899.

[0072] The loop limit block 825 performs a loop (hereinafter loop 2) over four 32x32 blocks, and passes control to a decision block 830. The decision block 830 determines whether or not Intra32_flag is equal to one. If so, then control is passed to a function block 835. Otherwise, control is passed to a loop limit block 845.

[0073] The function block 835 determines whether or not Intra32_DC_flag is equal to one. If so, then control is passed to a function block 837. Otherwise, control is passed to a function block 838. The function block 837 performs an intra32x32 DC prediction, and passes control to a function block 840. The function block 838 performs an intra prediction other than intra 32x32 DC mode, and then passed the control to the function block 840. The function block 840 decodes a 32x32 block, and passes control to a loop limit block 875.

[0074] The loop limit block 875 ends the loop (i.e., loop 2) over the 32x32 blocks, and passes control to the loop limit block 880.

[0075] The loop limit block 845 performs a loop (hereinafter loop 3) over four 16x16 blocks, and passes control to a decision block 850. The decision block 850 determines whether or not sip_type = Intra16_DC. If so, then control is passed to a function block 855. Otherwise, control is passed to a function block 860.

[0076] The function block 855 performs Intra16x16_DC mode prediction, and passes control to a function block 865. The function block 860 performs mode prediction using other intra prediction modes (i.e., other than Intra16x16_DC mode), and passes control to the function block 865.

[0077] The function block 865 decodes a 16x16 block, and passes control to a loop limit block 870. The loop limit block 870 ends the loop (i.e., loop 3) over the 16x16 blocks, and passes control to the loop limit block 875.

[0078] A description will now be given of some of the many attendant advantages/features of the present invention, some of which have been mentioned above. For example, one advantage/feature is an apparatus having a video encoder for encoding picture data for at least one large block in a picture by signaling intra prediction for the at least one large block. The intra prediction is signaled by selecting a basic coding unit size and assigning a single spatial intra partition type for the basic coding unit size. The single spatial intra partition type is selectable from among a plurality of spatial intra partition types. The at least one large block has a large block size greater than a block size of the basic coding unit. The intra prediction is hierarchical layer intra prediction and is performed for the at least one large block by at least one of splitting from the large block size to the basic coding unit size and merging from the basic coding unit size to the large block size.

[0079] Another advantage/feature is the apparatus having the video encoder as described above, wherein for each of the plurality of spatial intra partition types, a higher priority is assigned to a particular intra prediction mode that is most frequently used from among a plurality of available intra prediction modes.

[0080] Yet another advantage/feature is the apparatus having the video encoder as described above, wherein the large block size is adaptively selected.

[0081] Still another advantage/feature is the apparatus having the video encoder as described above, wherein the signaling is performed using one or more high level syntax elements.

[0082] Moreover, another advantage/feature is the apparatus having the video encoder as described above, wherein at least one of a spatial intra partition type table and an intra prediction mode table is pre-stored and used by the video encoder to encode the at least one large block. The at least one of the spatial intra partition type table and the intra prediction mode table is arranged to be pre-stored and used by a corresponding video decoder to decode the at least one large block.

[0083] Further, another advantage/feature is the apparatus having the video encoder as described above, wherein at least one of a spatial intra partition type table and an intra prediction mode table, is used by the video encoder to encode the at least one large block, and is transmitted by the video encoder using one or more high level syntax elements.

[0084] These and other features and advantages of the present principles may be readily ascertained by one of ordinary skill in the pertinent art based on the teachings herein. It is to be understood that the teachings of the present principles may be implemented in various forms of hardware, software, firmware, special purpose processors, or combinations thereof.

[0085] Most preferably, the teachings of the present principles are implemented as a combination of hardware and software. Moreover, the software may be implemented as an application program tangibly embodied on a program storage unit. The application program may be uploaded to, and executed by, a machine comprising any suitable architecture. Preferably, the machine is implemented on a computer platform having hardware such as one or more central processing units ("CPU"), a random access memory ("RAM"), and input/output ("I/O") interfaces. The computer platform may also include an operating system and microinstruction code. The various processes and functions described herein may be either part of the microinstruction code or part of the application program, or any combination thereof, which may be executed by a CPU. In addition, various other peripheral units may be connected to the computer platform such as an additional data storage unit and a printing unit.

[0086] It is to be further understood that, because some of the constituent system components and methods depicted in the accompanying drawings are preferably implemented in software, the actual connections between the system components or the process function blocks may differ depending upon the manner in which the present principles are programmed. Given the teachings herein, one of ordinary skill in the pertinent art will be able to contemplate these and similar implementations or configurations of the present principles.

[0087] Although the illustrative embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the present principles is not limited to those precise embodiments, and that various changes and modifications may be effected therein by one of ordinary skill in the pertinent art without departing from the scope of the present principles. All such changes and modifications are intended to be included within the scope of the present principles as set forth in the appended claims.

REFERENCES CITED IN THE DESCRIPTION

cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US2008123977A1 [0010]

Non-patent literature cited in the description

- **KIM J. et al.**Enlarging MB size for high fidelity vido coding beyond HDVCEG Meeting, 2008, vol. 36, [0011]
- Video Coding Experts Group Of ITU-T SG., 2008, vol. 16, [0011]

Patentkrav

1. Afkodningsfremgangsmåde omfattende:

at afkode billeddata for mindst en stor blok i et billede ved at bestemme at intraprædiktion skal udføres for den mindst ene store blok (820, 830),

hvor den mindst ene store blok har en stor blok-størrelse større end en grundkodningsenhedsstørrelse, hvor stor blok-størrelsen er en af 32x32 og 64x64 og hvor grundkodningsenhedsstørrelsen er 16x16, hvor intraprædiktionen signaleres for den mindst ene store blok ved:

- at afkode et binært splitsignaleringssyntakselement, der specificerer hvorvidt den store blok yderligere splittes i fire lige store underblokke;

- at afkode en intraprædiktion-driftsform for nævnte store blok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok ikke splittes yderligere;

ellers i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok splittes yderligere:

- at afkode for hver underblok, i tilfældet hvor nævnte underblok er 32x32, et binært splitsignaleringssyntakselement, der specificerer hvorvidt 32x32-underblokken yderligere splittes i fire blokke af lige stor grundkodningsenhedsstørrelse og at afkode en intraprædiktion-driftsform for nævnte 32x32-underblok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at nævnte 32x32-underblok ikke splittes yderligere; og

- at afkode for hver underblok, i tilfældet hvor nævnte underblok er 16x16, en enkelt rumlig intrapartitionstype, hvor den enkelte rumlige intrapartitionstype kan bestemmes fra blandt en flerhed af rumlige intrapartitionstyper.

2. Fremgangsmåden ifølge krav 1, yderligere omfattende at afkode mindst et binært fletningssignaleringssyntakselement, der specificerer hvorvidt blokke med grundkodningsenhedsstørrelse flettes til en stor størrelse blok.

3. Fremgangsmåden ifølge krav 1, hvor mindst en af en rumlig intrapartitiontypetabel og en intraprædiktion-driftsformstabel forlagres og anvendes med afkodningsfremgangsmåden til at afkode den mindst ene store blok.

4. Fremgangsmåden ifølge krav 1, hvor mindst en af en rumlig intrapartitiontypetabel og en intraprædiktion-driftsformstabel modtages med nævnte afkodningsfremgangsmåde under anvendelse af et eller flere højniveau-syntakselementer og anvendes med afkodningsfremgangsmåden til at afkode den mindst ene store blok (810).

5. Kodningsfremgangsmåde omfattende:

at kode billeddata for mindst en stor blok i et billede ved at bestemme at intraprædiktion skal udføres for den mindst ene store blok (820, 830),

hvor den mindst ene store blok har en stor blok-størrelse større end en grundkodningsenhedsstørrelse, hvor stor blok-størrelsen er en af 32x32 og 64x64 og hvor grundkodningsenhedsstørrelsen er 16x16,

hvor intraprædiktionen signaleres for den mindst ene store blok ved:

- at kode et binært splitsignaleringssyntakselement, der specificerer hvorvidt den store blok yderligere splittes i fire lige store underblokke;

- at kode en intraprædiktion-driftsform for nævnte store blok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok ikke splittes yderligere;

ellers i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok splittes yderligere:

- at kode for hver underblok, i tilfældet hvor nævnte underblok er 32x32, et binært splitsignaleringssyntakselement, der specificerer hvorvidt nævnte 32x32-underblok yderligere splittes i fire blokke af lige stor grundkodningsenhedsstørrelse og at kode en intraprædiktion-driftsform for nævnte 32x32-underblok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at nævnte 32x32-underblok ikke splittes yderligere; og

- at kode for hver underblok, i tilfældet hvor nævnte underblok er 16x16, en enkelt rumlig intrapartitionstype, hvor den enkelte rumlige intrapartitionstype kan bestemmes fra blandt en flerhed af rumlige intrapartitionstyper.

6. Fremgangsmåden ifølge krav 5, yderligere omfattende at kode mindst et binært fletningssignaleringssyntakselement, der specificerer hvorvidt blokke med grundkodningsenhedsstørrelse flettes til en stor størrelse blok.

7. Fremgangsmåden ifølge krav 5, hvor mindst en af en rumlig intrapartitiontypetabel og en intraprædiktion-driftsformstabel forlagres og anvendes med kodningsfremgangsmåden til at kode den mindst ene store blok.

8. Fremgangsmåden ifølge krav 5, hvor mindst en af en rumlig intrapartitiontypetabel og en intraprædiktion-driftsformstabel kodes med nævnte kodningsfremgangsmåde under anvendelse af et eller flere højniveau-syntakselementer og anvendes med kodningsfremgangsmåden til at kode den mindst ene store blok (810).

9. Videoafkoder, omfattende:

organer til at afkode billeddata for mindst en stor blok i et billede ved at bestemme at intraprædiktion skal udføres for den mindst ene store blok (820, 830),

hvor den mindst ene store blok har en stor blok-størrelse større end en grundkodningsenhedsstørrelse, hvor stor blok-størrelsen er en af 32x32 og 64x64 og hvor grundkodningsenhedsstørrelsen er 16x16,

hvor intraprædiktionen signaleres for den mindst ene store blok med nævnte organer til afkodning konfigureret til:

- at afkode et binært splitsignaleringssyntakselement, der specificerer hvorvidt den store blok yderligere splittes i fire lige store underblokke;

- at afkode en intraprædiktion-driftsform for nævnte store blok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok ikke splittes yderligere;

ellers i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok splittes yderligere:

- at afkode for hver underblok, i tilfældet hvor nævnte underblok er 32x32, et binært splitsignaleringssyntakselement, der specificerer hvorvidt nævnte 32x32-underblok yderligere splittes i fire blokke af lige stor grundkodningsenhedsstørrelse og at afkode en intraprædiktion-driftsform for nævnte 32x32-underblok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at nævnte 32x32-underblok ikke splittes yderligere; og

- at afkode for hver underblok, i tilfældet hvor nævnte underblok er 16x16, en enkelt rumlig intrapartitionstype, hvor den enkelte rumlige intrapartitionstype kan bestemmes fra blandt en flerhed af rumlige intrapartitionstyper.

10. Videoafkoderen ifølge krav 9, hvor nævnte organer til at afkode er yderligere konfigureret til at afkode mindst et binært fletningssignaleringssyntakselement, der specificerer hvorvidt blokke med grundkodningsenhedsstørrelse flettes til en stor størrelse blok.

11. Videoafkoderen ifølge krav 9, hvor mindst en af en rumlig intrapartitiontypetabel og en intraprædiktion-driftsformstabel er forlagret og anvendt med videoafkoderen til at afkode den mindst ene store blok.

12. Videoafkoderen ifølge krav 9, hvor mindst en af en rumlig intrapartitiontypetabel og en intraprædiktion-driftsformstabel modtages med nævnte videoafkoder under anvendelse af et eller flere højniveau-syntakselementer og anvendes med videoafkoderen til at afkode den mindst ene store blok (810).

13. Videokoder, omfattende:

organer til at kode billeddata for mindst en stor blok i et billede ved at bestemme at intraprædiktion skal udføres for den mindst ene store blok (820, 830),

hvor den mindst ene store blok har en stor blok-størrelse større end en grundkodningsenhedsstørrelse, hvor stor blok-størrelsen er en af 32x32 og 64x64 og hvor grundkodningsenhedsstørrelsen er 16x16,

hvor intraprædiktionen signaleres for den mindst ene store blok med nævnte organer til kodning konfigureret til:

- at kode et binært splitsignaleringssyntakselement, der specificerer hvorvidt den store blok yderligere splittes i fire lige store underblokke;

- at kode en intraprædiktion-driftsform for nævnte store blok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok ikke splittes yderligere;

ellers i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok splittes yderligere:

- at kode for hver underblok, i tilfældet hvor nævnte underblok er 32x32, et binært splitsignaleringssyntakselement, der specificerer hvorvidt nævnte 32x32-underblok yderligere splittes i fire blokke af lige stor grundkodningsenhedsstørrelse og at kode en intraprædiktion-driftsform for nævnte 32x32-underblok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at nævnte 32x32-underblok ikke splittes yderligere; og

- at kode for hver underblok, i tilfældet hvor nævnte underblok er 16x16, en enkelt rumlig intrapartitionstype, hvor den enkelte rumlige intrapartitionstype kan bestemmes fra blandt en flerhed af rumlige intrapartitionstyper.

14. Videokoderen ifølge krav 13, hvor nævnte organer til at kode er yderligere konfigureret til at kode mindst et binært fletningssignaleringssyntakselement, der specificerer hvorvidt blokke med grundkodningsenhedsstørrelse flettes til en stor størrelse blok.

15. Videokoderen ifølge krav 13, hvor mindst en af en rumlig intrapartitiontypetabel og en intraprædiktion-driftsformstabel er forlagret og anvendt med videokoderen til at kode den mindst ene store blok.

16. Videokoderen ifølge krav 13, hvor mindst en af en rumlig intrapartitiontypetabel og en intraprædiktion-driftsformstabel er kodet med nævnte videokoder under anvendelse af et eller flere højniveau-syntakselementer og anvendt med videokoderen til at kode den mindst ene store blok (810).

17. Bitstrøm omfattende:

- kodet billeddata, der repræsenterer mindst en stor blok i et billede opnået ved at bestemme at intraprædiktion skal udføres for den mindst ene store blok (820, 830), hvor den mindst ene store blok har en stor blok-størrelse større end en grundkodningsenhedsstørrelse, hvor stor blok-størrelsen er en af 32x32 og 64x64 og hvor grundkodningsenhedsstørrelsen er 16x16,

- et binært splitsignaleringssyntakselement, der specificerer hvorvidt den store blok yderligere splittes i fire lige store underblokke;

- en intraprædiktion-driftsform for nævnte store blok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok ikke splittes yderligere;

ellers i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at den store blok splittes yderligere:

- for hver underblok, i tilfældet hvor nævnte underblok er 32x32, et binært splitsignaleringssyntakselement, der specificerer hvorvidt nævnte 32x32-underblok yderligere splittes i fire blokke af lige stor grundkodningsenhedsstørrelse og en intraprædiktion-driftsform for nævnte 32x32-underblok i tilfældet hvor nævnte binære splitsignaleringssyntakselement specificerer, at nævnte 32x32-underblok ikke splittes yderligere; og

- for hver underblok, i tilfældet hvor nævnte underblok er 16x16, en enkelt rumlig intrapartitionstype, hvor den enkelte rumlige intrapartitionstype kan bestemmes fra blandt en flerhed af rumlige intrapartitionstyper.

18. Bitstrømmen ifølge krav 17, hvor nævnte bitstrøm yderligere omfatter mindst et binært fletningssignaleringssyntakselement, der specificerer hvorvidt blokke med grundkodningsenhedsstørrelse er flettes til en stor størrelse blok.

19. Bitstrømmen ifølge krav 17, hvor nævnte bitstrøm yderligere omfatter data, der repræsenterer mindst en af en rumlig intrapartitiontypetabel og af en intraprædiktion-driftsformstabel kodet i et eller flere højniveau-syntakselementer, hvor nævnte mindst ene af en rumlig intrapartitiontypetabel og en intraprædiktion-driftsformstabel anvendes til at kode nævnte mindst ene store blok.

DRAWINGS

FIG. 1

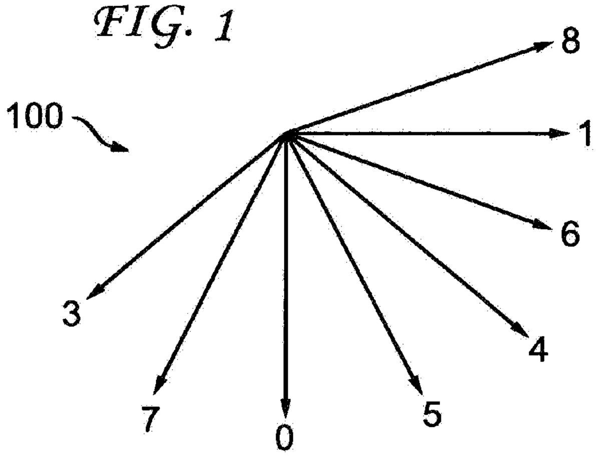
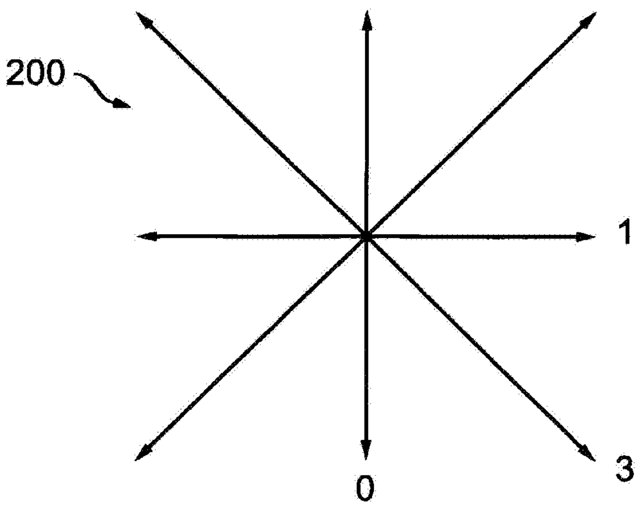


FIG. 2



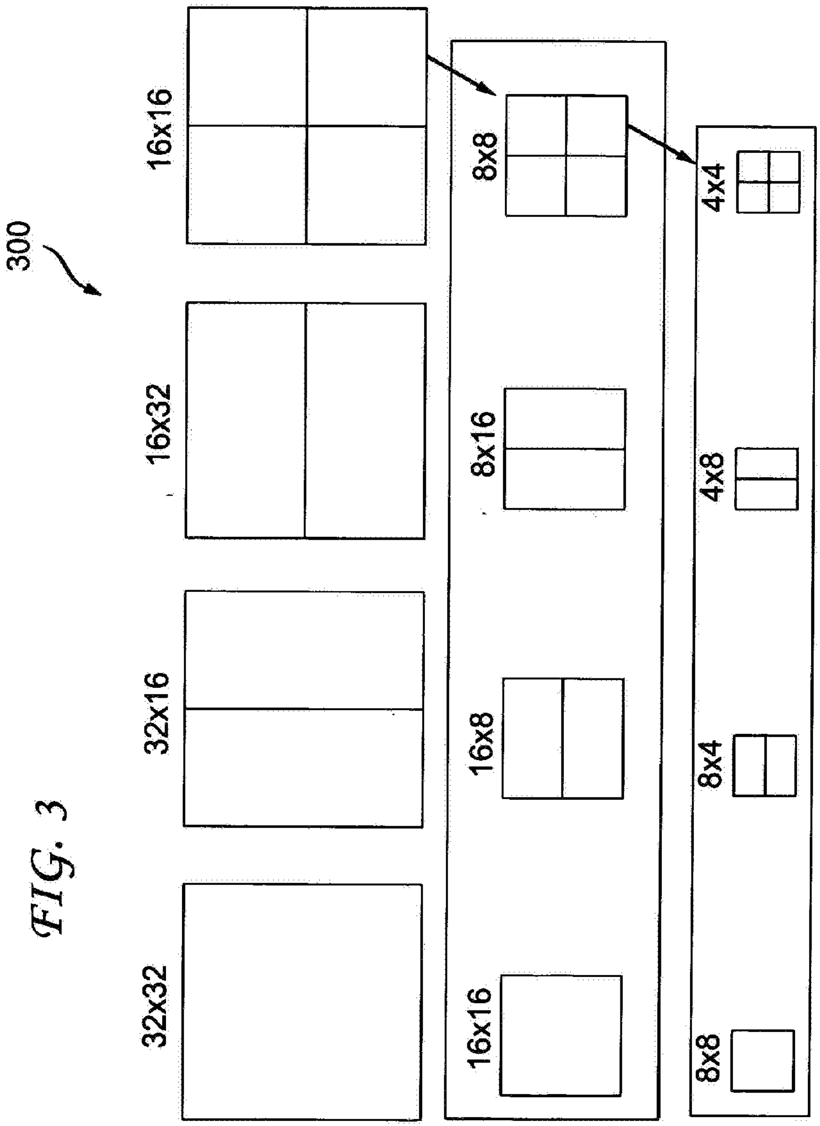
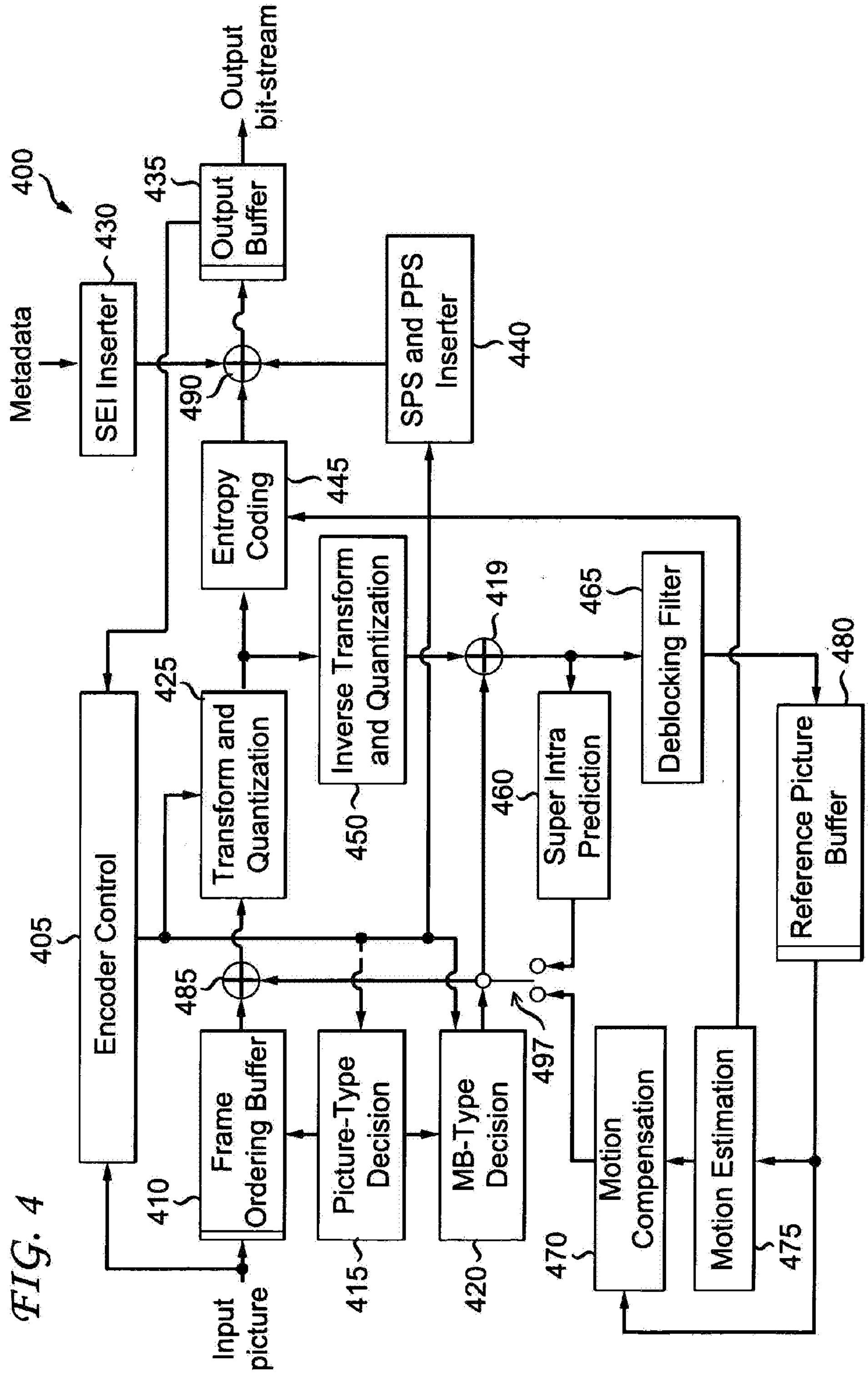

300
32x32
32x16
16x32
16x16
16x16
16x8
8x16
8x8
8x8
8x4
4x8
4x4

FIG. 3



400
Metadata
SEI Inserter
430
435
Output Buffer
Output bit-stream
490
SPS and PPS Inserter
440
Entropy Coding
445
Encoder Control
405
Transform and Quantization
425
Inverse Transform and Quantization
450
419
Super Intra Prediction
460
Deblocking Filter
465
Reference Picture Buffer
480
485
Frame Ordering Buffer
410
Picture-Type Decision
415
MB-Type Decision
420
497
Motion Compensation
470
Motion Estimation
475
Input picture

FIG. 4

FIG. 5

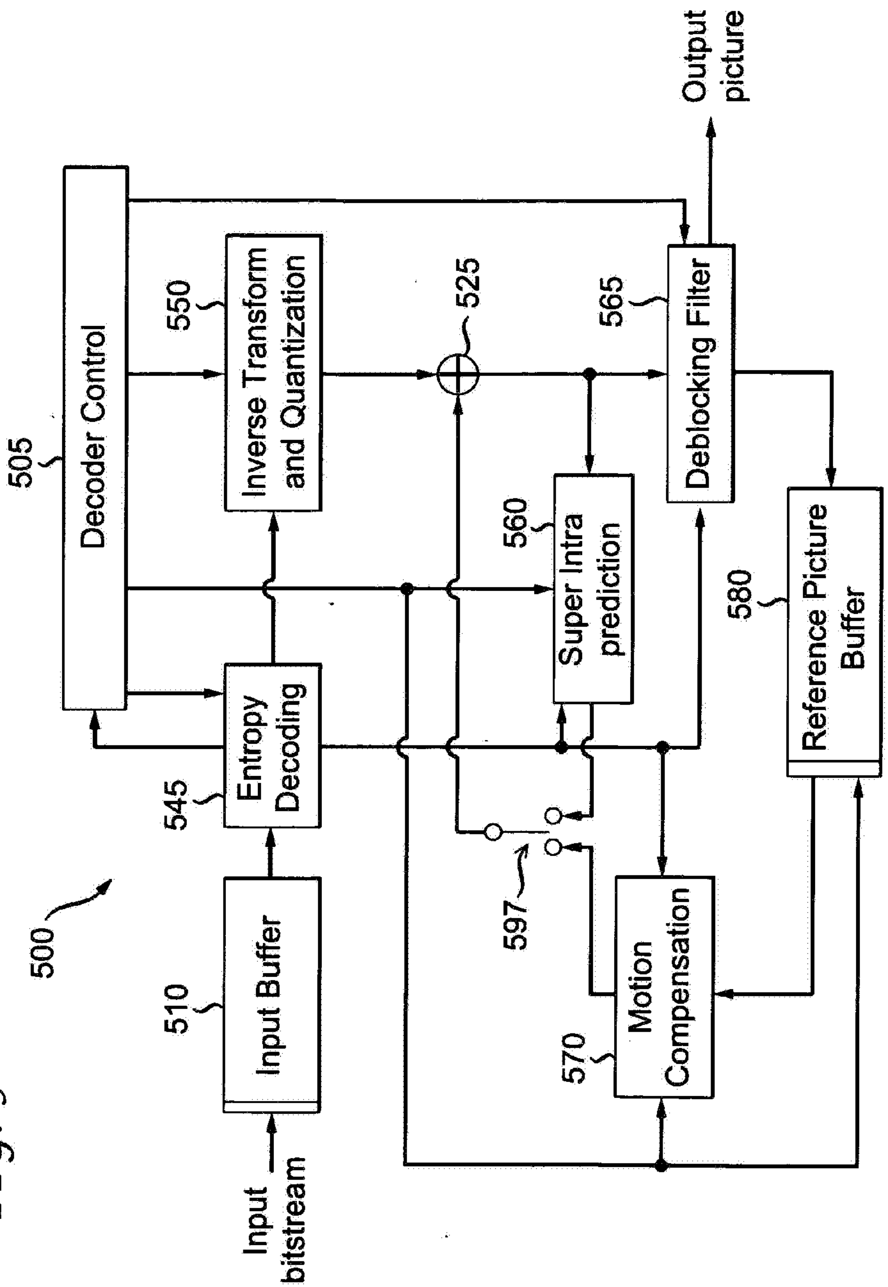
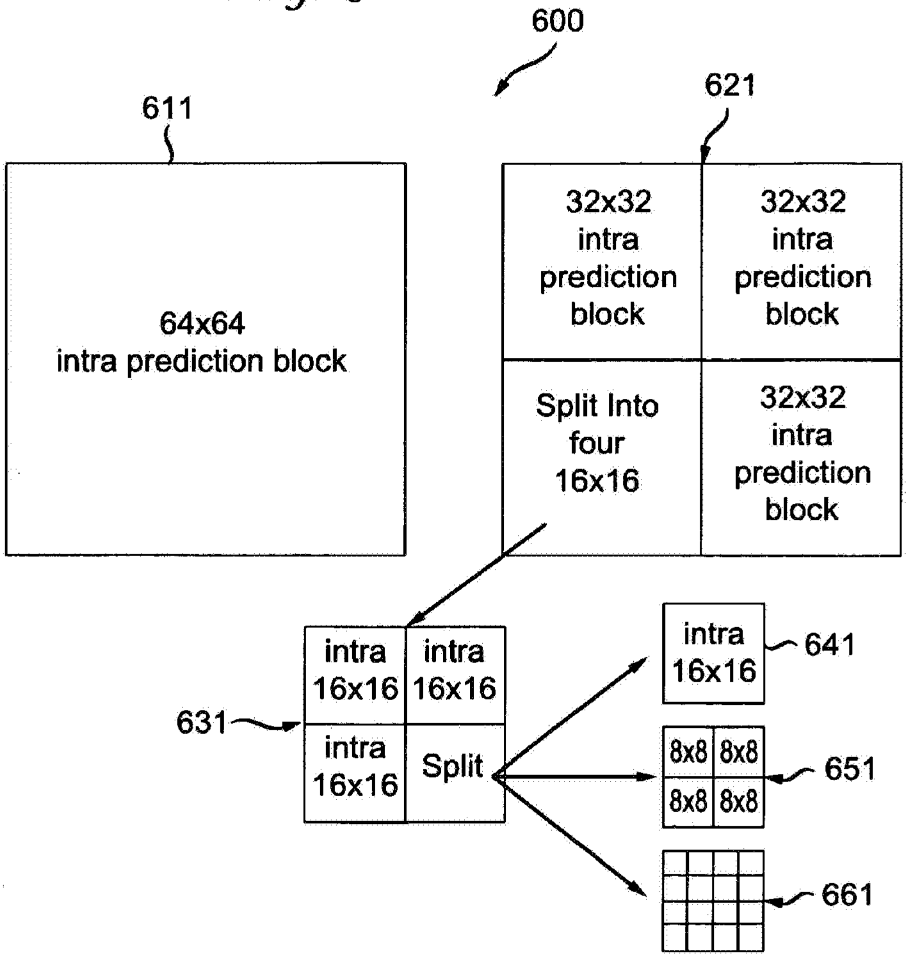

500
505
Decoder Control
510
Input Buffer
Input bitstream
545
Entropy Decoding
550
Inverse Transform and Quantization
525
560
Super Intra prediction
565
Deblocking Filter
Output picture
570
Motion Compensation
580
Reference Picture Buffer
597

FIG. 6


600
611
64x64
intra prediction block
621
32x32
intra
prediction
block
32x32
intra
prediction
block
Split Into
four
16x16
32x32
intra
prediction
block
631
intra
16x16
intra
16x16
intra
16x16
Split
intra
16x16
641
8x8
8x8
8x8
8x8
651
661

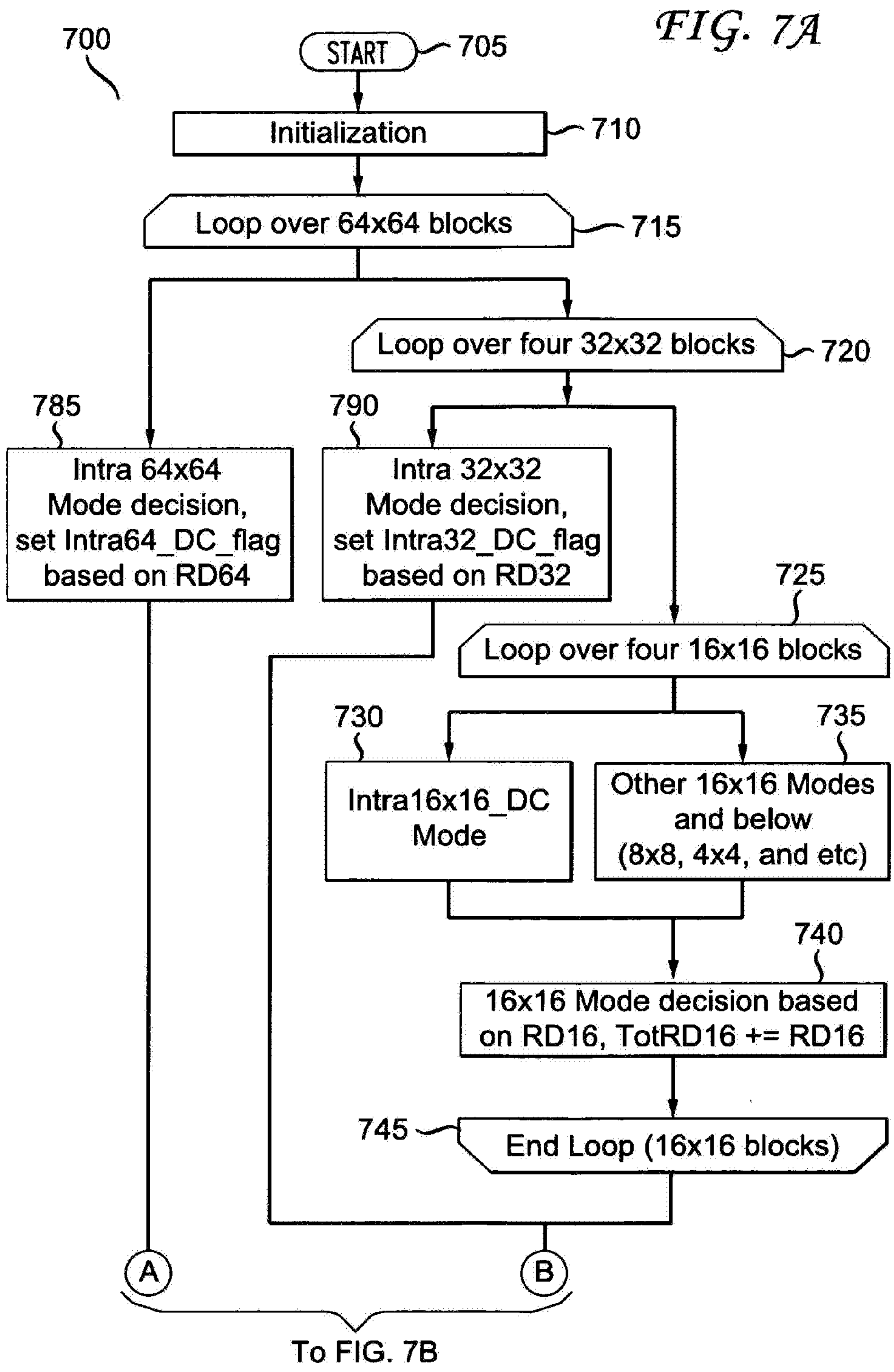


FIG. 7A
700
START
705
Initialization
710
Loop over 64x64 blocks
715
Loop over four 32x32 blocks
720
785
Intra 64x64
Mode decision,
set Intra64_DC_flag
based on RD64
790
Intra 32x32
Mode decision,
set Intra32_DC_flag
based on RD32
725
Loop over four 16x16 blocks
730
735
Intra16x16_DC
Mode
Other 16x16 Modes
and below
(8x8, 4x4, and etc)
740
16x16 Mode decision based
on RD16, TotRD16 += RD16
745
End Loop (16x16 blocks)
A
B
To FIG. 7B

FIG. 7B

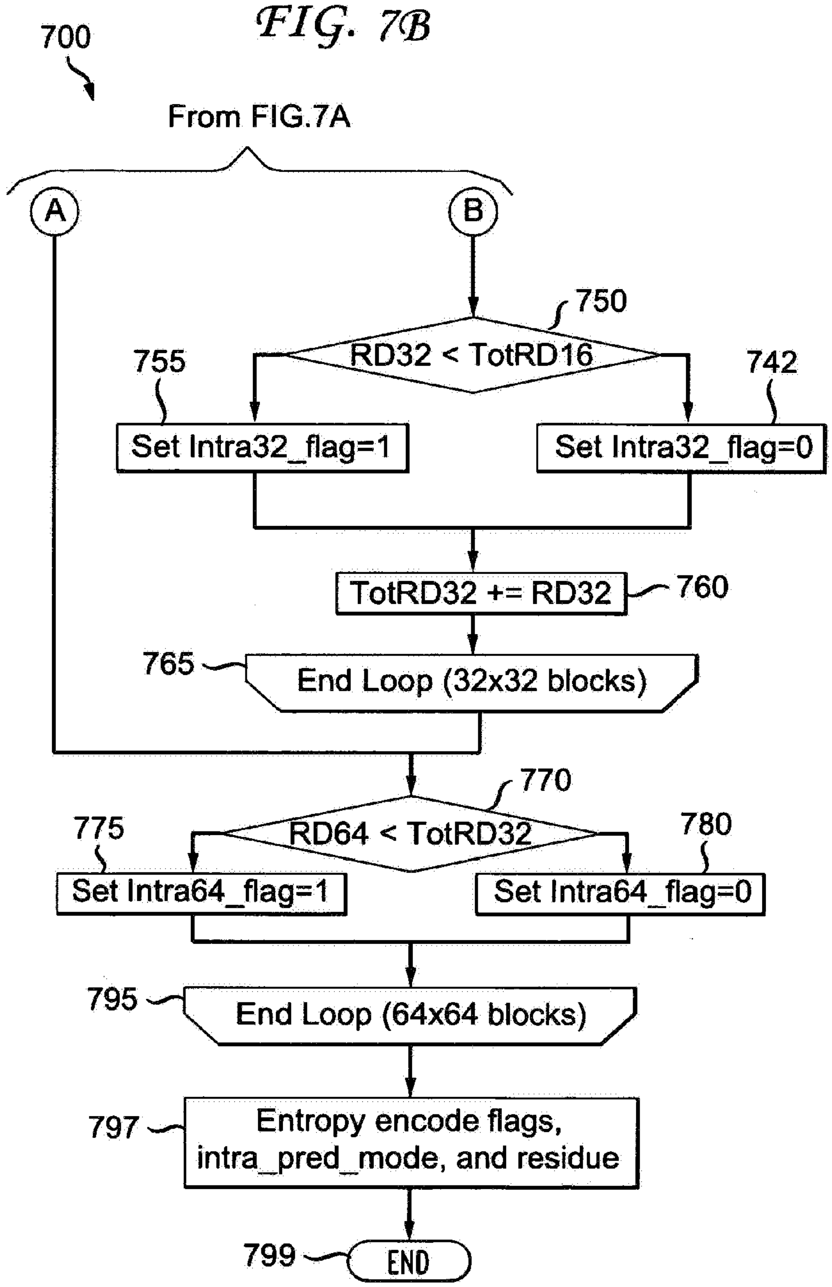

700
From FIG.7A
A
B
750
RD32 < TotRD16
755
742
Set Intra32_flag=1
Set Intra32_flag=0
TotRD32 += RD32
760
765
End Loop (32x32 blocks)
770
RD64 < TotRD32
775
780
Set Intra64_flag=1
Set Intra64_flag=0
795
End Loop (64x64 blocks)
797
Entropy encode flags, intra_pred_mode, and residue
799
END

FIG. 8A

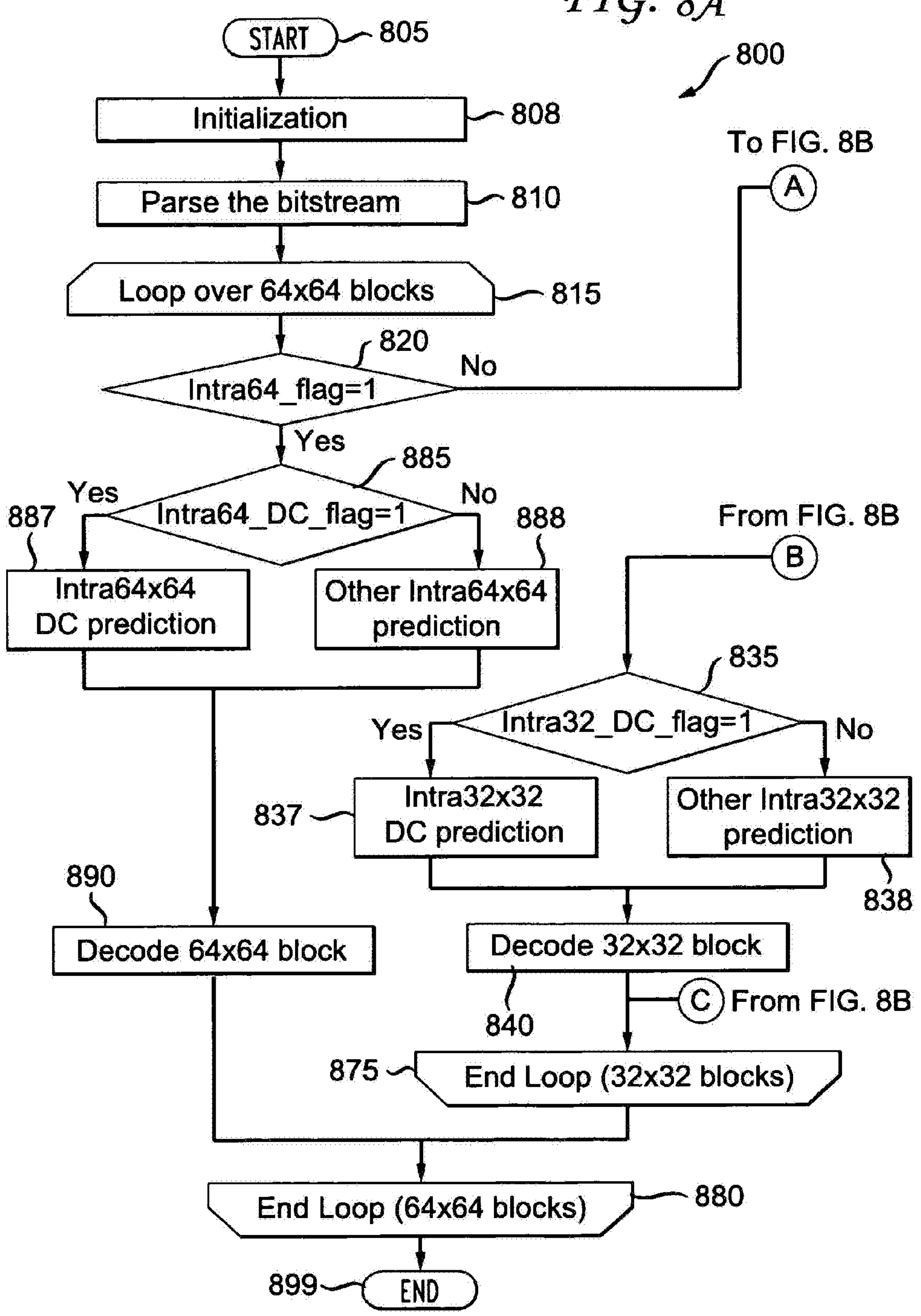
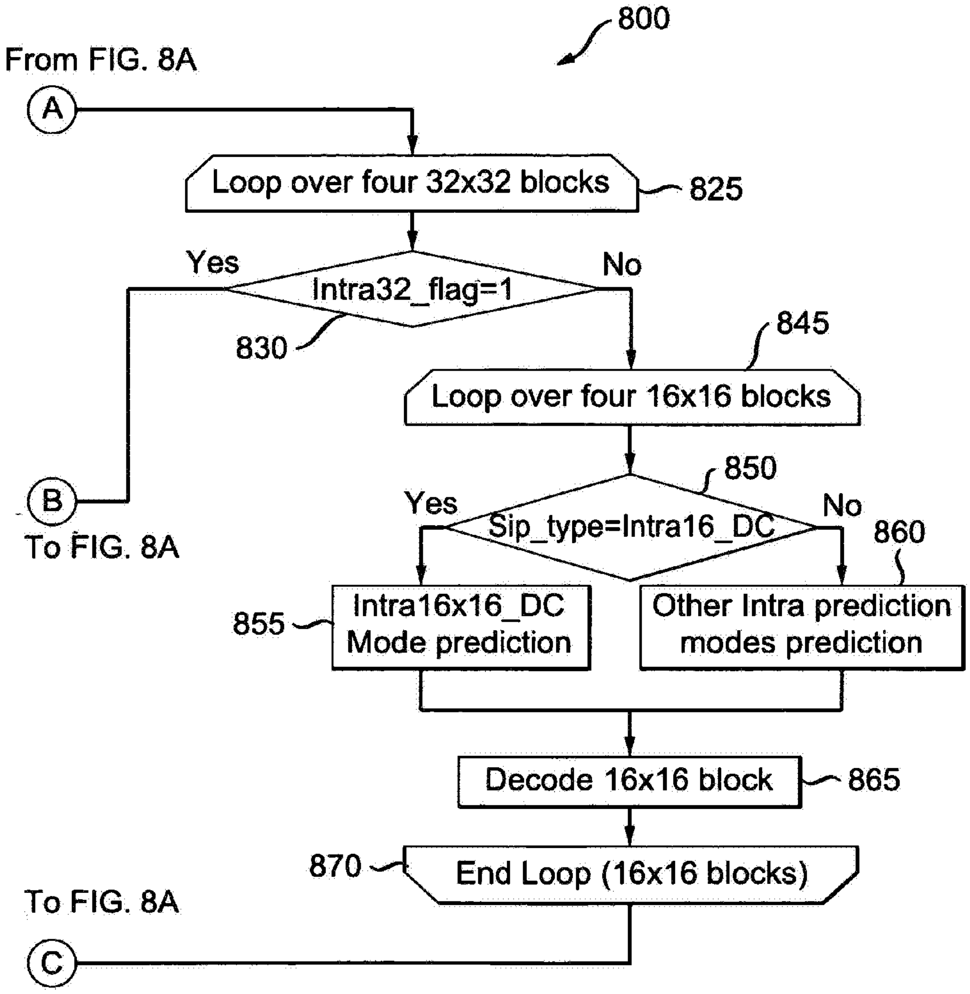

START
805
800
Initialization
808
Parse the bitstream
810
To FIG. 8B
A
Loop over 64x64 blocks
815
820
Intra64_flag=1
No
Yes
885
Yes
Intra64_DC_flag=1
No
887
888
Intra64x64
DC prediction
Other Intra64x64
prediction
From FIG. 8B
B
835
Yes
Intra32_DC_flag=1
No
837
Intra32x32
DC prediction
Other Intra32x32
prediction
838
890
Decode 64x64 block
Decode 32x32 block
840
C
From FIG. 8B
875
End Loop (32x32 blocks)
End Loop (64x64 blocks)
880
899
END

FIG. 8B


800
From FIG. 8A
A
Loop over four 32x32 blocks
825
Yes
Intra32_flag=1
No
830
845
Loop over four 16x16 blocks
B
To FIG. 8A
850
Yes
Sip_type=Intra16_DC
No
860
855
Intra16x16_DC
Mode prediction
Other Intra prediction
modes prediction
Decode 16x16 block
865
870
End Loop (16x16 blocks)
To FIG. 8A
C