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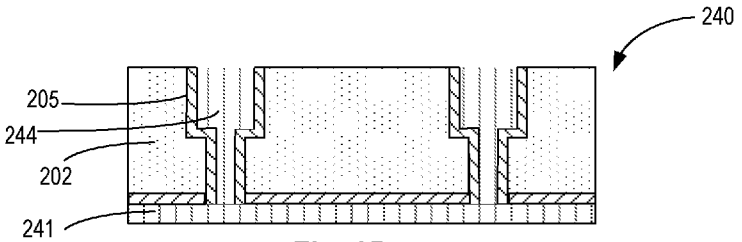

Fig. 2D

(57) Abstract: An apparatus is provided which comprises: a metal region having an ordered crystalline structure; and a barrier layer adjacent to the metal region, the barrier layer comprising Zinc. An apparatus is provided which comprises: a metal region having an ordered crystalline structure, the metal region having traces of zinc; a crystallinity templating layer adjacent to the metal region; and a barrier layer adjacent to the crystallinity templating layer, the barrier layer comprising zinc. An integrated circuit (IC) die is provided which comprises: a barrier layer comprising zinc; and an interconnect formed within the barrier layer, the interconnect comprising a crystalline metal.

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SELF-GENERATED BARRIERS WITH TEMPLATED METAL FOR EFFICIENT ELECTRIC CONDUCTION

BACKGROUND

[0001] Scaling the width of backend metal wires is a critical part of the Moore's law scaling. Moore's law scaling is the observation that the number of transistors in a dense integrated circuit (IC) doubles approximately every two years. As such, for the same die size or smaller die size, metal wires have to scale down in size to support more transistors. However, interconnect scaling increases the resistivity of the metals as the width/thickness of the metal approaches the electron mean free path. Interconnect scaling results in less control by processing or fabricating tools over the grain size of the metals. For example, the metal interconnect may have mixture of inconsistent grain sizes (e.g., smaller, medium, large grains) that may increase resistivity of the metal interconnect.

[0002] **Fig. 1** illustrates plot 100 showing resistivity ρ ($\mu\Omega$ cm) of Copper (Cu) layers at 298 degrees Kelvin (K) versus thickness d_{Cu} (nm). Plot 100 shows three curves—101, 102, and 103. Curve 101 is the resistivity of Cu with small grain size. Curve 102 is the resistivity of Cu with medium grain size, and curve 103 is the resistivity of Cu with large grain size. As the grain size getters larger, the resistivity reduces. However, as the metal interconnect scales down, the metal interconnect may have inconsistent grains which result in less control over resistivity of the metal interconnect.

[0003] Traditional metals such as Cu also require an electro-migration barrier around the metal interconnect which reduces the effective area available for low resistance metal interconnect. As metal interconnects scale down in size, the effective area available for low resistance metal interconnect further reduces.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The embodiments of the disclosure will be understood more fully from the detailed description given below and from the accompanying drawings of various embodiments of the disclosure, which, however, should not be taken to limit the disclosure to the specific embodiments, but are for explanation and understanding only.

[0005] **Fig. 1** illustrates a plot showing resistivity ρ ($\mu\Omega$ cm) of Copper (Cu) layers at 298 degrees Kelvin versus thickness d_{Cu} (nm).

[0006] **Figs. 2A-D** illustrate cross-sections of a die showing fabrication of templated metal interconnect and vias with self-generated barriers, in accordance with some embodiments of the disclosure.

[0007] **Figs. 3A-E** illustrate cross-sections of metal interconnect or vias with various templating configurations and with self-generated barriers adjacent to the metal interconnect or vias, in accordance with some embodiments of the disclosure.

[0008] **Figs. 4A-E** illustrate cross-sections of metal interconnect or vias with various templating configurations and with self-generated barriers adjacent to a layer of Heusler alloy(s), in accordance with some embodiments of the disclosure.

[0009] **Figs. 5A-C** illustrate cross-sections of metal interconnect or vias with various templating configurations and with self-generated barriers adjacent to a dielectric layer, in accordance with some embodiments of the disclosure.

[0010] **Figs. 6A-B** illustrate cross-sections of metal interconnect or vias with various templating configuration and with self-generated barrier adjacent to a dielectric layer which is adjacent to a layer of Heusler Alloy(s), in accordance with some embodiments of the disclosure.

[0011] **Fig. 7A** illustrates a phase diagram of CuZn alloy showing the transition in crystal structure at approximately 400°C, according to some embodiments.

[0012] **Fig. 7B** illustrates lattice structure of CuZn alloy with Cu atom in the center and Zn atoms around it, according to some embodiments. .

[0013] **Fig. 7C** illustrates lattice structure of Cu after the alloy of CuZn is heated for some time around temperature of 400 °C, according to some embodiments.

[0014] **Fig. 8** illustrates a smart device or a computer system or a SoC (System-on-Chip) templated metal interconnect and vias with self-generated barriers, according to some embodiments of the disclosure.

DETAILED DESCRIPTION

[0015] Some embodiments describe a highly efficient templating method and apparatus for creating high crystalline metal wires (or interconnect), vias, transistor gates, and/or contacts. In some embodiments, high crystalline metal wires are formed from a bi-metallic phase transition based templating. In some embodiments, the high crystalline metal wires (also referred to as templated metallic nanowires) exhibit crystalline order comprising one of the

metals: CuZn, Cu_3Zn, CuZn, AgZn, Ag_3Zn, AgZn, $Cu_{0.5}Ag_{0.5}Zn$, or $Cu_{1.5}Ag_{1.5}Zn$. In some embodiments, the templated metallic nanowires exhibiting crystalline order comprise a metallic layer stack A/B/C, where 'A' and 'C' are ZnO, and where 'B' is one of: Cu, Ag, CuAg, or Cu_xAg_y. As such, 'B' forms the conductive interconnect and 'A' and 'C' are surrounding barrier layers (e.g., 'B' is within barrier layers 'A' and 'C'). In some embodiments, the metallic nanowires have naturally formed barriers which are formed by one of: Zn, ZnO, Zn_xO_y, or other materials that are getters for Zn (e.g., MgO).

[0016] In some embodiments, the templated metallic nanowires exhibiting crystalline order comprise a metallic layer stack A/B/C/D/E, where 'A' and 'E' are dielectrics (e.g., MgO), where 'B' and 'D' is ZnO, and where 'C' is one of: Cu, Ag, CuAg, or Cu_xAg_y. As such, 'C' forms the conductive interconnect and 'B' and 'D' are barrier layers, and 'A' and 'E' are used for templating metal 'C'. In some embodiments, vias and other components such as transistor gates are formed of the templated metallic nanowires exhibiting crystalline order discussed here.

[0017] The materials used for creating templated metallic nanowires exhibiting crystalline order allow for use of damascene based processing methods, subtractive processing methods for creating templated, and/or recess processing methods. In some embodiments, super lattice interconnect stacks are formed comprising of repeated use of template enhancing materials.

[0018] There are many technical effects of the various embodiments. For example, in some embodiments the templating of metal improves crystallinity of the metal which in turn reduces the resistivity and electro-migration of the metal. As such, the metal can be used for forming interconnect and to mitigate the scaling impact of process technology nodes. The templating of metal as described with reference to the various embodiments also improves fabrication using subtracting processing. The templating technique described with reference to the various embodiments allow for self-generating conductive barriers (which comprise Zn). The various embodiments enable continued use of high conductivity Cu and Ag interconnects. Other technical effects or benefits will be evident from the description of various embodiments and figures.

[0019] In the following description, numerous details are discussed to provide a more thorough explanation of embodiments of the present disclosure. It will be apparent, however, to one skilled in the art, that embodiments of the present disclosure may be practiced without these

specific details. In other instances, well-known structures and devices are shown in block diagram form, rather than in detail, in order to avoid obscuring embodiments of the present disclosure.

[0020] Note that in the corresponding drawings of the embodiments, signals are represented with lines. Some lines may be thicker, to indicate more constituent signal paths, and/or have arrows at one or more ends, to indicate primary information flow direction. Such indications are not intended to be limiting. Rather, the lines are used in connection with one or more exemplary embodiments to facilitate easier understanding of a circuit or a logical unit. Any represented signal, as dictated by design needs or preferences, may actually comprise one or more signals that may travel in either direction and may be implemented with any suitable type of signal scheme.

[0021] Throughout the specification, and in the claims, the term "connected" means a direct physical, electrical, or wireless connection between the things that are connected, without any intermediary devices. The term "coupled" means either a direct electrical or wireless connection between the things that are connected or an indirect electrical or wireless connection through one or more passive or active intermediary devices. The term "circuit" means one or more passive and/or active components that are arranged to cooperate with one another to provide a desired function. The term "signal" means at least one current signal, voltage signal, magnetic signal, electromagnetic signal, or data/clock signal. The meaning of "a," "an," and "the" include plural references. The meaning of "in" includes "in" and "on."

[0022] The terms “substantially,” “close,” “approximately,” “near,” and “about,” generally refer to being within +/- 10% of a target value (unless specifically specified). Unless otherwise specified the use of the ordinal adjectives “first,” “second,” and “third,” etc., to describe a common object, merely indicate that different instances of like objects are being referred to, and are not intended to imply that the objects so described must be in a given sequence, either temporally, spatially, in ranking or in any other manner.

[0023] For the purposes of the present disclosure, phrases “A and/or B” and “A or B” mean (A), (B), or (A and B). For the purposes of the present disclosure, the phrase “A, B, and/or C” means (A), (B), (C), (A and B), (A and C), (B and C), or (A, B and C).

[0024] The terms "left," "right," "front," "back," "top," "bottom," "over," "under," and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions.

[0025] **Figs. 2A-D** illustrate cross-sections 200, 220, 230, and 240, respectively, of a die showing fabrication of templated metal interconnect and vias with self-generated barriers, in accordance with some embodiments of the disclosure.

[0026] Although the fabrication processes with reference to **Figs. 2A-D** are shown in a particular order, the order of the actions can be modified. Thus, the illustrated embodiments can be performed in a different order, and some actions/fabrication processes may be performed in parallel. Some of the fabrication processes listed in **Figs. 2A-D** are optional in accordance with certain embodiments. The numbering of the fabrication processes presented is for the sake of clarity and is not intended to prescribe an order of operations in which the various blocks must occur. Additionally, operations from the various flows may be utilized in a variety of combinations.

[0027] **Fig. 2A** illustrates one example of a starting point. Here, the die cross-section 200 shows deposition of a layer of dielectric 202 (e.g., SiO_2) over metal layer 201. In some embodiments, the layer of metal 201 (or metal region 201) is formed of a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. This layer of metal 201 may have an unordered crystalline structure.

[0028] Here, the term unordered crystalline structure generally refers to a crystalline structure in which the electron wave diffraction is not defined by Bragg's law. Unordered materials may exhibit high directional and angular isotropy without long range spatial/directional periodicity. Unordered materials are characterized by a signature on a TEM (Transmission Electron Microscopy), STEM (Scanning Transmission Electron Microscopy) or RHEED (Reflection High-Energy Electron Diffraction), XRD (X-ray Powder Diffraction) metrology.

[0029] **Fig. 2B** illustrates cross-section 220 of the die after trenches 203 are etched through dielectric layer 202. Any known suitable process of forming trenches 203 may be used. In this example, two trenches are etched (e.g., the left and right trenches) and each trench is a future location of a via to couple to a metal layer, and a future location of another metal layer. In some embodiments, the other metal layer extends orthogonal to metal layer 201. For example,

metal layer 201 is metal layer 1 (M1) and the other metal layer (later shown as 204) is metal layer 2 (M2).

[0030] **Fig. 2C** illustrates cross-section 230 of the die after metal 204 is deposited in trench 203. In some embodiments, material deposited for the via is different from the material deposited for the metal interconnect. For example, material for via is AgZn or Ag_3Zn while the material for the metal interconnect is selected from a group consisting of: CuZn; Cu_3Zn; CuZn. In some embodiments, metal 204 is selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. Metal 204 may have an unordered crystalline structure.

[0031] **Fig. 2D** illustrates cross-section 240 of the die after metal 201 and metal 204 are heated to cause phase change in the crystalline structures of metal 201 and metal 204, according to some embodiments of the disclosure. In some embodiments, after increasing temperature (e.g., to 298K, or approximately 400°C), metal 201 and metal 204 (which are also referred to as bi-metallic layers/regions 201 and 204) exhibit phase change in their crystalline order. The Zinc in these bi-metallic layers/regions 201 and 204 begins to escape at those temperatures leaving behind templated metal regions 241 and 244 with ordered crystalline structure. The escaped zinc forms a barrier region 205 around templated metal regions (or interconnects) 241 and 244. In some embodiments, templated metal regions 241 and 244 are formed of mostly (e.g., more than 80%) one of Cu or Ag with traces of Zn. In some embodiments, templated metal regions 241 and 244 are pure metal (e.g., one of Cu or Ag). The barrier region 205 comprises Zinc. In some embodiments, barrier layer 205 is formed of a material selected from a group consisting of: Zn, ZnO, and Zn_2SiO_4.

[0032] Here, the term "ordered" generally refers to material condition that shows electron wave diffraction as defined by Bragg's law. Ordered material may be characterized by one of the space groups combined with a unit cell. Ordered material exhibit long range periodicity both in direction and displacement. In Metrology tools such as XRD and RHEED, an interferometric signature is evident for ordered materials.

[0033] In some embodiments, super-lattice stacks comprises repeated patterns of template enhancing material (e.g., as those described with reference to **Figs. 4-6**) are deposited in outer regions of trenches 203 before metal 204 is deposited. In some embodiments, damascene based processing method are used for creating templated interconnect 241 and 244. In some

embodiments, subtractive processing methods are used for creating templating interconnect 241 and 244. In some embodiments, recess processing method are used to take advantage of the templated interconnect 241 and 244. In some embodiments, super-lattice stacks comprising of repeated patterns of template enhancing material (e.g., as those described with reference to **Figs. 5-6**) are used for metal interconnects 241 and 244. In some embodiments, the process of fabricating the templated metal interconnect and vias can start at various points in the fabrication process as described with reference to various embodiments.

[0034] **Figs. 3A-E** illustrate cross-sections 300, 320, 330, 340, and 350, respectively, of metal interconnect or vias with various templating configurations and with self-generated barriers adjacent to the metal interconnect or vias, in accordance with some embodiments of the disclosure. Cross-section 300 illustrates metal 301 which is formed of a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. This layer of metal 301 may have an unordered crystalline structure. Cross-section 320 illustrates condition of metal 301 after phase change of crystalline structure of metal 301. In some embodiments, after increasing temperature (e.g., to 298K, or approximately 400°C), metal 301 (which is also referred to as bi-metallic layer/region 301) exhibits phase change in its crystalline order. The zinc in the bi-metallic layer/region 301 begins to escape at those temperatures leaving behind templated metal region 321 with ordered crystalline structure. The escaped zinc forms a barrier region 323 around templated metal region (or interconnect) 321. In some embodiments, templated metal region 321 is formed of mostly (e.g., more than 80%) one of Cu or Ag with traces of Zn. In some embodiments, templated metal region 321 is pure metal (e.g., one of Cu or Ag).

[0035] The barrier region 323 comprises Zinc. In some embodiments, barrier layer 323 is formed of a material selected from a group consisting of: Zn, ZnO, and Zn_2SiO_4. Cross-section 330 illustrates cross-section of templated metal 321 with one side of barrier 333 removed. Cross-section 340 illustrates cross-section of templated metal 321 with three sides of barrier 343 removed. Cross-section 350 illustrates templated metal 321 after all four sides of barrier 323 are moved. Barriers 333 and 343 have the same material composition as that of barrier 323.

[0036] **Figs. 4A-E** illustrate cross-sections 400, 420, 430, 440, and 450, respectively, of metal interconnect or vias with various templating configurations and with self-generated

barriers adjacent to a layer of Heusler alloy(s), in accordance with some embodiments of the disclosure. Cross-section 400 illustrates metal 401 which is formed of a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. This layer of metal 401 may have an unordered crystalline structure.

[0037] Cross-section 420 illustrates condition of metal 401 after phase change of crystalline structure of metal 401. In some embodiments, after increasing temperature (e.g., to 298K, or approximately 400°C), metal 401 (which is also referred to as bi-metallic layer/region 401) exhibits phase change in its crystalline order. Compared to cross-section 320, here a templating layer 422 is formed around metal 401 before temperature based phase change in metal 401 occurs. In some embodiments, the crystallinity templating layer 422 is formed of a Heusler alloy metal. In some embodiments, the Heusler alloy metal is selected from a group consisting of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa, Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, and Co_2FeGe.

[0038] The zinc in the bi-metallic layer/region 401 begins to escape at those high temperatures leaving behind templated metal region 421 with ordered crystalline structure. The escaped zinc forms a barrier region 423 around the crystallinity templating layer 422. In some embodiments, templated metal region 421 is formed of mostly (e.g., more than 80%) one of Cu or Ag with traces of Zn. In some embodiments, templated metal region 421 is pure metal (e.g., one of Cu or Ag). The barrier region 423 comprises Zinc. In some embodiments, barrier layer 423 is formed of a material selected from a group consisting of: Zn, ZnO, and Zn_2SiO_4.

[0039] Cross-section 430 illustrates cross-section of templated metal 421 with one side of barrier 433 removed. Cross-section 440 illustrates cross-section of templated metal 421 with three sides of barrier 443 removed. Cross-section 450 illustrates templated metal 421 after all four sides of barrier 423 are moved. Barriers 433 and 443 have the same material composition as that of barrier 423. In some embodiments, templating material 422 is a sacrificial layer which is removed after the crystalline structure of metal layer 401 is ordered to be metal layer 421. In some embodiments, templating material 422 remains as is and further processing steps are performed above templating material 422.

[0040] **Figs. 5A-C** illustrate cross-sections 500, 520, and 530, respectively, of metal interconnect or vias with various templating configurations and with self-generated barriers

adjacent to a dielectric layer, in accordance with some embodiments of the disclosure. Cross-section 500 illustrates metal 501 which is formed of a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. This layer of metal 501 may have an unordered crystalline structure.

[0041] Cross-section 520 illustrates condition of metal 501 after phase change of crystalline structure of metal 501. In some embodiments, after increasing temperature (e.g., to 298K, or approximately 400°C), metal 501 (which is also referred to as bi-metallic layer/region 501) exhibits phase change in its crystalline order. Compared to cross-section 320, here a templating layer 522 is formed around metal 501 before temperature based phase change in metal 501 occurs. In some embodiments, the templating layer is a dielectric layer (e.g., MgO).

[0042] The zinc in the bi-metallic layer/region 501 begins to escape at those high temperatures leaving behind templated metal region 521 with ordered crystalline structure. The escaped zinc forms a barrier region 523 around dielectric layer 522. In some embodiments, templated metal region 521 is formed of mostly (e.g., more than 80%) one of Cu or Ag with traces of Zn. In some embodiments, templated metal region 521 is pure metal (e.g., one of Cu or Ag). The barrier region 523 comprises Zinc. In some embodiments, barrier layer 523 is formed of a material selected from a group consisting of: Zn, ZnO, and Zn_2SiO_4.

[0043] Cross-section 530 illustrates a super lattice with multiple layers of dielectric 522 surrounding metal 501. Cross-section 530 shows the condition of the materials after phase change in its crystalline order of metal 501 to form 521. In some embodiments, un-ordered metal (selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$) is deposited around layer of dielectric 522, and this metal after phase change becomes metal 533 (e.g., Cu or Ag with traces of Zn). In some embodiments, another dielectric layer 534 (e.g., MgO) is deposited around un-ordered metal (which after phase changes becomes metal 533).

[0044] The zinc in the bi-metallic layer/region 501 (and second metal region around dielectric layer 522) begins to escape at those high temperatures leaving behind templated metal regions 521 and 533 with ordered crystalline structure. The escaped zinc forms a barrier region 535 around the dielectric layer 534. In some embodiments, templated metal regions 521 and 533 are formed of mostly (e.g., more than 80%) one of Cu or Ag with traces of Zn. In some embodiments, templated metal regions 521 and 533 are pure metal (e.g., one of Cu or Ag). The

barrier region 535 comprises Zinc. In some embodiments, barrier layer 535 is formed of a material selected from a group consisting of: Zn, ZnO, ZnMgO, and Zn_2SiO_4.

[0045] **Figs. 6A-B** illustrate cross-sections 600 and 620, respectively, of metal interconnect or vias with various templating configuration and with self-generated barrier adjacent to a dielectric layer which is adjacent to a layer of Heusler Alloys, in accordance with some embodiments of the disclosure. Cross-section 600 illustrates metal 601 which is formed of a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. This layer of metal 601 may have an unordered crystalline structure.

[0046] Cross-section 620 illustrates condition of metal 601 after phase change of crystalline structure of metal 601. In some embodiments, after increasing temperature (e.g., to 298K, or approximately 400°C), metal 601 (which is also referred to as bi-metallic layer/region 601) exhibits phase change in its crystalline order and becomes metal 621 (with ordered crystalline order). Compared to cross-section 320, here templating layers 622 and 623 are formed around metal 601 before temperature based phase change in metal 601 occurs. In some embodiments, the crystallinity templating layers include layer of a Heusler alloy metal 622. In some embodiments, the Heusler alloy metal 622 is selected from a group consisting of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa, Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, and Co_2FeGe. In some embodiments, the crystallinity templating layers include layer of dielectric 623 (e.g., MgO) formed over the layer of Heusler alloy metal 622. In some embodiments, a supper lattice is formed with repeated layer of metal 601, layer of Heusler alloy metal 622, and layer of dielectric 623.

[0047] In some embodiments, the zinc in the bi-metallic layer/region 601 begins to escape at those high temperatures leaving behind templated metal region 621 with ordered crystalline structure. The escaped zinc forms a barrier region 624 around the dielectric layer 623. In some embodiments, templated metal region 621 is formed of mostly (e.g., more than 80%) one of Cu or Ag with traces of Zn. In some embodiments, templated metal region 621 is pure metal (e.g., one of Cu or Ag). The barrier region 624 comprises zinc. In some embodiments, barrier layer 624 is formed of a material selected from a group consisting of: Zn, ZnO, ZnMgO, and Zn_2SiO_4.

[0048] **Fig. 7A** illustrates a phase diagram 700 of CuZn showing the transition in crystal structure at approximately 400°C. Here, x-axis is percentage (%) weight of Zn in CuZn alloy used in metal 204, for example, and y-axis is temperature in Celsius. Phase diagram 700 illustrates that as temperature increases and rises to about 400°C, the percentage weight of Zn in CuZn alloy of metal 204 reduces because Zn begins to escape (which forms the basis of the barrier layer 205).

[0049] **Fig. 7B** illustrates lattice structure 720 of CuZn with Cu atom 721 in the center and Zn atoms 722 around it. Lattice structure 720 shows the crystal structure of CuZn with about 50% of Zn by weight. **Fig. 7C** illustrates lattice structure 730 of Cu after the alloy of CuZn is heated for some time around temperature of 400 °C. Lattice structure 730 shows the FCC (face centered cube) crystal structure of Cu 721 with most (in this case all) Zn atoms having left the CuZn alloy.

[0050] **Fig. 8** illustrates a smart device or a computer system or a SoC (System-on-Chip) 1600 with templated metal interconnect and vias with self-generated barriers, according to some embodiments of the disclosure. It is pointed out that those elements of **Fig. 8** having the same reference numbers (or names) as the elements of any other figure can operate or function in any manner similar to that described, but are not limited to such.

[0051] **Fig. 8** illustrates a block diagram of an embodiment of a mobile device in which flat surface interface connectors could be used. In some embodiments, computing device 1600 represents a mobile computing device, such as a computing tablet, a mobile phone or smart-phone, a wireless-enabled e-reader, or other wireless mobile device. It will be understood that certain components are shown generally, and not all components of such a device are shown in computing device 1600.

[0052] For purposes of the embodiments, the transistors in various circuits and logic blocks described here are metal oxide semiconductor (MOS) transistors, which include drain, source, gate, and bulk terminals. The transistors also include Tri-Gate and FinFET transistors, Gate All Around Cylindrical Transistors, Tunneling FET (TFET), Square Wire, or Rectangular Ribbon Transistors or other devices implementing transistor functionality like carbon nanotubes or spintronic devices. MOSFET symmetrical source and drain terminals i.e., are identical terminals and are interchangeably used here. A TFET device, on the other hand, has asymmetric Source and Drain terminals. Those skilled in the art will appreciate that other transistors, for

example, Bi-polar junction transistors—BJT PNP/NPN, BiCMOS, CMOS, eFET, etc., may be used without departing from the scope of the disclosure.

[0053] In some embodiments, computing device 1600 includes first processor 1610 with templated metal interconnects, contacts, transistor gates, and/or vias, according to some embodiments discussed. Other blocks of the computing device 1600 may also include with templated metal interconnect and vias with self-generated barriers, according to some embodiments. The various embodiments of the present disclosure may also comprise a network interface within 1670 such as a wireless interface so that a system embodiment may be incorporated into a wireless device, for example, cell phone or personal digital assistant.

[0054] In some embodiments, processor 1610 (and/or processor 1690) can include one or more physical devices, such as microprocessors, application processors, microcontrollers, programmable logic devices, or other processing means. The processing operations performed by processor 1610 include the execution of an operating platform or operating system on which applications and/or device functions are executed. The processing operations include operations related to I/O (input/output) with a human user or with other devices, operations related to power management, and/or operations related to connecting the computing device 1600 to another device. The processing operations may also include operations related to audio I/O and/or display I/O.

[0055] In some embodiments, computing device 1600 includes audio subsystem 1620, which represents hardware (e.g., audio hardware and audio circuits) and software (e.g., drivers, codecs) components associated with providing audio functions to the computing device. Audio functions can include speaker and/or headphone output, as well as microphone input. Devices for such functions can be integrated into computing device 1600, or connected to the computing device 1600. In one embodiment, a user interacts with the computing device 1600 by providing audio commands that are received and processed by processor 1610.

[0056] In some embodiments, computing device 1600 comprises display subsystem 1630. Display subsystem 1630 represents hardware (e.g., display devices) and software (e.g., drivers) components that provide a visual and/or tactile display for a user to interact with the computing device 1600. Display subsystem 1630 includes display interface 1632, which includes the particular screen or hardware device used to provide a display to a user. In one embodiment, display interface 1632 includes logic separate from processor 1610 to perform at

least some processing related to the display. In one embodiment, display subsystem 1630 includes a touch screen (or touch pad) device that provides both output and input to a user.

[0057] In some embodiments, computing device 1600 comprises I/O controller 1640. I/O controller 1640 represents hardware devices and software components related to interaction with a user. I/O controller 1640 is operable to manage hardware that is part of audio subsystem 1620 and/or display subsystem 1630. Additionally, I/O controller 1640 illustrates a connection point for additional devices that connect to computing device 1600 through which a user might interact with the system. For example, devices that can be attached to the computing device 1600 might include microphone devices, speaker or stereo systems, video systems or other display devices, keyboard or keypad devices, or other I/O devices for use with specific applications such as card readers or other devices.

[0058] As mentioned above, I/O controller 1640 can interact with audio subsystem 1620 and/or display subsystem 1630. For example, input through a microphone or other audio device can provide input or commands for one or more applications or functions of the computing device 1600. Additionally, audio output can be provided instead of, or in addition to display output. In another example, if display subsystem 1630 includes a touch screen, the display device also acts as an input device, which can be at least partially managed by I/O controller 1640. There can also be additional buttons or switches on the computing device 1600 to provide I/O functions managed by I/O controller 1640.

[0059] In some embodiments, I/O controller 1640 manages devices such as accelerometers, cameras, light sensors or other environmental sensors, or other hardware that can be included in the computing device 1600. The input can be part of direct user interaction, as well as providing environmental input to the system to influence its operations (such as filtering for noise, adjusting displays for brightness detection, applying a flash for a camera, or other features).

[0060] In some embodiments, computing device 1600 includes power management 1650 that manages battery power usage, charging of the battery, and features related to power saving operation. Memory subsystem 1660 includes memory devices for storing information in computing device 1600. Memory can include nonvolatile (state does not change if power to the memory device is interrupted) and/or volatile (state is indeterminate if power to the memory device is interrupted) memory devices. Memory subsystem 1660 can store application data, user

data, music, photos, documents, or other data, as well as system data (whether long-term or temporary) related to the execution of the applications and functions of the computing device 1600.

[0061] Elements of embodiments are also provided as a machine-readable medium (e.g., memory 1660) for storing the computer-executable instructions (e.g., instructions to implement any other processes discussed herein). The machine-readable medium (e.g., memory 1660) may include, but is not limited to, flash memory, optical disks, CD-ROMs, DVD ROMs, RAMs, EPROMs, EEPROMs, magnetic or optical cards, phase change memory (PCM), or other types of machine-readable media suitable for storing electronic or computer-executable instructions. For example, embodiments of the disclosure may be downloaded as a computer program (e.g., BIOS) which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals via a communication link (e.g., a modem or network connection).

[0062] In some embodiments, computing device 1600 comprises connectivity 1670. Connectivity 1670 includes hardware devices (e.g., wireless and/or wired connectors and communication hardware) and software components (e.g., drivers, protocol stacks) to enable the computing device 1600 to communicate with external devices. The computing device 1600 could be separate devices, such as other computing devices, wireless access points or base stations, as well as peripherals such as headsets, printers, or other devices.

[0063] Connectivity 1670 can include multiple different types of connectivity. To generalize, the computing device 1600 is illustrated with cellular connectivity 1672 and wireless connectivity 1674. Cellular connectivity 1672 refers generally to cellular network connectivity provided by wireless carriers, such as provided via GSM (global system for mobile communications) or variations or derivatives, CDMA (code division multiple access) or variations or derivatives, TDM (time division multiplexing) or variations or derivatives, or other cellular service standards. Wireless connectivity (or wireless interface) 1674 refers to wireless connectivity that is not cellular, and can include personal area networks (such as Bluetooth, Near Field, etc.), local area networks (such as Wi-Fi), and/or wide area networks (such as WiMax), or other wireless communication.

[0064] In some embodiments, computing device 1600 comprises peripheral connections 1680. Peripheral connections 1680 include hardware interfaces and connectors, as well as

software components (e.g., drivers, protocol stacks) to make peripheral connections. It will be understood that the computing device 1600 could both be a peripheral device ("to" 1682) to other computing devices, as well as have peripheral devices ("from" 1684) connected to it. The computing device 1600 commonly has a "docking" connector to connect to other computing devices for purposes such as managing (e.g., downloading and/or uploading, changing, synchronizing) content on computing device 1600. Additionally, a docking connector can allow computing device 1600 to connect to certain peripherals that allow the computing device 1600 to control content output, for example, to audiovisual or other systems.

[0065] In addition to a proprietary docking connector or other proprietary connection hardware, the computing device 1600 can make peripheral connections 1680 via common or standards-based connectors. Common types can include a Universal Serial Bus (USB) connector (which can include any of a number of different hardware interfaces), DisplayPort including MiniDisplayPort (MDP), High Definition Multimedia Interface (HDMI), Firewire, or other types.

[0066] Reference in the specification to "an embodiment," "one embodiment," "some embodiments," or "other embodiments" means that a particular feature, structure, or characteristic described in connection with the embodiments is included in at least some embodiments, but not necessarily all embodiments. The various appearances of "an embodiment," "one embodiment," or "some embodiments" are not necessarily all referring to the same embodiments. If the specification states a component, feature, structure, or characteristic "may," "might," or "could" be included, that particular component, feature, structure, or characteristic is not required to be included. If the specification or claim refers to "a" or "an" element, that does not mean there is only one of the elements. If the specification or claims refer to "an additional" element, that does not preclude there being more than one of the additional element.

[0067] Furthermore, the particular features, structures, functions, or characteristics may be combined in any suitable manner in one or more embodiments. For example, a first embodiment may be combined with a second embodiment anywhere the particular features, structures, functions, or characteristics associated with the two embodiments are not mutually exclusive.

[0068] While the disclosure has been described in conjunction with specific embodiments thereof, many alternatives, modifications and variations of such embodiments will be apparent to those of ordinary skill in the art in light of the foregoing description. The embodiments of the disclosure are intended to embrace all such alternatives, modifications, and variations as to fall within the broad scope of the appended claims.

[0069] In addition, well known power/ground connections to integrated circuit (IC) chips and other components may or may not be shown within the presented figures, for simplicity of illustration and discussion, and so as not to obscure the disclosure. Further, arrangements may be shown in block diagram form in order to avoid obscuring the disclosure, and also in view of the fact that specifics with respect to implementation of such block diagram arrangements are highly dependent upon the platform within which the present disclosure is to be implemented (i.e., such specifics should be well within purview of one skilled in the art). Where specific details (e.g., circuits) are set forth in order to describe example embodiments of the disclosure, it should be apparent to one skilled in the art that the disclosure can be practiced without, or with variation of, these specific details. The description is thus to be regarded as illustrative instead of limiting.

[0070] The following examples pertain to further embodiments. Specifics in the examples may be used anywhere in one or more embodiments. All optional features of the apparatus described herein may also be implemented with respect to a method or process.

[0071] For example, an apparatus is provided which comprises: a metal region having an ordered crystalline structure; and a barrier layer adjacent to the metal region, the barrier layer comprising Zinc. In some embodiments, the metal region comprises a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. In some embodiments, the metal region comprises mostly one of Cu or Ag with traces of Zn.

[0072] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, wherein at least one of the processor or memory includes an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[0073] In another example, an apparatus is provided which comprises: a metal region having an ordered crystalline structure, the metal region having traces of zinc; a crystallinity templating layer adjacent to the metal region; and a barrier layer adjacent to the crystallinity

templating layer, the barrier layer comprising zinc. In some embodiments, a crystalline axis of a metal of the metal region is aligned with the crystallinity of the templating layer. In some embodiments, the metal region and the crystallinity templating layer together form at least one of: a via; an interconnect; or a transistor gate. In some embodiments, the crystallinity templating layer is adjacent to three sides of the metal region. In some embodiments, the crystallinity templating layer is adjacent to four sides of the metal region. In some embodiments, the crystallinity templating layer is adjacent to one side of the metal region. In some embodiments, the apparatus comprises a region of MgO adjacent to the barrier layer. In some embodiments, the crystallinity templating layer has an unordered structure. In some embodiments, the crystallinity templating layer comprises of Heusler alloy metals. In some embodiments, the Heusler alloy metals is selected from a group consisting of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa, Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, and Co_2FeGe. In some embodiments, the metal region comprises a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. In some embodiments, the metal region is formed of mostly one of Cu or Ag with traces of Zn.

[0074] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, wherein at least one of the processor or memory includes an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[0075] In another example, an apparatus is provided which comprises: a metal region having an ordered crystalline structure; a dielectric layer adjacent to the metal region; and a barrier layer adjacent to the dielectric layer, the barrier layer comprises of a material selected from a group consisting of: Zn, ZnO, and Zn_2SiO_4. In some embodiments, the dielectric layer is MgO. In some embodiments, the metal region comprises a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. In some embodiments, the metal region comprises mostly one of Cu or Ag with traces of Zn.

[0076] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, wherein at least one of the processor or memory includes an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[0077] In another example, an integrated circuit (IC) die is provided which comprises: a barrier layer comprising zinc; and an interconnect formed within the barrier layer, the interconnect comprising a crystalline metal. In some embodiments, the crystalline metal is selected from a group consisting of: Cu, Ag, and their alloys. In some embodiments, the IC comprises a crystallinity templating layer adjacent to the interconnect. In some embodiments, the crystallinity templating layer comprises Heusler alloy metals. In some embodiments, the Heusler alloy metals is selected from a group consisting of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa, Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, and Co_2FeGe. In some embodiments, the interconnect comprises material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. In some embodiments, the interconnect comprises mostly one of Cu or Ag with traces of Zn.

[0078] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, wherein at least one of the processor or memory includes an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[0079] In another example, an apparatus is provided which comprises: a first metal layer; a first crystallinity templating layer adjacent to the first metal layer; a second metal layer adjacent to the first crystallinity templating layer such that the first crystallinity templating layer is sandwiched between the first metal layer and the second metal layer; a second crystallinity templating layer adjacent to the second metal layer; and a barrier layer adjacent to the second crystallinity templating layer, the barrier layer comprises a material selected from a group consisting of: Zn, ZnO, and Zn_2SiO_4. In some embodiments, material of the first crystallinity templating layer is same as material of the second crystallinity templating layer. In some embodiments, material of the first crystallinity templating layer is different from material of the second crystallinity templating layer. In some embodiments, material for at least one of first or second crystallinity templating layers comprises Heusler alloy metals. In some embodiments, the Heusler alloy metals is at least one of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa, Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, and Co_2FeGe. In some embodiments, the first and second metals are selected from a group consisting of: Cu, Ag, and

their alloys. In some embodiments, the first and second metals comprises mostly one of Cu or Ag with traces of Zn.

[0080] In another example, a system is provided which comprises: a memory; a processor coupled to the memory, wherein at least one of the processor or memory includes an apparatus according to the apparatus described above; and a wireless interface for allowing the processor to communicate with another device.

[0081] In another example, a method is provided which comprises: depositing a metal region having an ordered crystalline structure, wherein a barrier layer is formed adjacent to the metal region, the barrier layer comprising Zinc. In some embodiments, the metal region comprises a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. In some embodiments, the metal region comprises mostly one of Cu or Ag with traces of Zn.

[0082] In another example, a method is provided which comprises: depositing a metal region having an ordered crystalline structure, the metal region having traces of zinc; and depositing a crystallinity templating layer adjacent to the metal region; and wherein a barrier layer is formed adjacent to the crystallinity templating layer, the barrier layer comprising zinc. In some embodiments, a crystalline axis of a metal of the metal region is aligned with the crystallinity of the templating layer. In some embodiments, the metal region and the crystallinity templating layer together form at least one of: a via; an interconnect; or a transistor gate. In some embodiments, the crystallinity templating layer is adjacent to three sides of the metal region. In some embodiments, the crystallinity templating layer is adjacent to four sides of the metal region. In some embodiments, the crystallinity templating layer is adjacent to one side of the metal region. In some embodiments, the method comprises depositing a region of MgO adjacent to the barrier layer. In some embodiments, the crystallinity templating layer has an unordered structure. In some embodiments, the crystallinity templating layer comprises of Heusler alloy metals. In some embodiments, the Heusler alloy metals is selected from a group consisting of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa, Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, and Co_2FeGe. In some embodiments, the metal region comprises a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn;

$Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. In some embodiments, the metal region is formed of mostly one of Cu or Ag with traces of Zn.

[0083] In another example, a method is provided which comprises: depositing a metal region having an ordered crystalline structure; depositing a dielectric layer adjacent to the metal region; and wherein a barrier layer is formed adjacent to the dielectric layer, the barrier layer comprises of a material selected from a group consisting of: Zn, ZnO, and Zn_2SiO_4. In some embodiments, the dielectric layer is MgO. In some embodiments, the metal region comprises a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$. In some embodiments, the metal region comprises mostly one of Cu or Ag with traces of Zn.

[0084] An abstract is provided that will allow the reader to ascertain the nature and gist of the technical disclosure. The abstract is submitted with the understanding that it will not be used to limit the scope or meaning of the claims. The following claims are hereby incorporated into the detailed description, with each claim standing on its own as a separate embodiment.

CLAIMS

We claim:

1. An apparatus comprising:
   a metal region having an ordered crystalline structure; and
   a barrier layer adjacent to the metal region, the barrier layer comprising Zinc.

2. The apparatus of claim 1, wherein the metal region comprises a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$.

3. The apparatus of claim 1, wherein the metal region comprises mostly one of Cu or Ag with traces of Zn.

4. An apparatus comprising:
   a metal region having an ordered crystalline structure, the metal region having traces of zinc;
   a crystallinity templating layer adjacent to the metal region; and
   a barrier layer adjacent to the crystallinity templating layer, the barrier layer comprising zinc.

5. The apparatus of claim 4, wherein a crystalline axis of a metal of the metal region is aligned with the crystallinity of the templating layer.

6. The apparatus of claim 4, wherein the metal region and the crystallinity templating layer together form at least one of: a via; an interconnect; or a transistor gate.

7. The apparatus of claim 4, wherein the crystallinity templating layer is adjacent to three sides of the metal region.

8. The apparatus of claim 4, wherein the crystallinity templating layer is adjacent to four sides of the metal region.

9. The apparatus of claim 4, wherein the crystallinity templating layer is adjacent to one side of the metal region.

10. The apparatus of claim 4 comprises a region of MgO adjacent to the barrier layer.

11. The apparatus of claim 4, wherein the crystallinity templating layer has an unordered structure.

12. The apparatus of claim 4, wherein the crystallinity templating layer comprises of Heusler alloy metals.

13. The apparatus of claim 12, wherein the Heusler alloy metals is selected from a group consisting of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa, Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, and Co_2FeGe.

14. The apparatus of claim 4, wherein the metal region comprises a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$.

15. The apparatus of claim 4, wherein the metal region is formed of mostly one of Cu or Ag with traces of Zn.

16. An apparatus comprising:

a metal region having an ordered crystalline structure;

a dielectric layer adjacent to the metal region; and

a barrier layer adjacent to the dielectric layer, the barrier layer comprises of a material selected from a group consisting of: Zn, ZnO, and Zn_2SiO_4.

17. The apparatus of claim 16, wherein the dielectric layer is MgO.

18. The apparatus of claim 16, wherein the metal region comprises a material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$.

19. The apparatus of claim 16, wherein the metal region comprises mostly one of Cu or Ag with traces of Zn.

20. An integrated circuit (IC) die comprising:

a barrier layer comprising zinc; and

an interconnect formed within the barrier layer, the interconnect comprising a crystalline metal.

21. The IC die of claim 20, wherein the crystalline metal is selected from a group consisting of: Cu, Ag, and their alloys.

22. The IC of claim 20 comprising a crystallinity templating layer adjacent to the interconnect.

23. The IC of claim 22, wherein the crystallinity templating layer comprises Heusler alloy metals.

24. The IC of claim 23, wherein the Heusler alloy metals is selected from a group consisting of: Cu_2MnAl, Cu_2MnIn, Cu_2MnSn, Ni_2MnAl, Ni_2MnIn, Ni_2MnSn, Ni_2MnSb, Ni_2MnGa, Co_2MnAl, Co_2MnSi, Co_2MnGa, Co_2MnGe, Pd_2MnAl, Pd_2MnIn, Pd_2MnSn, Pd_2MnSb, Co_2FeSi, Co_2FeAl, Fe_2VAl, Mn_2VGa, and Co_2FeGe.

25. The IC of claim 20, wherein the interconnect comprises material selected from a group consisting of: CuZn; Cu_3Zn; CuZn; AgZn; Ag_3Zn; $Cu_{0.5}Ag_{0.5}An$; and $Cu_{1.5}Ag_{1.5}Zn$, or wherein the interconnect comprises mostly one of Cu or Ag with traces of Zn.

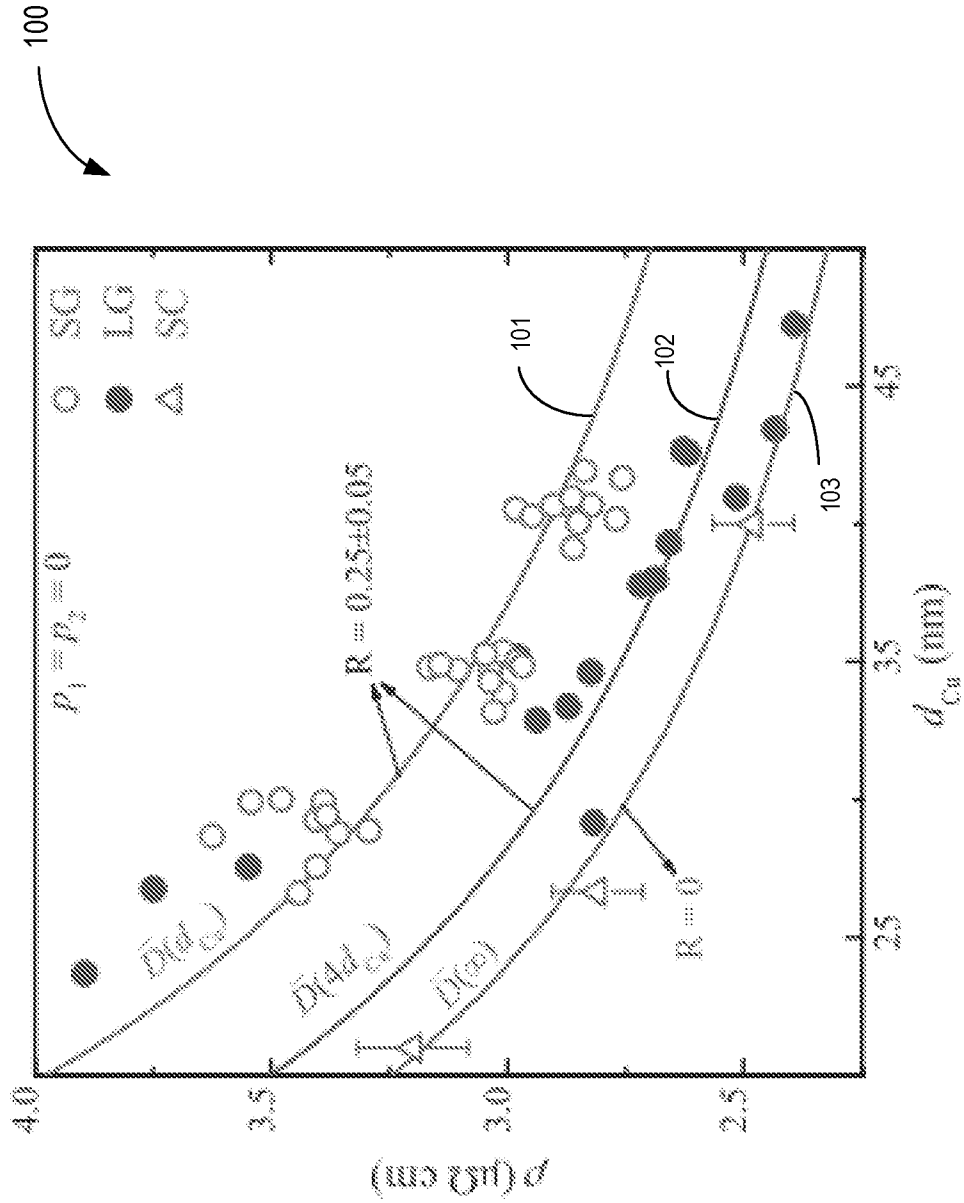
100
SQ
LQ
SQ
$\rho_1 = \rho_2 = 0$
R = 0.25±0.05
R = 0
101
102
103
$D(d_{Cu})$
$D(d_{Cu})$
$D(\rho)$
ρ (μΩ cm)
4.0
3.5
3.0
2.5
2.5
3.5
4.5
d_{Cu} (nm)

Fig. 1

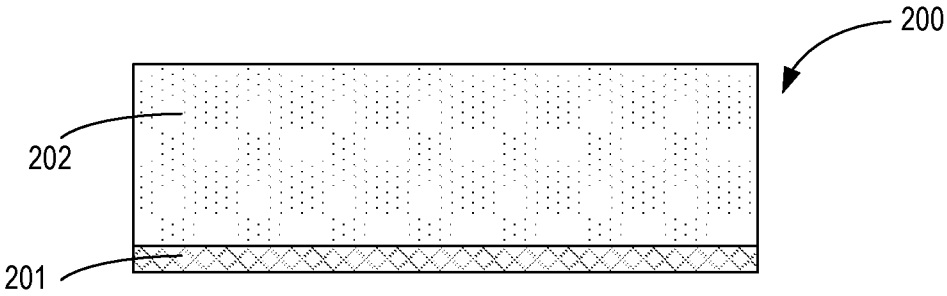

Fig. 2A

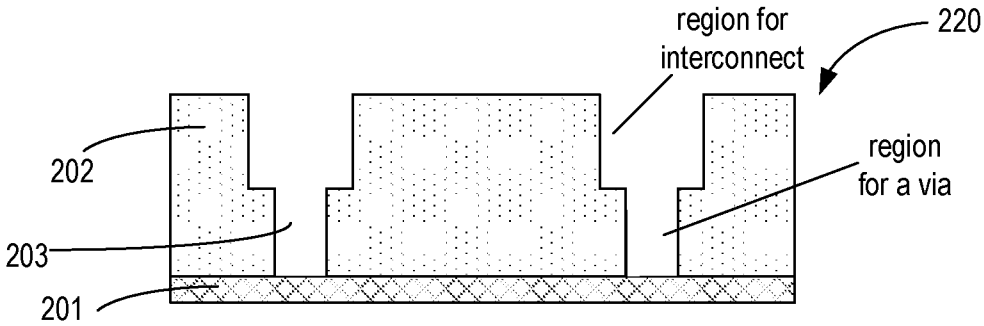

Fig. 2B

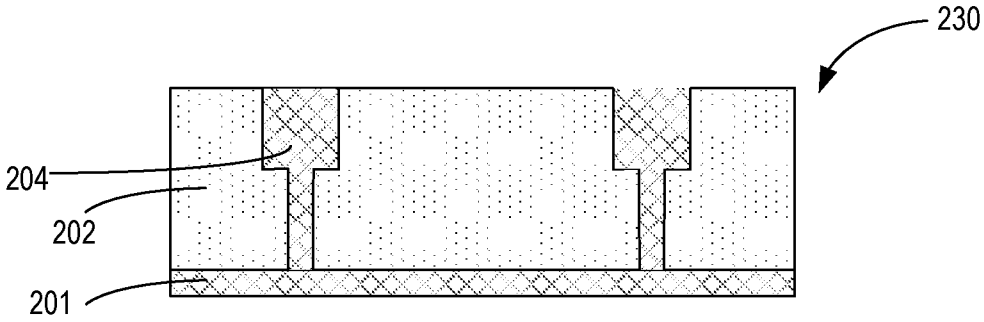

Fig. 2C

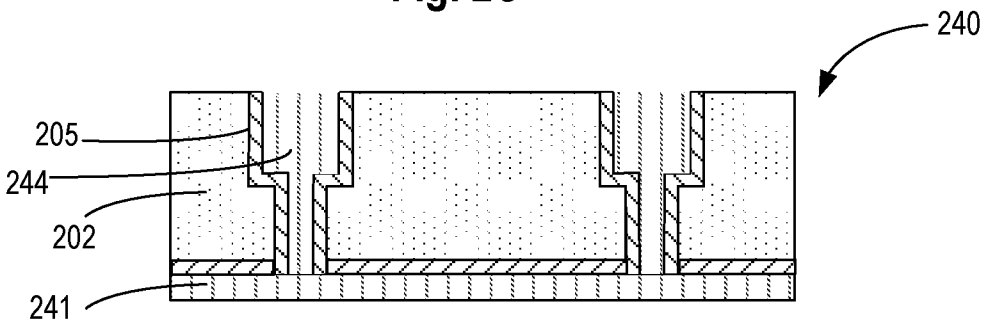

Fig. 2D

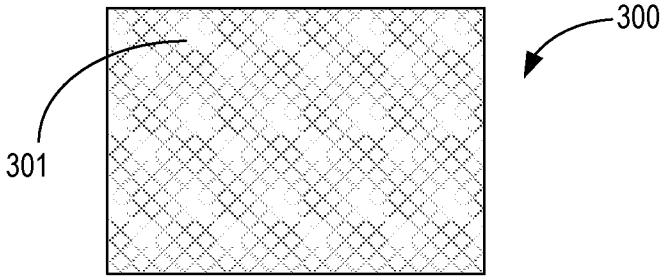

Fig. 3A

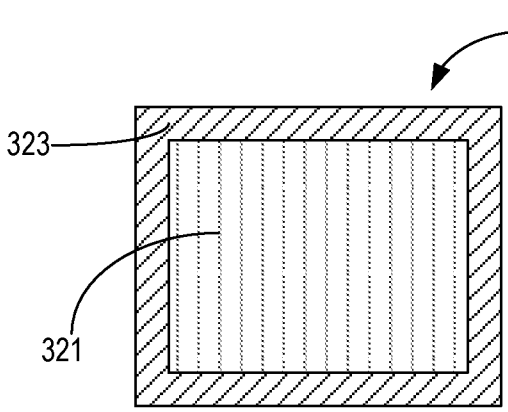

Fig. 3B

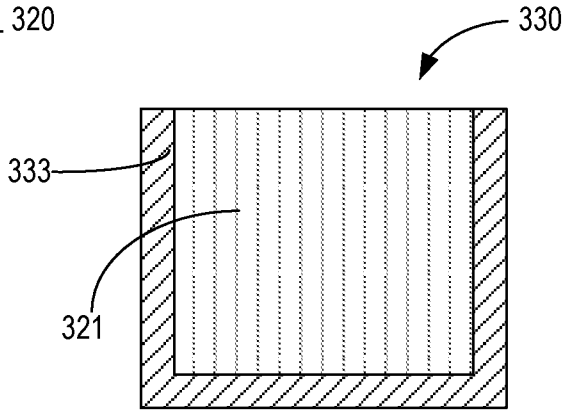

Fig. 3C

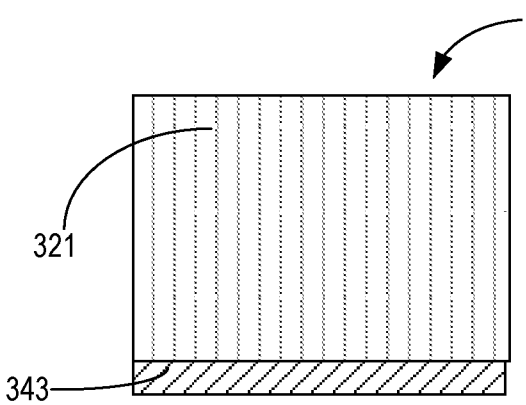

Fig. 3D

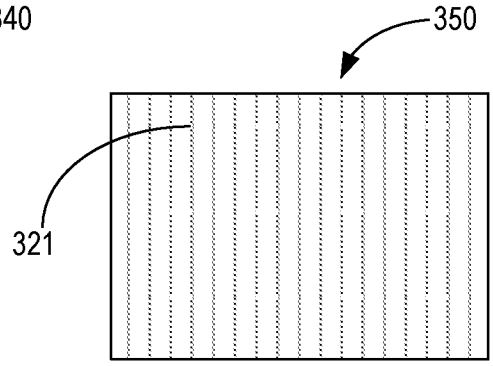

Fig. 3E

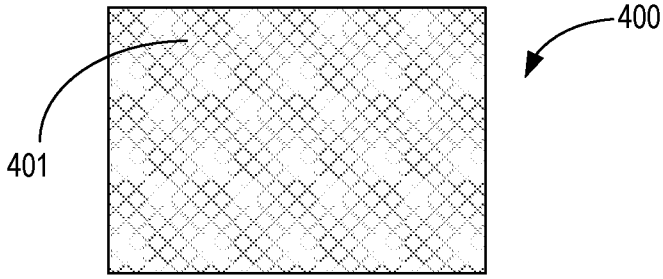

Fig. 4A

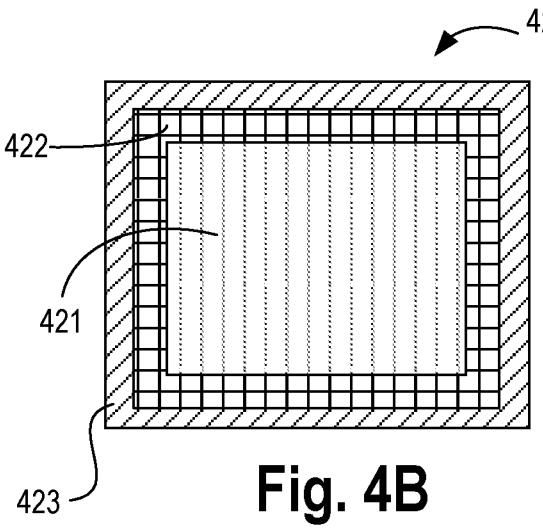

Fig. 4B

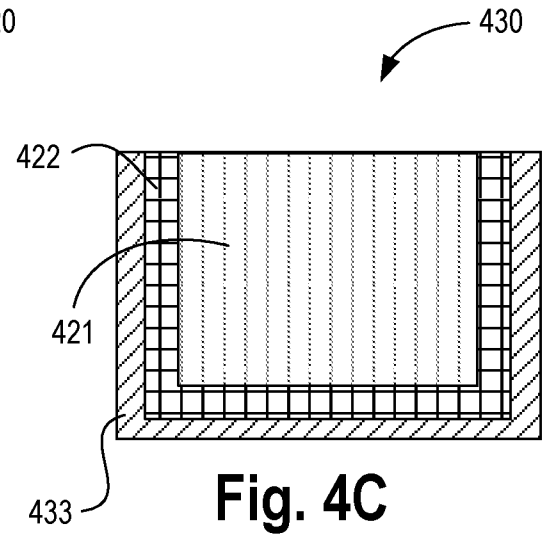

Fig. 4C

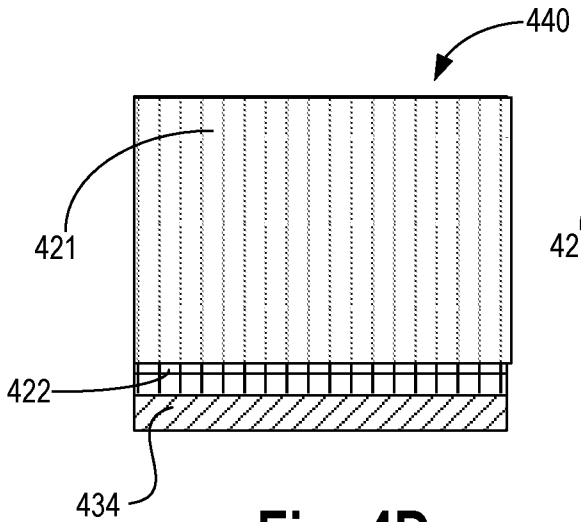

Fig. 4D

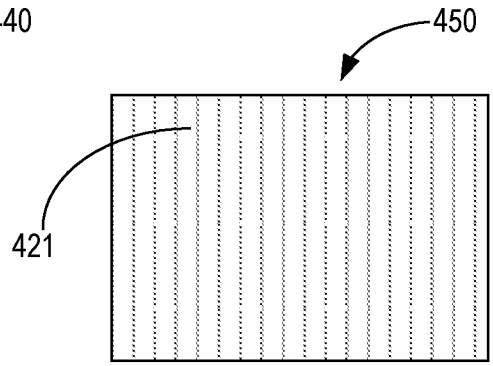

Fig. 4E

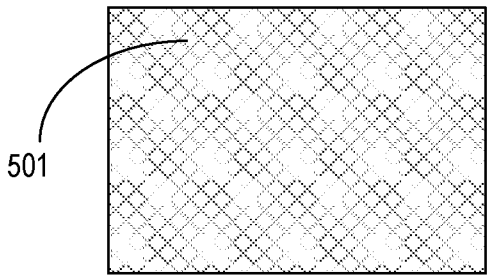

Fig. 5A

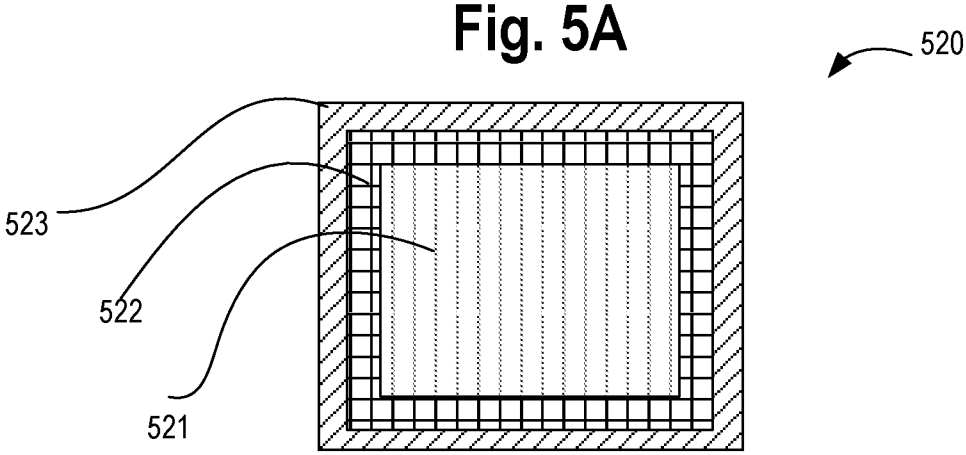

Fig. 5B

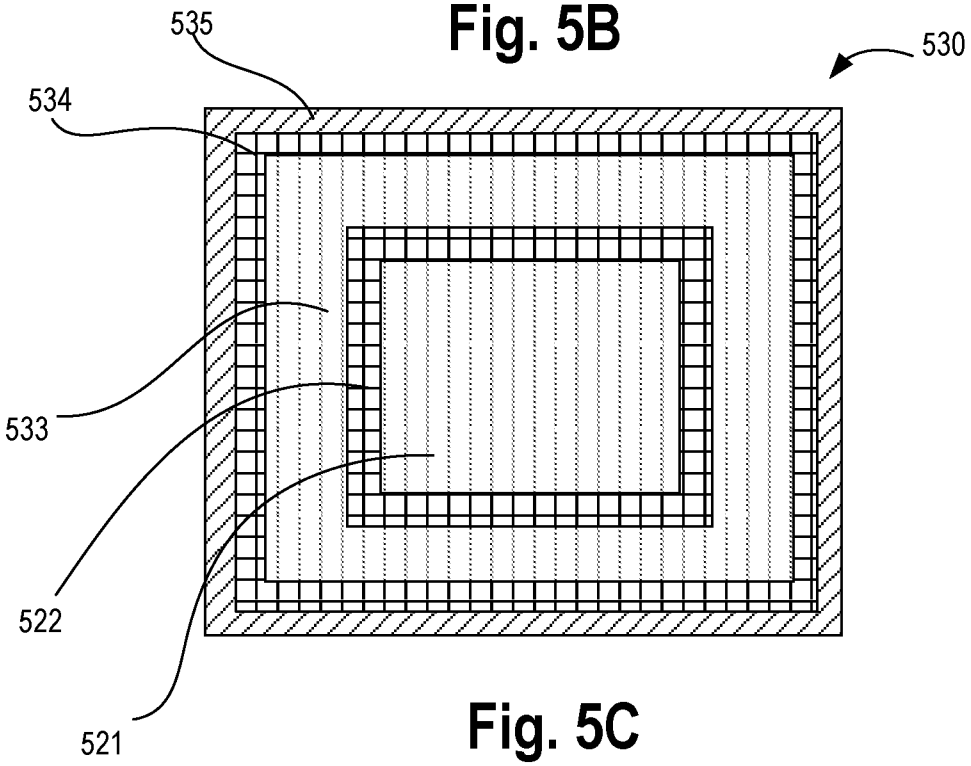

Fig. 5C

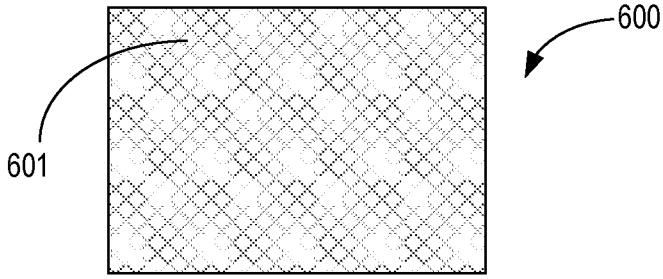

Fig. 6A

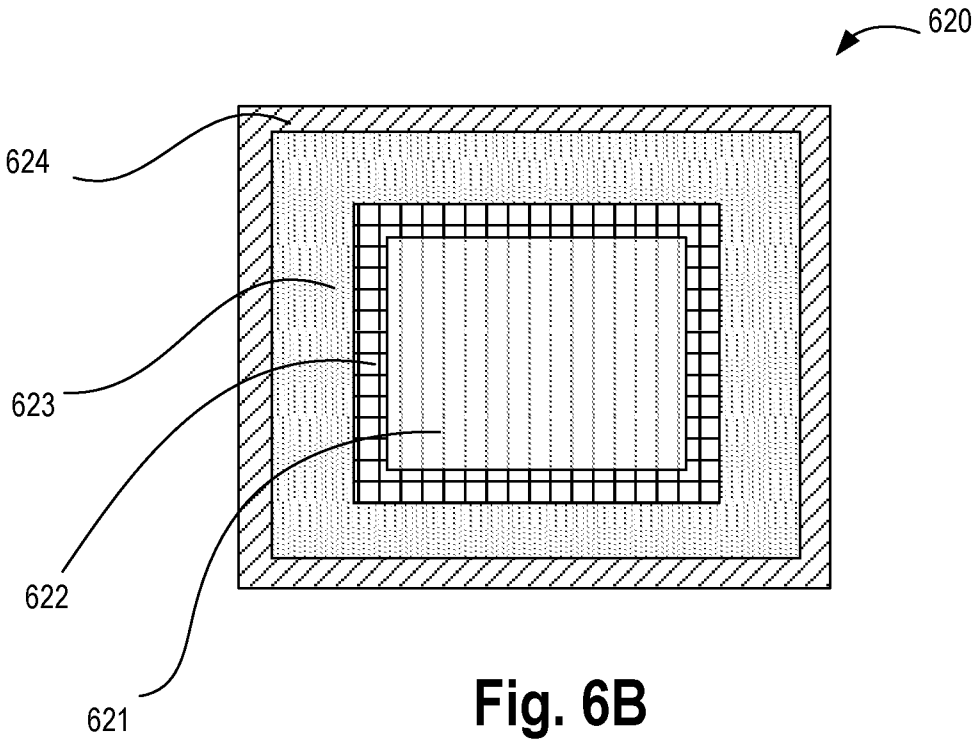

Fig. 6B

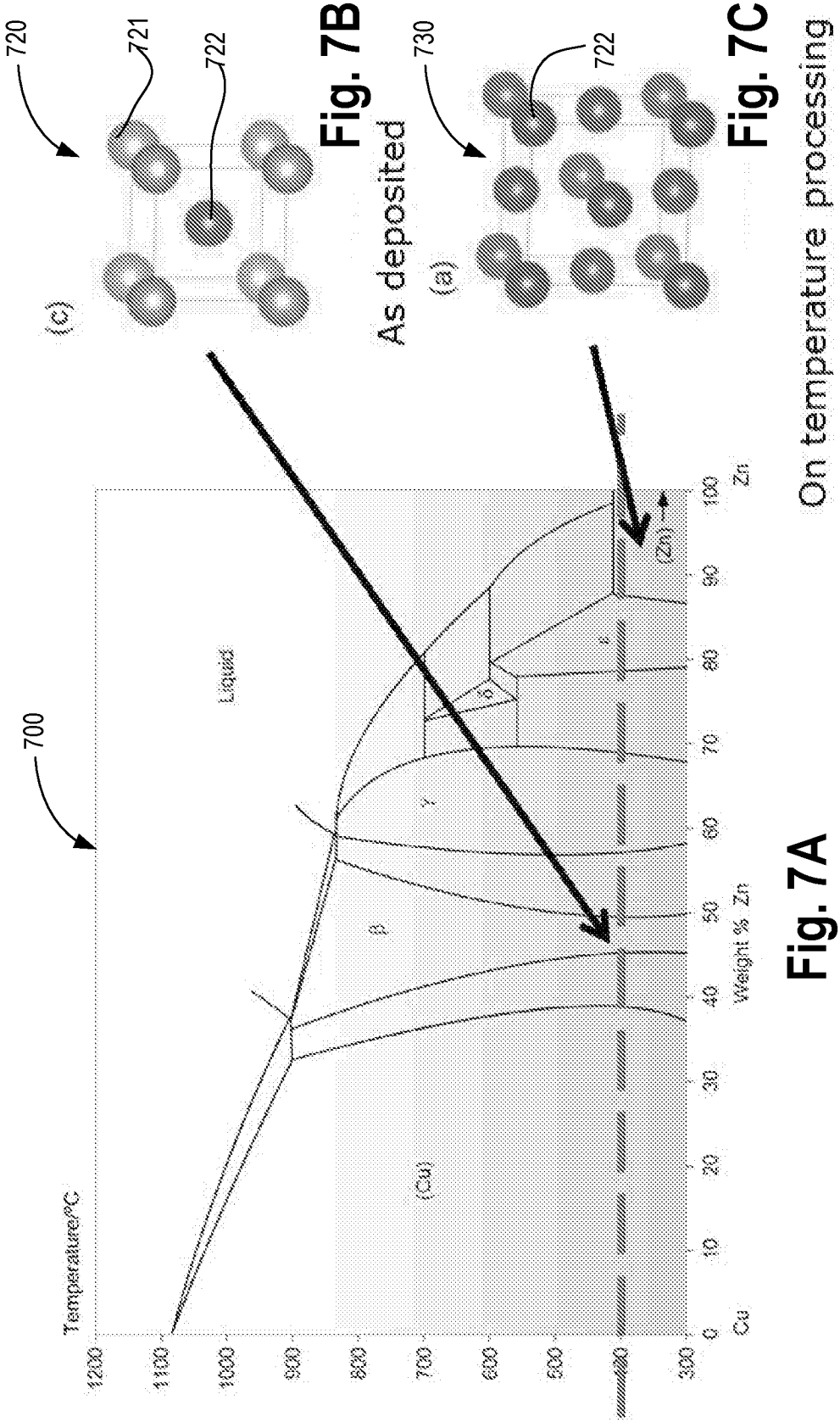

Fig. 7A

Fig. 7B

Fig. 7C

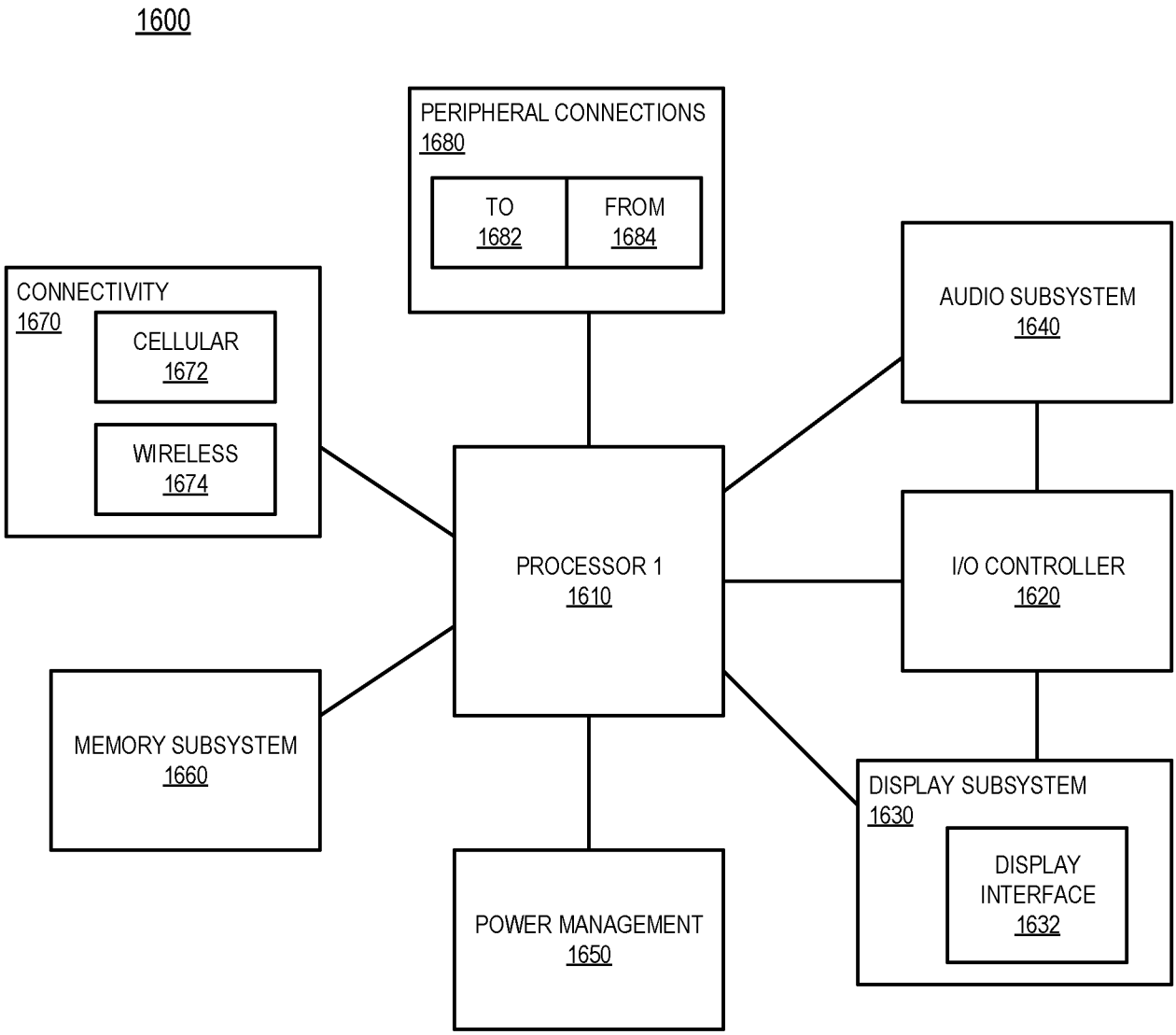
1600
PERIPHERAL CONNECTIONS
1680
TO
1682
FROM
1684
CONNECTIVITY
1670
CELLULAR
1672
WIRELESS
1674
AUDIO SUBSYSTEM
1640
PROCESSOR 1
1610
I/O CONTROLLER
1620
MEMORY SUBSYSTEM
1660
DISPLAY SUBSYSTEM
1630
DISPLAY
INTERFACE
1632
POWER MANAGEMENT
1650

Fig. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2016/039903

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/28(2006.01)i, H01L 21/285(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/28; H01L 21/768; G02F 1/136; H01L 23/532; H01L 21/3205; H01L 21/285

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: metal interconnect, copper, zinc, crystalline, resistivity

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014-0291847 A1 (GLOBALFOUNDRIES INC.) 02 October 2014 See paragraphs [0029]-[0031] and figures 2C, 2D.	1-25
A	KR 10-2016-0056463 A (SAMSUNG DISPLAY CO., LTD.) 20 May 2016 See paragraphs [0037]-[0049] and figures 1a, 1b.	1-25
A	US 2014-0127898 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 08 May 2014 See paragraphs [0017]-[0029] and figures 2-11.	1-25
A	JP 2004-047846 A (OKI ELECTRIC IND. CO., LTD.) 12 February 2004 See paragraphs [0016]-[0021] and figures 1-5.	1-25
A	US 2014-0106562 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 17 April 2014 See the whole document.	1-25

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
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"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 April 2017 (28.04.2017)	**28 April 2017 (28.04.2017)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2016/039903

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		US 8653663 B2	18/02/2014
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