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(54) **MULTI-PHASE DC-DC CONVERTER USING AUXILIARY RESISTOR NETWORK TO FEED BACK MULTIPLE SINGLE-ENDED SENSED CURRENTS TO SUPERVISORY CONTROLLER FOR BALANCED CURRENT-SHARING AMONG PLURAL CHANNELS**

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G05F 1/56 (2006.01)

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(58) **Field of Classification Search** **323/222, 323/223, 225, 265, 268, 271, 272, 282, 285; 363/65, 71**

See application file for complete search history.

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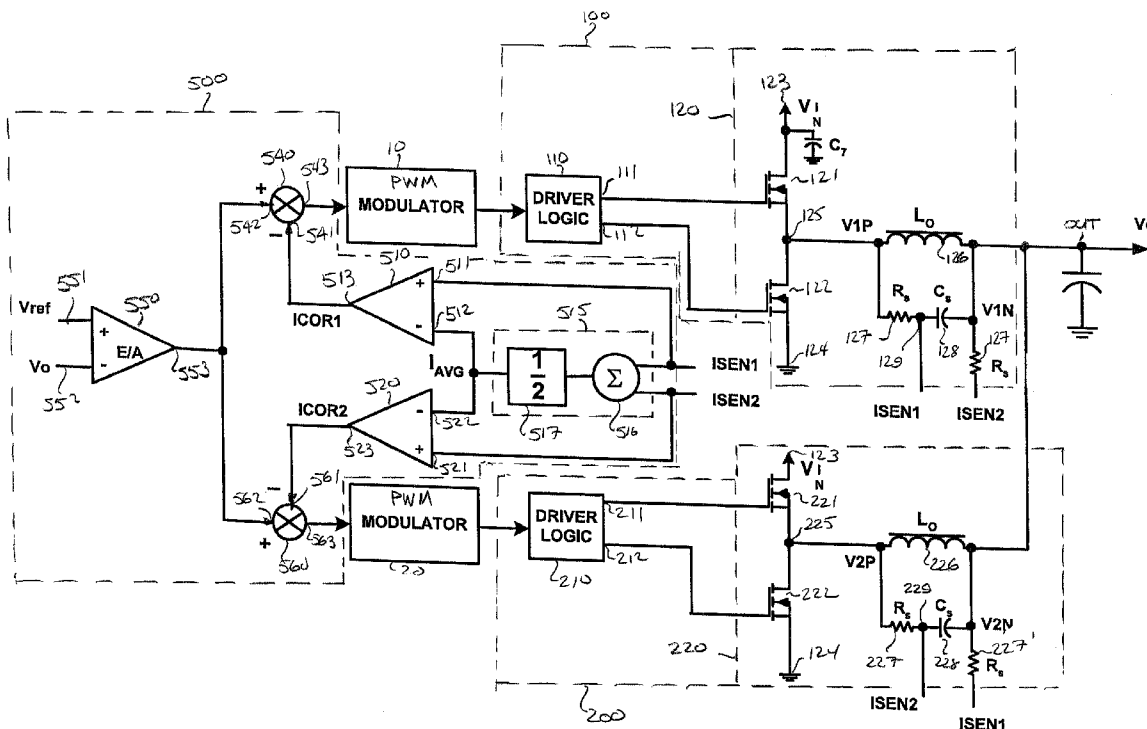
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(57) **ABSTRACT**

A multi-phase DC-DC converter incorporates auxiliary resistor networks to feed back to the converter's supervisory controller voltages representative of secondary sensed currents associated with primary currents sensed relative to the common nodes of the respective phases, and derived from the output nodes for each phase. The auxiliary resistor network-coupling of these secondary sensed currents enables the controller to more completely take into account the influence of the currents of each channel on every other channel, whereby phase-balanced control of all converter channels is achieved, irrespective of symmetry of the integrated circuit layout of the different phases of the converter.

20 Claims, 4 Drawing Sheets



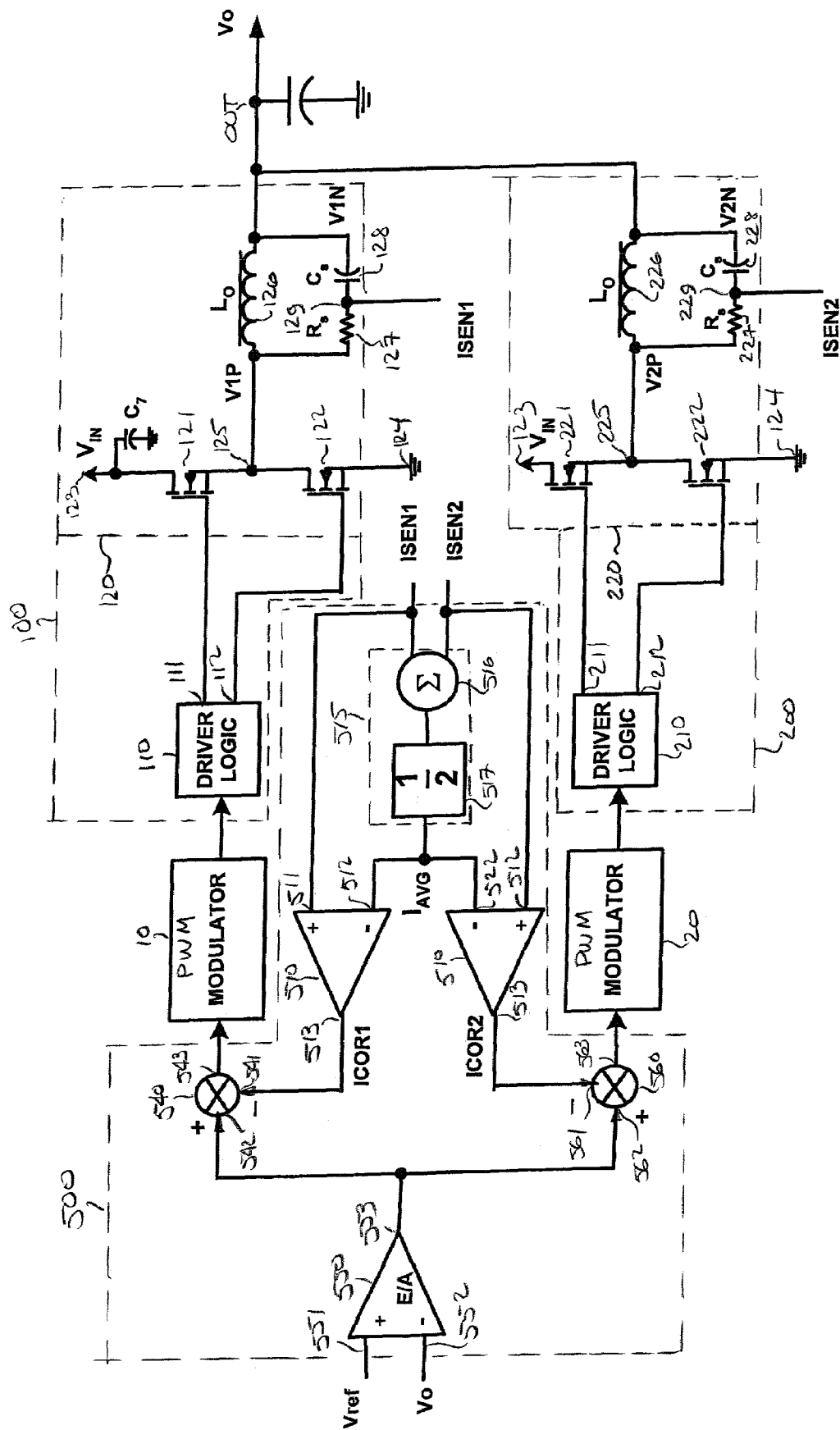


FIGURE 1 (PRIOR ART)

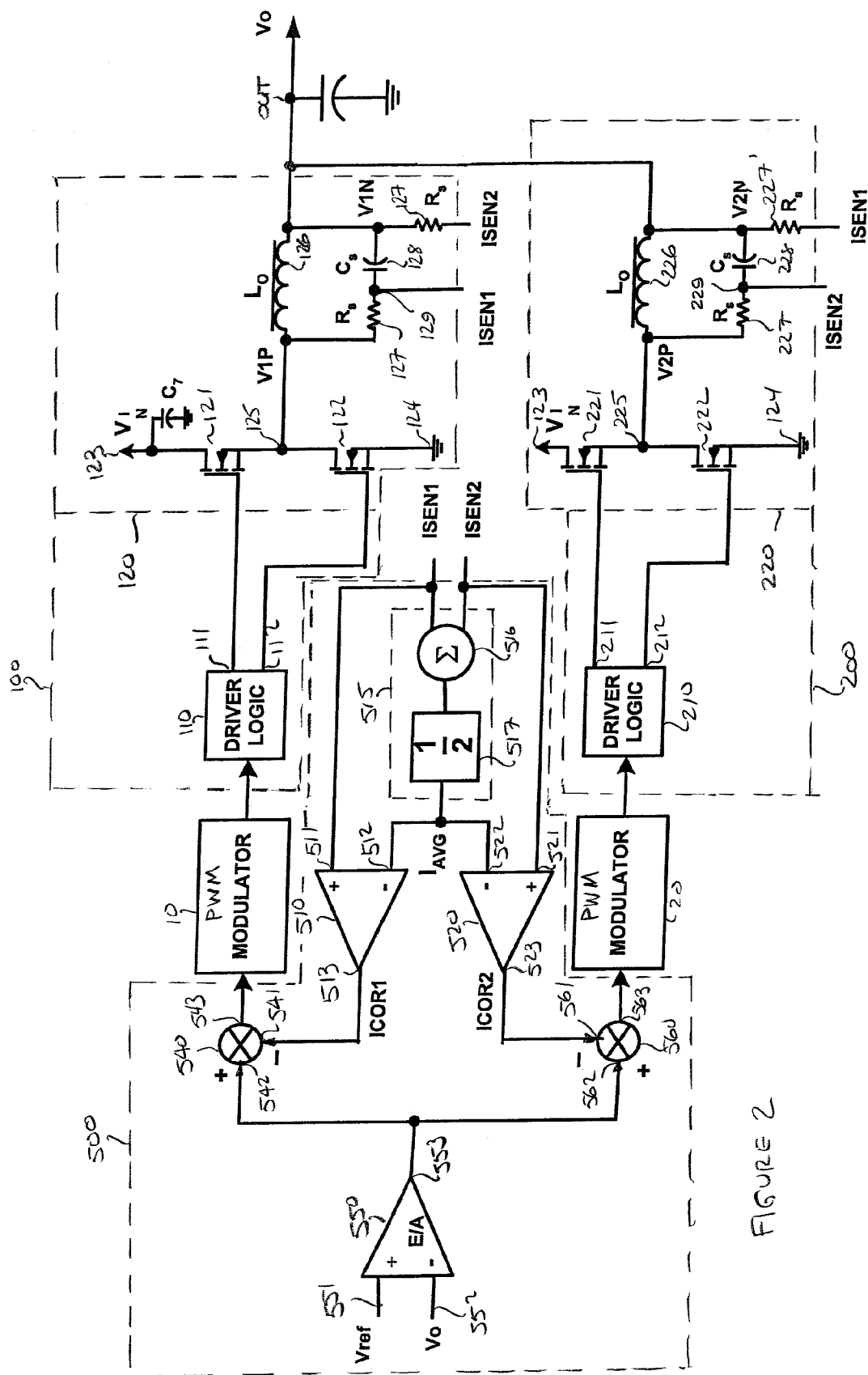
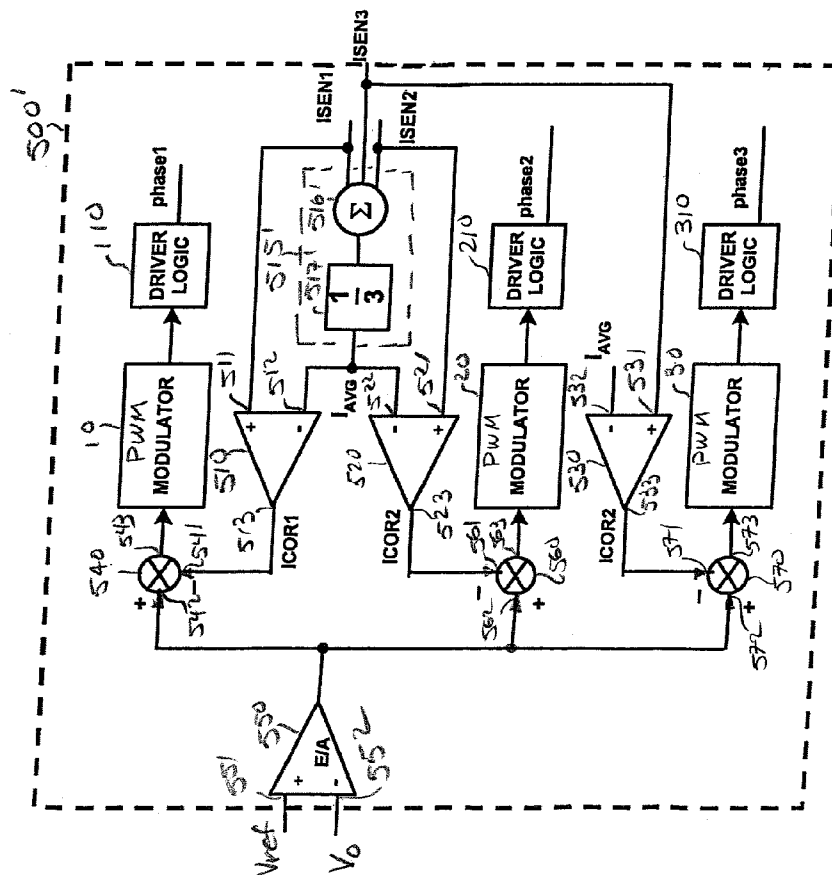
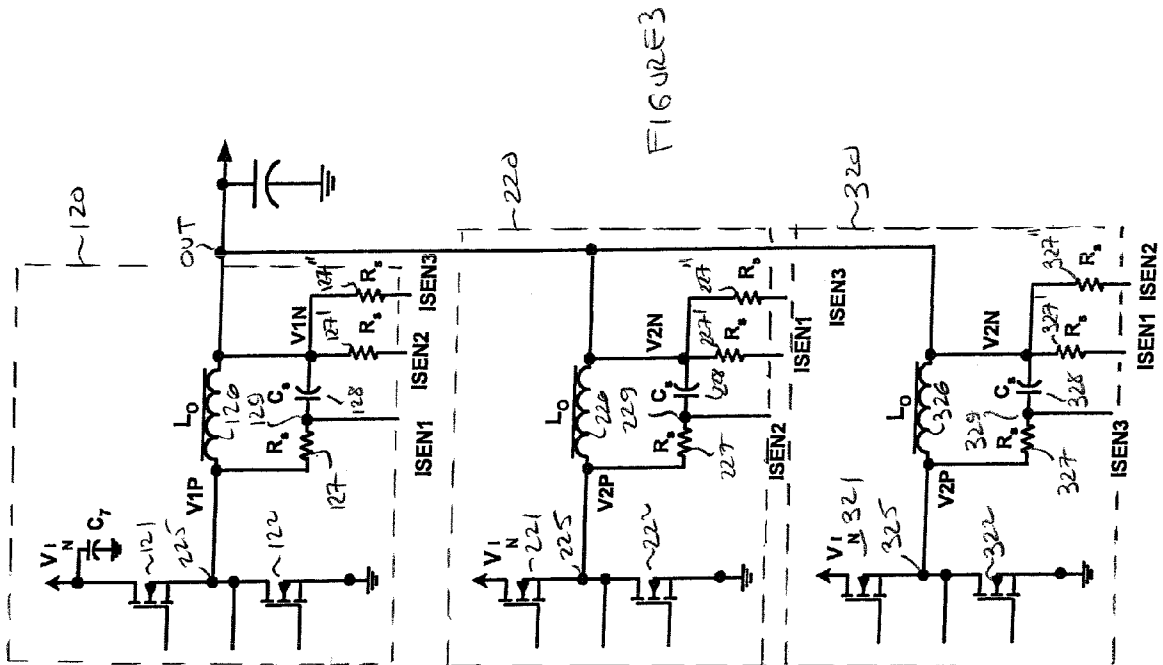


FIGURE 2



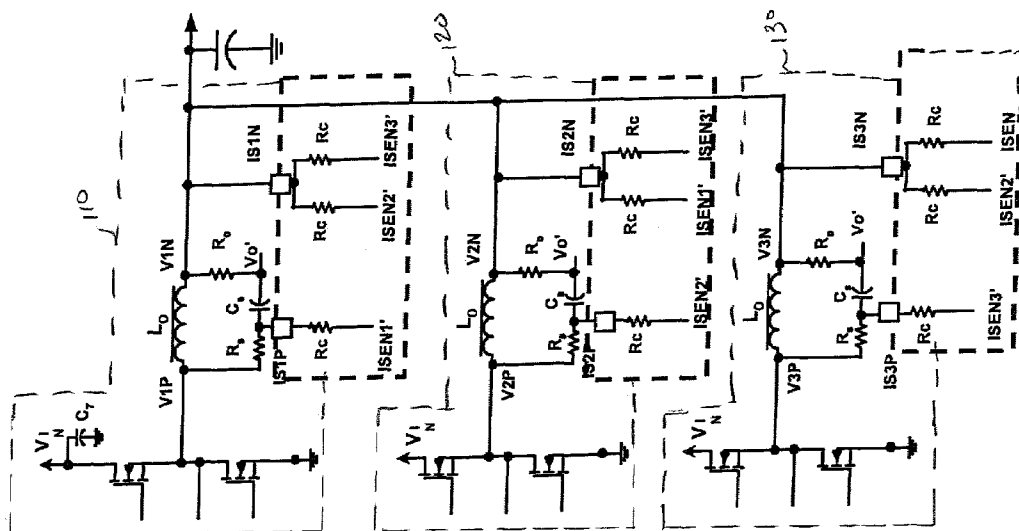


FIGURE 5

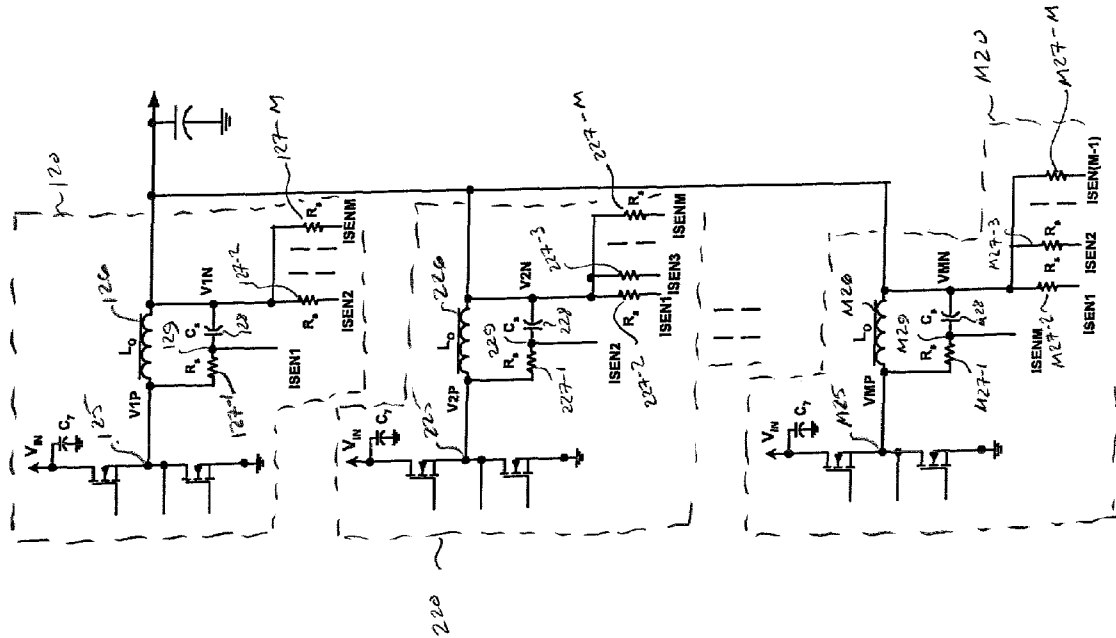


FIGURE 6

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MULTI-PHASE DC-DC CONVERTER USING AUXILIARY RESISTOR NETWORK TO FEED BACK MULTIPLE SINGLE-ENDED SENSED CURRENTS TO SUPERVISORY CONTROLLER FOR BALANCED CURRENT-SHARING AMONG PLURAL CHANNELS

FIELD OF THE INVENTION

The present invention relates in general to DC-DC converters and subsystems thereof, and is particularly directed to a new and improved multi-phase DC-DC converter of the type that employs single-ended current sensing for current-sharing control of the operation of the respective power channels/phases of the DC-DC converter. In addition to coupling primary sensed currents sensed relative to the phase nodes of power stages of the respective phases to differential measurement and control circuitry of a supervisory controller, additional, secondary sensed currents, associated with the primary currents, are fed back from output nodes of all channels by way of reduced circuitry complexity auxiliary resistor networks to the supervisory controller. This enables the controller to more completely take into account the influence of the currents of each channel on every other channel, whereby phase-balanced control of all converter channels is achieved, irrespective of symmetry of the integrated circuit layout of the different phases of the converter.

BACKGROUND OF THE INVENTION

A multi-phase DC-DC converter uses a supervisory multi-channel controller to regulate the power delivered by multiple phases or power channels of the converter to an output node feeding a load. As a non-limiting example, FIG. 1 diagrammatically illustrates a conventional dual-phase DC-DC converter, which contains two power channels 100 and 200, that drive an output node OUT with an output voltage V_o . The output voltage is regulated by a supervisory controller 500, which monitors output currents ISEN1 and ISEN2 sensed at current sensing ports coupled to phase nodes 125 and 225 of respective power switching stages 120 and 220 of the two channels, and uses this current information to precisely control the pulse widths of associated streams of pulse width modulation (PWM) waveforms applied by respective PWM generators 10 and 20 to drivers 110 and 210 that control switching times of switching devices (e.g., MOSFETs) of the output power switching stages 120 and 220. The PWM waveforms are sequenced and timed such that the interval between rising edges (or in some implementations, falling edges) thereof is constant, for the purpose of equalizing the currents delivered by the two power channels. (The sum of the current measurements may also be also used to precisely regulate the output resistance in a method commonly known as droop regulation or load-line regulation.)

More particularly, in the two-phase DC-DC converter architecture of FIG. 1, the first power switching stage 120 is shown as including an upper power semiconductor switch (e.g., MOSFET) 121, and a lower power semiconductor switch (e.g., MOSFET) 122 having the source-drain paths thereof coupled in series between an input voltage (V_{in}) supply terminal 123 and a reference voltage (ground) terminal 124. The control or gate input of the upper MOSFET switch 121 is coupled to a first output 111 of the first channel driver 110, while the control or gate input of lower MOSFET

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switch 122 is coupled to a second output 112 of the first channel driver. The common or phase node 125 between the upper and lower MOSFET switches 121 and 122 provides a voltage V_{1P} , and is coupled by way of an output inductor (Lo) 126 to the output node OUT, to which a first phase/channel output voltage V_{1N} from the first power channel is applied. An output current sense resistor 127 (having a resistor value R_s) is coupled between the phase node 125 and a current sense node 129 by way of which a measure ISEN1 of the output current of the first channel is derived for application to the controller 500. A capacitor (Cs) 128 is coupled between current sense node 129 and the output node OUT.

In a like manner, the second power switching stage 220 contains an upper power semiconductor switch (MOSFET) 221, and a lower power semiconductor switch (MOSFET) 222 having the source-drain paths thereof coupled in series between the input voltage (V_{in}) supply terminal 123 and the reference voltage (ground) terminal 124. The control or gate input of upper MOSFET switch 221 is coupled to a first output 211 of the second channel driver 210, while the control or gate input of lower MOSFET switch 222 is coupled to a second output 212 of the second channel driver. The common or phase node 225 between the upper and lower MOSFET switches 221 and 222, which provides a voltage V_{2P} , is coupled by way of an output inductor (Lo) 226 to the output node OUT, to which a second phase/channel output voltage V_{2N} from the second power channel is applied. An output current sense resistor 227 (having a resistor value R_s) is coupled between the phase node 225 and a current sense node 229 by way of which a measure ISEN2 of the output current of the second channel is derived for application to the controller 500. A capacitor (Cs) 228 is coupled between current sense node 229 and the output node OUT.

To control the operation of the first power channel 100, controller 500 includes a first difference amplifier 510, which has a first, non-inverting (+) input 511 coupled to the first channel's current sense node 129, so as to receive a measure of the first sensed current ISEN1, and a second, inverting input (-) 512 coupled to receive a voltage representative of the average I_{AVG} of the first and second currents ISEN1 and ISEN2 as produced by an averaging circuit 515. Averaging circuit 515 includes a summing unit 516 coupled to the two current sensed nodes 129 and 229 from which the sensed currents ISEN1 and ISEN2 are supplied. The output of summing unit 516 is coupled to a divide-by-two divider 517, which outputs a voltage representative of the average current value I_{AVG} of the two sense currents ISEN1 and ISEN2. The output 513 of difference amplifier 510 is used to provide a first correction voltage ICOR1 representative of the difference between the first channel's sensed current ISEN1 and the average I_{AVG} of the two sensed currents.

For controlling the operation of the second power channel 200, controller 500 includes a second difference amplifier 520, which has a first, non-inverting (+) input 521 thereof coupled to the second channel's current sense node 229, so as to receive a measure of the second sensed current ISEN2, and a second, inverting input (-) 522 coupled to receive the voltage representative of the average output I_{AVG} of averaging circuit 515. The output 523 of difference amplifier 520 is used to provide a second correction voltage ICOR2 representative of the difference between the second channel's sensed current ISEN2 and the average I_{AVG} of the two sensed currents.

The first correction voltage ICOR1 is coupled to a first (-) input 541 of a subtraction unit 540, which has a second (+)

input 542 coupled to receive an error voltage generated at the output 553 of an error amplifier 550. Error amplifier 550 generates an error voltage representative of the difference between a reference voltage Vref coupled to a first, non-inverting (+) input 551 thereof, and the output voltage Vo that is fed back from the output node OUT to a second, inverting (-) input 551 thereof, and couples this error voltage to second (+) inputs 542 and 562 of respective subtraction units 540 and 560. Subtraction unit 560 has a first (-) input coupled to receive the second correction voltage ICOR2 at the output 523 of difference amplifier 520. The output 543 of subtraction unit 540 serves as the control input for the PWM modulator 10 of the first power channel 100, while the output 563 of subtraction unit 560 serves as the control input for the PWM modulator 20 of the second power channel 200.

In operation, any difference between the output voltage Vo sensed at the output terminal OUT and the reference voltage Vref produces an error voltage at the output of error amplifier 550. This error voltage constitutes a principal control metric for adjusting the PWM waveforms produced by PWM modulators 10 and 20 of the respective power channels/phases 100 and 200. Since it monitors the currents ISEN1 and ISEN2 sensed at the outputs of the two power channels 100 and 200, controller 500 is able to determine any imbalance in these currents for the two channels, by comparing each channel's sensed current with the average value I_{AVG} of the sensed currents for both phases. Any difference between a sensed current for a respective channel i and the average I_{AVG} of the sensed currents for the two channels results in a correction voltage ICORi that is used to offset or modify the error voltage produced by error amplifier 550, and thereby the pulse widths of the PWM waveforms generated by the PWM generators 10 and 20, so as to equalize the currents delivered by the two power channels.

Now although the output current monitoring and imbalance correction mechanism employed in the converter architecture of FIG. 1 is intended to effectively equalize the currents delivered by the two power channels, it can do so provided that the circuitry layouts of the respective power channels of the converter are symmetric with respect to one another. Otherwise—namely, in the case of a non-symmetric circuit layout—the output voltage V1N for the first channel/phase will not equal the output voltage V2N for the second channel/phase, resulting in a current imbalance between the different channels, and preventing the controller from equalizing the currents in the two power channels.

This lack of symmetry in the power channel circuit layouts of a multi-phase DC-DC converter—which is not uncommon as the number of power channels increases, and can be expected to be the case where the converter employs an odd number of channels/phases—is due principally to the fact that the distances from the controller to the most remote power channels increase substantially as the number of phases/channels increases. This makes it very difficult for the designer to preserve signal integrity of the current-sense lines, due to the fact that these lines typically traverse long distances through a noisy environment from the output current monitoring nodes and the controller, and the fact that the signals transmitted on the current-sense lines are voltage signals proportional to current, and voltage signals are prone to corruption from capacitively-coupled noise.

SUMMARY OF THE INVENTION

In accordance with the present invention, the above-described circuitry layout asymmetry-based current imbal-

ance problem in a multi-phase DC-DC converter is effectively obviated by a new and improved multi- or M-phase DC-DC converter architecture, where M corresponds to two or more phases, that incorporates auxiliary resistor networks to feed back voltages representative of secondary sensed currents derived from the output nodes for each phase, and associated with the primary currents, to the converter's supervisory controller, in addition to coupling thereto primary currents sensed relative to the common nodes of the respective phases. This enables the controller to more completely take into account the influence of the currents of each channel on every other channel, whereby phase-balanced control of all converter channels is achieved, irrespective of symmetry of the integrated circuit layout of the different phases of the converter.

To this end, similar to the dual-phase DC-DC converter of FIG. 1, which contains two phases or power channels, the M-phase converter architecture of the present invention includes M power channels, respective switched power stages of which are driven by associated channel drivers. Each of these M the power stages contains an upper power MOSFET switch and a lower power MOSFET switch having the source-drain paths thereof coupled in series between an input voltage supply terminal and a reference potential terminal. The control or gate input of the upper MOSFET switch is coupled to a first output of an associated driver for that stage, while the control or gate input of the lower MOSFET switch is coupled to a second output of the driver for that stage.

The common/phase nodes between the upper and lower MOSFET switches of the M respective power stages, at which voltages V1P, V2P, . . . , VMP are provided, are coupled to respective output inductors, which supply respective phase/channel output voltages V1N, V2N, . . . , VMN to the converter's output node. The common nodes are further coupled through first resistors to associated primary current sense nodes ISEN1, ISEN1, . . . , ISEN M, which are respectively coupled to first through Mth inputs ISEN1, ISEN2, . . . , ISEN M inputs of the converter's controller.

In addition, each of the M power channels includes a plurality of M-1 auxiliary current sense coupling resistors, that are coupled to sense secondary currents associated with the primary currents sensed in the other M-1 phases. Each of the primary and secondary resistors has the same resistance value. The M-1 auxiliary current sense resistors of a respective ith power channel are coupled between the output node of that ith power channel at which a respective output voltage ViN is provided, and the current sense input ports of the controller for the other M-1 phases. Thus, the M-phase converter architecture of the invention includes a total of M primary current sense resistors, respectively coupled to M phase nodes at which voltages V1P-VMP are provided, and an additional M*(M-1) secondary current sense resistors coupled to M output nodes at which voltages V1N-VMN are provided.

Since each of the secondary current sense resistors has the same value of resistance Rs as the primary current sense resistors, the values of the sensed output currents fed back to the controller's M input ports ISEN1-ISEN M will be defined in accordance with an average of the respective voltages to which the current sense resistors for each sensed current are coupled. This corresponds to one-Mth of the sum of the respective voltages, so that $ISEN1 = (1/M) * (V1P + V2N + \dots + VMN)$; $ISEN2 = (1/M) * (V2P + V1N + V3N + \dots + VMN)$; and $ISEN M = (1/M) * (VMP + V1N + \dots + V(M-1)N)$.

For controlling the respective power channels of the M-phase converter, the controller IC includes M difference

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amplifiers that are connected substantially as in the conventional converter of FIG. 1, except that the I_{AVG} reference for the M difference amplifiers is produced by the output of a divide-by-M divider within an averaging circuit, the front end of which sums the M sensed currents ISEN1-ISENM that are fed back from the M primary current sense resistors and the $M*(M-1)$ secondary current sense resistors of each power stage, described above. The outputs of the M difference amplifiers provide M correction voltages ICOR1-ICORM, that are respectively representative of differences between the M sensed currents ISEN1-ISENM and the average I_{AVG} of the N sensed currents. These M correction voltages ICOR1-ICORM are subtracted in M subtraction units from an error voltage generated at the output of the error amplifier. The outputs of these subtraction units serve as control inputs for respective PWM modulators of the M power channels.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 diagrammatically illustrates the architecture of a conventional dual phase DC-DC converter employing single ended current sensing for current-sharing control of the power delivered by two power channels to a load;

FIG. 2 diagrammatically illustrates the architecture of a dual-phase DC-DC converter employing single ended current sensing for current-sharing control in accordance with the invention, which incorporates auxiliary resistor networks to couple secondary current sense ports of both power channels/phases to the converter's supervisory controller;

FIGS. 3 and 4 diagrammatically illustrate the architecture of a three-channel/phase DC-DC converter employing single ended current sensing for current-sharing control in accordance with the invention, which incorporates auxiliary resistor networks to couple multiple secondary current sense ports of each of the power channels/phases to the differential measurement and control circuitry of the supervisory controller;

FIG. 5 diagrammatically illustrates an alternative integrated circuit implementation of the primary and auxiliary current sense resistors networks that are employed to couple monitored currents at the outputs of the respective power stages of the power channels of the three-phase converter of FIGS. 3 and 4 to the supervisory controller therefor; and

FIG. 6 diagrammatically illustrates the architecture of an M-phase DC-DC converter employing single ended current sensing for current-sharing control in accordance with the invention, which incorporates auxiliary resistor networks to couple secondary current sense ports of all power channels/phases to the converter's supervisory controller.

DETAILED DESCRIPTION

Before describing the new and improved multi-phase DC-DC converter architecture in accordance with the present invention, it should be observed that the invention resides primarily in a modular arrangement of conventional power supply circuits and electronic signal processing circuits and components therefor. In a practical implementation that facilitates packaging in a hardware-efficient equipment configuration, these modular arrangements may be readily implemented as field programmable gate array (FPGA)-, or application specific integrated circuit (ASIC)-based chip sets. Consequently, the configuration of such an arrangement of circuits and components and the manner in which they are interfaced with one another have, for the most part, been illustrated in the drawings by readily understandable block

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diagrams, which show only those specific details that are pertinent to the present invention, so as not to obscure the disclosure with details which will be readily apparent to those skilled in the art having the benefit of the description herein. The block diagram illustrations within the various Figures are primarily intended to show the major components of a DC-DC converter according to the invention in a convenient functional grouping, whereby the present invention may be more readily understood.

Attention is now directed to FIG. 2, which is a block diagram of a two-channel or dual-phase DC-DC converter that incorporates auxiliary resistor networks to feed back secondary sensed currents derived from the output nodes of each channel to the differential measurement and control circuitry of the converter's supervisory controller. It should be noted that the invention is not limited to this or any particular number of power channels/phases; a two phase/channel architecture has been illustrated to reduce the complexity of the drawings. The invention is also applicable to multi-phase converter architectures that include three or more phases, as will be described.

As can be seen from a comparison of the dual-phase DC-DC converter architecture of FIG. 2 with that of FIG. 1, the architecture of FIG. 2 for the most part corresponds to the converter architecture shown in FIG. 1, but additionally includes an augmentation thereof, in that a first auxiliary (secondary) current sense coupling resistor 127', associated with the current ISEN2 sensed in the second phase/channel 200, has been incorporated into the current sense network circuitry of the first phase/channel 100, and a second auxiliary (secondary) current sense coupling resistor 227' associated with the primary current ISEN1 sensed in the first phase/channel 100, has been incorporated into the current sense network circuitry of the second phase/channel 200. The values (R_s) of the auxiliary current sense-coupling resistors 127' and 227' are the same as those (R_s) of resistors 127 and 227. The architectures of the DC-DC converters of the two Figures are otherwise the same. As such, for purposes of conciseness, a description of the like portions of the two Figures will not be repeated here. Instead, attention may be directed to the above description of FIG. 1 for a description of its like components in FIG. 2.

In the dual-phase DC-DC converter architecture of FIG. 2, a first end of the auxiliary current sense resistor 127' of the first power channel 100 is coupled to the V1N voltage output of the first power stage 120 delivered to the output node OUT, while a second end thereof is coupled to the ISEN2 input of the controller 500, to which the ISEN2 current sense port/node 229 of the second power channel 200 is coupled. Since the value R_s of the auxiliary current sense resistor 127' is the same as that (R_s) of current sense resistor 227, the current ISEN2 applied to the controller's input port ISEN2 will be defined in accordance with an average of a primary sensed current based upon the voltage V2P to which the resistor 227 is coupled, and a secondary sensed current based upon the voltage V1N to which the resistor 127' is coupled. In the present example of a two channel converter, this average is proportional to one-half the sum of the respective voltages V2P and V1N; namely, $ISEN2=0.5*(V2P+V1N)/R_s$.

In a complementary manner, a first end of the auxiliary current sense resistor 227' of the second power channel 200 is coupled to the V2N voltage output of the first power stage 220 delivered to the output node OUT, while a second end thereof is coupled to the ISEN1 input of the controller 500, to which the ISEN1 current sense port/node 129 of the first power channel 100 is coupled. As in the case of the first

power channel, since the value R_s of the auxiliary current sense resistor **227'** is the same as that (R_s) of current sense resistor **127**, the current I_{SEN1} applied to the controller's input port I_{SEN1} will be defined in accordance with an average of a primary sensed current based upon the voltage V_{1P} to which resistor **127** is coupled, and a secondary sensed current based upon the voltage V_{2N} to which resistor **2271** is coupled. In the present example of a two channel converter, this average is proportional to one-half the sum of the respective voltages V_{2P} and V_{1N} ; namely, $I_{SEN2}=0.5*(V_{2P}+V_{1N})/R_s$.

From inspection, it can be seen that $(V_{1P}-V_{1N})=(V_{2P}-V_{2N})$, so that the feed back connections from the auxiliary current sense resistors **127'** and **227'** effectively provides a differential sensing effect for the controller **500**, without having to employ a differential amplifier per channel that entails more complexity and cost. Thus, through the addition of relatively simple auxiliary circuitry (resistor network), the present invention ensures that the converter's supervisory controller is able to independently control the pulse widths of the PWM waveforms for the two different phases/channels **100** and **200** in a manner that effectively balances the outputs currents delivered by the two power channels. Whether or not there is symmetry between the integrated circuit layouts of the two phases of the converter is immaterial.

As described briefly above, the present invention can be extended beyond the two-phase example of FIG. 2 to three or more phases. For example, FIGS. 3 and 4 diagrammatically illustrate the manner in which the auxiliary current sense resistor networks of the two-phase converter architecture of FIG. 2 may be modified to achieve circuit layout-independent current balancing for a three-phase DC-DC converter. In particular, FIG. 3 shows respective power stages **120**, **220** and **320** of power channels **100**, **200** and **300** of a three-phase converter, which are respectively driven by first, second and third channel driver ICs **110**, **210** and **310** of a controller/driver IC diagrammatically illustrated in broken lines **500'** in FIG. 4.

Like the two-phase DC-DC converters of FIGS. 1 and 2, each of the power stages **120**, **220** and **320** of the three-phase converter of FIG. 3 contains an upper power semiconductor switch (e.g., MOSFET) and a lower power semiconductor switch (e.g., MOSFET) having the source-drain paths thereof coupled in series between an input voltage (V_{in}) supply terminal and a reference voltage (ground) terminal. The control or gate input of the upper MOSFET switch is coupled to a first output of an associated driver for that stage, while the control or gate input of the lower MOSFET switch is coupled to a second output of the driver for that stage. Common or phase nodes **125**, **225** and **325** between the upper and lower MOSFET switches of the respective power stages, at which voltages V_{1P} , V_{2P} and V_{3P} are provided, are coupled to respective output inductors (L_o) **126**, **226** and **326**, which supply respective phase/channel output voltages V_{1N} , V_{2N} and V_{3N} to the converter's output node OUT.

As in the two-phase embodiment of FIG. 2, the V_{1P} output of the first power stage **120** is coupled through a resistor (R_s) **127** to a primary sense current I_{SEN1} port or node **129**, which is further coupled through a capacitor **128** to the output node OUT. Similarly, the V_{2P} output of the second power stage **220** is coupled through a resistor (R_s) **227** to a primary sensed current I_{SEN2} port or node **229**, which is further coupled through a capacitor **228** to the output node OUT, while the V_{3P} output of the third power stage **320** is coupled through a resistor (R_s) **327** to a primary sense current I_{SEN3} port or node **329**, which is further

coupled through a capacitor **328** to the output node OUT. The first, second and third primary sense current ports **129**, **229** and **329** are coupled to I_{SEN1} , I_{SEN2} and I_{SEN3} input ports of the controller/driver IC **500'** of FIG. 4. In addition, each of the power channels of the three-phase embodiment of FIGS. 3 and 4 further includes a pair of secondary sense current coupling resistors, respective ones of which are associated with the primary currents sensed in the other two phases, coupled between the output node of that power channel and the current sense input ports of the controller/driver IC **500'** for the other two phases.

In particular, the first power channel **100** includes first and second secondary sense current coupling resistors **127'** and **127''**, first ends of which are connected to the V_{1N} voltage output of the first power stage **120**, while second ends thereof are coupled to the I_{SEN2} port and the I_{SEN3} input, respectively, of the controller **500'**, to which the primary sense current I_{SEN2} port/node **229** of the second power channel **200** and the primary sense current I_{SEN3} port/node **329** of the third power channel **300** are coupled. The value R_s of each of the auxiliary current sense resistors **127'** and **127''** is the same as that (R_s) of current sense resistors **227** and **327**.

Similarly, the second power channel **200** includes first and second secondary sense current coupling resistors **227'** and **227''**, first ends of which are connected to the V_{2N} voltage output of the second power stage **220**, while second ends thereof are coupled to the I_{SEN1} port and the I_{SEN3} input, respectively, of the controller **500'**, to which the primary sense current I_{SEN1} port/node **129** of the first power channel **100** and the primary sense current I_{SEN3} port/node **329** of the third power channel **300** are coupled. The value R_s of each of the auxiliary current sense resistors **227'** and **227''** is the same as that (R_s) of current sense resistors **127** and **327**.

Also, the third power channel **300** includes first and second secondary sense current coupling resistors **327'** and **327''**, first ends of which are connected to the V_{3N} voltage output of the third power stage **320**, while second ends thereof are coupled to the I_{SEN1} port and the I_{SEN2} input, respectively, of the controller **500'**, to which the primary sense current I_{SEN1} port/node **129** of the first power channel **100** and the primary sense current I_{SEN2} port/node **229** of the third power channel **300** are coupled. The value R_s of each of the auxiliary current sense resistors **327'** and **327''** is the same as that (R_s) of current sense resistors **127** and **227**.

As in the case of the dual-phase DC-DC converter architecture of FIG. 2, since each of the secondary sense current coupling resistors has the same value of resistance R_s as the primary sense current coupling resistors, the values of the combined sense currents that are fed back to the controller's three input ports I_{SEN1} , I_{SEN2} and I_{SEN3} will be defined in accordance with an average of the respective voltages to which the sense current coupling resistors for each sensed current are coupled, which, in the present example of a three-channel converter, corresponds to one-third of the sum of the respective voltages. Namely $I_{SEN1}=0.33*(V_{1P}+V_{2N}+V_{3N})$; $I_{SEN2}=0.33*(V_{2P}+V_{1N}+V_{3N})$; and $I_{SEN3}=0.33*(V_{3P}+V_{1N}+V_{2N})$.

For controlling the respective power channels **100** and **200** of the three-phase converter of FIGS. 3 and 4, controller **500'** includes first and second difference amplifiers **510** and **520** that are connected in the same manner as in the dual-phase architecture of FIG. 2. The first, non-inverting (+) input **511** of difference amplifier **510** is coupled to each of the resistors **127**, **227'** and **327'** associated with the sensed current I_{SEN1} , while the first, non-inverting (+) input **521** of difference amplifier **520** is coupled to each of the resistors

127', 227 and 327" associated with the sensed current ISEN2. The second, inverting (−) inputs 512 and 522 of difference amplifiers 510 and 520, respectively, are coupled to the output I_{AVG} of a divide-by-three divider 517' of an averaging circuit 515'. This average corresponds to one-third of the summation of the sensed currents ISEN1, ISEN2 and ISEN3 that are fed back to a summation circuit 516' from the three current sense resistors of each power stage, described above. The output 513 of difference amplifier 510 provides a first correction voltage ICOR1 representative of the difference between the first channel's sensed current ISEN1 and the average I_{AVG} of the three sensed currents (ISEN1, ISEN2 and ISEN3), while the output 523 of difference amplifier 520 provides a second correction voltage ICOR2 representative of the difference between the second channel's sensed current ISEN2 and the average I_{AVG} of the three sensed currents. To control the third power channel 300, controller 500' includes a third difference amplifiers 530 having a first, non-inverting (+) input 531 coupled to each of the resistors 127", 227" and 327 associated with the sensed current ISEN3, while the second, inverting (−) input 532 difference amplifier 530 is coupled to coupled to the output I_{AVG} of the divide-by-three divider 517' of averaging circuit 515'. The output 533 of difference amplifier 530 provides a third correction voltage ICOR3 representative of the difference between the third channel's sensed current ISEN3 and the average I_{AVG} of the three sensed currents (ISEN1, ISEN2 and ISEN3).

As in the dual-phase architecture of FIG. 2, the first correction voltage ICOR1 is coupled to a first (−) input 541 of subtraction unit 540, while the second correction voltage ICOR2 is coupled to a first (−) input 561 of subtraction unit 560. The third correction voltage ICOR3 is coupled to a first (−) input 571 of a subtraction unit 570. The subtraction units 540, 560 and 570 have second (+) inputs 542, 562 and 572, respectively, that are coupled to receive the error voltage generated at the output 553 of error amplifier 550. The output 543 of subtraction unit 540 serves as the control input for PWM modulator 10 of the first power channel 100, the output 563 of subtraction unit 560 serves as the control input for PWM modulator 20 of the second power channel 200, and the output 573 of subtraction unit 570 serves as the control input for PWM modulator 30 of the third power channel 300.

Similar to the dual-phase architecture of FIG. 2, for the three-phase embodiment of FIGS. 3 and 4, it can be seen that $(V1P-V1N)=(V2P-V2N)=(V3P-V3N)$, so that the feedback connections from the additional pair of secondary sense current coupling 127' and 127" in the first channel, the additional pair of secondary sense current coupling resistors 227' and 227" in the second channel, and the additional pair of secondary sense current coupling resistors 327' and 327" in the third channel effectively provide differential sensing for the controller 500, without the need for costly differential amplifiers. Such differential sensing enables the controller to balance the currents delivered by the three power channels, even though the circuit layouts of the three phases of the integrated circuit layout of the converter are not symmetric.

In addition to reducing cost and complexity by eliminating the need for differential amplifiers, the number of sense nodes (e.g., ISEN1, ISEN2, ISEN3, Vo) is also reduced in accordance with the invention, as compared with conventional differential schemes, which require a larger number of sense nodes (e.g., ISEN1P, ISEN1N, ISEN2P, ISEN2N, ISEN3P, ISEN3N). It may also be noted that the resistor networks may be implemented exterior to, or integrated within, the IC controller. In either implementation, there will

be a number of pins saving benefit, in addition to a reduced complexity benefit, as far as the IC is concerned.

FIG. 5 diagrammatically illustrates an alternative implementation of the primary and auxiliary current sense resistor networks that are employed to couple output voltage nodes of the respective power stages of the power channels of the three-phase converter of FIGS. 3 and 4 to the controller therefor. In accordance with this alternative implementation, each power channel includes a multi-resistor, resistor-capacitor network, that is connected across the power stage's output inductor L_o . As shown in FIG. 5, the multi-resistor network for a respective i th power stage is comprised of a first resistor R_s , one end of which is connected to the common/phase node at which output voltage V_{iP} for that i th stage is produced, and the other end of which is connected to a capacitor C_s . The capacitor C_s is further coupled to a first end of a second resistor R_o , a second end of which is connected to the output node V_{iN} for that stage. The common node $ISiP$ between the second resistor R_s and the capacitor C_s is coupled through a third, primary current sense resistor R_c to a primary current sense port ISEN' i for that i th power stage, while the common node Vo' between the capacitor C_s and the resistor R_c serves as the output voltage-monitoring input to the error amplifier. Fourth and fifth (current sense) resistors R_c are coupled between the output node V_{iN} and respective auxiliary current sense ports ISEN' j and ISEN' k . The letters i , j and k correspond to one of the first (1), second (2) and third (3) sensed output currents. The three current sense ports ISEN1', ISEN2' and ISEN3' for each power channel are coupled to associated inputs ISEN1', ISEN2' and ISEN3' of the controller, as in the implementation of FIGS. 3 and 4, so that, as in that implementation, the values of the sensed output currents fed back to the controller's three input ports ISEN1', ISEN2' and ISEN3' will be defined in accordance with the average of the currents sensed by the current sense resistors R_c for each sensed current, whereby $ISEN1' = 0.33 \cdot (V1P+V2N+V3N)$; $ISEN2' = 0.33 \cdot (V2P+V1N+V3N)$; and $ISEN3' = 0.33 \cdot (V3P+V1N+V2N)$.

FIG. 6 diagrammatically illustrates the manner in which the auxiliary current sense resistor networks of the multi-phase DC-DC converter architecture described above with reference to FIGS. 2-4 may achieve circuit layout-independent current balancing for the general case of an M -phase DC-DC converter. In particular, FIG. 6 shows respective power stages 120, 220, . . . , M20 of plurality M of power channels of an M -phase converter, which are respectively driven by first, second, . . . , M th channel drivers of an associated M -phase controller/driver (not shown in FIG. 6, but effectively corresponding to that of FIGS. 2-4, and coupled to M2 current sense resistors of the M output stages, as will be described).

Like the multi-phase DC-DC converters of FIGS. 2-4, each of the power stages of the M -phase converter of FIG. 6 contains an upper power semiconductor switch (e.g., MOSFET) and a lower power semiconductor switch (e.g., MOSFET) having the source-drain paths thereof coupled in series between an input voltage (V_{in}) supply terminal and a reference voltage (ground) terminal. The control or gate input of the upper MOSFET switch is coupled to a first output of an associated driver for that stage, while the control or gate input of the lower MOSFET switch is coupled to a second output of the driver for that stage.

The common/phase nodes 125, 225, . . . , M25 between the upper and lower MOSFET switches of the respective power stages, at which voltages $V1P$, $V2P$, . . . , VMP are provided, are coupled to respective output inductors (L_o)

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126, 226, M26, which supply respective phase/channel output voltages V1N, V2N, . . . , VMN to the converter's output node OUT. The V1P output of the first power stage 120 is coupled through a resistor (Rs) 127-1 to an ISEN1 port or node 129, which is further coupled through a capacitor 128 to the output node OUT. The V2P output of the second power stage 220 is coupled through a resistor (Rs) 227-1 to an ISEN2 port or node 229, which is further coupled through a capacitor 228 to the output node OUT, while the VMP output of the Mth power stage M20 is coupled through a resistor (Rs) M27-1 to an ISENM port or node M29, which is further coupled through a capacitor M28 to the voltage output node OUT. The first through Mth current sense ports 129, 229, . . . , M29 are coupled to ISEN1, ISEN2, . . . , ISENM inputs of the converter's controller/driver.

In addition, each power channel of the M-phase converter architecture of FIG. 6 further includes a plurality of M-1 auxiliary current sense coupling resistors, coupled to sense secondary currents associated with the primary currents sensed in the other M-1 phases. The (M-1) auxiliary current sense resistors of a respective ith power channel are coupled between the output node of that ith power channel at which a respective output voltage ViN is provided, and the current sense input ports of the controller/driver for the other M-1 phases. Thus, the M-phase architecture of FIG. 6 includes a total of M primary current sense resistors 127-1-M27-1, each having the value Rs and being respectively coupled to M phase nodes at which voltages V1P-VMP are provided, and an additional M*(M-1) secondary current sense resistors 127-2-127-M, . . . , M27-1-M27-M, each having the same value Rs, and being coupled to M output nodes at which voltages V1N-VMN are provided.

Namely, the first power channel includes M-1 auxiliary resistors 127-2-127-M, first ends of which are connected to the V1N voltage output of the first power stage 120, while second ends thereof are coupled to the ISEN2 through ISENM inputs, respectively, of the controller. Similarly, the second power channel includes M auxiliary current sense resistors 227-2-227-M, first ends of which are connected to the V2N voltage output of the second power stage 220, while second ends thereof are coupled to the ISEN1 input and to the ISEN3-ISENM inputs, respectively, of the controller. Also, the Mth power channel includes M auxiliary resistors M27-2-M27-M, first ends of which are connected to the VMN voltage output of the Mth power stage M20, while second ends thereof are coupled to the ISEN1-ISEN(M-1) inputs, respectively, of the controller.

Again, since each of the secondary current sense resistors has the same value of resistance Rs as the primary current sense resistors, the values of the sensed output currents fed back to the controller's M input ports ISEN1-ISENM will be defined in accordance with an average of the respective voltages to which the current sense resistors for each sensed current are coupled. For the present example of an M-channel converter, this corresponds to one-Mth of the sum of the respective voltages. Namely $ISEN1 = (1/M) * (V1P + V2N + \dots + VMN)$; $ISEN2 = (1/M) * (V2P + V1N + V3N + \dots + VMN)$; and $ISENM = (1/M) * (VMP + V1N + V$ (M-1)N).

For controlling the respective power channels of the M-phase converter, the controller IC includes M difference amplifiers that are connected in the same manner as in the two-phase and three-phase embodiments of FIGS. 2-4, except that the I_{AVG} reference for the M difference amplifiers is produced by the output of a divide-by-M divider within an averaging circuit, the front end of which sums the M primary

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sensed currents sensed by the M primary sensed current coupling resistors with the M*(M-1) secondary sensed currents ISEN1-ISENM that are fed back from the M*(M-1) auxiliary, secondary current sense resistors of each power stage, described above. The outputs of the M difference amplifiers provide M correction voltages ICOR1-ICORM, that are respectively representative of differences between the composite values of the M sensed currents ISEN1-ISENM and the average I_{AVG} of the composite values of the M sensed currents. Similar to the above embodiments, these M correction voltages ICOR1-ICORM are coupled to first inputs of respective ones of M subtraction units, second inputs of which are coupled to receive the error voltage generated at the output of the error amplifier. The outputs of these subtraction units serve as control inputs for respective PWM modulators of the M power channels. Similar to the two-phase and three-phase embodiments, described above, in the M-phase embodiment $(V1P-V1N) = (V2P-V2N) = (VMP-VMN)$.

As will be appreciated from the foregoing description, the above-described asymmetry circuitry layout-based current imbalance problem encountered in a multi-phase DC-DC converter is effectively obviated in accordance with the multi-phase DC-DC converter architecture of the present invention, which uses reduced complexity implementation-based, resistor-coupling to feed back values of sensed currents at secondary current sense ports that couple the output nodes for each phase to differential measurement and control circuitry within the converter's supervisory controller. This enables the controller to perform current-balanced control of pulse widths of the switching waveforms produced by the PWM modulators for all channels, whether or not there is symmetry among the integrated circuit layouts of those channels.

While we have shown and described several embodiments in accordance with the present invention, it is to be understood that the same is not limited thereto but is susceptible to numerous changes and modifications as known to a person skilled in the art, and we therefore do not wish to be limited to the details shown and described herein, but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.

What is claimed:

1. A multi-phase DC-DC converter comprising:

- a plurality of power channels, which are operative to deliver a DC output voltage to an output node adapted to be coupled to a load, a respective ith power channel including an output voltage switching stage coupled between said output node and an input voltage terminal, to which a DC input voltage is applied, and being controllably switched by a respective ith switching waveform applied thereto, so as to deliver a respective ith DC voltage waveform to said output node;
- a primary output current sensing circuit having a plurality of first inputs, coupled to monitor primary sensed currents associated with voltages produced by output voltage switching stages of said plurality of power channels, and a plurality of first outputs, respectively coupled to inputs of a controller, said controller being operative to individually control parameters of respective switching waveforms that are used to controllably switch output voltage switching stages of said plurality of power channels; and
- a secondary output current sensing circuit, having a plurality of second inputs coupled to monitor secondary sensed currents associated with said primary sensed currents and derived in accordance with voltages

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applied by said output voltage switching stages to said output node, and a plurality of second outputs coupled to said inputs of said controller; and wherein said controller is operative to control parameters of said respective *i*th switching waveform in accordance with a primary sensed current of said *i*th power channel and secondary sensed currents of each of one or more others of said plurality of power channels.

2. The multi-phase DC-DC converter according to claim 1, wherein said plurality of power channels comprises *M* power channels, said primary output current sensing circuit has a plurality of *M* first inputs coupled to monitor *M* primary sensed currents associated with voltages produced by said output voltage switching stages and a plurality of *M* first outputs respectively coupled to *M* inputs of said controller, and said secondary output current sensing circuit has a plurality of *M* second inputs coupled to monitor $M^*(M-1)$ secondary sensed currents associated with voltages applied by said output voltage switching stages to said output node, and a plurality of $M^*(M-1)$ second outputs coupled to said *M* inputs of said controller, and wherein said controller is operative to control parameters of said respective *i*th switching waveform in accordance with a difference between a combination of said *i*th primary sensed current and said *M*-1 secondary sensed currents for said *i*th power channel and the average value of said *M* primary sensed currents and said $M^*(M-1)$ secondary sensed currents.

3. The multi-phase DC-DC converter according to claim 2, wherein said *i*th switching waveform comprises an *i*th pulse width modulated (PWM) waveform, and wherein said controller is operative to control the pulse width of said *i*th PWM waveform.

4. The multi-phase DC-DC converter according to claim 2, including an error amplifier that is operative to generate an error voltage in accordance with a relationship between a DC reference voltage and said DC output voltage, and wherein said controller is operative to modify said error voltage in accordance with said difference between a combination of said *i*th primary sensed current and said *M*-1 secondary sensed currents for said *i*th power channel and the average value of said *M* primary sensed currents and said $M^*(M-1)$ secondary sensed currents, to produce an *i*th modified error voltage for said *i*th power channel, and to control said *i*th switching waveform in accordance with said *i*th modified error voltage.

5. The multi-phase DC-DC converter according to claim 2, wherein said output voltage switching stage of said respective *i*th power channel comprises first and second controlled switching devices coupled between said input voltage terminal and a reference terminal, and having control inputs thereof coupled to receive first and second control signals that are defined in accordance with said *i*th switching waveform, and wherein a common node between said first and second controlled switching devices is coupled to an *i*th one of said plurality of *M* first inputs of said primary output current sensing circuit.

6. The multi-phase DC-DC converter according to claim 5, wherein said primary output current sensing circuit includes a plurality of *M* first resistors, a respective *i*th first resistor being coupled between said common node and an *i*th first output of said output voltage switching stage of said respective *i*th power channel, and wherein said secondary output current sensing circuit includes a plurality of $M^*(M-1)$ second resistors, and wherein respective ones of *M*-1 second resistors are coupled between *M*-1 second inputs of said second output current sensing circuit that are coupled between *M*-1 voltages, applied by *M*-1 of said output

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voltage switching stages to said output node, and *M*-1 of said *M* inputs of said controller.

7. The multi-phase DC-DC converter according to claim 5, wherein said primary output current sensing circuit includes a plurality of *M* first resistors, a respective *i*th first resistor being coupled to a resistor-capacitor network that is coupled between said common node and an *i*th first output of said output voltage switching stage of said respective *i*th power channel, and wherein said secondary output current sensing circuit includes a plurality of $M^*(M-1)$ second resistors, and wherein respective ones of *M*-1 second resistors are coupled between *M*-1 second inputs of said second output current sensing circuit that are coupled between *M*-1 voltages, applied by *M*-1 of said output voltage switching stages to said output node, and *M*-1 of said *M* inputs of said controller.

8. The multi-phase DC-DC converter according to claim 7, wherein said resistor-capacitor network includes a pair of resistors and a capacitor coupled in parallel with an inductor between said common node and said *i*th first output of said output voltage switching stage of said respective *i*th power channel, and wherein one of said pair of resistors is coupled between said common node and one end of said capacitor, and another of said pair of resistors is coupled between said *i*th first output of said output voltage switching stage of said respective *i*th power channel and a second end of said capacitor, and wherein said respective *i*th first resistor is coupled to said one end of said capacitor.

9. The multi-phase DC-DC converter according to claim 8, wherein each of said plurality of *M* first resistors has the same resistance value, that is different than resistance values of said one and said another of said pair of resistors.

10. A method of controlling the operation of a multi-phase DC-DC converter, said multi-phase DC-DC converter having a plurality of power channels, which are operative to deliver a DC output voltage to an output node adapted to be coupled to a load, a respective *i*th power channel including an output voltage switching stage coupled between said output node and an input voltage terminal, to which a DC input voltage is applied, and being controllably switched by a respective *i*th switching waveform applied thereto, so as to deliver a respective *i*th DC voltage waveform to said output node, said method comprising the steps of:

(a) monitoring primary sensed currents associated with voltages produced by output voltage switching stages of said plurality of power channels, and coupling first signals representative of said primary sensed currents to inputs of a controller, which is operative to individually control parameters of respective switching waveforms that are used to controllably switch output voltage switching stages of said plurality of power channels;

(b) monitoring secondary sensed currents associated with said primary sensed currents and being derived in accordance with voltages applied by said output voltage switching stages to said output node and coupling second signals representative of said secondary sensed currents to said inputs of said controller; and

(c) causing said controller to control parameters of said respective *i*th switching waveform in accordance with a primary sensed current of said *i*th power channel and secondary sensed currents of each of one or more others of said plurality of power channels.

11. The method according to claim 10, wherein said plurality of power channels comprises *M* power channels, and said step (a) comprises monitoring *M* primary sensed currents associated with voltages produced by said output

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voltage switching stages, and producing M first signals that are coupled to M inputs of said controller, and step (b) comprises monitoring $M*(M-1)$ secondary sensed currents associated with voltages applied by said output voltage switching stages to said output node, and producing $M*(M-1)$ signals that are coupled to said M inputs of said controller, and wherein step (c) comprises causing said controller to control parameters of said respective ith switching waveform in accordance with a difference between a combination of an ith first signal and M-1 second signals for said ith power channel and the average value of said M first signals and said $M*(M-1)$ second signals.

12. The method according to claim 11, wherein said ith switching waveform comprises an ith pulse width modulated (PWM) waveform, and wherein step (c) comprises causing said controller to control the pulse width of said ith PWM waveform.

13. The method according to claim 11, further including the step of:

(d) generating an error voltage in accordance with a relationship between a DC reference voltage and said DC output voltage; and wherein

step (c) comprises causing said controller to modify said error voltage in accordance with said difference between a combination of said first signal and said M-1 second signals for said ith power channel and the average value of said M first signals and said $M*(M-1)$ second signals, so as to produce an ith modified error voltage for said ith power channel, and to control said ith switching waveform in accordance with said ith modified error voltage.

14. The method according to claim 11, wherein said output voltage switching stage of said respective ith power channel comprises first and second controlled switching devices coupled between said input voltage terminal and a reference terminal, and having control inputs thereof coupled to receive first and second control signals that are defined in accordance with said ith switching waveform, and a common node between said first and second controlled switching devices, step (a) comprises monitoring said common nodes of said output voltage switching stages of said plurality of M power channels to derive said first signals.

15. The method according to claim 14, wherein step (a) comprises monitoring said common nodes of said output voltage switching stages of said plurality of M power channels by way of a plurality of M first resistors to produce said first signals, a respective ith first resistor being coupled between said common node and an ith first output of said output voltage switching stage of said respective ith power channel, and wherein step (b) comprises monitoring voltages applied by said output voltage switching stages to said output node by way of a plurality of $M*(M-1)$ second resistors to derive said second signals representative of said secondary sensed currents, and coupling said $M*(M-1)$ second resistors to M-1 of said M inputs of said controller.

16. The method according to claim 15, wherein a respective ith first resistor is coupled to a resistor-capacitor network coupled between said common node and an ith first output of said output voltage switching stage of said respective ith power channel.

17. The method according to claim 16, wherein said resistor-capacitor network includes a pair of resistors and a capacitor coupled in parallel with an inductor between said common node and said ith first output of said output voltage switching stage of said respective ith power channel, and wherein one of said pair of resistors is coupled between said common node and one end of said capacitor, and another of

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said pair of resistors is coupled between said ith first output of said output voltage switching stage of said respective ith power channel and a second end of said capacitor, and wherein said respective ith first resistor is coupled to said one end of said capacitor.

18. The method according to claim 17, wherein each of said plurality of M first resistors has the same resistance value, that is different than the resistance values of said one and said another of said pair of resistors.

19. In a multi-phase DC-DC converter having a plurality of power channels, which are operative to deliver a DC output voltage to an output node adapted to be coupled to a load, a respective ith power channel including an output voltage switching stage coupled between said output node and an input voltage terminal, to which a DC input voltage is applied, and being controllably switched by a respective ith switching waveform applied thereto, so as to deliver a respective ith DC voltage waveform to said output node, and a primary output current sensing circuit having a plurality of first inputs, coupled to monitor primary sensed currents associated with voltages produced by output voltage switching stages of said plurality of power channels, and a plurality of first outputs, respectively coupled to inputs of a controller, said controller being operative to individually control parameters of respective switching waveforms that are used to controllably switch output voltage switching stages of said plurality of power channels, the improvement comprising:

a secondary output current sensing circuit, having a plurality of second inputs coupled to monitor secondary sensed currents associated with said primary sensed currents and derived in accordance with voltages applied by said output voltage switching stages to said output node, and a plurality of second outputs coupled to said inputs of said controller; and wherein

said controller is operative to control parameters of said respective ith switching waveform in accordance with a primary sensed current of said ith power channel and secondary sensed currents of each of one or more others of said plurality of power channels.

20. The improvement according to claim 19, wherein said plurality of power channels comprises M power channels, said primary output current sensing circuit has a plurality of M first inputs coupled to monitor M primary sensed currents associated with voltages produced by said output voltage switching stages and a plurality of M first outputs respectively coupled to M inputs of said controller, and said secondary output current sensing circuit has a plurality of M second inputs coupled to monitor $M*(M-1)$ secondary sensed currents associated with voltages applied by said output voltage switching stages to said output node, and a plurality of $M*(M-1)$ second outputs coupled to said M inputs of said controller, and wherein said controller is operative to control parameters of said respective ith switching waveform in accordance with a difference between a combination of said ith primary sensed current and said M-1 secondary sensed currents for said ith power channel and the average value of said M primary sensed currents and said $M*(M-1)$ secondary sensed currents, and wherein said primary output current sensing circuit includes a plurality of M first resistors, a respective ith first resistor being coupled between said common node and an ith first output of said output voltage switching stage of said respective ith power

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channel, and wherein said secondary output current sensing circuit includes a plurality of $M*(M-1)$ second resistors, and wherein respective ones of $M-1$ second resistors are coupled between $M-1$ second inputs of said second output current sensing circuit that are coupled between $M-1$ voltages,

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applied by $M-1$ of said output voltage switching stages to said output node, and $M-1$ of said M inputs of said controller.

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