Drive device for liquid crystal display panel

Antriebsvorrichtung für Flüssigkristallanzeigetafel

Dispositif de commande de panneau d'affichage à cristaux liquides
Description

TECHNICAL FIELD

[0001] The present invention relates to a drive device for a liquid crystal display panel, which drives a liquid crystal display panel by column inversion driving.

BACKGROUND ART

[0002] When a liquid crystal display panel using TFT (Thin Film Transistor) is to be driven, a gate-on voltage $V_{GH}$ to switch on a TFT gate provided for every pixel at an intersection of a gate wiring and a source wiring, a gate-off voltage $V_{GL}$ to switch off the TFT gate, a data voltage (source voltage) $V_D$ to be applied to a TFT source and a common voltage $V_{COM}$ to be applied to a common electrode, are required.

[0003] If a liquid crystal display panel is driven by a DC voltage, its useful life tends to be short. For such a reason, it is common to use an AC voltage in a drive method for driving a liquid crystal display panel. AC driving includes, for example, line inversion driving, column inversion driving and dot inversion driving (e.g. Patent Document 1).

[0004] Column inversion driving is a drive method wherein a liquid crystal display panel having pixels arranged in a matrix form, when pixel groups in a horizontal direction (lines: rows) are to be driven, for example, sequentially from the upper side towards the lower side, in one frame, the data voltage is made to be, for example, from a left hand side source wiring (column) towards a right hand side column, positive polarity, negative polarity, positive polarity, negative polarity, ..., and in the next frame, the polarity of the data voltage in each column is made to be opposite to the polarity in the last frame.

[0005] Hereinafter, a state where the potential of a source electrode is higher than the common voltage is regarded as a positive polarity state, and a state where the potential of a source electrode is lower than the common voltage is regarded as a negative polarity state.

[0006] Patent Document 1 discloses a method wherein in order to reduce power consumption of the drive device, the voltage applied to source wirings during the vertical blanking period is inverted, or when the vertical blanking period is started, the source wirings are once charged to the common potential. By such a construction, a rush current (inrush current) flowing in the source driver at the time of changing the polarity, can be reduced.

[0007] Further, Patent Document 1 discloses a method wherein in the vertical blanking period, charge sharing is carried out to short-circuit adjacent source wirings, then positively and negatively polarized data voltages with prescribed voltages are supplied to source wirings, and further charge sharing is carried out to bring the potential of the source wirings close to the common voltage. Here, a data voltage with a prescribed voltage to be supplied to a source wiring, is supplied to a source driver which outputs the data voltage to the source wiring, in the first horizontal effective period in the vertical blanking period.

PRIOR ART DOCUMENT

PATENT DOCUMENT


[0009] US 2006/0227092 A1 discloses a liquid crystal display device composed of first and second data lines, first and second operational amplifiers, and a short-circuiting circuit. The first operational amplifier is configured to drive the first data line to a potential of a first polarity during a first period, and to drive the second data line to a potential to the first polarity during a second period following the first period. The second operational amplifier is configured to drive the second data line to a potential of a second polarity complementary to the first polarity during the first period, and to drive the first data line to a potential to the second polarity during the second period. The short-circuiting circuit is configured to short-circuit the first and second data lines during a short-circuiting period between the first and second periods. Drive capabilities of the first and second operational amplifiers are controlled in response to a short-circuit potential of the first and second data lines during the short-circuiting period.

[0010] US 2006/221035 A1 discloses a method of driving a liquid crystal display in two-dot inversion for a low vertical frequency and in one-dot inversion for a high vertical frequency. The method determines whether the vertical frequency of the LCD changes, changes the inversion type into one-dot inversion if the vertical frequency is changed from a low frequency to a high frequency, and changes the inversion type into two-dot inversion if the vertical frequency is changed from a high frequency to a low frequency. Moreover, if a flicker is generated when driving in one-dot inversion, the inversion type is changed into two-dot inversion. To avoid the unequal charging generated in the LCD driven in two-dot inversion, the pulse width of the gate signals are adjusted after measuring the load of the data line.

[0011] EP 2 075 790 A2 discloses a Thin Film Transistor-Liquid Crystal Display (TFT-LCD) driver circuit having a source drive buffer with an operational amplifier having two differential amplifiers operating alternatively according to timing signals and bias voltage signals. The differential amplifiers are further capable of functioning as a voltage follower by buffering and outputting voltage signals from a Digital to Analog Converter for charging display points. The TFT-LCD driver circuit may also be incorporated within an LCD device. However, it is not disclosed that the source driver is adapted to drive the source wirings by column inversion and to invert the polarity every frame period. Furthermore, it is not disclosed that the source driver is adapted to drive in the initial period at least the first one horizontal line in each frame, and that the source driver includes interval adjusting means for adjusting the length of the first half interval

[0012] Depending upon the size or the number of pixels of the liquid crystal display panel.

[0013] However, if the drive device for a liquid crystal display panel disclosed in Patent Document 1 is to be used, it is necessary to preliminarily determine by calculation, etc. the voltage value for the data voltage to be output in the first horizontal effective period in the vertical blanking period. Further, the number of types of the voltage values for the data voltages which can be used, is usually limited to a number corresponding to the number of gradations and cannot be set to be an optional desired value. Further, in order to make it possible for the data voltages to be output in the first horizontal effective period in the vertical blanking period, the construction of a timing control circuit to supply a clock signal or a latch signal to a source driver or a gate driver, has to be substantially changed from a common construction of a timing control circuit. Further, power consumption is not reduced in a period wherein driving is carried out for actual display (hereinafter referred to as a display period).

[0014] Accordingly, it is an object of the present invention to reduce the power consumption of a liquid display panel while preventing deterioration of the display quality.

SOLUTION TO PROBLEM

[0015] The problem is solved by a drive device for a liquid crystal display panel having the features of independent claim 1. Preferred embodiments are defined in dependent claim 2. By such a construction, it is possible to reduce consumption current while preventing deterioration of the display quality, taking into consideration the properties of the liquid crystal display panel. Furthermore, it is possible to reduce power consumption, with a simpler construction, by suppressing a rush current which flows in the source driver when the polarity is changed over.

ADVANTAGEOUS EFFECTS OF INVENTION

[0016] According to the present invention, in a drive device for driving a liquid crystal display panel by column inversion driving, it is possible to further reduce power consumption by a simple construction.

BRIEF DESCRIPTION OF DRAWINGS

[0017] Fig. 1 is a block diagram illustrating a construction example of a liquid crystal display device to which a drive device of the present invention is applied.

Fig. 2 is a schematic diagram illustrating data voltages.

Fig. 3 is a timing diagram illustrating an operation example of the drive device.

Fig. 4 is a timing diagram illustrating an operation of the drive device.

Fig. 5 is a block diagram illustrating a construction example of an output buffer.

Fig. 6 is a schematic diagram illustrating an example of a relation between a signal state of a control signal Cont 1 and an output state of an amplifier, and an example of an output state of the amplifier.

Fig. 7 is a block diagram illustrating a construction of the output side of the output buffer.

Fig. 8 is a schematic view illustrating a relation between the control signal Cont 1 and a state of each switch.

Fig. 9 is a schematic diagram which schematically illustrates a consumption current when column inversion driving is employed.

Fig. 10 is a timing diagram illustrating an operation example in the embodiment of the invention (EMBODIMENT 2 or second embodiment) of the drive device.

Fig. 11 is a timing diagram illustrating, as enlarged, an operation example in the second embodiment.

Fig. 12 is a timing diagram illustrating, as enlarged, another operation example in the second embodiment.

DESCRIPTION OF EMBODIMENTS

[0018] Now, examples useful for understanding the invention and embodiments of the present invention will be described with reference to the drawings.

Example 1

[0019] Fig. 1 is a block diagram illustrating a construction example of a liquid crystal display device to which the drive device of the present invention is applied. In the liquid crystal display device shown in Fig. 1, many pixels 12 are formed in a matrix form on a liquid display panel 10. To form the pixels, many gate wirings 13 are provided in a horizontal direction (row direction), and many source wirings 14 are provided in a column direction to intersect with the gate wirings 13. And, TFT15 is formed at an intersection of a gate wiring 13 and a source wiring 14. A drain electrode 16 of TFT 15 is connected to a pixel.
A facing substrate (not shown) is provided to face the substrate having the gate wirings 13, the source wirings 14 and the pixels 12 formed thereon, and liquid crystal is sandwiched between the substrate having the pixels 12 formed, and the facing substrate. On the facing substrate, a counter electrode (common electrode) is formed, and the counter electrode is set at a common potential VCOM. Here, electrically, liquid crystal may be regarded as an element having a capacity, and in Fig. 1, a capacitor 17 is shown, of which one end is connected to a pixel electrode and the potential of the other end becomes the common potential VCOM.

A gate driver 30 drives gate wirings 13, for example, line-sequentially. To a pixel electrode of a pixel electrode.

A gate-on voltage VGH is applied, a data voltage is connected to a selected gate wiring 13 i.e. a gate wiring 13 to which a gate-on voltage VGH is applied, a data voltage (voltage corresponding to a data signal) VD is applied via a source wiring 14.

In the construction example shown in Fig. 1, the source driver 20 to drive the source wirings 14, comprises a shift register 21, a first latch circuit 22 which sequentially latches and outputs data signal DATA, a second latch circuit 23 which collectively takes in the output from the first latch circuit 22, a D-A converter 24 which outputs an analog signal (analog voltage) corresponding to the value of the output (digital data) from the second latch circuit 23, and a buffer circuit 25 which current-amplifies the output from the D-A converter 24.

Taking as a starting point a horizontal start pulse STH corresponding to a signal for initiation of a selected period output by a control unit (timing control circuit) 40, the shift register 21 forms a data-taking-in signal from a clock signal CLK for data shift and outputs it. In this example, the number of source wirings 14 is assumed to be m (m: a positive integer in multiples of 3). With respect to the data signals, corresponding to one clock signal CLK in the case of RGB parallel, are three RGB. Accordingly, the number of output signals of the shift register 21 is m/3. For example, in response to the Ith clock (I:1 to m/3) of the clock signal CLK, the shift register 21 brings about a first set of outputs to an on-state (data taking-in state). To the first latch circuit 22, m signals are input from the timing control circuit 40, but the power source circuit may be provided separately by the m signals, odd-numbered signals are made to be signals with a value appropriate for positive polarity and the level of a signal input from the second latch circuit 23, and among the m signals, even-numbered signals are made to be signals with a value appropriate for negative polarity and the level of a signal input from the second latch circuit 23. Whereas, in a case where the level of the polarity conversion signal POL is a low level, among the m signals, odd-numbered signals are made to be signals with a value appropriate for negative polarity and the level of a signal input from the second latch circuit 23, and among the m signals, even-numbered signals are made to be signals with a value appropriate for positive polarity and the level of a signal input from the second latch circuit 23.

Further, to simplify the description, the source driver 20 realizes 64 tones by means of a resistor ladder in the driver by inputting eight standard voltages in positive polarity by using voltages V8 to V15 and displays 64 tones by eight standard voltages in negative polarity by using voltages V0 to V7. The present invention may be applied to a case where a larger number of tones are to be realized. Further, the D-A converter 24 is provided with a resistor ladder at the input portion to realize multitone.

To the first latch circuit 22, data signals DATA from the timing control circuit 40 are sequentially output. Further, to the first latch circuit 22, m/3 signal is input from the shift register 21. When among m signals, the Ith signal (I:1 to m/3) of signals becomes an on-state, the first latch circuit 22 latches and outputs the first set of data (data signals DATA).

The second latch circuit 23 collectively takes in signals latched by the first latch circuit 22, for example, at the time of falling of a strobe signal STB (hereinafter referred to as a latch signal STB) output from the timing control circuit 40.

To the D-A converter 24, e.g. a voltage Vn (n: 0 to 15) is supplied from a power source circuit (not shown) included in the timing control circuit 40. As shown in Fig. 2, V8 to V15 are voltages higher than the common voltage VCOM, and V0 to V7 are voltages lower than the common voltage VCOM. Here, V8 to V15 are voltages for positive polarity driving, and V0 to V7 are voltages for negative polarity driving.

From the D-A converter 24, m signals are output which show values appropriate for the level (a high level or a low level) of a polarity inversion signal POL output from the timing control circuit 40. For example, in a case where the level of the polarity inversion signal POL is a high level, among m signals, odd-numbered signals are made to be signals with a value appropriate for positive polarity and the level of a signal input from the second latch circuit 23, and among the m signals, even-numbered signals are made to be signals with a value appropriate for negative polarity and the level of a signal input from the second latch circuit 23. Whereas, in a case where the level of the polarity conversion signal POL is a low level, among the m signals, odd-numbered signals are made to be signals with a value appropriate for negative polarity and the level of a signal input from the second latch circuit 23, and among the m signals, even-numbered signals are made to be signals with a value appropriate for positive polarity and the level of a signal input from the second latch circuit 23.

Further, in the construction shown in Fig. 1, the power source circuit is included in the timing control circuit 40, but the power source circuit may be provided separately from the timing control circuit 40.

The D-A converter 24 outputs signals of voltage (voltage signals) corresponding to the values shown respectively by the m signals output from the second latch circuit 23, to the buffer circuit 25.

The buffer circuit 25 applies the respective m voltage signals output from the D-A converter 24 to m source wirings 14.

Further, the source driver 20, the gate driver 30 and the timing control circuit 40 shown in Fig. 1 are constituting elements of the drive device for a liquid crystal display panel.

Figs. 3 and 4 are timing diagrams illustrating operation examples of the drive device. As shown in Fig. 3, the timing control circuit 40 outputs a control signal Cont 1 before the control for an image display in each frame is initiated. Specifically, the control signal Cont 1 is made to be a significant level for a period of at least
one horizontal period (a period between two horizontal synchronizing signals) in the vertical blanking period. In the example shown in Fig. 3, the significant level is a high level. The source driver 20 carries out the control as described hereinafter, based on the control signal Cont 1. The maximum value of the period wherein the control signal Cont 1 can be made to be a significant level, is the vertical blanking period.

Further, as shown in Fig. 3, the level of the polarity inversion signal POL is inverted every one frame. When the polarity inversion signal POL is at a high level, odd-numbered source wirings $S_{(2n-1)}$ are subjected to positive polarity driving, and even-numbered source wirings $S_{(2n)}$ are subjected to negative polarity driving. When the polarity inversion signal POL is at a low level, odd-numbered source wirings $S_{(2n-1)}$ are subjected to negative polarity driving, and even-numbered source wirings $S_{(2n)}$ are subjected to positive polarity driving. Here, $n$ is from 1 to $(m/2)$, and $m$ is an even number.

Further, the timing control circuit 40 outputs a control signal Cont 2 as shown in Fig. 4. Specifically, the level of the control signal Cont 2 is made to be a prescribed level for a period of at least one horizontal period (corresponding to one selected period) (e.g., from 1 to 3 horizontal periods) from the time when the control for an image display in each frame is initiated. Fig. 4 illustrates an example wherein the level of the control signal Cont 2 is made to be a prescribed level for a period corresponding to two horizontal periods. The source driver 20 carries out the special control as described hereinafter, based on the control signal Cont 2.

In Fig. 4, the period wherein the level of the control signal Cont 2 is at a prescribed level, is shown as the high level period. However, as described hereinafter, the prescribed level may not practically be a high level. Further, the period wherein the level is not a prescribed level is shown as a low level period, but it may not practically be a low level.

Fig. 5 is a block diagram illustrating a construction example of one output buffer 251 in buffer circuit 25. The buffer circuit 25 is provided with the same number as the source wirings 14 i.e. m output buffers. The construction of each output buffer in the buffer circuit 25 is the same as the construction shown in Fig. 5.

In the example shown in Fig. 5, the output buffer 251 comprises an amplifier 261 having a variable driving ability, to which a signal output from the D-A converter 24 is input, a first switch 263 to make either a state where the input to the amplifier 261 is supplied to an output terminal or a state where such an input is not supplied to the output terminal, a second switch 264 to make either a state where an output of the amplifier 261 is supplied to the output terminal or a state where such an output is not supplied to the output terminal, and a bias circuit 262 to change the output current (the maximum output current) of the amplifier 261 depending upon the control signal Cont 2. Here, the output terminal is an output terminal to a source wiring 14.

Further, the first switch 263 and the second switch 264 realize an output pathway setting unit which sets either one of a state where a voltage signal corresponding to a data signal is applied to a source wiring 14 via the amplifier 261 and a state where the voltage signal is applied to the source wiring without via the amplifier 261.

The control signal Cont 2 is, for example, a 2 bit signal. Fig. 6(A) is a schematic diagram illustrating an example of a relation between a signal state of the control signal Cont 2 and the output state of the amplifier 261. Fig. 6(B) is a schematic diagram illustrating a specific example of the output state of the amplifier 261. The control signal Cont 2 may be 1 bit, but it is preferably a 2 bit signal in view of the applicability due to the size of the liquid crystal display panel or improvement in the selection range of the power consumption.

As shown in Fig. 6, when the level of the control signal Cont 2 is $(L, L)$, the driving ability of the amplifier 261 is 130%; when the level of the control signal Cont 2 is $(L, H)$, the driving ability is 100%; and when the level of the control signal Cont 2 is $(H, L)$, the driving ability is 80%. Further, when the level of the control signal Cont 2 is $(H, H)$, the voltage signal from the D-A converter 24 is, as it is, output to the output terminal. Here, “H” means a high level, and “L” means a low level.

Here, the driving ability of 130% or 80% represents a relative maximum output current based on the driving ability when the level of the control signal Cont 2 is $(L, H)$.

Further, the driving ability by the voltage signal from the D-A converter 24 is lower than the driving ability when the level of the control signal Cont 2 is $(H, L)$ (corresponding to output C shown in Fig. 6(A)). Accordingly, as compared with the output current in a case where a signal of a voltage corresponding to a data signal is, as it is, applied to a source wiring 14 (in a case where the first switch 261 is a closed state, and the second switch 264 is an open state), the output current is higher in a case where a signal of a voltage corresponding to a data signal is applied to a source wiring 14 via the amplifier 261 when the level of the control signal Cont 2 is $(H, L)$.

Fig. 7 is a block diagram illustrating output side constructions of output buffers 251 and 252 which drive adjacent two source wirings 14 in the buffer circuit 25. The output buffer 251 is to drive an odd-numbered source wiring 14 (e.g. the first line source wiring 14), and the output buffer 252 is to drive an even-numbered source wiring 14 (e.g. a second line source wiring 14).

As shown in Fig. 7, on the output side of the output buffer 251, a first output switch 266 is provided to switch to a state where the output of the output buffer 251 is permitted to pass or a state where such an output is not permitted to pass. On the output side of the output buffer 252, a second output switch 268 is provided to switch to a state where the output of the output buffer 252 is permitted to pass or a state where such an output is not permitted to pass. Further, a third switch 267 is...
provided to switch to a state where the adjacent two source wirings 14 are connected or a state where they are not connected.

[0046] Here, the first output switch 266, the second output switch 268 and the third switch 267 are an example of a source wiring initial setting unit to short-circuit the adjacent source wirings 14.

[0047] Further, the internal construction of the output buffer 252 is the same as the internal construction of the output buffer 251 shown in Fig. 5. Further, in the buffer circuit 25, the first output switch 266 is provided as shown in Fig. 7 on the output side of all output buffers for driving source wirings $S_{(2n-1)}$. Further, the second output switch 268 is provided as shown in Fig. 7 on the output side of all output buffers for driving source wirings $S_{(2n)}$. Further, the third switch 267 is provided as shown in Fig. 7 between an output buffer for driving a source wiring $S_{(2n-1)}$ and an output buffer for driving a source wiring $S_{(2n)}$. However, the first output switch 266 and the second output switch 268 become an open state, the output side of an output buffer for driving an odd-numbered buffer circuit 25, the first output switch 266 provided on the control signal Cont 1 becomes a high level, in the vertical blanking period. Referring to Figs. 7 and 8, when during a period of at least one horizontal period in the controls the control signal Cont 1 to be at a high level

[0050] As shown in Fig. 4, the timing control circuit 40 in the same manner as the output buffers 251 and 252 in the buffer circuit 25 will also be operated in the same manner as the output buffers 251 and 252.

[0055] Referring to Figs. 5 and 6, in the output buffer 251 in the buffer circuit 25, a bias circuit 262 gives a bias voltage depending upon the level of the control signal Cont 2 so that the driving ability of the amplifier 261 is made to be 80%. Further, depending upon the level of the control signal Cont 2, the first switch 263 becomes an open state (a state where the input to the amplifier 261 will not be supplied to the output terminal), and the second switch 264 becomes a closed state (a state where the output of the amplifier 261 is supplied to the output terminal).

[0056] Thus, the source wiring 14 is driven in the state of the driving ability of 80% during the prescribed period where the level of the control signal Cont 2 is at a pre-scribed level.

[0057] Upon completion of the prescribed period, the timing control circuit 40 controls the level of the control signal Cont 2 to be at a level other than the prescribed level, in this example, the level other than the prescribed level is (H, H).

[0058] Referring to Figs. 5 and 6, in the output buffer 251 in the buffer circuit 25, the first switch 263 becomes a closed state (a state where the input to the amplifier 261 is supplied to the output terminal), and the second switch 264 becomes an open state (a state where the output of the amplifier 261 will not be supplied to the output terminal). Accordingly, the source wiring 14 is driven by a voltage signal from the D-A converter 24.

[0059] The driving ability by the voltage signal from the D-A converter 24 is lower than the driving ability when the level of the control signal Cont 2 is (H, L), and accordingly, after completion of the prescribed period, the source wiring 14 is driven by a lower driving ability. As a result, consumption current of the source driver 20 becomes low.

[0060] Fig. 9 is a schematic diagram which schematically illustrates consumption current when column inver-
power increases. As shown in Fig. 9, when column inversion driving is employed as AC driving, consumption current during the display period is small as compared with the case of employing other AC driving such as dot inversion driving. That is, the source wiring 14 can be driven even in a state where the driving ability is low in the display period. Further, in a case where dot inversion driving is employed to carry out polarity inversion for every pixel, the output voltage amplitude of the source driver 20 becomes large, and the consumption power increases.

[0061] As shown in Fig. 9, in the column inversion driving, the polarity of source lines is inverted for every frame. That is, at the time of initiation of the display period, for example, transfer from positive polarity to negative polarity is required, and a rush current will flow (see A in Fig. 9). If the driving ability of the output buffer 251 is low, it becomes difficult to deal with the rush current, and the driving voltage of the source driver 20 decreases for a moment, thus leading to a deterioration of the display quality. Therefore, as described above, for a prescribed period after initiation of the display period, the driving ability (output current) of the source driver 20 is made high. And, thereafter, the source wiring 14 can be driven by a low driving ability, whereby consumption current can be reduced.

[0062] Further, as described above, the potential of each source wiring 14 is adjusted to be close to the common voltage \( V_{COM} \) before initiation of the display period, by the charge sharing in the vertical blanking period, whereby the rush current at the initiation of the display period is reduced. Thus, it is possible to reduce the degree of rising of the driving ability in the prescribed period after initiation of the display period. That is, in the prescribed period after initiation of the display period, the driving ability of the output buffer 251 is increased, but is not required to be increased so much.

[0063] However, even in a case where no charge sharing is carried out in the vertical blanking period, it is effective to control the driving ability of the source driver 20 to be high in a prescribed period after initiation of the display period.

[0064] Further, in a prescribed period (e.g. a period of at least one horizontal period) after initiation of the display period, the source wiring 14 is driven at 80% of the driving ability exemplified in Fig. 6(B), but in the example shown in Fig. 6(B), the source wiring 14 may be driven by a driving ability of 100% or 130%. Further, in a prescribed period after initiation of the display period, the source wiring is driven in a state of a driving ability of 80%, and after expiration of the prescribed period, the source wiring 14 is driven by a voltage signal from the D-A converter 24, but so long as the driving ability in the prescribed period is higher than the driving ability after expiration of the prescribed period, a combination other than the combination of the driving ability of 80% and the driving ability of a voltage signal from the D-A converter 24, may be used.

[0065] As one example, in a prescribed period after initiation of the display period, driving is carried out in a state of a driving ability of 130% or 100% (see Fig. 6), and after expiration of the prescribed period, driving may be carried by a driving ability of 80%. In such a case, the first switch 263 and the second switch 264 shown in Fig. 5 are unnecessary, and a voltage signal from the D-A converter 24 is always applied to the source wiring 14 via the amplifier 261, and in the period where the driving ability is made high, the amplifier 261 applies a signal of a voltage corresponding to a data signal to the source wiring 14 in a state where the output current is increased as compared with the output current in the period after such a period.

[0066] Further, in this example, charge sharing is carried out in the vertical blanking period, but instead of the charge sharing, precharging may be carried out wherein a prescribed precharge voltage (e.g. the common voltage \( V_{COM} \)) is applied to the source wiring 14. In a case where such precharging is to be carried out, in the construction shown in Fig. 7, instead of the third switch 267, a fourth switch is provided to switch the state to a state where the precharge voltage is connected to the source wiring 14 or a state where the precharge potential is not connected to the source wiring 14. And, when the control signal Cont 1 becomes a high level, in the buffer circuit 25, the first output switch 266 becomes an open state (the same applies to the second output switch 268) (see Fig. 7), and the fourth switch becomes a state where the source wiring 14 is connected to the precharge voltage.

[0067] In such a case, the first output switch 266, the second output switch 268 and the fourth switch, correspond to a source wiring initial setting unit to connect each source wiring 14 to a prescribed potential.

[0068] As described in the foregoing, in this example, the source driver 20 makes, as compared with the driving ability in at least a period to drive the first one line in each frame i.e. in a period of at least a period to drive one line, the driving ability to be low in a period after such a period. In other words, the driving ability in at least a period to drive the first one line in each frame, is made to be higher than the driving ability in a period after such a period, whereby with a simple construction, it is possible to reduce power consumption while preventing deterioration of the display quality.

EMBODIMENT OF THE INVENTION: EMBODIMENT 2

[0069] In the above described example, the drive device is designed to carry out a control in such a manner that in a prescribed period (specifically an initial period being a period of at least a period to drive one line) after initiation of the display period, a source wiring 14 is driven by e.g. a driving ability of 80% as shown in Fig. 6(B) (corresponding to a high driving ability), and upon expiration of the prescribed period, the source wiring 14 is driven by a voltage signal from the D-A converter 24 (corresponding to a low driving ability). While in the pre-
scribed period (initial period), the control is carried out by such a high driving ability, in a period after expiration of the prescribed period, a control different from the case after expiration of the prescribed period in the first example may be carried out.

[0070] In the second embodiment, in the period subsequent to the prescribed period, while in a first half interval in each periodically occurring period, a source wiring 14 is driven by a high driving ability, in a second half interval, the source wiring 14 is driven by a low driving ability as compared with the first half interval.

[0071] Here, in order to make the description simple, in the following description, each periodically occurring period is regarded as a period to drive each line (a period for each line).

[0072] As an example useful for understanding the invention, the operation of the source driver 20 in will be described with reference to the timing diagrams in Figs. 10 and 11. The timing diagram in Fig. 11 is one wherein the periods for the first to third lines in each frame disclosed in Fig. 10 are shown as enlarged. Here, in Fig. 10, the control signal Cont 2 is at a prescribed level only in the period for the first line. However, in this embodiment, the control signal Cont 2 is utilized to realize such a control that in a period subsequent to the period for the first line, in the first half interval, the source wiring 14 is driven by a high driving ability, and in the second half interval, the source wiring 14 is driven by a low driving ability, and accordingly, in an actual operation, the control signal becomes a prescribed level also in the period for the second and subsequent line periods as shown in Fig. 11.

[0073] Further, in Figs. 10 and 11, a period wherein the level of the control signal Cont 2 is at a prescribed level is shown as a high level period, but as described hereinafter, the prescribed level may not practically be a high level. Further, a period wherein the level is not a prescribed level is shown as a low level period, but such a period may not practically be a low level. Further, “change” indicated in Fig. 11 means that the length of the first half interval may optionally be set.

[0074] The constructions of the source driver 20 and the gate driver 30 are the same as their constructions in the first embodiment shown in Fig. 1. The constructions of the amplifier 261 and its output side are the same as their constructions in the first embodiment shown in Figs. 5 and 7. The construction of the timing control circuit 40 is the same as the construction of the timing control circuit 40 in the first embodiment shown in Fig. 1 except that the manner of the output of the control signal in periods for the second line and subsequent lines is partially different, as will be described hereinafter. Further, the examples shown in Fig. 6 are used for the relation between the signal state of the control signal Cont 2 and the output state of the amplifier 261, and the output state of the amplifier 261.

[0075] Hereinafter, description will be made by paying attention to two output buffers 251 and 252 (see Figs. 5 and 7) in the buffer circuit 25, but output buffers other than the two output buffers 251 and 252 in the buffer circuit 25 will operate in the same manner as the output buffers 251 and 252.

[0076] As shown in Fig. 10, the timing control circuit 40 controls the control signal Cont 1 to be at a high level during at least for one horizontal period in the vertical blanking period. Depending upon the state of the control signal Cont 1, charge sharing may be carried out by setting the contact state of the output buffers 251 and 252 in the same manner as in the first embodiment.

[0077] Further, also in this embodiment, as shown in Fig. 10, the timing control circuit 40 controls the level of the control signal Cont 2 to be a prescribed level over a prescribed period of at least one horizontal period from the initiation of the control for the image display in each frame i.e. in a prescribed period (a period for the first line) after initiation of driving in the first frame. In this embodiment, the prescribed level is (H, L).

[0078] Thus, in the same manner as in the case of the first example, the source wiring 14 is driven in a state of the driving ability of 80% during a prescribed period wherein the level of the control signal Cont 2 is a prescribed level.

[0079] In the first example, the timing control circuit 40 controls the level of the control signal Cont 2 to be a level other than the prescribed level upon completion of the prescribed period. Specifically, the level of the control signal Cont 2 is adjusted to be (H, H). Thus, the source wiring 14 is driven by a voltage signal from the D-A converter 24 (see Fig. 6).

[0080] That is, in the first example, the timing control circuit 40 is controlled so that the source wiring 14 is driven by a low driving ability over the entire period in the period for the second line et seq.

[0081] However, in this embodiment, in each period for the second line or subsequent line, in the first half interval, the source wiring 14 is driven by a high driving ability, but in a second half interval, the source wiring 14 is driven by a low driving ability as compared with the first half interval, and accordingly, the manner for the output of the control signal Cont 2 is made different from the case of the first embodiment.

[0082] That is, as shown in Fig. 11, in the second and subsequent lines, in a prescribed period (a first half interval) from initiation of the driving of each line, the timing control circuit 40 adjusts the level of the control signal Cont 2 to a prescribed level. In this embodiment, the prescribed level is (H, L) (see Figs. 6(A) and (B)). Further, upon completion of the first half interval, the level of the control signal Cont 2 is adjusted to (H, H). Thus, in the second half interval, the source wiring 14 is driven by a low driving ability (see Figs. 6(A) and (B)).

[0083] In this embodiment, as compared with the first example, power consumption is reduced in consideration of the properties of the liquid crystal display panel 10. That is, in a case where if the first example is applied, the electric current tends to be inadequate, thus leading
to a phenomenon such as deterioration of the display quality, due to such a cause that the size or the number of pixels of the liquid crystal display panel 10 is large, by applying this embodiment, an increase of the power consumption can be controlled by not driving by a high driving ability over the entire period of one frame, while preventing deterioration of the display quality by prolonging the period of driving at a high driving ability, as compared with the first embodiment.

Further, in the periods of the second and subsequent lines, after the timing control circuit 40 has adjusted the output level of the control signal Cont 2, by changing the period to release the prescribed level output (corresponding to the timing of completion of the first half interval), it is possible to change the length of the period where the driving ability is made high (i.e. the first half interval). Thus, depending upon e.g. the size or the number of pixels of the liquid crystal display panel 10, it is possible to adjust the length of the first half interval. That is, it becomes possible to realize a fine control to reduce consumption current while preventing deterioration of the display quality. For example, the first half interval is prolonged, in a case where if the period where the driving ability is made high, is shortened too much in order to reduce consumption current, the display quality becomes lower than the desired quality.

As a construction to realize the control to adjust the length of the first half interval, there is, for example, a construction wherein a control input terminal is provided in the timing control circuit 40. In such a case, the timing control circuit 40, after adjusting the output level of the control signal Cont 2 to a prescribed level, counts the number of pulses of the block signal and releases the prescribed level output when the counted value becomes a preliminarily determined value corresponding to the type of signal (specifically the type of the signal level) input in the control input terminal. When such a construction is taken, by the timing control circuit 40, the interval adjusting means to adjust the length of the first half interval, is realized.

Further, in this embodiment, the control signal Cont 2 is utilized to realize the control to drive a source wiring 14 by a high driving ability in the first half interval and to drive the source wiring 14 by a low driving ability in the second half interval. However, a practical method is not limited to such a method of using the control signal Cont 2. For example, as shown in Fig. 12, the timing control circuit 40 may be designed so that in the periods of the second and subsequent lines, the first half interval or the second half interval is set by a control signal Cont 3 separate from the control signal Cont 2. When the control signal Cont 3 is used, the timing control circuit 40 adjusts the level of the control signal Cont 3 to a prescribed level in a prescribed period (the first half interval). In this embodiment, the prescribed level is (H, L) (see Figs. 6(A) and (B)). Further, upon completion of the first half interval, the level of the control signal Cont 3 is adjusted to (H, H). Thus, in the second half interval, the source wiring 14 is driven by a low driving ability (see Figs. 6(A) and (B)).

Further, in the periods of the second and subsequent lines, without using the control signal Cont 2 or the control signal Cont 3, the buffer circuit 25 may input e.g. a clock signal CLK for data shift and counts the number of times of rising or falling of the clock signal CLK, whereby the timing for completion of the first half interval may be independently set. When such a construction is adopted, it is possible that by the buffer circuit 25, an interval-adjusting means to adjust the length of the first half interval, is realized.

Further, in this embodiment, in the first half interval, the source wiring 14 is driven by a driving ability of 80% as exemplified in Fig. 6(B), but the source wiring 14 may be driven by a driving ability of 100% or 130% in an example shown in Fig. 6(B). Further, in this embodiment, driving is carried out in a state of a driving ability of 80% in the first half interval, and in the second half interval, the source wiring 14 is driven by a voltage signal from the D-A converter 24, but provided that the driving ability in the second half interval is higher than the driving ability in a prescribed period after initiation of the display period (e.g. the first line period) and the driving ability in the first half interval, a combination other than the combination of the driving ability of 80% and the driving ability of the voltage signal from the D-A converter 24, may be employed.

As an example, the combination may be such that in the first half interval, driving is carried out in a state of a driving ability of 130% or 100% (see Fig. 6), and in the second half interval, the driving is carried out in a state of a driving ability of 80%.

Further, in this embodiment, the driving ability in a prescribed period (initial period) after initiation of the display period and the driving ability in the first half interval in a period subsequent to the prescribed period, may made to be the same, but the driving ability in the first half interval is made lower than the driving ability in the initial period. Further, in a case where the first half interval or the second half interval is designed to be set by a control signal Cont 3 separate from the control signal Cont 2, it is easier to carry out such a control that the driving ability in the first half interval is made different from the driving ability in the initial period.

Further, in the foregoing description, the liquid crystal display panel 10 may be either a monochromatic panel or a color panel.

INDUSTRIAL APPLICABILITY

The present invention is applicable to a liquid crystal display device to be mounted on portable devices, in-vehicle devices, image display devices, etc.

REFERENCE SYMBOLS
10: Liquid crystal display panel
20: Source driver
21: Shift register
22: First latch circuit
23: Second latch circuit
24: D-A converter
25: Buffer circuit
30: Gate driver
40: Control unit (timing control circuit)
251, 252: Output buffer
261: Amplifier
262: Bias circuit
263: First switch
264: Second switch
266: First output switch
267: Third switch
268: Second output switch

Claims

1. A drive device for a liquid crystal display panel (10) having a plurality of gate wirings (13) and a plurality of source wirings (14) arranged to intersect with each other, the drive device comprising a source driver (20) adapted to drive the source wirings (14), wherein:

   the source driver (20) is adapted to drive the source wirings by column inversion and to invert the polarity in every one frame,
   the device is adapted to control the source driver (20) during an initial period and during a plurality of periodically occurring periods subsequent to the initial period in each frame, the source driver (20) is adapted to drive in each frame at least a first one horizontal line during the initial period and a subsequent horizontal line during each period subsequent to the initial period, respectively, wherein each said period subsequent to the initial period comprises a first half interval and a second half interval, the device is adapted to control the source driver (20) so that in each frame the driving ability in the initial period is higher than the driving ability in each first half interval and the driving ability in each first half interval is higher than the driving ability in each second half interval, and the source driver (20) includes interval adjusting means for adjusting the length of the first half interval depending upon the size or the number of pixels of the liquid crystal display panel.

2. The drive device for a liquid crystal display panel (10) according to Claim 1, wherein the source driver (20) includes a source wiring initial setting unit which, in a vertical blanking period, short-circuits adjacent source wirings (14), or connects each source wiring (14) to a prescribed potential.

Patentansprüche

1. Eine Treiber-Vorrichtung für eine Flüssigkristall-Anzeigetafel (10) die eine Vielzahl an Gate-Verdrahtungen (13) und eine Vielzahl an Source-Verdrahtungen (14) aufweist, die angeordnet sind, um sich zu überschneiden, wobei die Treiber-Vorrichtung einen Source-Treiber (20) umfasst, der angepasst ist, um die Source-Verdrahtungen (14) anzusteuern, wobei:

   der Source-Treiber (20) angepasst ist, um die Source-Verdrahtungen durch Spalteninversion anzusteuern und um die Polarität in jedem einzelnen Frame (frame) zu invertieren, die Treiber-Vorrichtung angepasst ist, um den Source-Treiber (20) während eines Anfangszeitraums und während einer Vielzahl von periodisch auftretenden Zeiträumen im Anschluss an den Anfangszeitraum in jedem Frame zu steuern, der Source-Treiber (20) angepasst ist, um in jedem Frame mindestens eine erste horizontale Linie während des Anfangszeitraums und je- weils eine nachfolgende horizontale Linie in jedem Zeitraum nach dem Anfangszeitraum anzusteuern, wobei jeder genannte Zeitraum nach dem Anfangszeitraum ein erstes Halbintervall und ein zweites Halbintervall umfasst, die Treiber-Vorrichtung angepasst ist, um den Source-Treiber (20) anzusteuern, sodass in jedem Frame die Ansteuerfähigkeit im Anfangszeitraum besser ist als die Ansteuerfähigkeit in jedem ersten Halbintervall und sodass die Ansteuerfähigkeit in jedem ersten Halbintervall besser ist als die Ansteuerfähigkeit in jedem zweiten Halbintervall, und wobei der Source-Treiber (20) Intervalleinstellungs- mittel zur Einstellung der Länge des ersten Halbintervalls in Abhängigkeit der Größe oder der Anzahl von Pixeln der Flüssigkristall-Anzeigetafel.

2. Die Treiber-Vorrichtung für eine Flüssigkristall-Anzeigetafel (10) nach Anspruch 1, wobei der Source-Treiber (20) eine Source-Verdrahtungs-Anfangs- wert-Einstelleinheit enthält, die in einer vertikalen Austastperiode, angrenzende Source-Verdrahtungen (14) kurzschließt oder jede Source-Verdrahtung (14) mit einem vorgegebenen Potenzial verbindet.

Revendications

1. Un dispositif d’attaque pour un panneau d’affichage...
à cristaux liquides (10) présentant une pluralité de câblages de grille (13) et une pluralité de câblages de source (14) disposés de manière à s’entrecroiser, le dispositif d’attaque comprenant un pilote de source (20) adapté pour piloter les câblages de source (14), sachant que :

le pilote de source (20) est adapté pour piloter les câblages de source par inversion de colonne et pour inverser la polarité dans chaque cadre (frame),

le dispositif d’attaque est adapté pour commander le pilote de source (20) pendant une période initiale et pendant une pluralité de périodes survenant périodiquement consécutivement à la période initiale dans chaque cadre, le pilote de source (20) est adapté pour piloter dans chaque cadre au moins une première ligne horizontale pendant la période initiale, et respectivement une ligne horizontale suivante pendant chaque période postérieure à la période initiale, sachant que chaque période nommée postérieure à la période initiale comprend un premier demi intervalle et un deuxième demi intervalle, le pilote de source (20) est adapté pour commander le pilote de source (20) de manière que dans chaque cadre l’aptitude à l’attaque pendant la période initiale est supérieure à l’aptitude à l’attaque dans chaque premier demi intervalle, et que l’aptitude à l’attaque dans chaque premier demi intervalle est supérieure à l’aptitude à l’attaque dans chaque deuxième demi intervalle, et que le pilote de source (20) inclut des moyens d’ajustage d’intervalle pour ajuster la longueur du premier demi intervalle en fonction de la dimension ou du nombre de pixels du panneau d’affichage à cristaux liquides.

2. Le dispositif d’attaque pour un panneau d’affichage à cristaux liquides (10) d’après la revendication 1, sachant que le pilote de source (20) inclut une unité de réglage initial de câblage de source, laquelle, pendant une période d’effacement vertical, court-circuite des câblages de source (14) adjacents ou bien connecte chaque câblage de source (14) à un potentiel prescrit.
Fig. 1
Fig. 4

Fig. 5

FROM D-A CONVERTER

 Cont2

261

262

BIAS

263

251

264
Fig. 6

(A)  

<table>
<thead>
<tr>
<th>Cont2</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

(B)  

<table>
<thead>
<tr>
<th>OUTPUT</th>
<th>DRIVING ABILITY</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>130%</td>
</tr>
<tr>
<td>B</td>
<td>100%</td>
</tr>
<tr>
<td>C</td>
<td>80%</td>
</tr>
<tr>
<td>D</td>
<td>*</td>
</tr>
</tbody>
</table>

* D-A CONVERTER OUTPUT

Fig. 7

Fig. 8

<table>
<thead>
<tr>
<th>Cont1</th>
<th>SW266</th>
<th>SW267</th>
<th>SW268</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
</tr>
<tr>
<td>H</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
</tr>
</tbody>
</table>

(ON: CLOSED, OFF: OPEN)
Fig. 9

![Vertical Synchronizing Signal](image)

Fig. 10

![Waveform Diagram](image)

** Cont1 ** POL

** STB **

** S (2n-1) **

** S (2n) **

** Cont2 **

---

** First Frame ** ** Second Frame ** ** Third Frame ** ** Fourth Frame **

---

** AT LEAST 1H **

** 1H **

** Partly C/Rest D **
REFERENCES CITED IN THE DESCRIPTION

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