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(54) Title: LOW POWER RADIO FREQUENCY DIVIDER

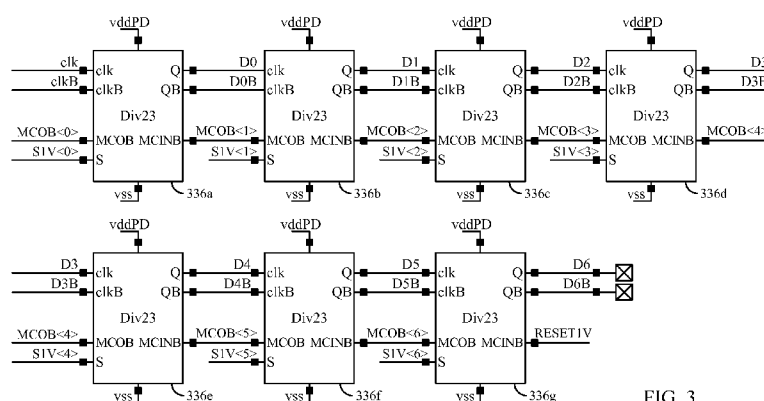


FIG. 3

(57) Abstract: In accordance with the present disclosure, a multi-modulus divider (MMD) circuit configured for operation at high frequencies may include a cascade of multiple divide-by-2-or-3 cells that divides an input clock signal to produce a pulse signal. The MMD circuit may also include a pulse stretching circuit that extends the duration of the pulse signal, thereby outputting an output clock signal. The cascade of divide-by-2-or-3 cells and the pulse stretching circuit may be implemented using full-swing complementary metal-oxide-semiconductor (CMOS) circuits. Each divide-by-2-or-3 cell may be organized so that a critical path of the divide-by-2-or-3 cell comprises a first dynamic flip flop, a second dynamic flip flop, and no more than two logic stages between the first dynamic flip flop and the second dynamic flip flop.