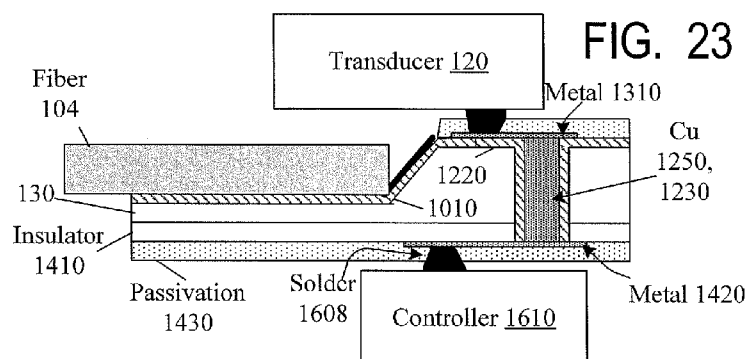




- (51) **International Patent Classification:**  
*G02B 6/42* (2006.01) *G02B 6/36* (2006.01)
- (21) **International Application Number:**  
PCT/US2013/020578
- (22) **International Filing Date:**  
7 January 2013 (07.01.2013)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**  
61/585,217 10 January 2012 (10.01.2012) US  
13/362,898 31 January 2012 (31.01.2012) US  
13/454,713 24 April 2012 (24.04.2012) US
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- (81) **Designated States** (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States** (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:**  
— with international search report (Art. 21(3))

(54) Title: OPTICAL INTERPOSER



(57) **Abstract:** An optical interposer includes grooves (310) for optical fiber cables (104) coupled to a transducer (120). The grooves are formed by etching a cavity (410) in a substrate (130), filling the cavity with some layer (520), then etching the layer to form the grooves. The cavity has outwardly sloped sidewalls on which mirrors (144) are later formed. The groove etch is selective not to damage the sidewalls. The groove depth is uniform due to high etch selectivity of the layer, and also because of good control over the cavity etch due to the low aspect ratio of the cavity. Electrical circuitry for connection to the transducer is fabricated after the cavity filling but before the groove etch. The cavity filling leaves the wafer planar, facilitating fabrication of the electrical circuitry. Grooves can be provided on top and bottom of the interposer.

## OPTICAL INTERPOSER

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** The present application claims priority of the following patent applications:

- U.S. provisional patent application no. 61/585,217 filed by V. Kosenko et al. on  
5 January 10, 2012, incorporated herein by reference;
  - U.S. patent application no. 13/362,898, filed January 31, 2012, incorporated herein by reference; and
  - U.S. patent application no. 13/454,713, filed April 24, 2012, incorporated herein by reference.
- 10 For the U.S. designation, the present application is a continuation of the aforementioned U.S. patent application no. 13/362,898.

## BACKGROUND OF THE INVENTION

**[0002]** The present invention relates to optical interposers for providing interface between optical fibers and electrical circuits. (The terms “optical” and “light” as used  
15 herein denote electromagnetic radiation of any spectrum, not limited to visible light; the terms “optical fiber” or just “fiber” denote an optical fiber cable.)

**[0003]** Fiber optics is increasingly used to transmit information to and from electrical circuits. Energy conversion between optical fiber and electrical circuitry is performed by opto-electrical transducers. Miniature packages have been created which combine the  
20 transducers, the optical fiber, and electrical circuitry to achieve high speed and low power losses. One example is described in Hsu-Liang Hsiao et al., “Compact and passive-alignment 4-channel x 2.5-Gbps optical interconnect modules based on silicon optical benches with 45° micro-reflectors”, OPTICS EXPRESS, 21 December 2009, Vol. 17, No. 26, pages 24250-24260, illustrated in Figs. 1-3.

**[0004]** Fig. 1 shows optical fibers 104 (104.1 and 104.2) used to interconnect  
25 integrated circuits (chips) 110.1, 110.2 mounted on respective printed circuit boards (PCBs) 114.1, 114.2. Chip 110.1, fiber 104.1, and PCB 114.1 are part of a signal transmitting module 116.1. Chip 110.2, fiber 104.2, and PCB 114.2 are part of a signal receiving module 116.2. Electrical signals from chip 110.1 are provided to an opto-  
30 electronic transducer 120.1 for conversion to light. Transducer 120.1 is an integrated circuit (IC or “chip”) containing a semiconductor laser (vertical-cavity surface emitting laser, “VCSEL”). Transducer 120.1 is mounted on a silicon interposer (silicon optical

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bench, or SiOB) 124.1 made using a silicon substrate 130.1. Conductive lines 134.1 transmit electrical signals from chip 110.1 to transducer 120.1. In response, the transducer produces optical signals in a vertical light beam 140.1. Light beam 140.1 is reflected by a mirror 144.1 formed of a gold layer deposited on the silicon interposer's surface inclined at 45° to the horizontal. The reflected beam from mirror 144.1 enters the optical fiber 104.1.

[0005] Fiber 104.1 is connected to a fiber 104.2 of module 116.2 by a connector 150. Module 116.2 is similar to module 116.1. The optical signals are emitted from fiber 104.2 in a horizontal beam 140.2, which is reflected by a 45° mirror 140.2 to travel vertically to a transducer 120.2. The mirror is part of a silicon interposer 124.2 made using silicon substrate 130.2. Transducer 120.2 is mounted on interposer 124.2. Transducer 120.2 is a photodetector integrated circuit which converts the optical signals into electric signals provided, via conductive lines 134.2, to chip 110.2. Interposer 124.2 and chip 110.2 are mounted on PCB 114.2.

[0006] Figs. 2 and 3 illustrate a module 116 which can be 116.1 or 116.2. Fig. 2 is a top view, and Fig. 3 shows a cross section by a plane transversal to fibers 104. Each module 116.1, 116.2 has four fibers 104 (i.e. 104.1 or 104.2); transducer 120.1 has four lasers emitting four respective beams 140.1 entering four respective fibers 104.1; transducer 120.2 has four photodetectors which receive four respective beams 114.2 passing through four respective fibers 114.2. As shown in Fig. 2, in each module, monocrystalline silicon substrate 130 having (100)-orientation supports all the four fibers 104. The fibers are mounted in V-grooves 310 formed by a wet etch of substrate 130. The etch also forms the silicon surface underlying the mirror 144. The V-grooves have 45°-sloped sidewalls. The 45° angle is produced due to the crystal structure of the silicon substrate 130, which is a monocrystalline silicon wafer of (100)-orientation. The angle so produced is highly precise, and this helps in precise positioning of fibers 104 because the fibers do not reach the groove bottom and the fiber position is therefore determined by the angle of the grooves' sidewalls (45°) and the groove's width at the top, not by the groove's depth.

## SUMMARY

[0007] This section summarizes some features of the invention. Other features may be described in the subsequent sections. The invention is defined by the appended claims, which are incorporated into this section by reference.

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[0008] Some embodiments of the present invention provide optical interposers and methods of their fabrication that allow precise fiber positioning in grooves of different shapes. For example, rectangular grooves can be used (with vertical sidewalls). Vertical sidewalls may be desirable to reduce the pitch between the adjacent fibers (measured as the distance between the centers of the adjacent fibers or adjacent grooves). For example, in Fig. 3, the width of each groove at the top is greater than each fiber's diameter. If the sidewalls are vertical, then the width of each groove can be equal to the fiber's diameter. A denser, more compact structure can therefore be provided for a given fiber diameter (i.e. the diameter-to-pitch ratio can be increased). Further, if the sidewalls are vertical, then the groove width, and the spacing between the grooves, are independent of the grooves' depth (with V-grooves, the grooves' width at the top increases with depth, and the spacing between the grooves correspondingly decreases). If the groove width and the spacing between the grooves are independent of the grooves' depth, then the fibers' vertical position (defined by the depth) is independent of the spacing between the grooves. This is advantageous because the areas between the grooves can be used for various purposes (e.g. for circuitry or for mechanical support of cantilevered transducers), and the spacing between the grooves can be optimized independently from the fibers' vertical positions.

[0009] However, the invention includes V-groove embodiments, and is not limited to vertical sidewalls or other features described herein except as defined by the claims. Also, in the V-groove embodiments, the sidewall angle may be different than  $45^\circ$ . The angle may be any value. In some embodiments, the angle is above  $85^\circ$  (measured from the horizontal) but not greater than  $90^\circ$ . In other embodiment, the angle is above  $90^\circ$ , i.e. the grooves' sidewalls overhang the grooves. Rounded sidewalls and other groove shapes are also possible. See e.g. U.S. patent no. 6,332,719 issued December 25, 2001 to Nishikawa et al. and U.S. patent no. 8,031,993 issued October 4, 2011 to Bowen, both incorporated herein by reference.

[0010] The interposers can be based on substrates made of silicon or some other semiconductor material, and/or glass, metal, and/or other materials.

[0011] Figs. 4-6 illustrate one embodiment of the present invention in the same cross sectional view (transversally to the fibers) as in Fig. 3. In this embodiment, grooves 310 are formed by two etches as follows:

[0012] First, a cavity 410 is etched in substrate 130. This cavity will eventually house

all the fibers 104. If desired, the cavity sidewalls can be inclined at 45° or some other angle “ $\alpha$ ” to provide mirrors (not shown in Fig. 4) or other elements.

[0013] The cavity is then filled with some material 520 (Fig. 5). Layer 520 is then patterned and etched to form grooves 310 (Fig. 6). The etch is selective to substrate 130.

5 Due to the etch selectivity, the 45° sidewall supporting the mirrors will not be damaged by the etch even though the sidewall is exposed early during the etch.

[0014] In some embodiments, the process is tolerant to misalignment between the cavity mask (the etch mask, not shown, used to form the cavity in Fig. 4) and the groove mask (not shown) because the cavity mask can be shifter right or left in the view of Fig. 6  
10 relative to the groove mask.

[0015] In some embodiments, high depth uniformity is achieved in groove formation for the following reasons. Cavity 410 (Fig. 4) has a low aspect ratio (height-to-depth ratio), so the etch of cavity 410 can be easily controlled to provide a precise uniform depth throughout the cavity. In some embodiments, the aspect ratio is at most 1:2. The  
15 etch of layer 520 can also be easily controlled because this etch is selective to substrate 130 serving as an etch stop. For example, substrate 130 can be silicon, and layer 520 silicon dioxide. Depending on the materials involved, the etch selectivity can be improved by forming an additional etch-stop layer on cavity 410 before deposition of layer 520. In some embodiments, the etch selectivity is at least 2:1.

20 [0016] Further, in some embodiments, the process of Figs. 4-6 is easy to integrate with other steps that form conductive lines or other circuitry in or over substrate 130. Such circuitry can be formed between the stages of Figs. 5 and 6, i.e. after the deposition of layer 520 before the groove etch. The wafer is flat at this stage, and many conventional processes for circuit fabrication work better on flat wafers. (We will sometimes refer to  
25 substrate 130 together with other elements integral with the substrate as a “wafer”; in some embodiments multiple interposers are simultaneously fabricated in the same wafer.) In particular, wafer handling and photolithography work better with flat wafers. The material 520 can be chosen consistently with the processes forming other circuitry. For example, if high temperatures are required by these processes, the material 520 can be  
30 chosen to withstand high temperatures. If mirrors 144 (not shown in Figs. 4-6) or other elements need to be formed of non-refractory metal (such as gold), the metal deposition can be postponed until after the high temperature steps.

[0017] Fig. 7 is a view of an interposer 124 with a mirror 144 and a fiber or fibers

104 in a cross section taken along a fiber 104. The fibers are inserted into grooves 310 from the interposer's left side. The cavity 410 does not have a sidewall on that side. The cavity is initially formed with the sidewalls on all sides (Fig. 4), but one side is then removed during dicing of wafer 130. More particularly, one sidewall of cavity 410 is positioned on the wafer's scribe line. This sidewall is removed by the dicing process.

[0018] The invention is not limited to the features and advantages described above except as defined by the appended claims.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0019] Fig. 1 shows a vertical cross section of an opto-electrical system according to prior art.

[0020] Fig. 2 is a top view of a part of the system of Fig. 1.

[0021] Fig. 3 shows a vertical cross section of a part of the system of Fig. 1.

[0022] Figs. 4-6 show vertical cross sections of optical interposers during fabrication according to some embodiments of the present invention.

[0023] Fig. 7 shows a vertical cross section of an optical interposer with fibers according to some embodiments of the present invention.

[0024] Fig. 8 shows a vertical cross section of an optical interposer during fabrication according to some embodiments of the present invention.

[0025] Fig. 9 is a top view of an optical interposer during fabrication according to some embodiments of the present invention.

[0026] Figs. 10, 11, 12, 13, 14, 15, 16 show vertical cross sections of optical interposers during fabrication according to some embodiments of the present invention.

[0027] Fig. 17A is a top view of an optical interposer during fabrication according to some embodiments of the present invention.

[0028] Fig. 17B shows a vertical cross section of an optical interposer during fabrication according to some embodiments of the present invention.

[0029] Figs. 18, 19 are top views of optical interposers during fabrication according to some embodiments of the present invention.

[0030] Fig. 20 is a top view of an optical interposer with fibers according to some embodiments of the present invention.

[0031] Fig. 21 is a top view of a module with an optical interposer according to some embodiments of the present invention.

[0032] Figs. 22, 23 show vertical sections of modules with optical interposers

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according to some embodiments of the present invention.

[0033] Fig. 24 is a top view of an optical interposer according to some embodiments of the present invention.

5 [0034] Fig. 25 is a top view of an optical interposer with fibers according to some embodiments of the present invention.

[0035] Fig. 26 is a top view of a module with an optical interposer according to some embodiments of the present invention.

[0036] Fig. 27 shows possible spacer shapes in top view for optical interposers according to some embodiments of the present invention.

10 [0037] Fig. 28 is a top view showing some features of an optical interposer with fibers according to some embodiments of the present invention.

[0038] Figs. 29, 30 show vertical cross sections of optical interposers during fabrication according to some embodiments of the present invention.

15 [0039] Fig. 31 is a top view of an optical interposer according to some embodiments of the present invention.

[0040] Figs. 32, 33, 34, 35A, 35B, 35C, 35D, 35E, 35F, 36, 37, 38, 39A, 39B, 39C show vertical cross sections of optical interposers during fabrication according to some embodiments of the present invention.

20 [0041] Fig. 40 is a top view of an optical interposer during fabrication according to some embodiments of the present invention.

[0042] Figs. 41, 42 show vertical cross sections of optical interposers according to some embodiments of the present invention.

[0043] Fig. 43 is a top view of an optical interposer during fabrication according to some embodiments of the present invention.

## 25 DESCRIPTION OF SOME EMBODIMENTS

[0044] The embodiments described in this section illustrate but do not limit the invention. The invention is not limited to particular materials, dimensions, process steps, or other features except as defined by the appended claims.

30 [0045] Fig. 8 (cross sectional view) and Fig. 9 (top view) illustrate substrate 130 with cavity 410 at the beginning stages of fabrication of an optical interposer according to some embodiments of the present invention. Substrate 130 can be silicon, silicon on insulator (SOI), glass, metal, or other materials. In some embodiments, substrate 130 is part of a wafer in which multiple interposers are simultaneously fabricated. In an

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exemplary embodiment discussed immediately below, substrate 130 is monocrystalline silicon having a thickness of 750  $\mu\text{m}$ .

5 [0046] Substrate 130 is initially planar on top and bottom. Cavity 410 is formed by a masked timed etch. More particularly, substrate 130 is cleaned, and a masking layer 810 is deposited on the entire top surface to provide a hard mask. In some embodiments, layer 810 is silicon dioxide thermally grown to an exemplary thickness of 1.0  $\mu\text{m}$ , but silicon nitride and other layers and fabrication processes can also be used. (Layer 810 is optional, and can be omitted; the hard mask may or may not be desirable depending on the type of etch used to form the cavity, the cavity depth, the material of substrate 130, and possibly other factors.)

10 [0047] Masking layer 810 is patterned with photoresist (not shown) to define cavity 410. The photoresist is removed, and substrate 130 is etched through the mask opening to form the cavity. The cavity has a horizontal bottom surface (parallel to the substrate's bottom surface) and sloped sidewalls 910.1 through 910.4 that are inclined at an exemplary angle of  $45^\circ$  to the bottom surface of the substrate. The mirrors will be formed on one of these sidewalls, e.g. on sidewall 910.2. (The invention is not limited to a cavity having four sidewalls; the cavity can be non-rectangular in top view, and may have rounded and other shapes.)

15 [0048] An exemplary etch of cavity 410 is wet etch which provides the  $45^\circ$  sidewalls if wafer 130 is a common (100)-silicon wafer. A suitable wet etch is KOH with Isopropyl Alcohol as an additive. The etch is timed to provide the desired cavity depth. In some embodiments, the cavity depth is 100  $\mu\text{m}$ , and the etching time is about 100 minutes. Other etching processes can also be used. See e.g. Hsiao et al. cited above. The cavity depth can be any suitable value, e.g. 100 to 500  $\mu\text{m}$  or smaller or larger. In some 25 embodiments, the cavity is rectangular, and the dimensions of the cavity's top surface are 2.1 mm along the sidewall 910.1 and 2.0 mm along the sidewall 910.2, but other shapes and dimensions are possible. The aspect ratio of the cavity is thus about 1:21. The low aspect ratio is desirable to provide a uniform, highly controllable cavity depth. Other aspect ratios can also be used.

30 [0049] Then an optional etch stop layer 1010 (Fig. 10) is deposited over the substrate to provide an etch stop in subsequent etch of layer 520 (Figs. 5, 6). In some embodiments, layer 520 will be polysilicon, and layer 1010 is silicon dioxide thermally grown on silicon substrate 130 to a thickness of 2.0  $\mu\text{m}$  or deposited by CVD (e.g. from TEOS). The

thickness of layer 810 increases in this step.

5 [0050] The material of layer 520 is chosen for compatibility with other fabrication processes that will form circuitry in substrate 130. Polysilicon is desirable for its tolerance to high temperatures such as present in thermal oxidation of silicon. Polysilicon is also easy and inexpensive to deposit. In some embodiments, layer 520 will be used to provide mechanical support for a cantilevered transducer 120 as described below but will not be used to provide semiconductor circuit elements such as transistor regions. Low quality polysilicon and inexpensive deposition methods can therefore be used. In particular, layer 520 can be metallurgical polysilicon formed by LTCVD (Low  
10 Temperature Chemical Vapor Deposition). Another possibility is polysilicon deposited by high temperature (1200°C) CVD. Other processes can also be used. Layer 520 can be amorphous silicon or polysilicon having very small fine size (nano-grain), or can be epitaxially grown silicon, or other kind. Other suitable materials include polyimide and photoresist (especially if high temperatures will not be used). Other materials are also  
15 possible.

[0051] In embodiments other than discussed immediately below, one or more (possibly all) process steps that form the circuitry in substrate 130 are performed before or during the deposition of layer 520, and the material for layer 520 is chosen based on other considerations.

20 [0052] Layer 520 initially covers the whole wafer, but then is polished by chemical mechanical polishing (CMP) stopping on oxide 810. See Fig. 11. Cavity 410 remains filled by layer 520 but layer 520 is removed outside the cavity. In other embodiments, the CMP or other process leaves layer 520 covering the entire wafer, with a planar top surface. (Non-planar top surface is also possible.)

25 [0053] Before etching the layer 520 to form the grooves 310, the wafer is processed to form circuitry for connection to transducer or transducers 120 and possibly for other purposes. The wafer is planar at the stage of Fig. 11, as desirable for many IC fabrication processes. If desired, an additional planar layer (e.g. silicon nitride) can be deposited over the wafer as a protective layer to protect the layer 520.

30 [0054] The wafer can be processed to create circuitry 134 (Fig. 1) or any other desired circuitry, including for example circuit elements both at the top and the bottom of substrate 130, with through-wafer interconnects between such circuit elements. See for example the following U.S. patents incorporated herein by reference:

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- [0055]** No. 7,964,508 (“Dielectric trenches, nickel/tantalum oxide structures, and chemical mechanical polishing techniques”) issued June 21, 2011 to Savastiouk et al.;
- [0056]** No. 7,521,360 (“Electroplating and electroless plating of conductive materials into openings, and structures obtained thereby”) issued April 21, 2009 to Halahan et al.;
- 5 **[0057]** No. 7,241,675 (“Attachment of integrated circuit structures and other substrates to substrates with vias”);
- [0058]** No. 7,186,586 (“Integrated circuits and packaging substrates with cavities, and attachment methods including insertion of protruding contact pads into cavities”);
- [0059]** No. 7,060,601 (“Packaging substrates for integrated circuits and soldering  
10 methods”);
- [0060]** No. 7,034,401 (“Packaging substrates for integrated circuits and soldering methods”);
- [0061]** No. 7,001,825 (“Semiconductor structures having multiple conductive layers in an opening, and methods for fabricating same”);
- 15 **[0062]** No. 6,897,148 (“Electroplating and electroless plating of conductive materials into openings, and structures obtained thereby”);
- [0063]** No. 6,787,916 (“Structures having a substrate with a cavity and having an integrated circuit bonded to a contact pad located in the cavity”).
- [0064]** See also U.S. patent application no. 13/042,186 filed March 7, 2011; and no.  
20 13/181,006 filed July 12, 2011, both filed by V. Kosenko et al. and both incorporated herein by reference.
- [0065]** An exemplary process forming such circuitry is as follows. A via 1210 (Fig. 12) is formed in the top surface of substrate 130 at each location of a desired through-substrate via (through-silicon via if the substrate is made of silicon). The via initially does  
25 not go through the substrate, but is deeper than the substrate’s final thickness (the substrate will be thinned as described below). A silicon dioxide layer 1220 is grown over the substrate by thermal oxidation, at an exemplary temperature of 1100°C for 160 minutes to an exemplary thickness of 1.0 μm. Layer 1220 also forms on polysilicon 520 unless polysilicon 520 is covered by a protective layer described above in connection  
30 with Figs. 10-11 but not shown in the figures. The thermal oxidation increases the thickness of oxide 810 if this oxide is not covered by the protective layer.
- [0066]** Then a seed layer 1230 (e.g. copper) is sputtered on the wafer for subsequent electroplating. A photoresist film 1240 (e.g. dry-film-resist) is deposited on the wafer and

patterned to expose the vias 1210 and adjacent areas. Copper 1250 is electroplated to fill the vias 1210 and protrude above the resist 1240.

[0067] A subsequent stage is illustrated in Fig. 13. More particularly, copper 1250 is polished by CMP to provide a planar top surface. Then resist 1240 is stripped, and copper layers 1250 and 1230 are polished down by CMP to the level of oxide 1220. Oxide 1220 becomes exposed. (Both layers 1250, 1230 remain in vias 1210 but are shown simply at 1250 in some drawings.) Another metal layer 1310 is sputtered on the wafer and patterned photolithographically to form conductive lines that will connect the metalized vias 1210 (i.e. the copper in vias 1210) to transducer contacts and/or other circuit elements (e.g. transistors, resistors, diodes, capacitors, or other elements that can be formed in the interposer). Metal pads 1310 are also formed on oxide 1220 over cavity 1410 to provide mechanical support for cantilevered transducers as described below. These and other metal pads may or may not be part of electrical circuitry and may or may not be connected to other circuit elements. Additional dielectric and metal layers (not shown) can be deposited to create multiple interconnect layers and other circuit elements for circuitry connected to the transducers and for other circuitry. Then a passivation layer 1330 (e.g. polyimide) is formed to cover the top side of the wafer.

[0068] Then (Fig. 14) the wafer is thinned to turn the vias 1210 into through-vias (through holes). Copper 1250 (and 1230) and insulator 1220 protrude down from substrate 130. Then insulator 1410 (e.g. polyimide) is deposited on the bottom surface, and the bottom surface is planarized by CMP which does not remove all of insulator 1410 but exposes the copper. See Fig. 15.

[0069] Metal 1420 (e.g. copper) is deposited (e.g. by physical vapor deposition, "PVD") on the bottom surface of the wafer. Metal 1420 is patterned photolithographically to provide interconnect lines for connecting the metalized vias to a controller chip (shown in Figs. 22, 23) that will control the transducers 120, and possibly to provide other interconnect lines or other circuit elements. Other interconnect layers (not shown) and other circuit elements (e.g. transistors, diodes, resistors, capacitors, etc., not shown) can also be formed at the bottom.

[0070] A passivation layer 1430 (e.g. polyimide) is deposited on the bottom surface and is patterned photolithographically to form contact openings exposing the metal 1420. See Fig. 16. The exposed portions of metal 1420 form contact pads that can be soldered or otherwise attached to the controller chip or other circuits.

**[0071]** The top surface of the wafer is then processed to form contact openings to metal 1310 and to form grooves 310. Fig. 17A is a top view of the resulting structure, and Fig. 17B shows the wafer's cross section perpendicular to the grooves. For example, in some embodiments, the wafer is covered with photoresist (not shown), and the photoresist is patterned to define grooves 310 and the contact openings to metal 1310 (Fig. 16). Passivation 1330 is etched away through the photoresist openings over the grooves to be formed and in the contact openings. Oxide 1220 becomes exposed over the grooves 310. (Alternatively, the etch of passivation 1330 can remove the oxide 1220 over the grooves and expose the layer 520). After the etch of passivation 1330, the photoresist is removed, and another photoresist layer (not shown) is deposited and patterned to define the grooves 310. If oxide 1220 was not removed over the grooves, it is removed at this time to expose layer 520 in the grooves. Layer 520 is etched selectively to the photoresist and to layer 1010 to form the grooves and expose the layer 1010. In this embodiment, the groove sidewalls are vertical, but non-vertical sidewalls are formed in other embodiments. In this embodiment, layer 520 is polysilicon etched by DRIE (deep reactive ion etch), possibly the Bosch process, and layer 1010 is silicon dioxide. The etch selectivity of polysilicon to silicon dioxide is at least 100:1. Other fabrication processes and selectivity values can also be used.

**[0072]** Exemplary dimensions that can be achieved for rectangular grooves 310 with monocrystalline substrate 130 and polysilicon spacers 520, using silicon oxide 1010 as an etch stop, are as follows: the groove width is 135  $\mu\text{m}$ ; the groove pitch (the distance between the centers of adjacent grooves) is 250  $\mu\text{m}$ ; the groove depth is 100  $\mu\text{m}$ . In some embodiments with rectangular grooves, a suitable groove width is 50 to 1000  $\mu\text{m}$ , the groove pitch is 150 to 2000  $\mu\text{m}$ , and the groove depth is 100 to 500  $\mu\text{m}$ . Other ranges are also possible.

**[0073]** A reflective layer (e.g. aluminum, gold, or some other metal) with desired reflectivity properties is deposited and patterned to form mirrors 144 (Fig. 18) at the grooves' ends on the cavity sidewall 910.2.

**[0074]** Then the wafer is diced. In the embodiment of Fig. 18, the left sidewall 910.4 of cavity 410 is on a dice line, so the sidewall 910.4 is removed. See Fig. 19. The grooves 310 become exposed on the left for fiber insertion. Fibers 104 are inserted into the grooves as shown in Fig. 20. Transducer 120 and possibly other circuits are connected to the interposer (to metal contacts 1310, 1420). In the exemplary embodiment of Figs. 21-

23, transducer 120 is flip-chip attached to the top contacts 1310 of the interposer with solder 1604 or some other means, and controller 1610 is flip-chip attached to the bottom contacts 1420 with solder 1608 or some other means. Fig. 21 is the top view; Fig. 22 shows a longitudinal cross section along a spacer 520/1220/1330 between adjacent grooves 310; Fig. 22B shows a cross section along a fiber 104. Multiple transducers, controllers, and other integrated circuits and discrete circuit elements can be connected to the interposer. As seen in Fig. 22, solder 1604 is also placed on metal 1310 over polysilicon spacers 520 to provide mechanical support for supporting cantilevered transducer chip or chips 120 or other circuits that may overlie the cavity 410. The transducer size can therefore be increased without increasing the stress on the transducer and without increasing the overall area of the module.

[0075] The module can be mounted on a PCB or in any other desired way.

[0076] To reduce thermal stresses during fabrication and operation, the materials used in the interposer should preferably have similar thermal expansion coefficients, e.g. substrate 130 can be monocrystalline silicon and spacers 520 can be polysilicon. Also, to reduce thermal and other mechanical stresses during operation, each spacer 520 can be made discontinuous and/or hollow. In addition, discontinuous spacers can define multiple channels overlying each other, as illustrated in Fig. 24 (top view without fibers and transducers), Fig. 25 (top view with two layers of fibers 104 but without transducers), and Fig. 26 (top view with two layers of fibers 104 and two transducers 120). In Figs. 25 and 26, contacts 1310 between the grooves are not shown for simplicity. Grooves 310X and fibers 104X run in the X direction (horizontally in the view of Figs. 24-26) between the spacers. Grooves 310Y and fibers 104Y run in the Y direction over the fibers 104X. Mirrors 144 on side 910.2 are for the bottom fibers 104X. Mirrors 144 on side 910.1 are for the top fibers 104Y. Cavity sidewalls 910.3, 910.4 are removed during dicing or at some other processing stage.

[0077] Discontinuous spacers are less vulnerable to thermal stresses. They can be formed of metal or other materials. They may have any desired shape. Fig. 27 shows some non-limiting examples in top view: A (round spacer), B (parallelogram), C (hexagon), D (half-circle), E (trapezoid), F (half-ring), G (full ring), H (hollow rectangle), and I (hollow circle with a diameter). Spacer J is another hollow rectangle, but the spacer is continuous, i.e. running through the whole cavity. Other shapes can also be used. In side view, the spacers' sidewalls can be vertical or inclined, and can have conical or other

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shapes.

[0078] In Fig. 28 (top view), spacers 520 between each pair of fibers 104 form a double row of discontinuous spacers. Mirrors 144 can optionally be patterned to be a continuous layer on the cavity sidewall if the spacers do not overly the sidewall. The continuous mirror layer can also be provided for continuous spacers.

[0079] Figs. 29-30 illustrate use of SOI (silicon on insulator) substrate 130, having monocrystalline silicon layers 130.1, 130.2 separated by planar insulating layer 2910. The fabrication process is similar to the processes described above. Figs. 29-30 show the same views, and the same stages of fabrication, as respective Figs. 8, 11. The etch of cavity 410 stops on insulator 2920, and so will the etch of grooves 310 (described above in connection with Fig. 17B). Highly controllable cavity depth is achieved. In some embodiments, layer 130.2 has (100) orientation, and the cavity etch is a KOH wet etch described above.

[0080] Some interposer embodiments are used for optical coupling between different transducers mounted on the same interposer. For example, Fig. 31 is similar to Fig. 18, but mirrors 144 are formed at the groove ends on cavity sidewalls 910.2, 910.4.

Transducers (not shown) can be mounted on the interposer over all these mirrors, and can be optically coupled to each other by the optical fibers 104. Likewise, in a variation of Fig. 24, mirrors and transducers can be provided on all the four cavity sides 910.1-910.4.

[0081] A single transducer chip may have both light emitters and photodetectors. The grooves can be curved in the top and/or side views, and can have a varying width. The mirrors 144 can be absent since mirrors can be etched into fibers' end faces as described in U.S. patent no. 8,031,993 issued October 4, 2011 to Bowen. The mirrors 144, when present, can be planar as described above, or can be elliptic or have other shapes. Non-mirror optical elements (e.g. prisms, etc.) can also be used.

[0082] The spacers can be formed by a subtractive method as shown in Figs. 32-34. Fig. 32 is similar to Fig. 6, but layer 520 is patterned to remain at the groove locations, i.e. in regions complimentary to the spacer locations. The patterning uses a selective etch as described above. Then the spaces between features of layer 520 are filled with a material 3410 (Fig. 33). This can be any material suitable for the spacers, deposited by any suitable process, e.g. metal deposited over the wafer and then etched off to provide a planar top surface. Other techniques can also be used, e.g. electrodeposition on a seed layer (not shown) formed in the cavity before deposition of layer 520. Then layer 520 is

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etched away selectively to layer 3410 (Fig. 34) to form the grooves 310. Layer 3410 provides the spacers between the grooves. The subtractive method can be used with an etch-stop layer such as 1010 (Fig. 17B) and can be combined with other features described above.

5    **[0083]**     In some embodiments, grooves with optical fibers are provided both at the top and bottom surfaces of the interposer. The grooves at each surface can be formed using any techniques described above, including the prior art techniques described in connection with Figs. 1-3. One exemplary process is as follows. Substrate 130 is thinned to its final thickness. Then V-grooves or other grooves are etched in substrate 130 on both  
10   sides, possibly at the same time with a wet etch. Then each side is processed, possibly as the top side in Fig. 1-3, to finish the interposer fabrication.

**[0084]**     In some embodiments, the interposer is formed as follows. Substrate 130 is thinned to its final thickness. Then cavities 410.1, 410.2 (Fig. 35A) are etched respectively in the top and bottom surfaces of the substrate, possibly simultaneously,  
15   using the processes described above or any other suitable processes. In Fig. 35A, a mask 810 is used on the top and bottom to define the two cavities. (There can be any number of cavities on the top and bottom, possibly a different number of cavities on the top than on the bottom, and the cavities on the top do not have to overlie the bottom cavities and do not have to be aligned in any way.) Etch stop layer 1010 is formed on the top and bottom  
20   surfaces, possibly simultaneously (e.g. by thermal oxidation of silicon or by CVD), as described above. Then layer 520 is formed on the top and bottom surfaces of the wafer using the techniques described above or other techniques. This layer is shown as 520.1 on the top surface, and as 520.2 on the bottom surface. The top layer 520.1 is planarized as in Fig. 11, to be removed outside of cavity 410.1. The bottom layer may also be  
25   planarized, but it covers the whole bottom surface of the wafer. The thickness is chosen to accommodate the through-substrate-via process described below, and can be any suitable value.

**[0085]**     Then a blind via 1210 is formed in the top surface of the wafer by a masked etch of layer 810 and substrate 130 at each location of a desired through-substrate via as  
30   described above in connection with Fig. 12. Via 1210 passes through substrate 130 and through layer 810 above and below the substrate and partially, but not completely, passes through layer 520.2.

**[0086]**     As shown in Fig. 35B, vias 1210 are then oxidized and metalized, and

conductive lines 1310 and possibly other circuit elements and passivation 1330 are formed on top of the interposer, using processes described above in connection with Figs. 12-13.

5 [0087] Then (Fig. 35C) the interposer is thinned, by CMP or other processes, to remove the layer 520.2 down to the level of oxide 1010 at the interposer bottom. Vias 1220 become through holes. Copper 1250 (and seed 1230) and insulator 1220 protrude down from substrate 130. Then insulator 1410 (e.g. polyimide) is deposited on the bottom surface, and the bottom surface is planarized by CMP which does not remove all of insulator 1410 but exposes the copper. Suitable processes are described above in  
10 connection Figs. 14-15.

[0088] Conductive lines 1420 and other circuit elements and passivation 1430 are formed on the interposer bottom as described above in connection with Figs. 15-16 and illustrated in Fig. 35D.

15 [0089] Layers 520.1, 520.2 are etched to form grooves 310 and the interposer top and bottom, and mirrors 410 are formed at the top and bottom, as described above in connection with Figs. 17A, 17B, 18. Fig. 35E shows an exemplary vertical cross section perpendicular to grooves 310. The cavities 410.1, 410.2 do not have to be aligned, i.e. cavity 410.1 can be laterally shifted relative to cavity 410.2. The grooves 310 also may have different shapes and dimensions. More than one cavity can be provided on top  
20 and/or bottom, and the top grooves 310 do not have to be parallel to the bottom grooves.

[0090] The structure is further processed as described above in connection with any of Figs. 19-26, and any variations in the top or bottom processing can be used as described above in connection with Figs. 1-34. (In particular, prior art techniques for groove and mirror formation can be used on one or both interposer sides.) Fig. 35F shows  
25 an exemplary structure at a stage similar to Fig. 23, with transducers 120.1, 120.2 on top and bottom respectively. In this embodiment, the two transducers are connected to each other through a metalized via 1210, but this is not necessary. Different transducers can be connected to different vias, or not connected to any vias, and controllers 1610 (Fig. 22) and other circuits can be mounted on the interposer as needed.

30 [0091] In some embodiments, the through vias 1210 are created without first forming blind vias, i.e. the vias 1210 are etched through the interposer wafer right away. Also, the invention is not limited to through vias.

[0092] A wide variety of cavity shapes are possible to meet the requirements of a

particular application. For example, the “mirror” sidewall 910.2 can be formed by a separate etch or other process. In particular, the mirror sidewall 910.2 can be at a different angle and/or depth than sidewalls 910.1, 910.3, 910.4 of the cavity. One possible process is illustrated in Figs. 39A-39C. This process is suitable for a wide variety of substrate materials including monocrystalline silicon and other materials described above. Initially (Fig. 39A), cavity 410 is formed with all the sidewalls being vertical or at some other angle. In some embodiments, the cavity is formed by a masked dry etch with a photoresist mask (not shown, similar to mask 810 in Fig. 8). Then (Fig. 39B) the photoresist is removed, and sidewall 910.2 is etched to change its geometry. Other sidewalls of the cavity may or may not be similarly processed, and either an entire sidewall or only part of a sidewall may be so processed. In the embodiment shown, the geometry of sidewall 910.2 is defined by mechanical machining, and more particularly using a dicing saw 3910 having a 45° sidewall 3910A facing the sidewall 910.2. Saw 3910 rotates around a horizontal axis 3910X perpendicular to sidewall 910.2 to change the sidewall geometry. Sidewall 910.2 acquires a 45° profile matching the saw sidewall 3910A. See Fig. 39C (vertical cross section) and Fig. 40 (top view).

**[0093]** Subsequent steps can be as described above and below in connection with Figs. 1-38. In particular, the cavity can be filled with layer 520, possibly after deposition of layer 1010, and such cavities can be formed both at the top and the bottom of substrate 130 by the process of Figs. 39A-39C or other processes.

**[0094]** In some embodiments, the sawing or other processing of sidewall 910.2 (Fig. 39B) is performed to a controlled depth, and in the embodiment of Fig. 39C the depth is less than the depth of cavity 410. This results in a step 3930 along the cavity sidewall 910.2. This step can be used as a hard stop for fibers 104 to facilitate the fiber alignment as shown in Fig. 41 – the fibers are inserted in grooves 310 so that they abut the step 3930. (For simplicity, Fig. 41 does not show oxide 1010 and other features that may or may not be present as in Figs. 4-38.) If desired, the mirror sidewall 910.2 can be deeper than the rest of the cavity, or can be of the same depth.

**[0095]** As illustrated in Fig. 42, the cavity with grooves 310 and the electrical circuitry can initially be formed in separate wafers, shown as interposers 124.1 and 124.2, which are then assembled into a single optical interposer 124. An exemplary fabrication process is as follows. Optical interposer 124.1 is fabricated by processing a substrate 130.1 (monocrystalline silicon or other suitable material) as in Figs. 8-19 to form cavity

410 and grooves 310 and mirrors 144, but without electrical circuitry outside the cavity 410. Oxide 1220, metal 1310, and passivation 1330 may be present in interposer 124.1 in the cavity area as in Figs. 17A-19. Circuit elements and pads of metal 1310 can thus be formed in the cavity area. Then the wafer is thinned and diced to obtain a structure  
5 containing the cavity as shown in top view in Fig. 43. One or more sidewalls may (but does not have to) be removed in the dicing process as described above in connection with Fig. 19. Process variations can be used as described above, including the variation of Figs. 39A-39C.

**[0096]** In a separate process, interposer 124.2 is fabricated by processing a substrate  
10 130.2 (monocrystalline silicon or other suitable material) to form electrical circuitry for connection to transducers and other circuits. The wafer processing can be as described above in connection with Figs. 12-16. A cavity 4210 is formed in substrate 130.2. Optical interposer 124.1 is inserted into this cavity. Fibers 104 can be inserted in grooves 310 and suitably affixed (e.g. with adhesive) before or after the attachment of interposer 124.1 to  
15 interposer 124.2. Transducers and other circuits can be attached to combined interposer 124 as described above.

**[0097]** Interposer 124.1 may have discontinuous spacers and/or mirrors 144 on different sidewalls as Figs. 24-26, and interposer 124.1 or 124 may have other features described above in connection with Figs. 4-41. In particular, in some embodiments,  
20 interposer 124.2 has cavities 4210 on top and bottom, and a separate interposer or interposers 124.1 are inserted into each cavity.

**[0098]** The invention is not limited to the features described above. In some embodiments, an optical interposer (e.g. 124 or 124.1) comprises a top surface having a first cavity therein. For example, the first cavity can be 410 in Fig. 4, or can be the cavity  
25 defined by layer 1010 in Fig. 10 or in interposer 124.1 of Fig. 42, i.e. the cavity whose surface is the top surface of layer 1010. Alternatively, the first cavity can be defined by layer 1010 in cavity 410.1 or 410.2 of Fig. 35A. The first cavity may have sidewalls all around (as in Fig. 31) or some sidewalls may be removed (as in Fig. 19 or 24), i.e. the first cavity may be at an edge of the interposer.

**[0099]** The optical interposer also comprises one or more first spacers (e.g. 520, or 3410, or a combination of 520 (or 520.1 or 520.2) and 1220 in Fig. 17B or 35E, with or without 1330). The one or more first spacers are on a surface of the first cavity. The one or more first spacers define a plurality of first channels for supporting optical fiber cables.

The channels can be grooves 310, or grooves 310X and 310Y in Fig. 24, or other channels. Different channels can run in different directions as in Fig. 24, perpendicular or at some other angle to each other.

**[00100]** Each first spacer comprises a bottom region physically contacting the first cavity's surface and made of a different material than at least part of the first cavity's surface. The bottom region can be a spacer 520 or 520.1 or 520.2, and the first material can be polysilicon. The bottom region can also be less than a whole spacer. For example, in Fig. 36, layer 520 is covered by a layer 3610 made of a different material than 520, possibly of the same material as the cavity surface, and each first spacer can be viewed as made of layers 520, 3610 to define grooves 310 therebetween. For example, layer 3610 can be formed by selective deposition (e.g. thermal oxidation of polysilicon 520), or can be deposited to a greater thickness on top of layer 520 than on the cavity bottom and can be anisotropically etched until it is removed from the cavity bottom, or layer 3610 can be left on the cavity bottom (this is not shown in Fig. 36). The bottom region of each first spacer can be the region 520 made of a different material than the cavity surface. In Figs. 6 and 17B, the bottom region can be an entire spacer 520 which contacts a different material 1010 (Fig. 17B) or 130 (Fig. 6).

**[00101]** In some embodiments, the first cavity's surface comprises:

**[00102]** a bottom surface; and

**[00103]** a sidewall surface comprising one or more sidewall portions extending from the bottom surface upward and laterally outside of the first cavity. For example, in Fig. 18, the sidewall surface can be 910.2, and the sidewall portions can be the oxide sidewall portions underlying the metal mirrors 144.

**[00104]** Each first channel has a first end which is adjacent to an associated one of the one or more sidewall portions, each sidewall portion being for providing and/or supporting an optical element (e.g. a mirror 144, or a prism (not shown), or some other optical element) for directing light coming into and/or out of the first channel's respective optical fiber cable. For example, in Figs. 18, 42, 43 the first end of each channel is the end adjacent to the corresponding mirror 144.

**[00105]** In some embodiments, for at least one first spacer, the bottom region overlies and physically contacts the first cavity's bottom surface and is made of a different material than at least part of the first cavity's bottom surface adjacent to the bottom region. In some embodiments, for at least one first spacer, the bottom region overlies and

physically contacts the first cavity's sidewall surface and is made of a different material than at least part of the first cavity's sidewall surface adjacent to the bottom region. For example, in Figs. 17A and 17B, the bottom region 520 of each spacer overlies and physically contacts both the bottom surface and the sidewall surface 910.2 supporting the mirrors, the bottom and sidewall surfaces are made of a different material (e.g. polysilicon) than the cavity's surface (made of silicon dioxide for example).

**[00106]** In some embodiments, each optical element is a reflective surface (e.g. mirror 144) formed on the associated sidewall portion, the reflective surface being for reflecting light coming into and/or from a respective optical fiber cable in the first channel, the reflective surface having a different reflectivity property than at least one surface of the first cavity. For example, mirror 144 may be metal having a different reflective property than the silicon dioxide surface of the cavity. In other embodiments, the mirrors are provided by the cavity's sidewall surface, not be a separate layer (e.g. metal) on the cavity surface.

**[00107]** In some embodiments, the first cavity's bottom surface is planar, and each reflective surface is a flat surface being at an angle of  $45^\circ$  or some other angle at most  $60^\circ$  to the first cavity's planar bottom surface. (This angle is defined as the angle between the reflective surface and an imaginary extension of the planar bottom surface beyond the reflective surface – see e.g. angle  $\alpha$  in Fig. 4).

**[00108]** In some embodiments, at least one sidewall of at least one first spacer is at an angle  $90^\circ$  or some other angle of at least  $85^\circ$  to the first cavity's planar bottom surface. (This angle is defined as the angle between the first spacer's sidewall and the planar bottom surface underneath the first spacer – see e.g. angle  $\beta$  in Fig. 37).

**[00109]** In some embodiments, the interposer comprises a substrate and a layer on the substrate (e.g. 1010) of a different material than the substrate and than the bottom region of each first spacer. The layer's top surface provides the first cavity's surface.

**[00110]** In some embodiments, the channels comprise at least two channels running in different directions and overlying one another. See Fig. 24 for example.

**[00111]** In some embodiments, the optical interposer comprises one or more pads over the first spacers, for providing mechanical support to an integrated circuit mounted on the interposer. For example, in Figs. 16 and 22, a pad 1310 over spacers 520 is used to support solder 1604 which supports the transducer 120.

**[00112]** In some embodiments, at least one first spacer protrudes upward to provide

mechanical support for at least one of the transducers. One example illustrated in Fig. 38, showing a structure similar to Fig. 22 but without the metal 1310 and solder 1604 over the cavity. Transducer 120 rests on passivation 1330 above spacer 520. For example, at the stage of Fig. 11, layer 520 can be left to protrude upward above substrate 130. Layer 520 can then be etched off outside the cavity as needed to form the electrical circuitry. The upward protrusion of layer 520 at the cavity will result in the upward protrusion of passivation 1330 over the cavity.

**[00113]** Alternatively, the upward protrusion of passivation 1330 can be provided by patterning passivation 1330 and/or insulation 1220, and/or depositing and patterning other layers by conventional techniques.

**[00114]** In some embodiments, electrical circuitry is formed in at least one of the first spacers (e.g. transistors, interconnect lines, and other circuitry can be formed in spacers 520).

**[00115]** In some embodiments, the optical interposer further comprises a bottom surface having one or more second channels defined therein for supporting optical fiber cables (see e.g. Fig. 35F), the electrical circuitry comprising circuitry for connection to one or more opto-electrical transducers which are for being optically coupled to the optical fiber cables supported by the second channels.

**[00116]** In some embodiments, the optical interposer's bottom surface comprises a second cavity therein. The optical interposer also comprises, when viewed upside down (i.e. with the bottom surface on top), one or more second spacers on the second cavity's surface which define a plurality of the second channels. Each second spacer comprises a bottom region physically contacting the second cavity's surface and made of a different material than at least part of the second cavity's surface.

**[00117]** Some embodiments provide an optical interposer for interfacing one or more optical fiber cables to electrical circuitry, the optical interposer comprising a top surface having a first cavity therein. The optical interposer also comprises one or more spacers on a surface of the first cavity, wherein the one or more spacers define a plurality of first channels for supporting optical fiber cables. The optical interposer comprises electrical circuitry outside the first cavity, for connection to one or more opto-electrical transducers each of which is for being optically coupled to the optical fiber cables. For each first channel, the first cavity comprises a first surface at the end of the first channel (e.g. the surface on which the mirrors 144 are formed), the first surface being at an angle of at

most 60° to the first cavity's planar bottom surface (the angle being between the first surface and an imaginary extension of the planar bottom surface beyond the first surface. At least one sidewall of at least one spacer is at an angle of at least 85° to the first cavity's planar bottom surface (the angle being between the spacer's sidewall and the planar  
5 bottom surface underneath the spacer).

**[00118]** Some embodiments provide a method for fabricating an optical interposer.

The method comprises: forming a first cavity (e.g. 410.1 or 410.2) in a substrate; forming a first layer (e.g. 520 or 520.1 or 520.2) over the first cavity's bottom surface; and  
10 patterning the first layer to form one or more spacers in the first cavity, wherein the one or more spacers define a plurality of channels for supporting optical fiber cables. The spacers could be formed by the first layer (e.g. 520) or by another layer (e.g. 3410).

**[00119]** Patterning the first layer comprises a first etch of the first layer, wherein at least over the first cavity's surface, the first etch terminates based at least in part on etch selectivity to the first cavity's surface.

15 **[00120]** In some embodiments, the first cavity comprises: a bottom surface; and a sidewall (e.g. 910.2) extending from the bottom surface upward and laterally outside of the first cavity. At least over the first cavity's sidewall, the first etch terminates based at least in part on etch selectivity to the sidewall.

**[00121]** Some embodiments provide an optical interposer for interfacing one or more  
20 optical fiber cables to electrical circuitry, the optical interposer comprising a first surface and a second surface opposite to the first surface (for example, the top and bottom surfaces in Fig. 35F). The first surface comprises one or more first channels for supporting one or more optical fiber cables. The second surface comprises one or more second channels for supporting optical fiber cables. The optical interposer comprises  
25 electrical circuitry for connection to a plurality of opto-electrical transducers which are for being optically coupled to the optical fiber cables.

**[00122]** In some embodiments, the optical interposer comprises a substrate (e.g. 130), and the plurality of channels are formed in recesses in opposite surfaces of the substrate. For example, in Fig. 35F, the recesses are defined by the top surface of layers 1010 in  
30 cavities 410.1, 410.2. Alternatively, the recesses could be individual V-grooves as in Figs. 1-3.

**[00123]** In some embodiments, the optical interposer comprises electrical circuitry at the first and second surfaces, and comprises one or more conductive paths passing

through the substrate (e.g. metalized vias 1210) for interconnecting electrical circuitry at the first surface and electrical circuitry at the second surface.

**[00124]** Other embodiments and variations are within the scope of the invention, as defined by the appended claims.

## CLAIMS

1. An optical interposer for interfacing a plurality of optical fiber cables to one or more opto-electrical transducers which are for being coupled to the one or more optical fiber cables, the optical interposer comprising a top surface having a first cavity  
5 therein;  
wherein the optical interposer also comprises one or more first spacers on the first cavity's surface, wherein the one or more first spacers define a plurality of first channels for supporting optical fiber cables;  
wherein each first spacer comprises a bottom region physically contacting the first  
10 cavity's surface and made of a different material than at least part of the first cavity's surface.
2. The optical interposer of claim 1 further comprising, outside the first cavity, electrical circuitry for connection to the one or more transducers.
- 15 3. The optical interposer of claim 1 wherein the first cavity's surface comprises:  
a bottom surface; and  
a sidewall surface comprising one or more sidewall portions extending upward  
20 and laterally outside of the first cavity;  
wherein each first channel has a first end which is adjacent to an associated one of the one or more sidewall portions, each sidewall portion being for providing and/or supporting an optical element for directing light coming into and/or out of the first channel's respective optical fiber cable.
- 25 4. The optical interposer of claim 3 wherein the sidewall surface comprises a step underlying at least one sidewall portion, the sidewall surface being at a different angle below the step than the at least one sidewall portion.
- 30 5. The optical interposer of claim 3 wherein for at least one first spacer, the bottom region overlies and physically contacts the first cavity's bottom surface and is made of a different material than at least part of the first cavity's bottom surface adjacent to the bottom region.

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6. The optical interposer of claim 3 wherein for at least one first spacer, the bottom region overlies and physically contacts the first cavity's sidewall surface and is made of a different material than at least part of the first cavity's sidewall surface  
5 adjacent to the bottom region.

7. The optical interposer of claim 3 wherein each said optical element is a reflective surface formed on the associated sidewall portion, the reflective surface being for reflecting light coming into and/or from a respective optical fiber cable in the first  
10 channel, the reflective surface having a different reflectivity property than at least one surface of the first cavity.

8. The optical interposer of claim 7 wherein the first cavity's bottom surface is planar, and each reflective surface is a flat surface being at an angle of at most  $60^\circ$  to the first cavity's planar bottom surface (the angle being between the reflective surface  
15 and an imaginary extension of the planar bottom surface beyond the reflective surface).

9. The optical interposer of claim 8 wherein at least one sidewall of at least one first spacer is at an angle of at least  $85^\circ$  to the first cavity's planar bottom surface (the  
20 angle being between the first spacer's sidewall and the planar bottom surface underneath the first spacer).

10. The optical interposer of claim 7 wherein the reflective surface comprises metal.  
25

11. The optical interposer of claim 3 wherein the interposer comprises:  
a substrate;  
a layer on the substrate of a different material than the substrate and than the bottom region of each first spacer, the layer providing the first cavity's surface.  
30

12. The optical interposer of claim 3 wherein at least two of the first channels run in different directions and one of the two first channels overlies the other one of the two first channels.

13. The optical interposer of claim 3 wherein each first channel has longitudinal sides defined by one or more of the first spacers, and for at least one first channel, at least one longitudinal side is defined by a discontinuous plurality of the first  
5 spacers.

14. The optical interposer of claim 3 further comprising one or more pads over the first spacers, for providing mechanical support to an integrated circuit mounted on the interposer.  
10

15. The optical interposer of claim 14 wherein the one or more pads are metal pads for supporting solder which is for providing mechanical support to at least one of the transducers.

15 16. The optical interposer of claim 3 wherein at least one first spacer protrudes upward to provide mechanical support for at least one of the transducers.

17. The optical interposer of claim 3 further comprising electrical circuitry formed in at least one of the first spacers.  
20

18. The optical interposer of claim 3 further comprising the one or more transducers optically coupled to the optical fiber cables and electrically connected to electrical circuitry formed in the interposer outside the first cavity.

25 19. The optical interposer of claim 3 further comprising a bottom surface having one or more second channels defined therein for supporting optical fiber cables which are for being optically coupled to one or more opto-electrical transducers.

20. The optical interposer of claim 19 wherein the optical interposer's bottom  
30 surface comprises a second cavity therein;

wherein the optical interposer also comprises, when viewed upside down, one or more second spacers on the second cavity's surface which define a plurality of the second channels, wherein each second spacer comprises a bottom region physically contacting

the second cavity's surface and made of a different material than at least part of the second cavity's surface.

21. An optical interposer for interfacing a plurality of optical fiber cables to one or more opto-electrical transducers which are for being coupled to the one or more optical fiber cables, the optical interposer comprising a top surface having a first cavity therein;

wherein the optical interposer also comprises one or more spacers on a surface of the first cavity, wherein the one or more spacers define a plurality of first channels for supporting optical fiber cables;

wherein for each first channel, the first cavity comprises a first surface at the end of the first channel, the first surface being at an angle of at most  $60^\circ$  to the first cavity's planar bottom surface (the angle being between the first surface and an imaginary extension of the planar bottom surface beyond the first surface);

at least one sidewall of at least one spacer is at an angle of at least  $85^\circ$  to the first cavity's planar bottom surface (the angle being between the spacer's sidewall and the planar bottom surface underneath the spacer).

22. The optical interposer of claim 21 further comprising electrical circuitry outside the first cavity, for connection to the one or more opto-electrical transducers.

23. The optical interposer of claim 21 wherein for at least one first channel, the first cavity comprises a step underlying the first surface, wherein the first cavity's surface has a portion between the step and the first cavity's planar bottom surface and this portion is at a larger angle to the first cavity's planar bottom surface than the first surface of the first channel.

24. The optical interposer of claim 21 wherein in each first channel, for each spacer used to define the first channel, the spacer's sidewall facing the first channel is at an angle of at least  $85^\circ$  to the first cavity's planar bottom surface.

25. The optical interposer of claim 24 wherein in each first channel, the first surface is a reflective surface for directing light coming into and/or from the respective optical fiber in the first channel.

5           26. The optical interposer of claim 24 wherein each first surface comprises metal.

27. The optical interposer of claim 21 wherein at least two of the first channels run in different directions and one of the two first channels overlies the other one of the  
10 two first channels.

28. The optical interposer of claim 21 further comprising one or more metal pads over the spacers, to provide mechanical support to an integrated circuit mounted on the interposer.

15

29. The optical interposer of claim 28 wherein the one or more metal pads are for providing mechanical support to at least one of the transducers.

30. The optical interposer of claim 21 wherein at least one spacer protrudes  
20 upward to provide mechanical support for at least one of the transducers.

31. The optical interposer of claim 21 further comprising electrical circuitry formed in at least one of the spacers.

25           32. The optical interposer of claim 21 further comprising the one or more transducers optically coupled to the optical fiber cables and electrically connected to electrical circuitry formed in the interposer outside the first cavity.

33. The optical interposer of claim 21 further comprising a bottom surface  
30 having one or more second channels defined therein for supporting optical fiber cables which are for being optically coupled to one or more opto-electrical transducers.

34. A method for fabricating an optical interposer, the method comprising:

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forming a first cavity in a substrate;  
forming a first layer over the first cavity's bottom surface; and  
patterning the first layer to form one or more spacers in the first cavity, wherein  
the one or more spacers define a plurality of channels for supporting optical fiber cables  
5 which are to be optically coupled to one or more opto-electrical transducers;  
wherein patterning the first layer comprises a first etch of the first layer, wherein at  
least over the first cavity's surface, the first etch terminates based at least in part on etch  
selectivity to the first cavity's surface.

10 35. The method of claim 34 wherein forming the first cavity comprises:  
forming a first sidewall of the first cavity; and then  
removing material from the first sidewall to change geometry of the first sidewall.

36. The method of claim 35 wherein removing material from the first sidewall  
15 results in changing an angle of at least a portion of the first sidewall.

37. The method of claim 36 wherein removing material from the first sidewall  
comprises removing the material with a saw to change the angle of at least the portion of  
the first sidewall to match the angle of a surface of the saw.

20 38. The method of claim 34 wherein the first cavity comprises:  
a bottom surface; and  
a sidewall extending from the bottom surface upward and laterally outside of the  
first cavity; and

25 wherein at least over the first cavity's sidewall, the first etch terminates based at  
least in part on etch selectivity to the sidewall.

39. The method of claim 34 further comprising, after forming the first layer in  
the first cavity but before patterning the first layer to form the one or more spacers,  
30 forming electrical circuitry in the interposer, wherein the electrical circuitry is for being  
connected to the one or more transducers.

40. The method of claim 38 wherein:

the substrate is monocrystalline silicon;  
forming the first cavity comprises a wet etch of the substrate; and  
wherein the first etch creates a sidewall of the first layer which forms a different  
angle with a plane parallel to the first cavity's bottom surface than any sidewall of the  
5 first cavity.

41. An optical interposer for interfacing one or more optical fiber cables to  
electrical circuitry, the optical interposer comprising a first surface and a second surface  
opposite to the first surface;  
10 wherein the first surface comprises one or more first channels for supporting one  
or more optical fiber cables; and  
wherein the second surface comprises one or more second channels for supporting  
optical fiber cables.

42. The optical interposer of claim 41 further comprising electrical circuitry  
for connection to a plurality of opto-electrical transducers which are for being optically  
coupled to the optical fiber cables.

43. The optical interposer of claim 41 wherein the optical interposer comprises  
20 a substrate, and the plurality of channels are formed in recesses in opposite surfaces of the  
substrate.

44. The optical interposer of claim 43 wherein the optical interposer comprises  
electrical circuitry at the first and second surfaces, and comprises one or more conductive  
25 paths passing through the substrate for interconnecting electrical circuitry at the first  
surface and electrical circuitry at the second surface.

45. The optical interposer of claim 43 wherein the substrate is a  
semiconductor substrate.

30 46. The optical interposer of claim 43 further comprising circuitry formed at  
least partially in the semiconductor substrate, for connection to the opto-electrical  
transducers.

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47. An optical interposer for interfacing one or more optical fiber cables to one or more opto-electrical transducers which are for being coupled to the one or more optical fiber cables, the optical interposer comprising a top surface having a first cavity  
5 therein;

wherein the optical interposer also comprises one or more first spacers on the first cavity's surface, wherein the one or more first spacers define a plurality of first channels for supporting optical fiber cables; and

wherein the first cavity's surface comprises:  
10 a bottom surface; and

a sidewall surface comprising one or more sidewall portions extending upward and laterally outside of the first cavity;

wherein each first channel has a first end which is adjacent to an associated one of the one or more sidewall portions, each sidewall portion being for providing and/or  
15 supporting an optical element for directing light coming into and/or out of the first channel's respective optical fiber cable;

wherein the sidewall surface comprises a step underlying at least one sidewall portion, the sidewall surface being at a different angle below the step than the at least one sidewall portion.  
20

48. The optical interposer of claim 47 further comprising electrical circuitry outside the first cavity, for connection to the one or more opto-electrical transducers.

49. The optical interposer of claim 47 wherein the sidewall surface below the  
25 step is at a greater angle to the first cavity's bottom surface than the at least one sidewall portion.

50. The optical interposer of claim 49 wherein the first cavity's bottom surface comprises a planar bottom surface, and the sidewall surface below the step is at about 90°  
30 angle to the first cavity's planar bottom surface while the at least one sidewall portion is at about 45° angle to the first cavity's planar bottom surface.

51. A method for fabricating an optical interposer, the method comprising:

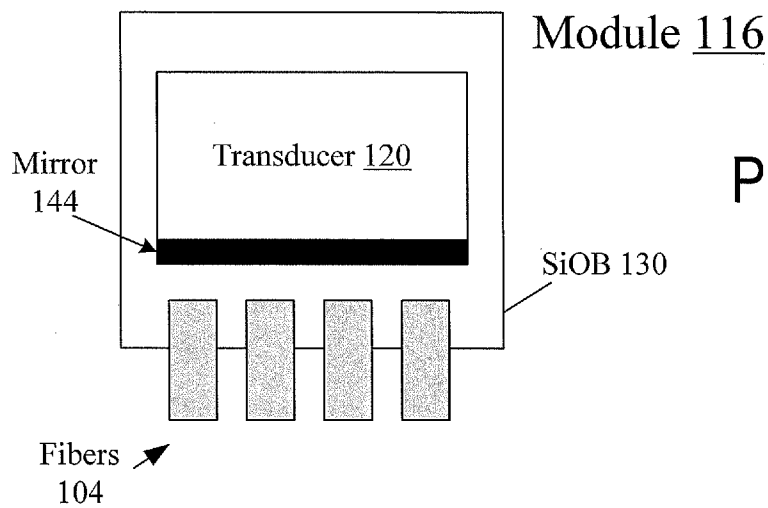
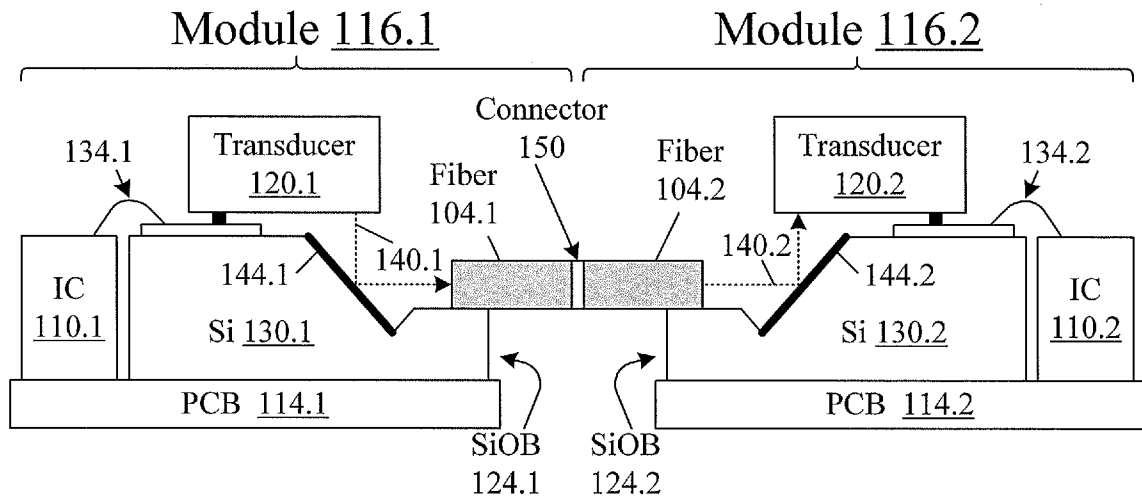
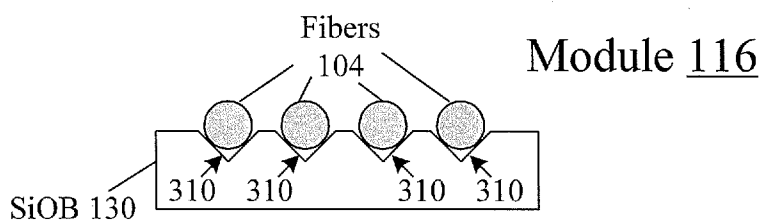
- forming a first cavity in a substrate;  
forming a first layer over the first cavity's bottom surface; and  
patterning the first layer to form one or more spacers in the first cavity, wherein  
the one or more spacers define a plurality of channels for supporting optical fiber cables  
5 which are to be optically coupled to one or more opto-electrical transducers;  
wherein forming the first cavity comprises:  
forming a first sidewall of the first cavity; and then  
removing material from the first sidewall to change an angle of at least a portion  
of the first sidewall.

10

52. The method of claim 51 wherein removing material from the first sidewall comprises removing the material with a saw to change the angle of at least the portion of the first sidewall to match the angle of a surface of the saw.

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FIG. 1 PRIOR ART

FIG. 2  
PRIOR ARTFIG. 3  
PRIOR ART

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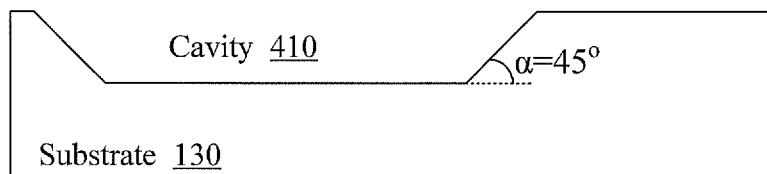


FIG. 4

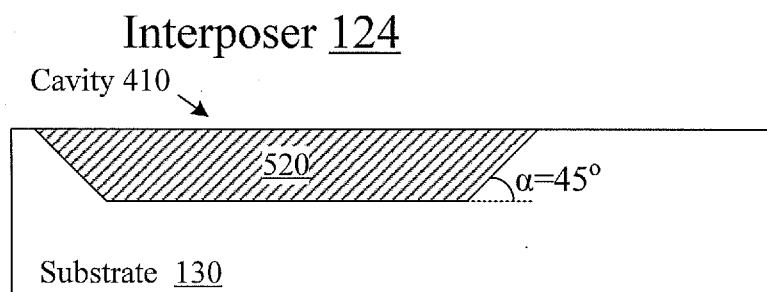


FIG. 5

Interposer 124

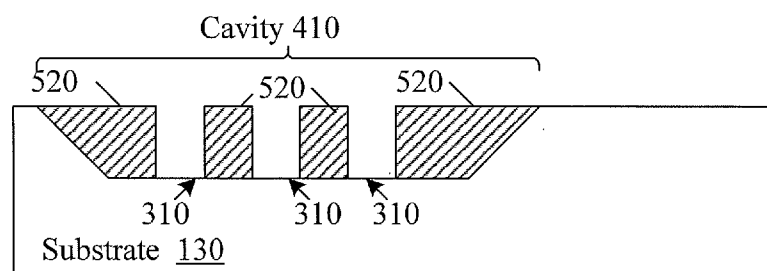


FIG. 6

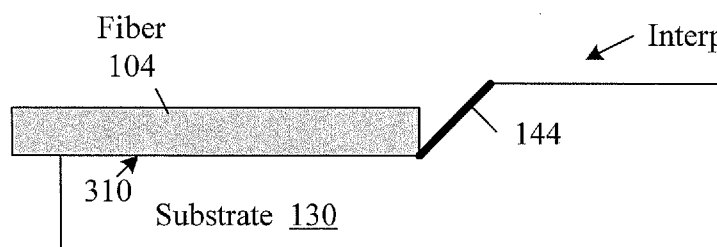


FIG. 7

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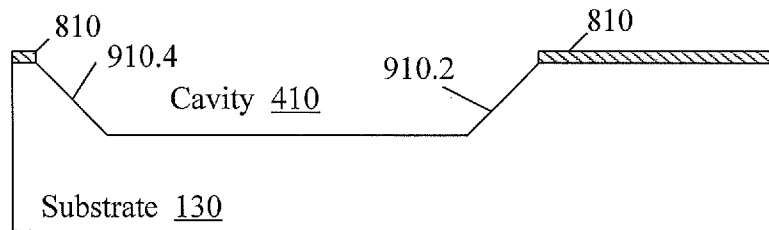


FIG. 8

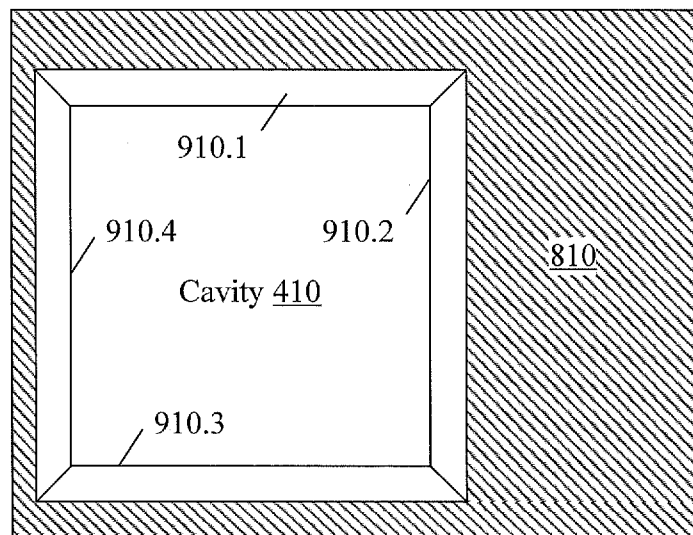


FIG. 9

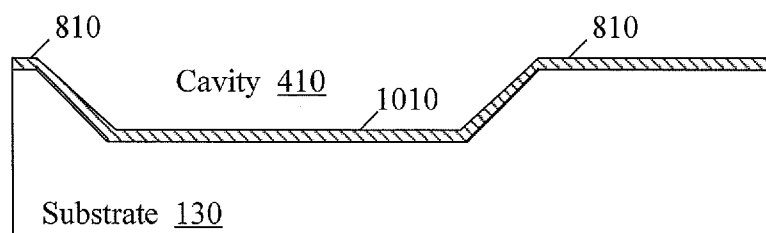


FIG. 10

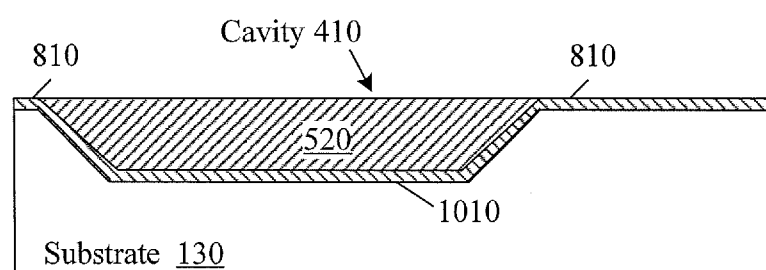


FIG. 11

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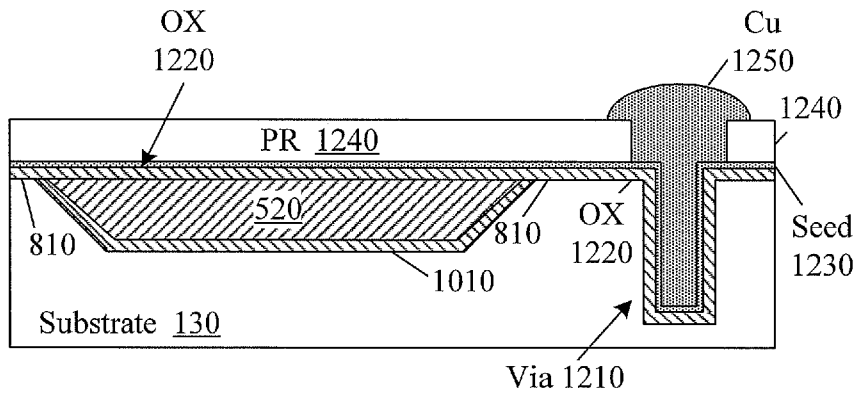


FIG. 12

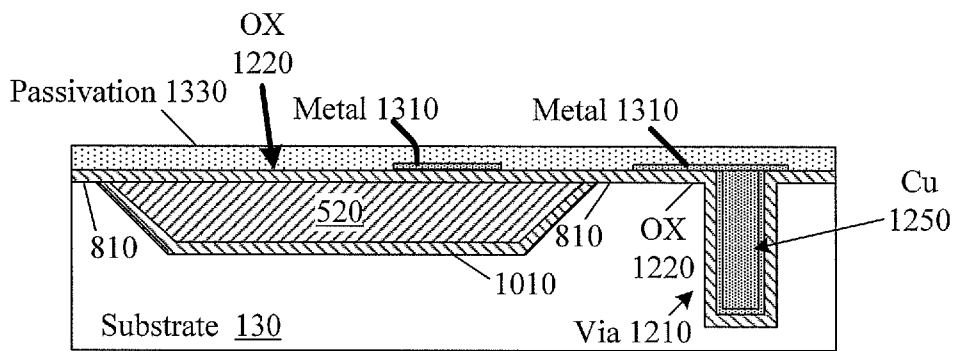


FIG. 13

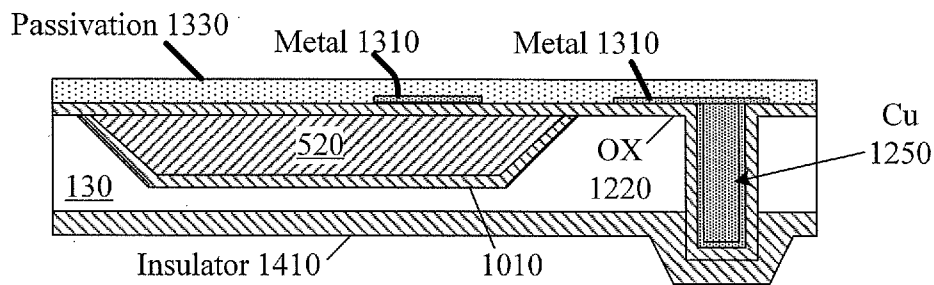


FIG. 14

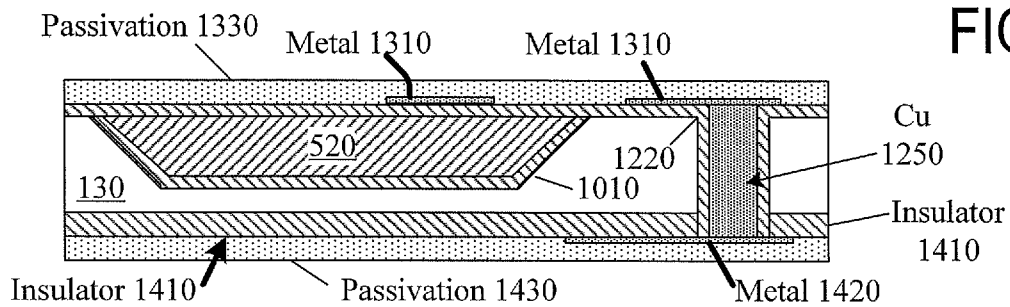


FIG. 15

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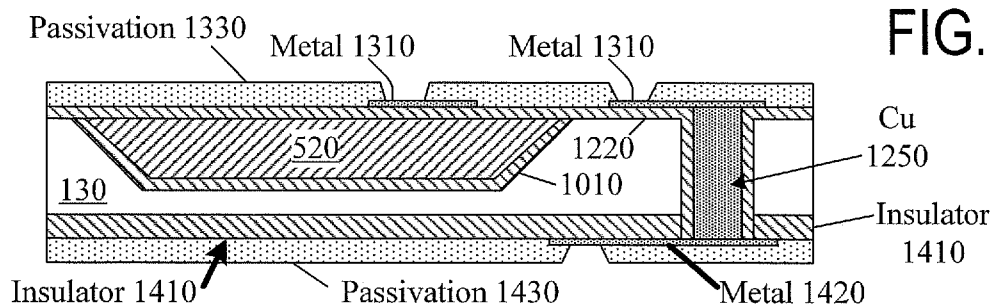


FIG. 16

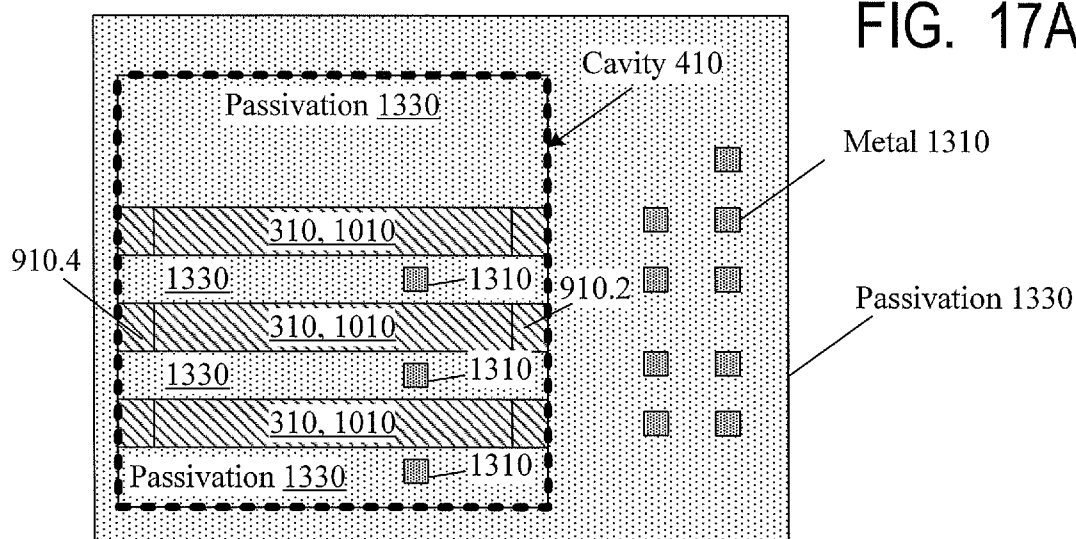


FIG. 17A

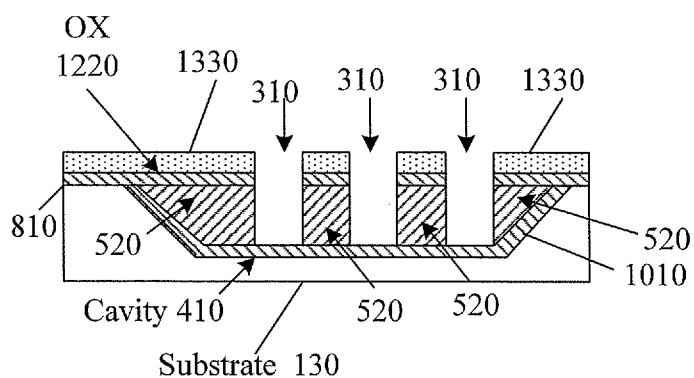


FIG. 17B

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FIG. 18

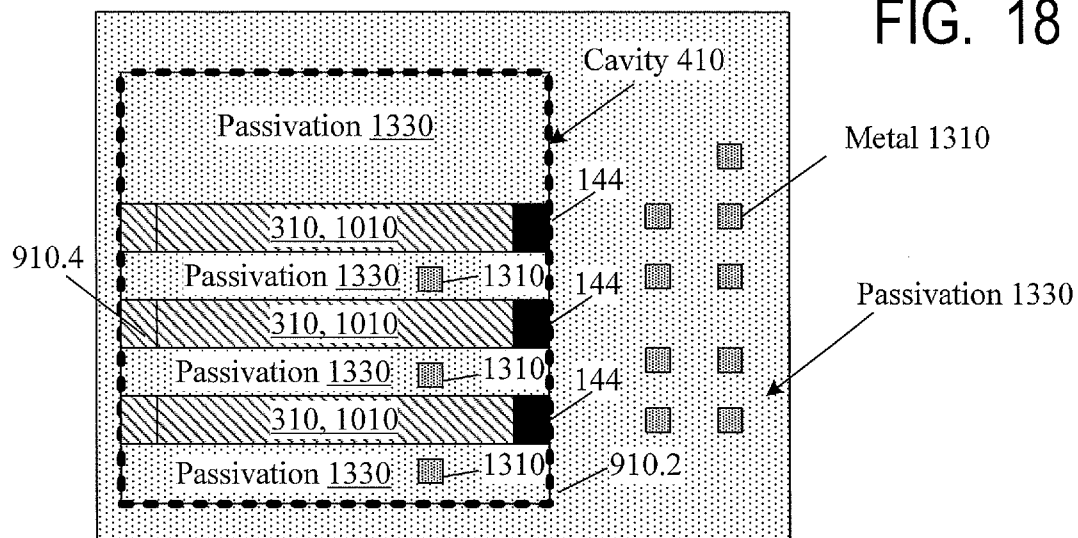


FIG. 19

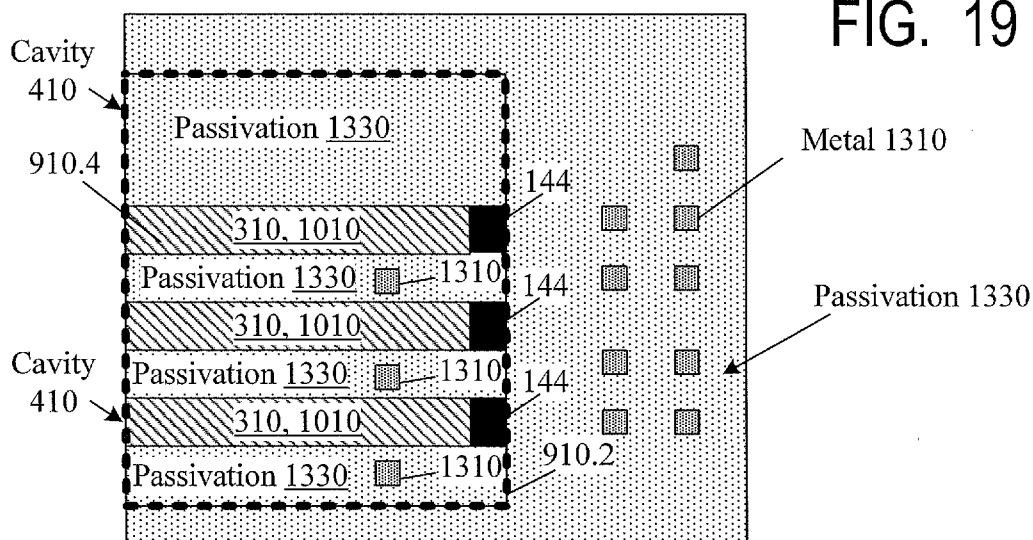
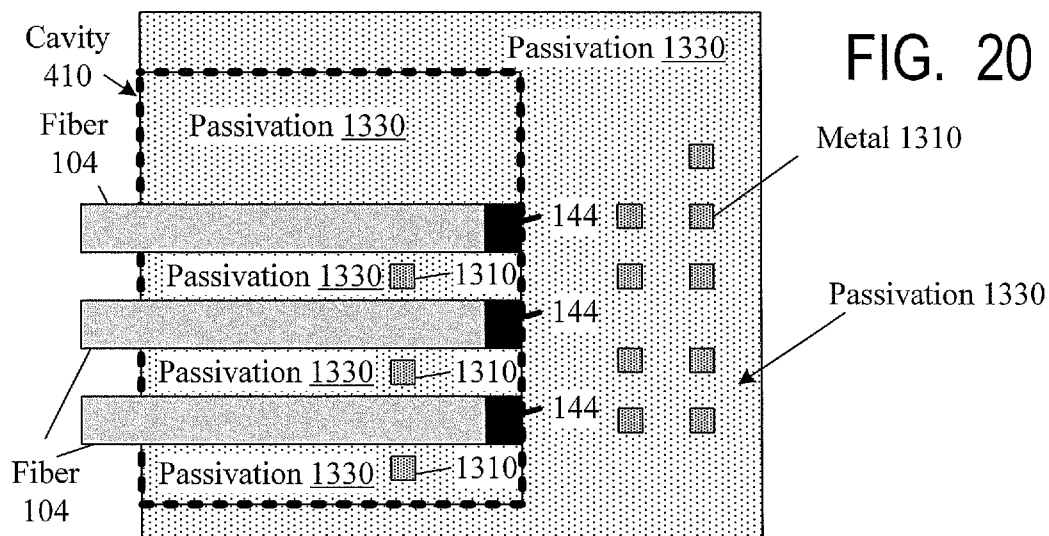
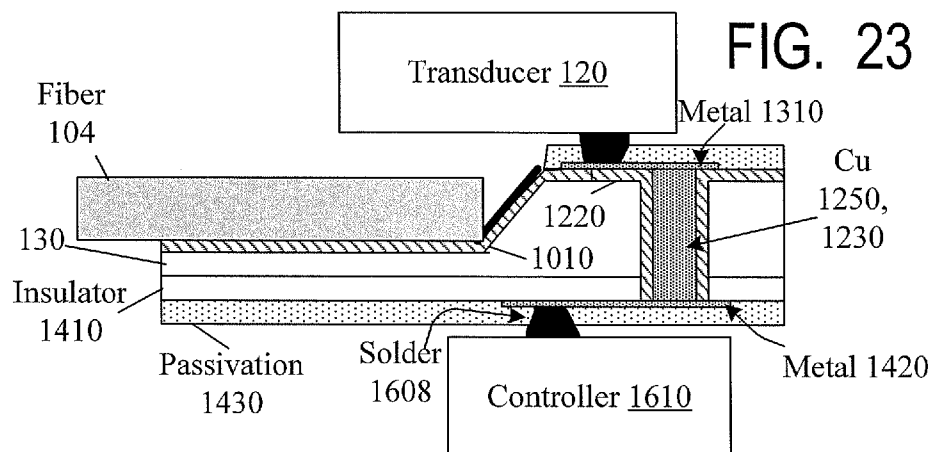
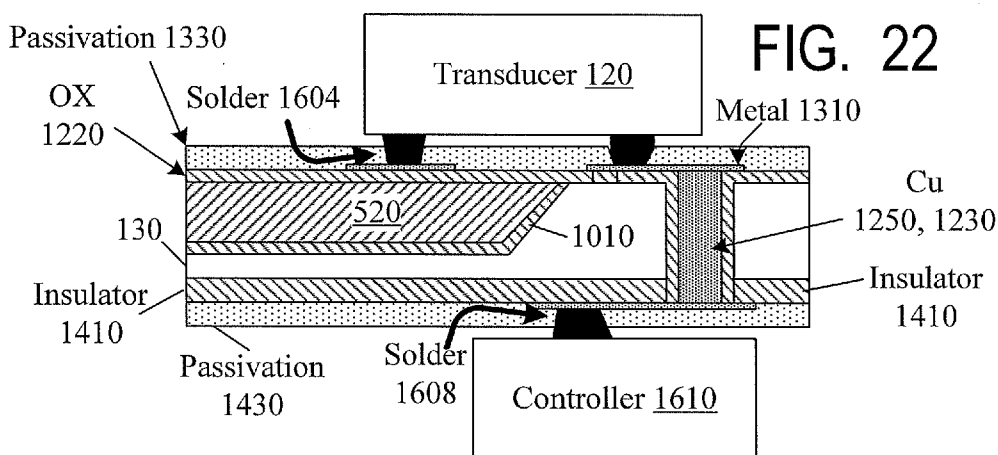
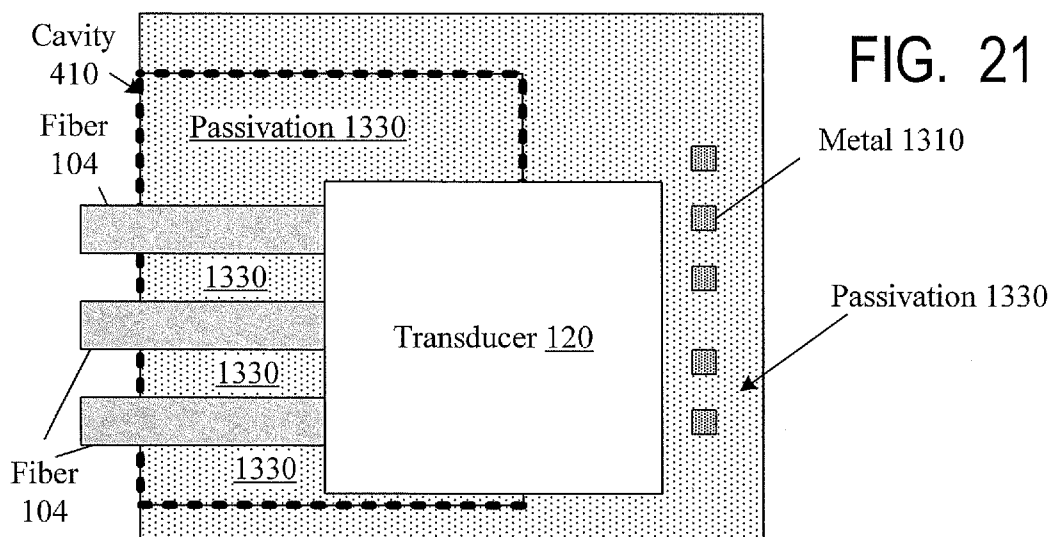


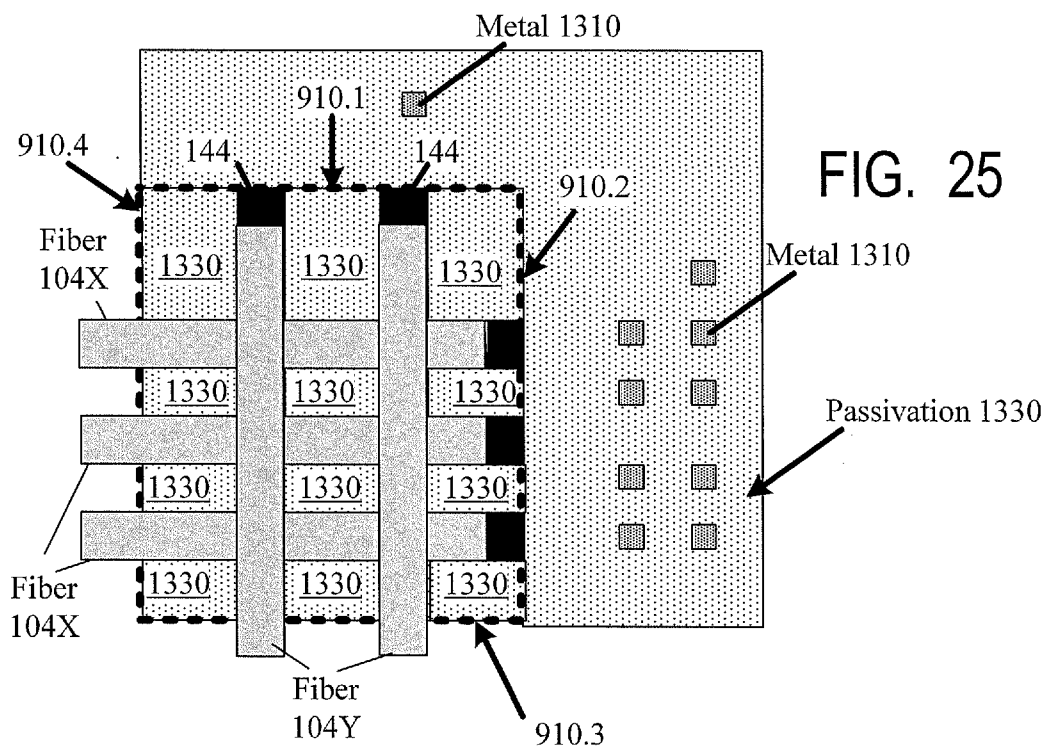
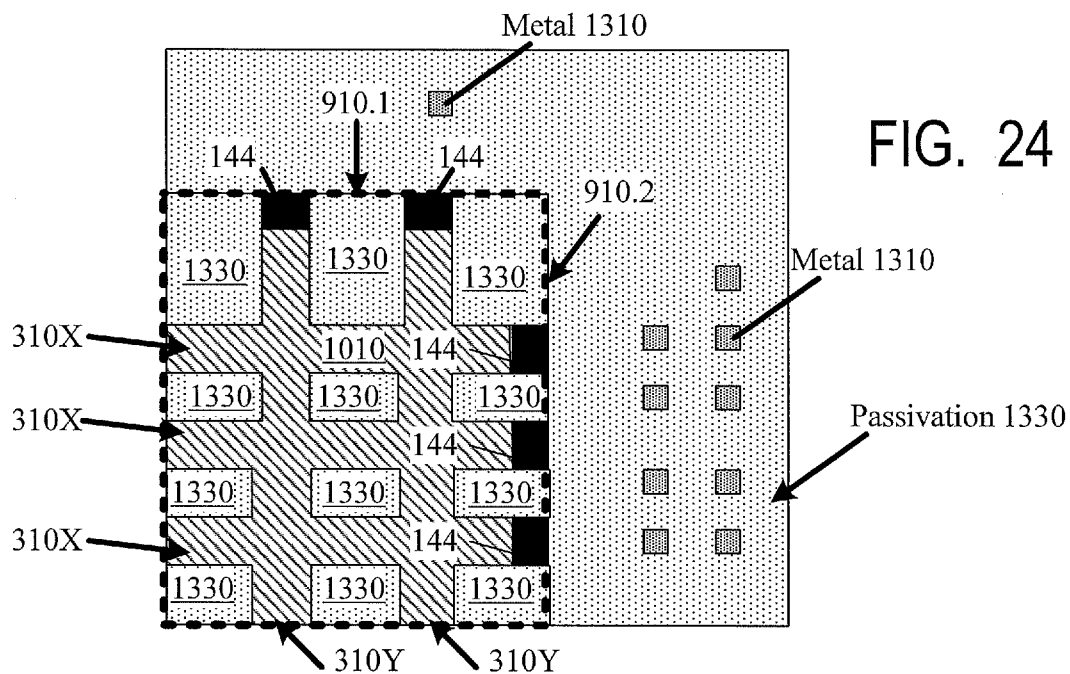
FIG. 20



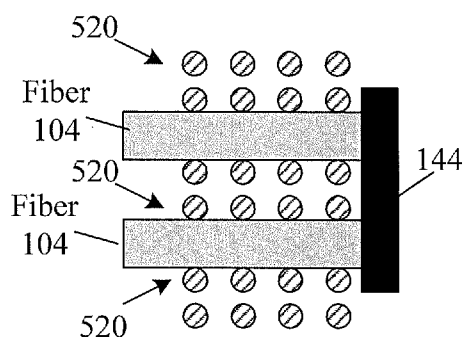
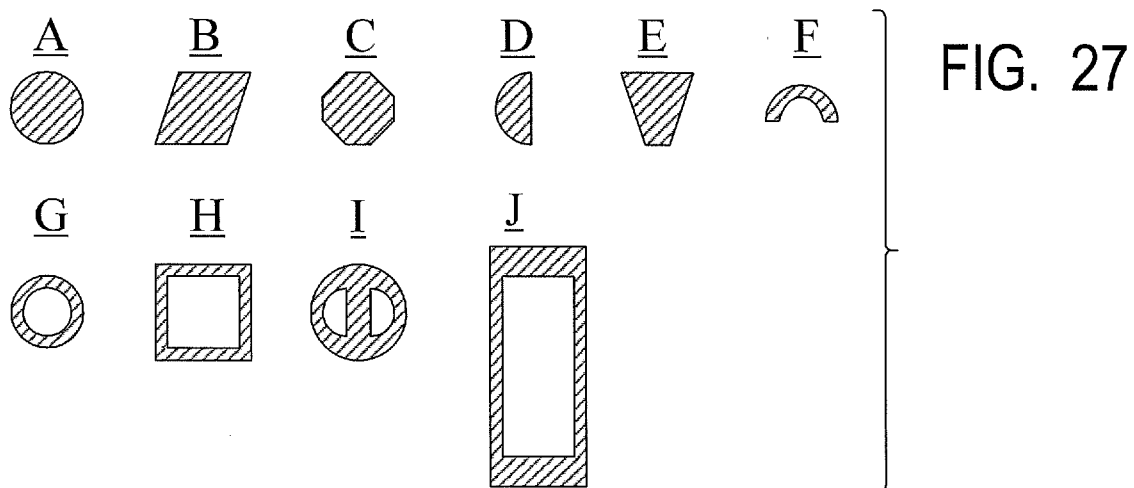
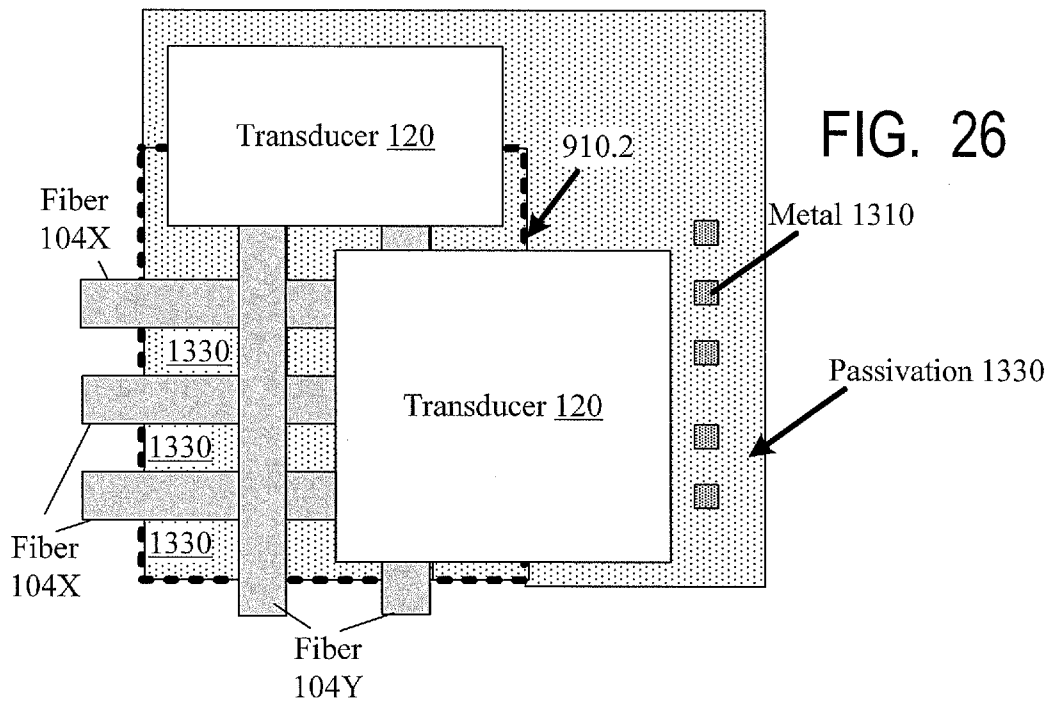
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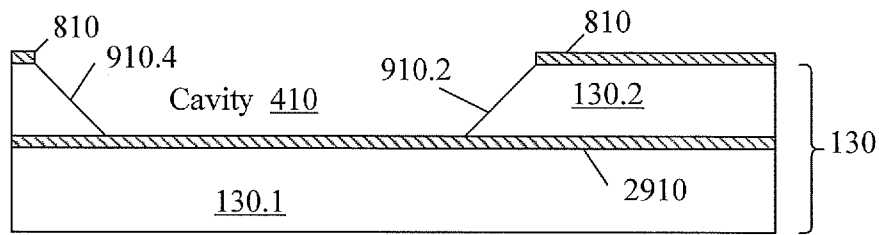


FIG. 29

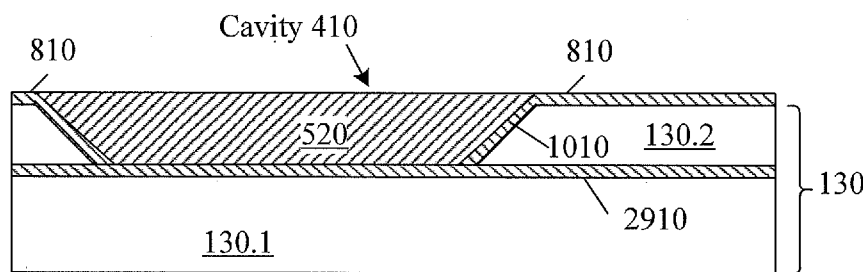


FIG. 30

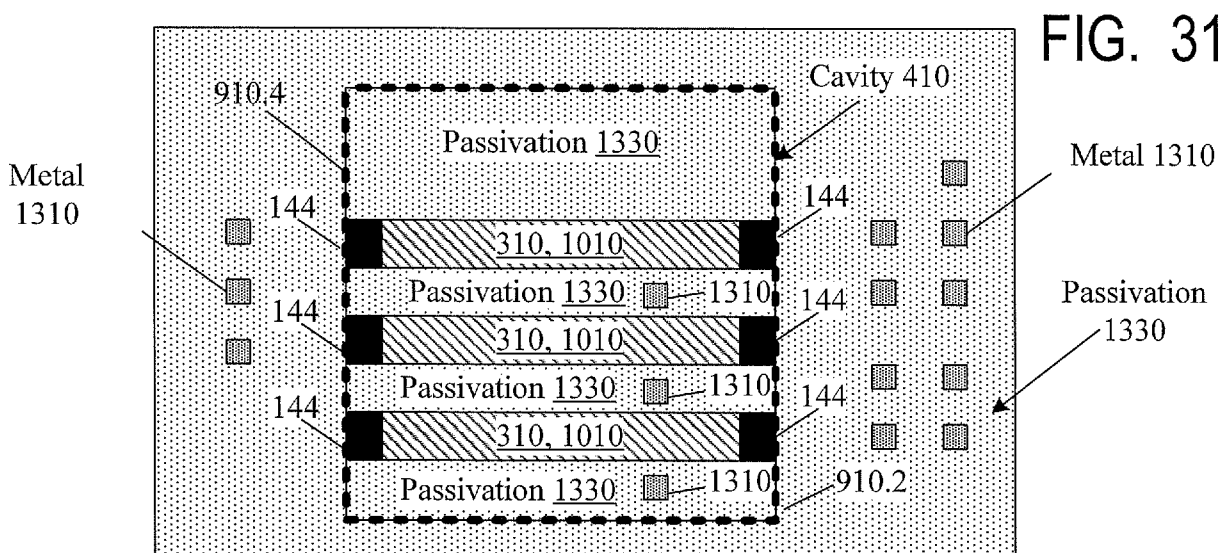


FIG. 31

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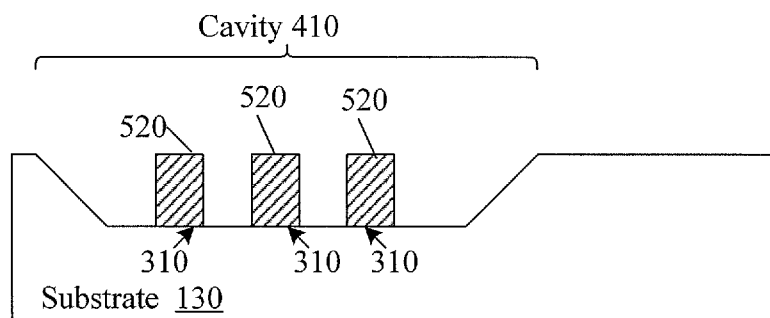


FIG. 32

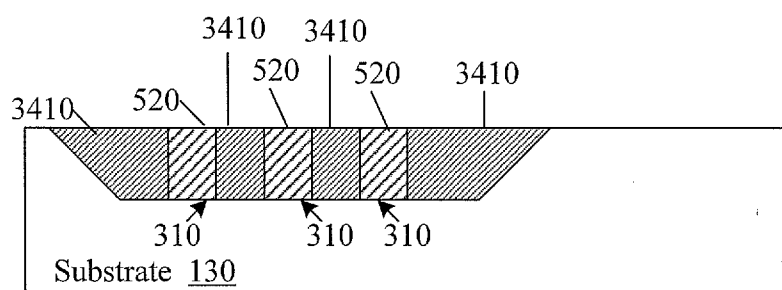


FIG. 33

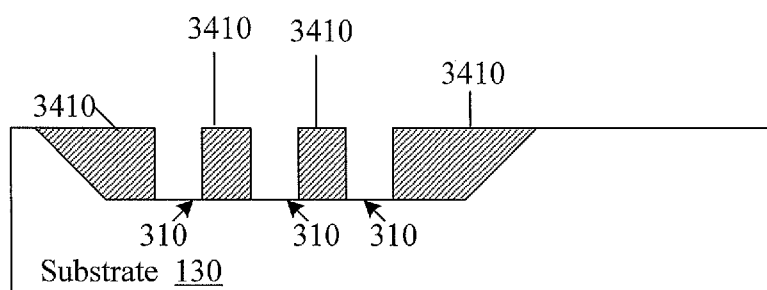


FIG. 34

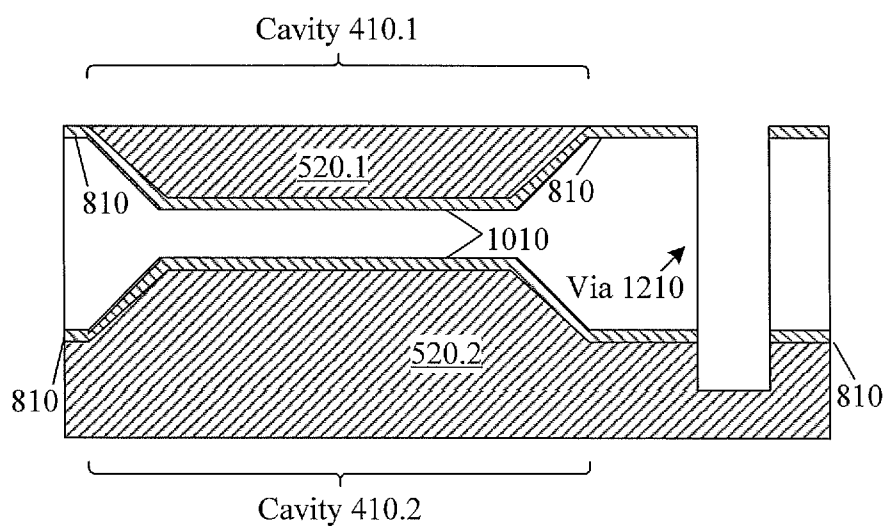
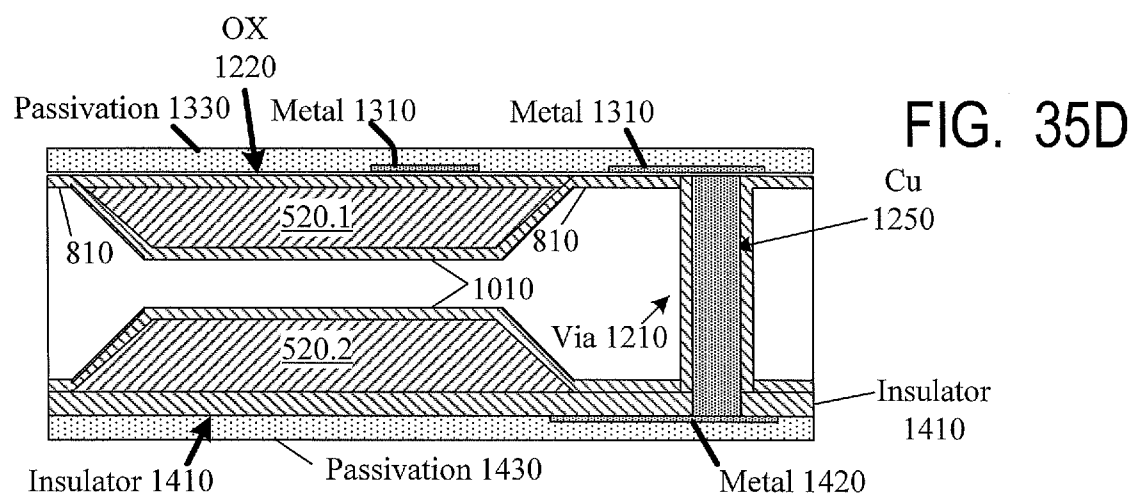
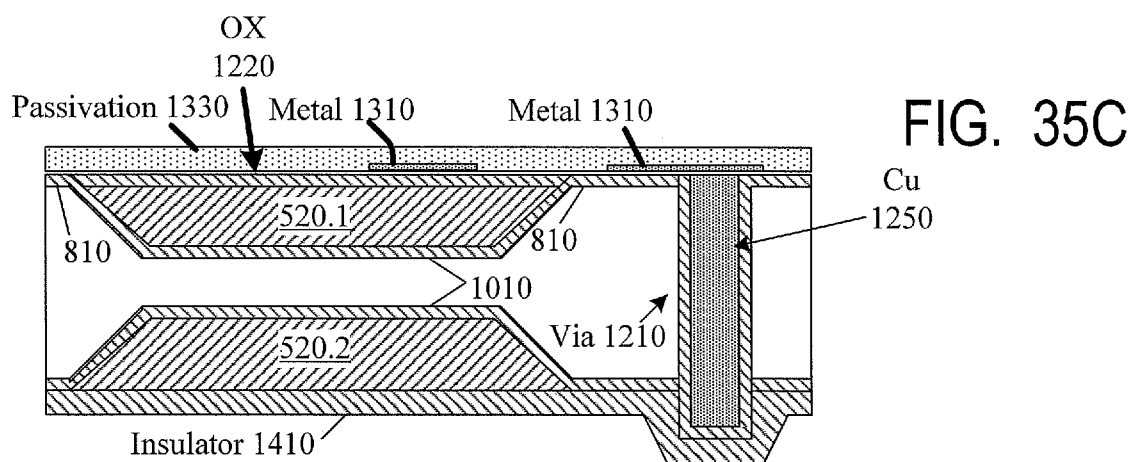
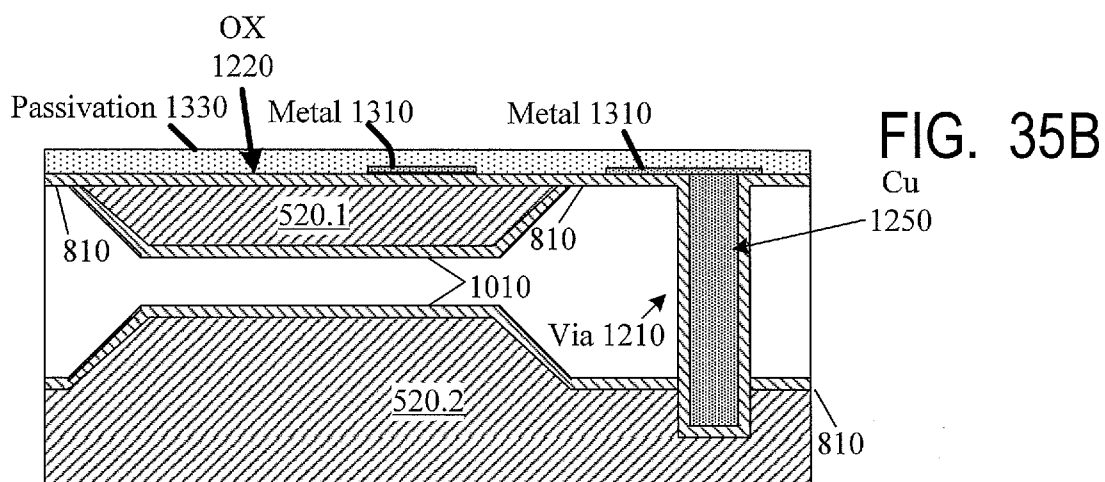
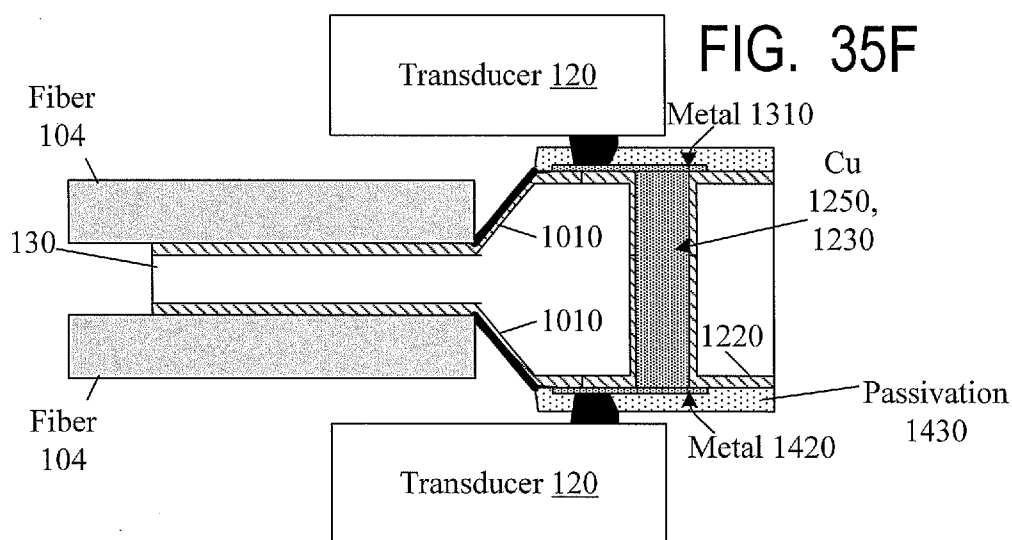
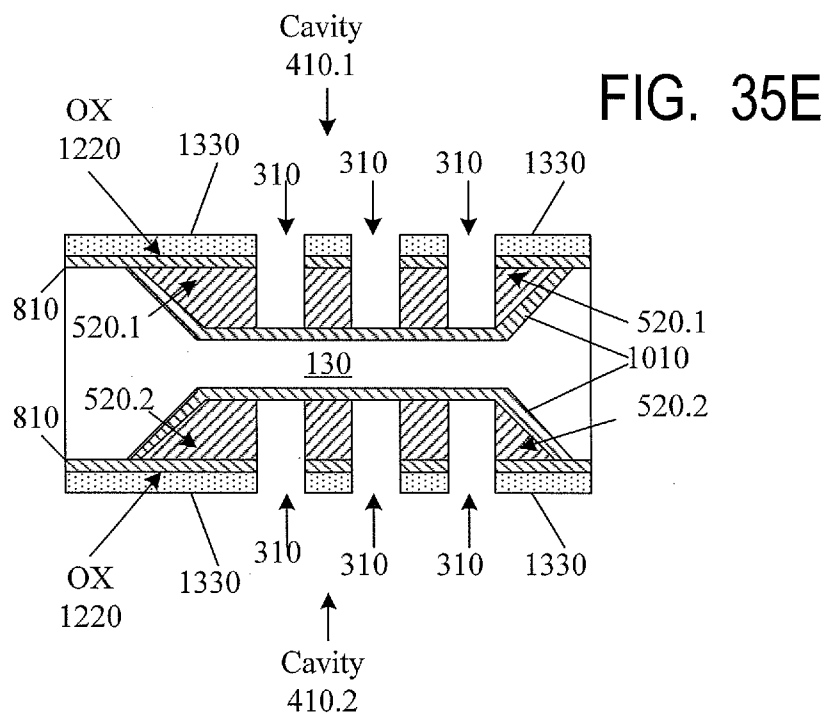


FIG. 35A

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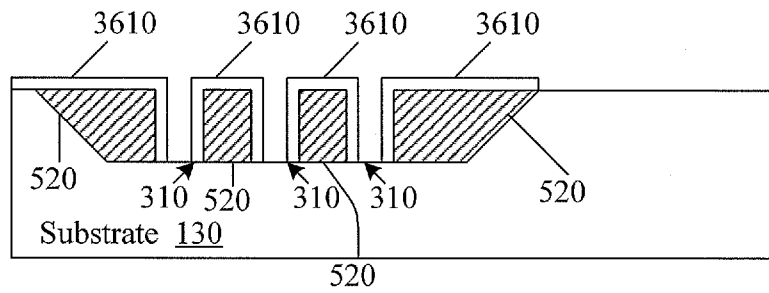


FIG. 36

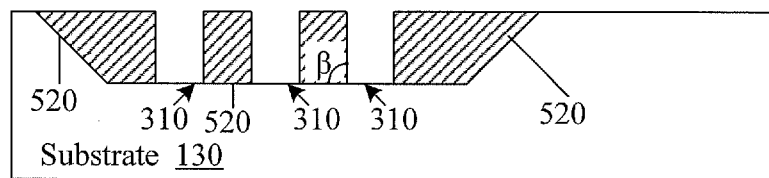


FIG. 37

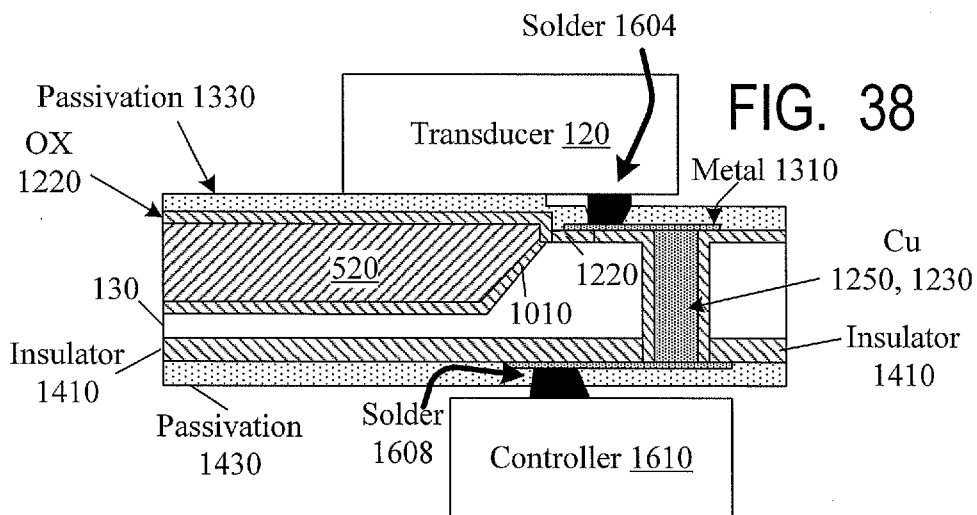


FIG. 38

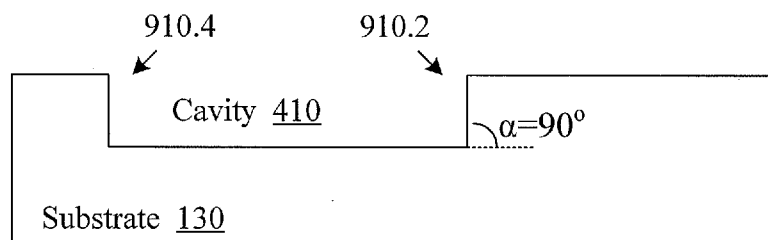
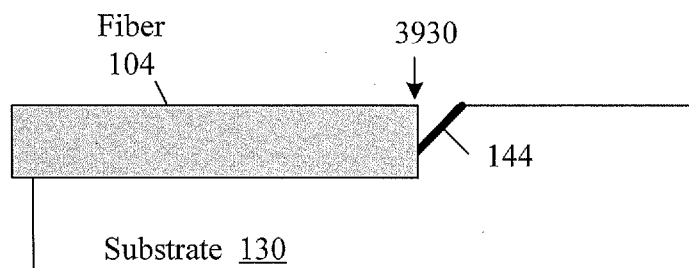
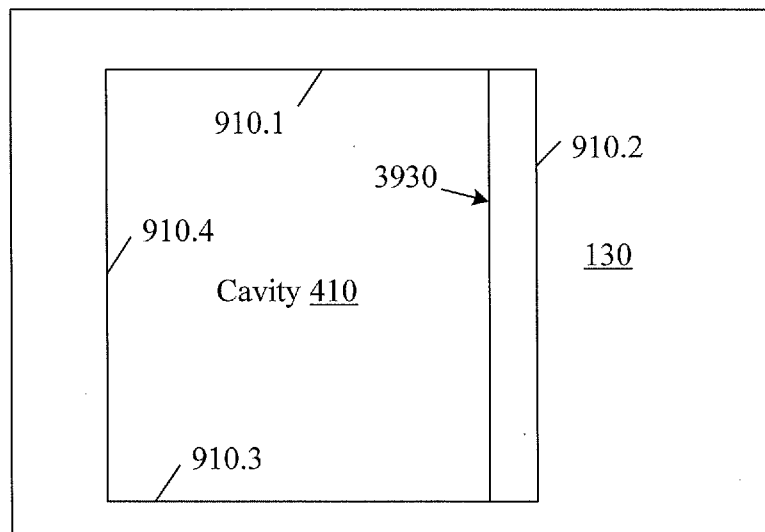
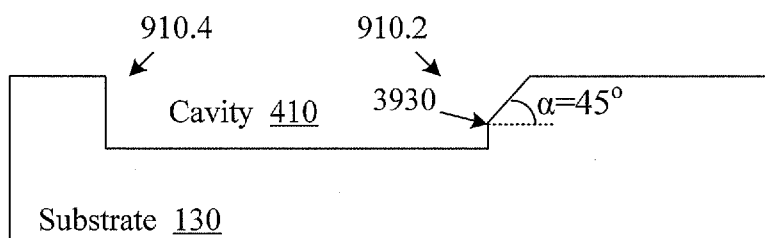
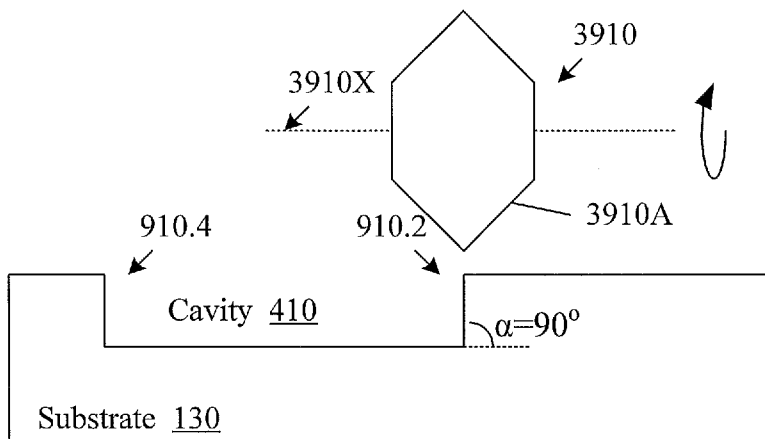


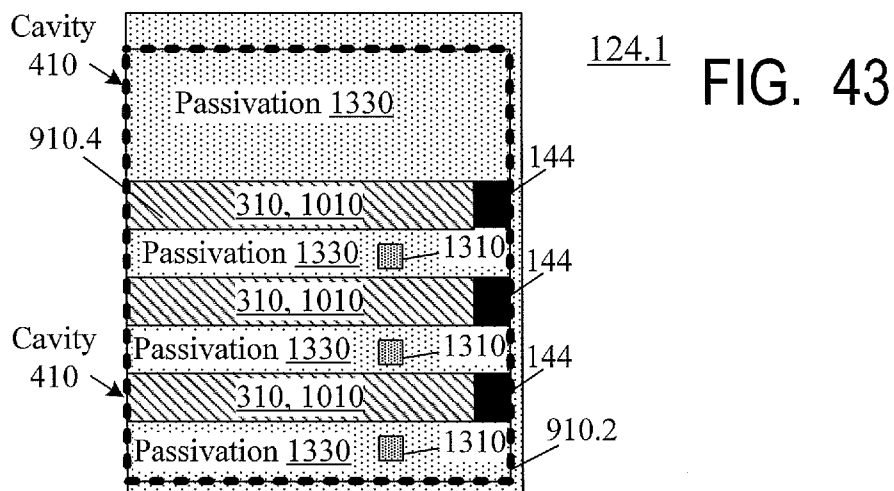
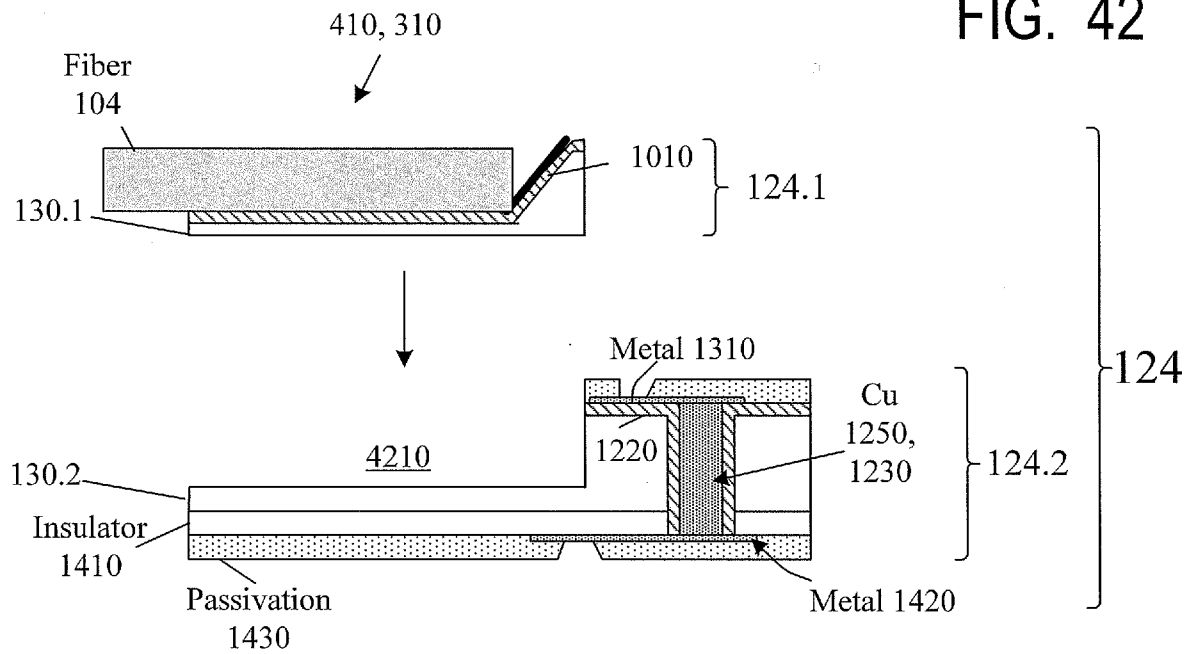
FIG. 39A

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FIG. 42



## INTERNATIONAL SEARCH REPORT

International application No  
PCT/US2013/020578

A. CLASSIFICATION OF SUBJECT MATTER  
INV. G02B6/42 G02B6/36  
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                   | Relevant to claim No. |
|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| X         | US 2003/123819 A1 (NAKANISHI HIROMI [JP]<br>ET AL) 3 July 2003 (2003-07-03)<br>paragraph [0102] - paragraph [0132];<br>figure 1<br>paragraph [0168] - paragraph [0172];<br>figure 10 | 1-20                  |
| X         | -----<br>US 2011/075965 A1 (DEMERITT JEFFERY ALAN<br>[US] ET AL) 31 March 2011 (2011-03-31)<br>paragraph [0087] - paragraph [0090];<br>figures 19, 22                                | 21-33                 |
| X         | -----<br>US 2002/015920 A1 (STEINBERG DAN A [US])<br>7 February 2002 (2002-02-07)<br>paragraph [0049] - paragraph [0053];<br>figures 11-17                                           | 34-40                 |
|           | -----<br>-/--                                                                                                                                                                        |                       |



Further documents are listed in the continuation of Box C.



See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

11 April 2013

Date of mailing of the international search report

24/04/2013

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040,  
Fax: (+31-70) 340-3016

Authorized officer

A. Jacobs

## INTERNATIONAL SEARCH REPORT

International application No

PCT/US2013/020578

| C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT |                                                                                                                                                                                                        |                       |
|------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Category*                                            | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                     | Relevant to claim No. |
| X                                                    | WO 2010/105369 A1 (REFLEX PHOTONICS INC [CA]; ROLSTON DAVID R [CA]; IYER RAJIV [CA]; FU S) 23 September 2010 (2010-09-23) paragraph [0068] - paragraph [0070]; figures 22-23 paragraph [0007]<br>----- | 41-46                 |
| X                                                    | EP 0 987 769 A2 (SUMITOMO ELECTRIC INDUSTRIES [JP])<br>22 March 2000 (2000-03-22)<br>paragraph [0048] - paragraph [0067];<br>figures 10-15<br>paragraph [0070]; figure 25<br>-----                     | 47-52                 |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2013/020578

| Patent document<br>cited in search report | Publication<br>date | Patent family<br>member(s) | Publication<br>date |
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|                                           |                     | WO 2010105369 A1           | 23-09-2010          |
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| EP 0987769 A2                             | 22-03-2000          | CA 2282612 A1              | 18-03-2000          |
|                                           |                     | DE 69907351 D1             | 05-06-2003          |
|                                           |                     | DE 69907351 T2             | 06-11-2003          |
|                                           |                     | DK 987769 T3               | 14-07-2003          |
|                                           |                     | EP 0987769 A2              | 22-03-2000          |
|                                           |                     | US 6257772 B1              | 10-07-2001          |
| -----                                     |                     |                            |                     |