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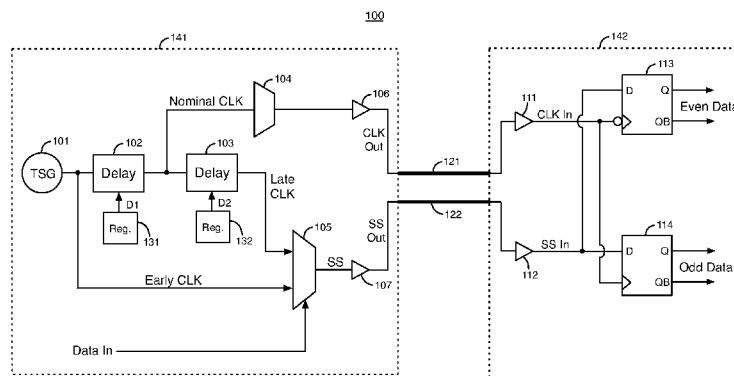


FIG. 1A

(57) **Abstract:** A system includes a transmitter circuit and a receiver circuit that are coupled together through transmission lines. The transmitter circuit generates an early timing signal, a nominal timing signal, and a late timing signal. A multiplexer circuit selects between the early and the late timing signals based on a data signal to generate an encoded output signal that encodes the data signal. The nominal timing signal and the encoded output signal are transmitted through the transmission lines to the receiver circuit. The receiver circuit samples the encoded output signal in response to the nominal timing signal to generate even and odd sampled data signals. Complementary timing signals can be transmitted through transmission lines on opposite sides of the encoded output signal to provide crosstalk cancellation.

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Methods and Apparatus for Transmission of Data

CROSS REFERENCE TO RELATED APPLICATION

[0001] This patent application claims the benefit of U.S. provisional patent application 61/320,878, filed April 5, 2010, which is incorporated by reference herein in its entirety.

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TECHNICAL FIELD

[0002] This disclosure relates to electronic circuits, and more particularly, to techniques for transmission of information between a transmitter and a receiver.

BACKGROUND

[0003] In some conventional source synchronous timing systems, a timing signal and a related data signal may experience timing skew relative to one another. Power supply induced jitter (PSIJ) in the timing signal may not be common with the PSIJ in the data signal. The different PSIJ between the clock and the data signals may have an adverse effect on the receiver's ability to accurately sample the data signal.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1A illustrates an example of a system that transmits a timing signal and a phase-modulated signal from a transmitter circuit to a receiver circuit.

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[0005] Figure 1B is a timing diagram that illustrates example waveforms for various signals in the system of Figure 1A.

[0006] Figure 2 illustrates another example of a system that transmits a timing signal and a phase-modulated signal from a transmitter circuit to a receiver circuit.

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[0007] Figure 3A illustrates an example of a system that provides crosstalk cancellation between signals transmitted through adjacent transmission lines from transmitter circuits to receiver circuits.

[0008] Figure 3B illustrates another example of a system that provides crosstalk cancellation between signals transmitted through adjacent transmission lines from transmitter circuits to receiver circuits.

DETAILED DESCRIPTION

[0009] According to embodiments described in more detail below, a system, circuits and techniques for exchanging information between two different circuits disposed on a single chip or two different circuits disposed on separate integrated circuit devices (ICs) is disclosed. In an embodiment, the system includes a transmitter circuit on a first IC and a receiver circuit on a second IC, which are coupled together through transmission lines. The transmitter circuit generates an early timing signal, a nominal timing signal, and a late timing signal. The nominal timing signal is delayed relative to the early timing signal. The late timing signal is delayed relative to the nominal timing signal. A multiplexer circuit selects between the early and the late timing signals based on a data signal to generate an encoded output signal that encodes the data signal. The nominal timing signal and the encoded output signal are transmitted through the transmission lines to the receiver circuit. The receiver circuit samples the encoded output signal in response to the nominal timing signal to generate sampled data signals. By delay encoding the data using early and late versions of the timing signal output at the transmitter as the encoded output signal, the edges of the nominal timing signal occur nominally centered in the sampling windows of the encoded output signal.

[0010] The system, in an embodiment, includes a first circuit disposed on a first IC, a second circuit disposed on a second IC, and three transmission lines. The three transmission lines are coupled to the first and the second circuits. The first circuit transmits a first timing signal through a first transmission line to the second circuit. The first circuit transmits a signal containing encoded data through a second transmission line to the second circuit. The first circuit transmits a second timing signal that is an inverse of the first timing signal through a third transmission line to the second circuit. The first and the third transmission lines are adjacent to and on opposite sides of the second transmission line. The timing signals transmitted through the first and the third transmission lines cancel crosstalk in the signal containing the encoded data that is transmitted through the second transmission line.

[0011] Figure 1A illustrates an example of a system 100 that transmits a timing signal and a phase-modulated signal from a transmitter circuit to a receiver circuit. The transmitter circuit encodes a data signal to be output as a phase-modulated signal. The receiver circuit decodes the data from the phase-modulated signal by sampling the phase modulated data using the timing signal.

[0012] System 100 includes a transmitter circuit 141 and a receiver circuit 142. The transmitter circuit 141 includes a timing signal generation (TSG) circuit 101, delay circuits 102-103, multiplexer circuits 104-105, registers 131-132, and driver circuits 106-107. The receiver circuit 142 includes receiver circuits 111-112 and flip-flops 113-114. The transmitter circuit 141 and the receiver circuit 142 can be in two different integrated circuits or on the same integrated circuit. The transmitter 141 and receiver 142 are coupled together through transmission lines 121-122. Transmission lines 121-122 can be

off-chip or on-chip and may be implemented using conductive signal traces such as striplines, microstrip traces or other types of signal lines.

[0013] As an example that is not intended to be limiting, one of these two integrated circuits can be a memory device, and the other integrated circuit can control the operation of the memory device. For example, one of the integrated circuits can be a memory controller device, such as a processor, application specific integrated circuit (ASIC), System on chip (SOC), etc., and the other integrated circuit can be a memory device such as DDR SDRAM, any generation of graphics memory (GDDR), or any memory device that includes an array of memory cells, for example, dynamic random access memory (RAM) cells, static RAM (SRAM) cells or a non volatile memory device such as a Flash device.

[0014] In one embodiment, timing signal generation circuit 101 generates a first timing signal Early CLK. Timing signal generation (TSG) circuit 101 can be an oscillator circuit (e.g., a voltage controlled oscillator of a phase-locked loop (PLL)), a delay-locked loop (DLL), or a timing reference that is sourced externally. Delay circuit 102 delays the Early CLK signal to generate a second timing signal Nominal CLK. Delay circuit 103 delays the Nominal CLK signal to generate a third timing signal Late CLK.

[0015] The timing signals Early CLK, Nominal CLK, and Late CLK can be, for example, periodic clock signals. In an embodiment, the Nominal CLK signal can be a strobe signal that indicates to the receiver circuit 142 when to sample the data.

[0016] Delay circuit 102 can provide any suitable delay to Nominal CLK relative to Early CLK, and delay circuit 103 can provide any suitable delay to Late CLK relative to

Nominal CLK. For example, delay circuit 102 can provide a delay of 90° or slightly less than 90° to Nominal CLK relative to Early CLK, and delay circuit 103 can provide a delay of 90° or slightly less than 90° to Late CLK relative to Nominal CLK. As another example, delay circuit 102 can provide a delay between 0° and 90° to Nominal CLK
5 relative to Early CLK, and delay circuit 103 can provide a delay between 0° and 90° to Late CLK relative to Nominal CLK.

[0017] Using delays of slightly less than 90° in each of the delay circuits 102-103 may generate runt pulses in the Nominal CLK signal. Runt pulses in the Nominal CLK signal limit the run length of the sampled data signals generated by the receiver circuit 142 to
10 less than 2 unit intervals (or 2 bits). Each unit interval is a symbol period in the data signal. The runt pulses reduce inter-symbol interference (ISI) in the sampled data signals.

[0018] Transmitter circuit 141 receives an input data signal Data In. In an embodiment, the Data In signal has a double data rate (DDR) with respect to the Nominal CLK signal
15 such that the encoded output signal can be referenced to both rising and falling edges of the timing signal CLK Out, described in more detail below.

[0019] In an embodiment, delay circuits 102 and 103 are programmable delay circuits. The programmable delay values D1-D2 of delay circuits 102-103 are stored in registers 131-132 and are transmitted to inputs of delay circuits 102-103, respectively, as shown in
20 Figure 1A. The programmable delay values of delay circuits 102-103 can be varied to accommodate Data In signals that have different data signaling rates.

[0020] The Data In signal is transmitted to the select input of multiplexer 105.

Multiplexer 105 selects either the Early CLK signal or the Late CLK signal as selected signal SS based on the logic state of the Data In signal. As an example, multiplexer 105 may select Early CLK when Data In is in a logic high state and Late CLK when Data In
5 is in a logic low state.

[0021] The selected signal SS is an encoded phase-modulated representation of the data embodied in the Data In signal. The phase of the selected signal SS is skewed by multiplexer 105 transitioning between selecting the Early and Late CLK signals. The selected signal SS is transmitted to the input of driver circuit 107. Driver circuit 107
10 drives the selected signal SS as signal SS Out to receiver circuit 142 through transmission line 122.

[0022] Multiplexer circuit 104 is configured to transmit the Nominal CLK timing signal from the output of delay circuit 102 to the input of driver circuit 106. In an embodiment, multiplexer circuit 104 induces power supply induced jitter (PSIJ) to the Nominal CLK
15 signal that matches the PSIJ induced in the output of multiplexer 105 which generates the selected signal SS. To this end, multiplexers 104 and 105 receive charge from the same power supply voltage.

[0023] Driver circuit 106 drives the Nominal CLK signal to receiver circuit 142 through transmission line 121 as timing signal CLK Out. Driver circuits 106-107 transmit the
20 CLK Out and SS Out signals in parallel through transmission lines 121-122 to inputs of receiver circuits 111-112, respectively, in receiver circuit 142. Driver circuits 106 and 107 can be implemented, for example, by respective pairs of pull-up and pull-down driver transistors.

[0024] Receiver circuit 111 buffers the CLK Out signal to generate a buffered timing signal CLK In. The CLK In signal is transmitted from the output of receiver circuit 111 to the timing inputs of flip-flops 113 and 114. Receiver circuit 112 buffers the selected signal SS Out to generate a buffered signal SS In. The SS In signal is transmitted from the output of receiver circuit 112 to the D inputs of flip-flops 113 and 114. Flip-flops 113-114 function as sampler circuits that generate Even and Odd samples of the data encoded in the selected signal SS In. The Even samples of the data are generated on the falling edges of the CLK In signal, and the Odd samples of the data are generated on the rising edges of the CLK In signal. Each Even and Odd sample of the data is generated in one unit interval of the data. The Even and Odd samples are generated as Even Data and Odd Data signals at the outputs of flip-flops 113-114, respectively.

[0025] Flip-flop 113 stores the value of the selected signal SS In at its Q and QB outputs as a differential Even Data signal in response to each falling edge of the CLK In signal. Flip-flop 114 stores the value of the selected signal SS In at its Q and QB outputs as a differential Odd Data signal in response to each rising edge of the CLK In signal.

[0026] Flip-flop 113 generates one sampled bit in the Even Data signal that represents a bit in the Data In signal for each even-numbered unit interval. Flip-flop 114 generates one sampled bit in the Odd Data signal that represents a bit in the Data In signal for each odd-numbered unit interval. Two unit intervals occur in each period of the Nominal CLK signal, and each unit interval corresponds to one symbol period in the Data In signal. Flip-flops 113-114 generate two sampled bits of data that represent the Data In signal in each period of the CLK In signal.

[0027] In an embodiment, delay circuits 102 and 103 cause the edges of the Nominal CLK signal to be halfway between corresponding edges of the Early and Late CLK signals. As a result, the edges of the CLK In signal are substantially in the centers of the sampling windows of the selected signal SS In. Receiver circuit 142 does not need to
5 shift the phase of the CLK In signal to achieve the phase alignment needed to sample data encoded in the selected signal SS In. As a result, system 100 may benefit from reduced power consumption and complexity at receiver circuit 142. For example, system 100 can operate at high signal frequencies without using an alignment circuit in receiver circuit 142 that centers a sampling timing signal in the data sampling window. In receiver
10 circuit 142, the CLK In signal is transmitted directly from an input pin through receiver circuit 111 to the timing inputs of flip-flops 113-114.

[0028] The Nominal CLK signal is routed through delay circuit 102, multiplexer 104, driver circuit 106, and receiver circuit 111 as signals CLK Out and CLK In. The selected signal SS is routed through multiplexer 105, driver circuit 107, and receiver circuit 112 as
15 signals SS Out and SS In. The selected signal SS is also routed through delay circuits 102-103 when the Data In signal is in one of its two logic states. Thus, in an embodiment, the Nominal CLK and SS signals are routed through matching circuit elements, except that the SS signal is routed through one more or one less delay circuit. Each of the circuits 102-107 receives charge from the same power supply voltage. In this
20 example, system 100 generates nearly the same PSIJ in the CLK Out and SS Out signals. The one extra delay circuit that is not in common between the paths of the CLK Out and SS Out signals generates different PSIJ between the CLK Out and SS Out signals that

accumulates for less than one-half of a unit interval. As a result, the extra delay circuit does not adversely affect the timing relationship between these signals.

[0029] Figure 1B is a timing diagram that illustrates example waveforms of the Early CLK, Nominal CLK, Late CLK, SS Out, SS In, CLK Out, CLK In, Odd Data and Even Data signals in system 100 of Figure 1A. In the example of Figure 1B, the Nominal CLK signal is delayed by 90° relative to the Early CLK signal, and the Late CLK signal is delayed by 90° relative to the Nominal CLK signal. The waveform of the SS Out signal is based on the Data In signal (not shown in Figure 1B) causing multiplexer 105 to transition between selecting the Early and Late CLK signals.

[0030] As shown in Figure 1B, transmission line 121 delays the CLK IN signal relative to the CLK Out signal, and transmission line 122 delays the SS In signal relative to the SS Out signal. Also, as shown in Figure 1B, the Odd Data signal transitions in response to each rising edge of the CLK In signal, and the Even Data signal transitions in response to each falling edge of the CLK In signal.

[0031] Figure 2 illustrates another example of a system 200 that transmits a timing signal and a phase-modulated signal from a transmitter circuit to a receiver circuit. System 200 also includes a transmitter circuit 210 and a receiver circuit 142.

[0032] The transmitter circuit 210 includes a timing signal generation (TSG) circuit 201, multiplexer circuits 104-105, and driver circuits 106-107. The receiver circuit 142 includes receiver circuits 111-112 and flip-flops 113-114. The transmitter circuit 210 and the receiver circuit 142 can be in two different integrated circuits or on the same

integrated circuit. Multiplexer circuits 104-105, driver circuits 106-107, receiver circuits 111-112, and flip-flops 113-114 function as described above with respect to Figure 1A.

[0033] In system 200, TSG circuit 201 generates the Early CLK signal, the Nominal CLK signal, and the Late CLK signal without using delay circuits 102-103. TSG circuit 201 can be, for example, a ring oscillator formed by delay circuits coupled in a ring configuration. The ring oscillator can be part of a phase-locked loop circuit (PLL) and instantiated as a voltage controlled oscillator. Delay circuits in the ring oscillator can generate the Early CLK, Nominal CLK, and Late CLK signals. As another example, TSG circuit 201 can be an inductor-capacitor (LC) tank oscillator or a crystal oscillator that generates the Early CLK, Nominal CLK, and Late CLK signals. TSG circuit 201 may cause the Early CLK and Nominal CLK signals to be offset in phase by 90° or less. TSG circuit 201 may cause the Nominal CLK and Late CLK signals to be offset in phase by 90° or less. Alternatively, or in combination with TSG circuit 201, a delay-locked loop circuit can be used where multiple output signals of the delay-locked loop are multiplexed from a delay line to create the delays in the Nominal and Late CLK signals.

[0034] Figure 3A illustrates an example of a system 300 that provides crosstalk cancellation between signals transmitted through adjacent transmission lines from transmitter circuits to receiver circuits. System 300 includes an integrated circuit 301, an integrated circuit 302, and transmission lines 311-320. Integrated circuits 301 and 302 can be any types of integrated circuits. As an example that is not intended to be limiting, integrated circuit 301 can be a memory controller integrated circuit, and integrated circuit 302 can be a memory integrated circuit.

[0035] Integrated circuit (IC) 301 includes a phase-locked loop (PLL) circuit 303 and transmitter circuits 321-324. PLL 303 generates timing signals CLK and CLKN. Timing signal CLKN is the inverse of timing signal CLK. Signals CLK and CLKN can be, for example, periodic clock signals. Integrated circuit (IC) 302 includes receiver circuits 331-334 and a storage array 341 of memory cells. Transmitter circuits 321-324 transmit signals through transmission lines 311-318 to receiver circuits 331-334.

[0036] In one embodiment, system 300 is implemented using the circuit architecture shown in Figure 1A. In this embodiment, TSG circuit 101 is located in PLL circuit 303, and each of the transmitter circuits 321-324 includes circuits 102-107 coupled as shown in Figure 1A. Alternatively or in combination, PLL circuit 303 may be a delay-locked loop circuit (DLL). Transmitter circuits 321 and 323 use timing signal CLK as the Early CLK signal. Delay circuits 102-103 in each of transmitter circuits 321 and 323 generate Nominal and Late CLK signals by delaying the CLK signal. Transmitter circuits 322 and 324 use timing signal CLKN as the Early CLK signal. Delay circuits 102-103 in each of transmitter circuits 322 and 324 generate Nominal and Late CLK signals by delaying the CLKN signal. Each of the receiver circuits 331-334 includes circuits 111-114 coupled as shown in Figure 1A.

[0037] In another embodiment, system 300 is implemented using the circuit architecture shown in Figure 2. In this embodiment, TSG circuit 201 is located in PLL circuit 303. Early, Nominal, and Late timing signals are transmitted from PLL 303 to transmitter circuits 321 and 323. Inverted versions of the Early, Nominal, and Late timing signals are transmitted from PLL 303 to transmitter circuits 322 and 324.

[0038] Transmitters 321 and 323 transmit Nominal CLK through transmission lines 311 and 315 to receivers 331 and 333 as the CLKOUT1 and CLKOUT2 signals, respectively. Transmitters 322 and 324 transmit Nominal CLK through transmission lines 313 and 317 to receivers 332 and 334 as the CLKOUTN1 and CLKOUTN2 signals, respectively.

5 CLKOUT1, CLKOUT2, CLKOUTN1, and CLKOUTN2 may be, for example, periodic clock signals or strobe signals.

[0039] Transmitter circuits 321-324 transmit phase-modulated signals SS1, SS2, SS3, and SS4 through transmission lines 312, 314, 316, and 318 to receiver circuits 331-334, respectively. IC 302 may, for example, store data sampled from signals SS1-SS4 in

10 memory storage array 341. Timing signals CLKOUT3 and CLKOUTN3 are transmitted from IC 301 to IC 302 through transmission lines 319-320, respectively. Timing signal CLKOUT3 may be CLKOUT1 or CLKOUT2. Timing signal CLKOUTN3 may be CLKOUTN1 or CLKOUTN2. Timing signals CLKOUT3 and CLKOUTN3 may be, for example, periodic clock signals.

15 [0040] Each of the transmission lines 312, 314, 316, and 318 that transmits a phase-modulated signal SS1, SS2, SS3, or SS4 is adjacent to two transmission lines that transmit complementary timing signals. For example, transmission line 312 is adjacent to transmission lines 311 and 313 that transmit timing signals CLKOUT1 and CLKOUTN1, respectively. Signals CLKOUT1 and CLKOUTN1 are complementary timing signals

20 that are 180° out of phase. Signals CLKOUT2 and CLKOUTN1 are complementary timing signals that are 180° out of phase. Signals CLKOUT2 and CLKOUTN2 are complementary timing signals that are 180° out of phase. Signals CLKOUTN2 and CLKOUT3 are complementary timing signals that are 180° out of phase.

[0041] As a result, crosstalk that CLKOUT1 generates in signal SS1 is cancelled out by crosstalk that CLKOUTN1 generates in SS1. Crosstalk that CLKOUTN1 generates in signal SS2 is cancelled out by crosstalk that CLKOUT2 generates in SS2. Crosstalk that CLKOUT2 generates in signal SS3 is cancelled out by crosstalk that CLKOUTN2 generates in SS3. Crosstalk that CLKOUTN2 generates in signal SS4 is cancelled out by crosstalk that CLKOUT3 generates in SS4.

[0042] Figure 3B illustrates another example of a system 350 that provides crosstalk cancellation between signals transmitted through adjacent transmission lines from transmitter circuits to receiver circuits. System 350 includes an integrated circuit 351, an integrated circuit 352, and transmission lines 361-370. Integrated circuits 351 and 352 can be any type of integrated circuits. As an example that is not intended to be limiting, IC 351 can be an integrated circuit device that controls the operation of a memory device, for example a memory controller device, such as a processor, application specific integrated circuit (ASIC), System on chip (SOC), etc. IC 352 can be a memory device, e.g., DDR SDRAM, any generation of graphics memory (GDDR), or any memory device that includes an array of memory cells, for example, dynamic random access memory (RAM) cells, static RAM (SRAM) cells or a non-volatile memory device such as a Flash device.

[0043] IC 351 includes PLL circuit 353, receiver circuits 371-374, and driver circuits 375-376. IC 352 includes transmitter circuits 381-384 and a storage array 391 of memory cells. Transmitter circuits 381-384 transmit signals through transmission lines 361-368 to receiver circuits 371-374. PLL 353 generates complementary timing signals CLK and CLKN that are 180° out of phase. Complementary timing signals CLK and

CLKN are transmitted from PLL 353 to driver circuits 375-376, respectively. Driver circuits 375-376 transmit timing signals CLK and CLKN from IC 351 to IC 352 through transmission lines 369-370, respectively.

[0044] In an embodiment, each of transmitter circuits 381-384 includes circuits 102-107
5 coupled as shown in Figure 1A, and TSG circuit 101 is located in PLL circuit 353. Each of the receiver circuits 371-374 includes circuits 111-114 coupled as shown in Figure 1A. In this embodiment, transmitter circuits 381 and 383 use signal CLK as the Early CLK signal. Delay circuits 102-103 in each of transmitter circuits 381 and 383 generate Nominal and Late CLK signals by delaying the CLK signal. Transmitter circuits 382 and
10 384 use signal CLKN as the Early CLK signal. Delay circuits 102-103 in each of transmitter circuits 382 and 384 generate Nominal and Late CLK signals by delaying the CLKN signal.

[0045] Transmitter circuits 381 and 383 transmit Nominal CLK through transmission lines 361 and 365 to receiver circuits 371 and 373 as the CLKOUT1 and CLKOUT2
15 signals, respectively. Transmitter circuits 382 and 384 transmit Nominal CLK through transmission lines 363 and 367 to receiver circuits 372 and 374 as the CLKOUTN1 and CLKOUTN2 signals, respectively. Transmitter circuits 381-384 transmit phase-modulated signals SS1, SS2, SS3, and SS4 through transmission lines 362, 364, 366, and 368 to receiver circuits 371-374, respectively. IC 352 may, for example, read data that is
20 encoded in signals SS1-SS4 from memory storage array 391.

[0046] In system 350, signals CLKOUT1 and CLKOUTN1 are 180° out of phase. Signals CLKOUT2 and CLKOUTN1 are 180° out of phase. Signals CLKOUT2 and CLKOUTN2 are 180° out of phase.

[0047] Each of the transmission lines 362, 364, and 366 that transmits a phase-modulated signal SS1-SS3 is adjacent to two transmission lines that transmit complementary timing signals. For example, transmission line 362 is adjacent to transmission lines 361 and 363 that transmit complementary timing signals CLKOUT1 and CLKOUTN1. Crosstalk that CLKOUT1 generates in signal SS1 is cancelled out by crosstalk that CLKOUTN1 generates in SS1. Crosstalk that CLKOUTN1 generates in signal SS2 is cancelled out by crosstalk that CLKOUT2 generates in SS2. Crosstalk that CLKOUT2 generates in signal SS3 is cancelled out by crosstalk that CLKOUTN2 generates in SS3. Although crosstalk generated by CLKOUTN2 and CLK in SS4 is not cancelled, a filter circuit can be placed in IC 351 to filter out the effects of crosstalk in SS4.

[0048] In another embodiment, system 350 is implemented using the circuit architecture shown in Figure 2. In this embodiment, TSG circuit 201 is located in PLL circuit 353. Early, Nominal, and Late timing signals are transmitted from PLL 353 to transmitter circuits 381 and 383. Inverted versions of the Early, Nominal, and Late timing signals are transmitted from PLL 353 to transmitter circuits 382 and 384.

[0049] The embodiments of Figures 3A-3B substantially reduce the crosstalk that timing signal transmission lines generate in adjacent transmission lines that transmit the phase-modulated signals. Transmission lines that are arranged to transmit an alternating pattern of timing and phase-modulated signals as shown in Figures 3A-3B can be placed closer together, reducing the routing impact of additional transmission lines.

[0050] Any two complementary timing signals transmitted through transmission lines in systems 300 and 350 can be used to generate a constant reference voltage. For example, a resistor divider can be coupled between transmission lines 311 and 313 in system 300

to generate a constant reference voltage. The reference voltage can be used for a variety of purposes. For example, if receiver circuits 111-112 are differential amplifiers, the reference voltage can be used by receiver circuits 111-112 to amplify the CLK Out and SS Out signals.

5 [0051] The integrated circuits shown and described herein can be, for example, memory integrated circuits, controller integrated circuits, processor integrated circuits, analog integrated circuits, digital integrated circuits, programmable integrated circuits, etc.

[0052] The foregoing description of the exemplary embodiments has been presented for the purposes of illustration and description. The foregoing description is not intended to
10 be exhaustive or limiting to the examples disclosed herein. In some instances, certain features of the embodiments can be employed without a corresponding use of other features as set forth. Many modifications, substitutions, and variations are possible in light of the above teachings, without departing from the scope of the claims.

What is claimed is:

- 1 1. An integrated circuit device comprising:
2 a first output driver to output a timing signal; and
3 a second output driver to output a phase modulated signal
4 generated by selecting, based on a logic state of a data signal, between early and
5 late phases of the timing signal.

- 1 2. The integrated circuit device of claim 1 wherein the timing signal
2 is generated by an oscillator.

- 1 3. The integrated circuit device of claim 2 wherein the oscillator is
2 part of a phase-locked loop circuit.

- 1 4. The integrated circuit device of claim 1 wherein the timing signal
2 is a strobe signal.

- 1 5. The integrated circuit device of claim 1 wherein the timing signal
2 is a clock signal.

- 1 6. The integrated circuit device of claim 1 further comprising a first
2 delay circuit that generates a nominal timing signal using the early phase of the timing
3 signal, and a second delay circuit to generate the late phase of the timing signal from the
4 nominal timing signal, wherein the nominal timing signal is output as the timing signal
5 by the first output driver.

1 7. The integrated circuit device of claim 6 further comprising a
2 multiplexer circuit to receive the early phase of the timing signal and the late phase of the
3 timing signal, the multiplexer circuit to provide, based on the logic state of the data
4 signal, a signal having one of the early and late phases of the timing signal to an input of
5 the second output driver.

1 8. The integrated circuit device of claim 6 further comprising:
2 a first register circuit to store a first value that is representative of a delay
3 time between the early phase of the timing signal and a phase of the nominal timing
4 signal; and
5 a second register circuit to store a second value that is representative of a
6 delay time between the phase of the nominal timing signal and the late phase of the
7 timing signal.

1 9. The integrated circuit device of claim 1, further comprising a
2 storage array that includes a plurality of memory cells.

1 10. The integrated circuit device of claim 1, wherein the integrated
2 circuit devices is a memory controller device.

1 11. A method of operation of an integrated circuit device, the method
2 comprising:
3 outputting a timing signal to a first external signal line;
4 generating a phase modulated signal by selecting, based on a logic state of
5 a data signal, between early and late phases of the timing signal; and

6 outputting the phase modulated signal to a second external signal line.

1 12. The method of claim 11, wherein outputting the timing signal
2 comprises outputting a transition of the timing signal, and wherein outputting the phase
3 modulated signal comprises:

4 for a first logic state of the data signal, outputting a transition of the phase
5 modulated signal that precedes the transition of the timing signal; and

6 for a second logic state of the data signal, outputting a transition of the
7 phase modulated signal that succeeds the transition of the timing signal.

1 13. The method of claim 12, wherein outputting the phase modulated
2 signal further comprises:

3 for the first logic state of the data signal, outputting a transition of the
4 phase modulated signal that precedes the transition of the timing signal by a first
5 predetermined phase amount; and

6 for the second logic state of the data signal, outputting a transition of the
7 phase modulated signal that succeeds the transition of the timing signal by a second
8 predetermined phase amount.

1 14. The method of claim 11, further comprising generating an internal
2 timing reference signal to provide the early phase of the timing signal.

1 15. The method of claim 14 further comprising:
2 delaying the early phase of the timing signal to generate the timing signal;

3 and

4 delaying the timing signal to generate the late phase of the timing signal.

1 16. The method of claim 11 wherein the timing signal is a strobe
2 signal.

1 17. The method of claim 11 wherein the timing signal is a clock signal.

1 18. A phase modulated signal generated by a transmitter circuit
2 comprising:

3 a circuit to provide an early timing signal and a late timing signal, wherein
4 the late timing signal is delayed relative to the early timing signal; and

5 a selection circuit to select, based on a logic state of a data signal, between
6 the early and the late timing signals, the selection circuit to generate the phase modulated
7 signal from the selection between the early and late timing signals.

1 19. A system comprising:

2 first and second circuits; and

3 first, second, and third signal lines coupled to the first and the second

4 circuits, wherein the first circuit transmits a first timing signal through the first signal line

5 to the second circuit, wherein the first circuit transmits a first signal containing encoded

6 data through the second signal line to the second circuit, wherein the first circuit

7 transmits a second timing signal through the third signal line to the second circuit,

8 wherein the first timing signal and the second timing signal are complementary signals,

9 and wherein the first and the third signal lines are adjacent to and on opposite sides of the
10 second signal line.

1 20. The system of claim 19 further comprising:

2 fourth and fifth signal lines coupled to the first and the second circuits,
3 wherein the first circuit transmits a second signal containing encoded data through the
4 fourth signal line to the second circuit, wherein the first circuit transmits a third timing
5 signal through the fifth signal line to the second circuit, wherein the second timing signal
6 and the third timing signal are complementary signals, and wherein the third and the fifth
7 signal lines are adjacent to and on opposite sides of the fourth signal line.

1 21. The system of claim 20 further comprising:
2 sixth and seventh signal lines coupled to the first and the second circuits,
3 wherein the first circuit transmits a third signal containing encoded data through the sixth
4 signal line to the second circuit, wherein the first circuit transmits a fourth timing signal
5 through the seventh signal line to the second circuit, wherein the third timing signal and
6 the fourth timing signal are complementary signals, and wherein the fifth and the seventh
7 signal lines are adjacent to and on opposite sides of the sixth signal line.

1 22. The system of claim 19 wherein the first circuit is disposed on a
2 first integrated circuit device, and wherein the second circuit is disposed on a second
3 integrated circuit device.

1 23. The system of claim 22 wherein one of the first and second
2 integrated circuits is a memory device, and the other of the first and second integrated
3 circuits is a controller device.

1 24. A method of operation of an integrated circuit device, the method
2 comprising:
3 receiving a timing signal from a first external signal line; and

4 in response to the timing signal, sampling from a second external signal
5 line, a phase modulated signal having early and late phases with respect to the timing
6 signal, the early and late phases selected based on a logic state of a data signal.

1 25. The method of claim 24, further comprising, at a transmitter that is
2 separate from the integrated circuit device:

3 outputting the timing signal to the first external signal line; and
4 generating the phase modulated signal having early and late phases with
5 respect to the timing signal, the early and late phases selected based on a logic state of a
6 data signal present in the transmitter; and

7 outputting the phase modulated signal to the second external signal line.

1 26. A transmitter circuit comprising:

2 a circuit to provide an early timing signal and a late timing signal, wherein
3 the late timing signal is delayed relative to the early timing signal; and

4 a selection circuit to select, based on a logic state of a data signal, between
5 the early and the late timing signals, the selection circuit to generate the phase modulated
6 signal from the selection between the early and late timing signals.

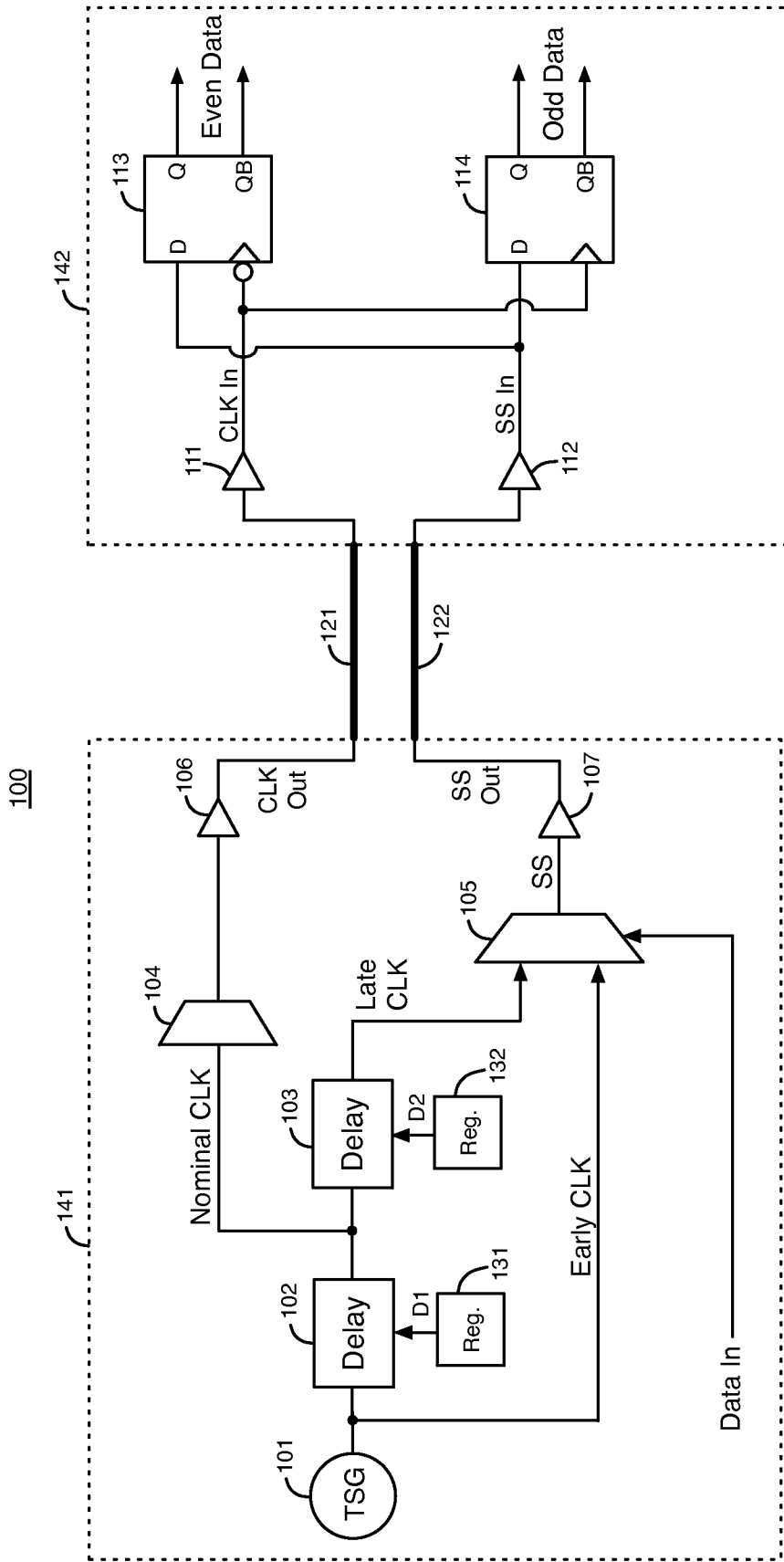


FIG. 1A

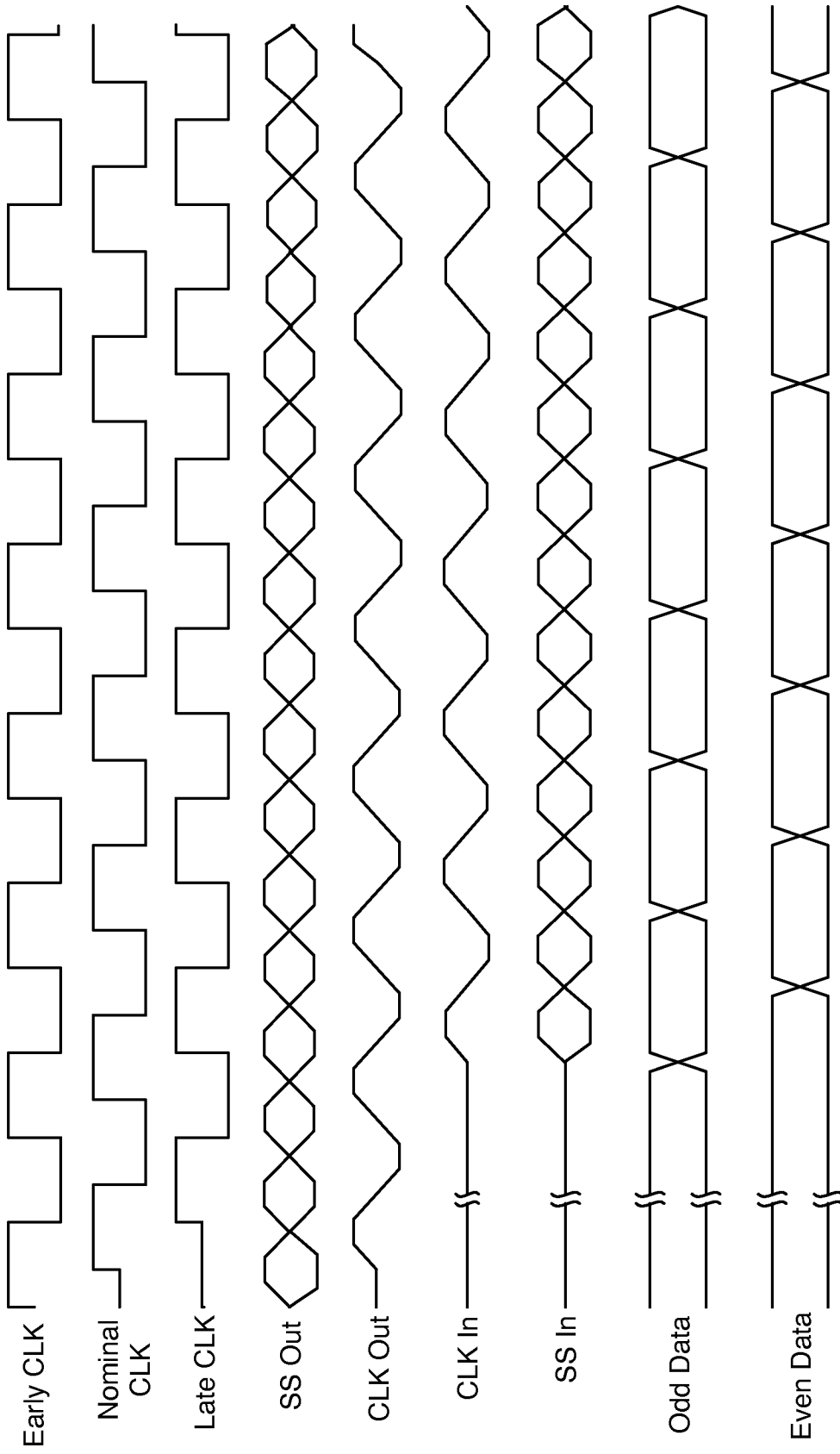


FIG. 1B

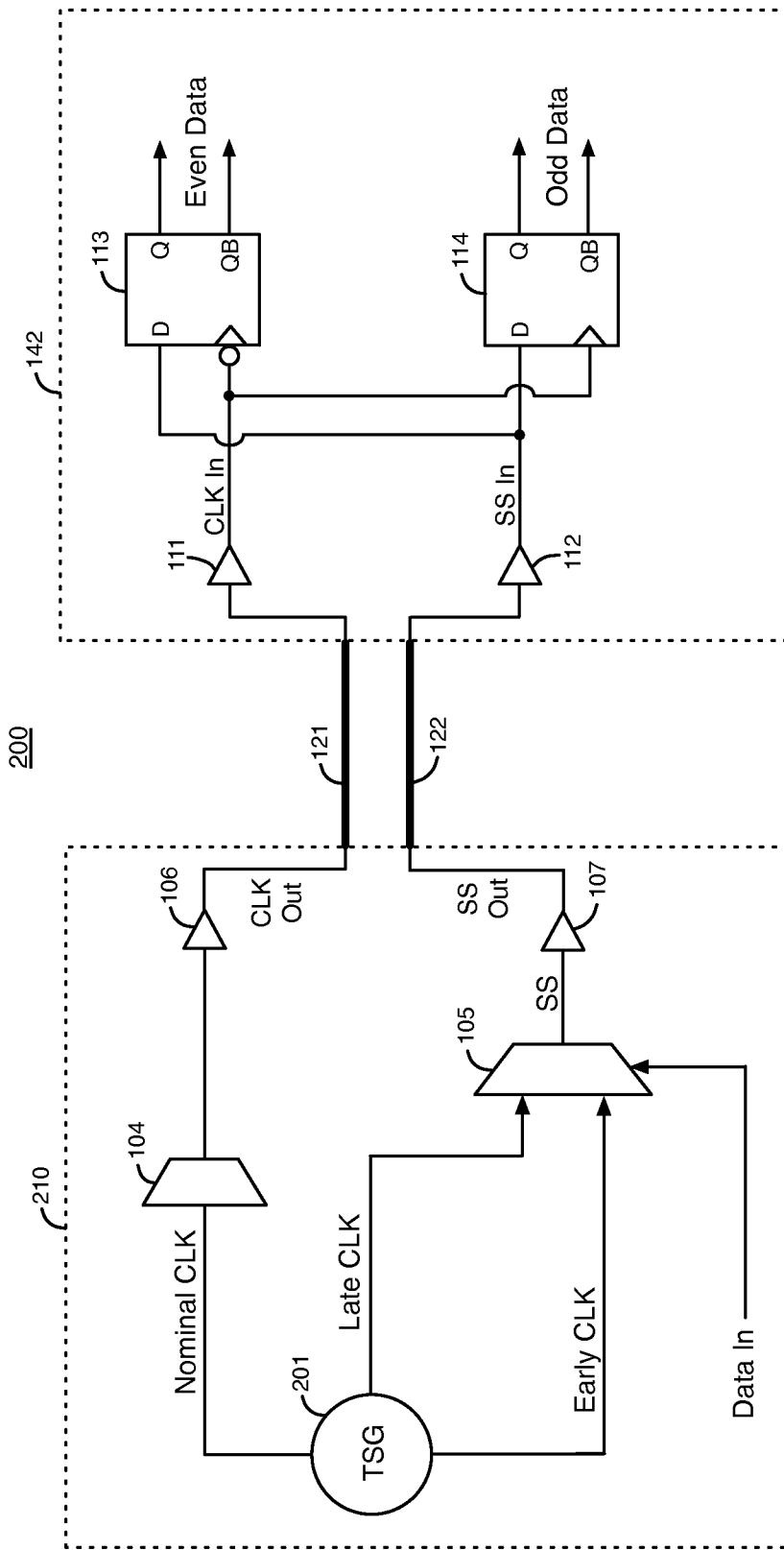


FIG. 2

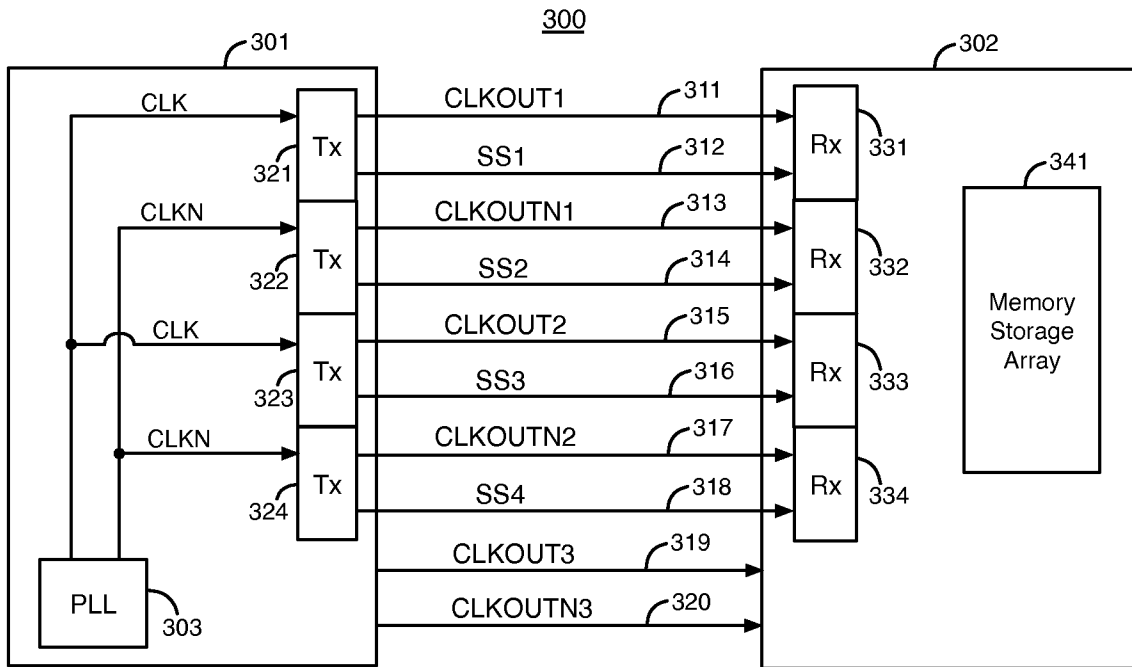


FIG. 3A

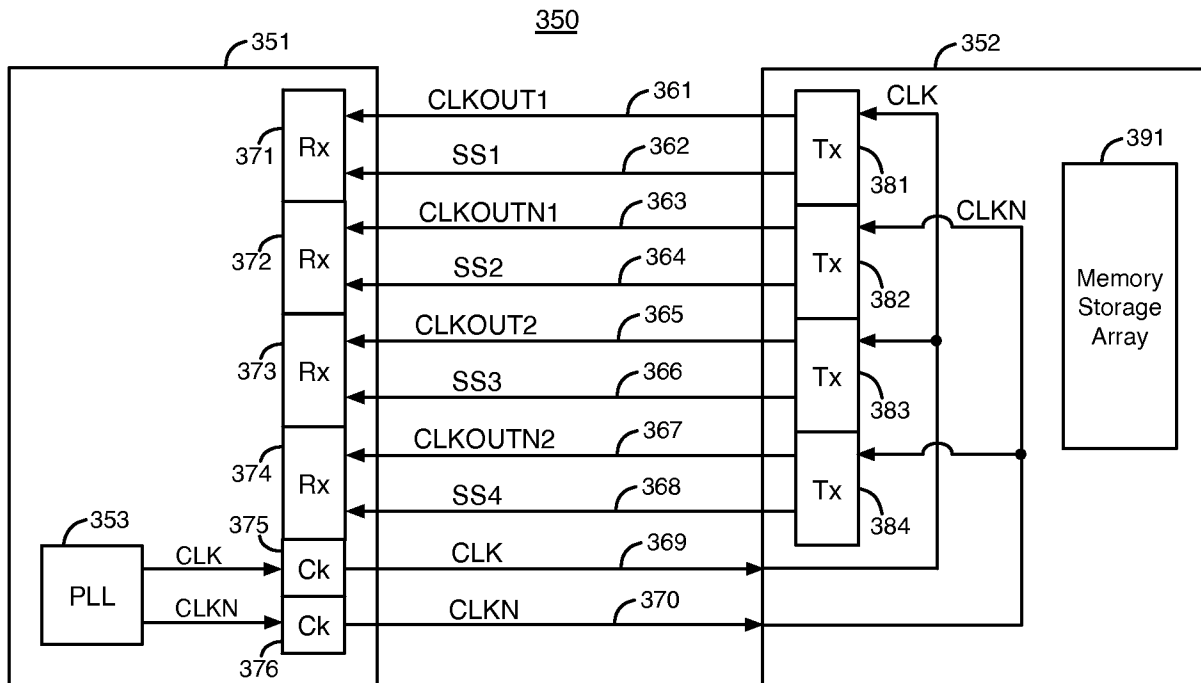


FIG. 3B

A. CLASSIFICATION OF SUBJECT MATTER*G11C 7/22(2006.01)i, G11C 8/00(2006.01)i*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC : G11C, H04L, G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: phase, modulated, data, output, cloack, driver

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007-0064462 A1 (MATSUI) 22 March 2007 See abstract, figures 1-2, claim 18.	1-17, 19-26
A	US 2010-0014610 A1 (JASO) 21 January 2010 See abstract, figure 1A, claims 1-2.	1-17, 19-26
A	US 2009-0323444 A1 (KIM et al.) 31 December 2009 See abstract, figures 1,3, paragraph 0013-0015.	1-17, 19-26

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

31 AUGUST 2011 (31.08.2011)

Date of mailing of the international search report

01 SEPTEMBER 2011 (01.09.2011)

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Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.: 18
because they relate to subject matter not required to be searched by this Authority, namely:
Claim 18 is directed to "a signal" which subject matter is not searched or examined in Korean national applications.
Therefore, claim 18 is not searched according to Agreement between the KIPO and the IB of the WIPO in relation to the functioning of the KIPO as an International Searching Authority and International Preliminary Examining Authority under the Patent Cooperation Treaty.
2. Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.
3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2011/026380

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		US 8000166 B2	16.08.2011