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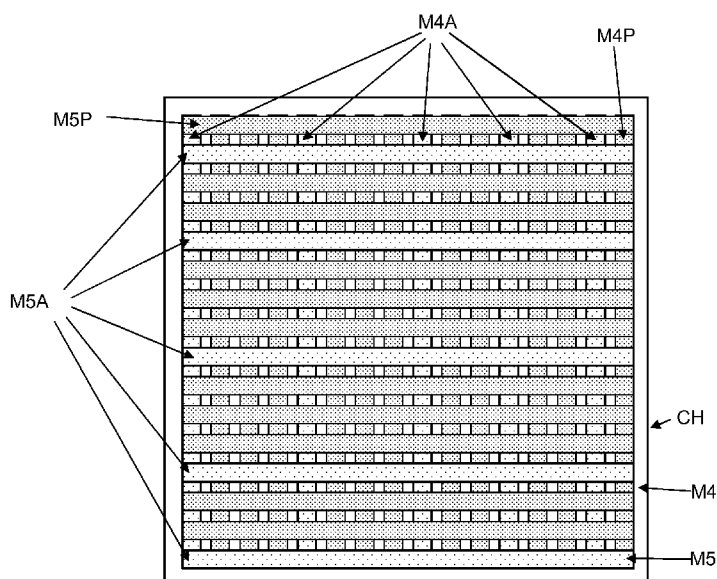


Fig. 1

- (57) Abstract: An integrated circuit chip and a method for protecting the integrated circuit chip against physical and/or electrical alterations are disclosed. The chip comprises at least one semiconductor layer including semiconductor components and conductive tracks, at least one layer formed by a first type of conductive tracks extending over all or part of a surface of the chip and at least one second type of conductive track connected to at least one detection circuit configured to detect an alteration of the at least one second type of conductive track. The chip is characterized in that the at least one first type of conductive track is mixed within the at least one second type of conductive track, the material and the layout of at least one second type of conductive track being indiscernible, by an observation device, from the material and the layout of the at least one first type of conductive track.

INTEGRATED CIRCUIT CHIP PROTECTION AGAINST PHYSICAL AND/OR ELECTRICAL ALTERATIONS

Field of the invention

The present invention relates to semiconductor integrated circuit chips as used for smartcards or security modules or systems on chip. In particular, an integrated circuit chip protected against physical and/or electrical alterations and a method to protect any chip are disclosed.

Technical background

Integrated circuit chips are often subjected to physical attacks, such as live hardware analysis, aimed at gaining knowledge of the internal functioning of the chip and consequently influencing the operation of the chip. During such an attack, the plastic housing protecting the chip against mechanical damage may be opened on its top face to reveal a passivation layer covering the electronic circuitry. The passivation layer may be selectively removed by etching methods using laser, or Focused Ion Beam (FIB) technology, or using chemical means to allow access to the signal lines. Live hardware analysis techniques may be performed on integrated circuit chips during their operation, whereas other techniques such as reverse engineering, which is aimed at analyzing and reconstructing the operation of the chip, usually result in the destruction of the chip.

An analysis of the integrated circuit chip is usually undesirable. Live hardware analysis should be prevented, if possible, particularly in the case of secure circuits such as a microprocessor on a smart card including an electronic wallet function or the like. In practice, various methods already exist to render such an analysis more difficult. In general, an integrated circuit chip is formed by a plurality of stacked layers of semiconductor components and tracks. Each layer may include metallic planes or a plurality of tracks mainly for powering, which may also act as a physical shield. The top surface of the chip is in general covered by a passivation layer used for redundant power distribution and/or for providing physical shielding. An attacker may create openings in one or more of these layers for injecting faults in the circuits or capturing signals for analysis.

Physical attacks of all or parts of the chip may be prevented by so-called passive shields, such as metallic planes or tracks connected to a circuit configured to perform analogue integrity measurements in order to detect cuts, short circuits or capacitive load variations for example. The passive shield may be defeated by deviating tracks
5 in an outside circuit or because of ineffective preset tolerance thresholds in the case of capacitive loads measurements.

Therefore, an active shield may be preferred. It may consist of a plurality of tracks arranged on the top of the chip in which random bit sequences are injected and checked for conformity from one end of a track to another. This active shield may be
10 defeated by methods using a Focused Ion Beam (FIB) apparatus if the functions of the tracks are known and if their geometrical arrangement may be modified without altering the signals carried by the concerned tracks.

Document US2008/313746A1 discloses a protection circuit for integrity monitoring of an electronic device. The protection circuit includes: a first grid check line interleaved
15 between a first set of conductor lines, each distributing a first potential reference to the electronic device, a second grid check line interleaved between a second set of conductor lines, each distributing a second potential reference to the electronic device, and a grid check circuit coupled to the first and second grid check lines. The first and second grid check lines are configured to provide first and second voltage
20 references, respectively, to the grid check circuit for monitoring the integrity of the electronic device. According to an exemplary embodiment, the top two layers of metal of an integrated circuit are utilized. Most high performance sub-micron processes utilize 7-8 layers of metal and the top two layers are typically used for power distribution, clock distribution and assembly. A grid check line that runs
25 parallel in each layer to the power grid is mixed within the top two layers of metal. The grid check lines are configured to be stimulated and sensed by grid check circuits located at various places around the die, preferably shielded by overlaying metal layers. The grid check circuits are configured to both stimulate the grid check lines as well as sense them. This allows the grid to be verified from multiple locations
30 around the die with an active send/receive capability.

Summary of the invention

According to one embodiment, a chip according to claim 1 is provided as well as a method according to claim 9 for protecting a chip against alterations such as physical and/or electrical alterations.

- 5 The chip comprises at least one semiconductor layer including semiconductor components and conductive tracks. The chip further comprises at least one layer formed by a first type of conductive tracks extending over all or part of a surface of the chip and at least one second type of conductive track associated with at least one detection circuit configured to detect an alteration of the at least one second type
- 10 of conductive track. The at least one first type of conductive track and the at least one second type of conductive track being made of a material including metal or alloy presenting a high electrical conductivity may be arranged according to a predefined layout on the at least one layer. The at least one first type of conductive track is mixed within the at least one second type of conductive track, the material
- 15 and the layout of at least one second type of conductive track being indiscernible, by an observation device, from the material and the layout of the at least one first type of conductive track.

The observation device may include an electronic microscope configured to visually observe material and layout of tracks, or any other analyzer capable of determining

20 nature, structure, and/or composition of material, arrangement or pattern formed by tracks on the chip.

The method for protecting a chip against alterations comprises forming at least one second type of conductive track in a predefined material and arranging the at least one second type of conductive track according to a predefined layout, mixing the at

25 least one second type of conductive track within the first type of conductive tracks, connecting the at least one second type of conductive track to at least one detection circuit configured to detect an alteration of the at least one second type of conductive track. The material and the layout of the at least one second type of conductive track are selected to be indiscernible from the material and the layout of the at least one

30 first type of conductive track by the observation device.

In a preferred embodiment, the at least one second type of conductive track is arranged to be mixed among first type of conductive tracks covering the top layer of the integrated circuit chip. This first type of conductive tracks forms a passive shield, also called passive shielding layer, playing a role of shielding the chip against external electromagnetic perturbations as well as electromagnetic radiation produced by the chip activity. In addition to the shielding effect, the passive shield, comprising a plurality of conductive tracks, may have a function of distributing power or ground to different parts of the integrated circuit chip. The first type of conductive tracks of the passive shield may be placed in a grid configuration, which is usually referred as “power grid”.

The chip of the invention comprises at least one second type of conductive track mixed within the first type of conductive tracks forming the power grid.

Thanks to a material similar to the material of the tracks of the power grid and a layout similar to the layout of the tracks of the power grid, the second type of conductive track cannot be distinguished by visual observation from the first type of conductive tracks forming the power grid.

In general, the chip comprises more than one conductive track of the second type, which may additionally form an active shield combined with the tracks of the power grid.

Regarding the material, the term “indiscernible” means at least indistinguishable from a visual point of view, i.e. an observation made through an optical or electronic microscope does not allow seeing any difference between the material of the first and second type of conductive tracks. According to one embodiment, the material used for manufacturing the conductive tracks of the first type corresponds or is identical to the material used for manufacturing the conductive tracks of the second type.

Regarding the layout, the term “indiscernible” means a layout of the second type of conductive tracks comparable to the layout of the first type of conductive tracks, i.e. an observation made through an optical or electronic microscope does not allow distinguishing first and second type of conductive tracks by their layout or pattern formed by the tracks. In other words, the layout of the second type of conductive

tracks may be an imitation of the layout of the first type of conductive tracks. The pattern formed by the second type of tracks may be a reproduction of the pattern formed by the first type of tracks even the second and first type of tracks are linked to different components or other tracks inside the chip.

- 5 A layout is to be understood as a geometrical substantially planar arrangement of the tracks, having given dimensions, on an internal or top layer of the chip. For example, the tracks having a predetermined width may be arranged to form continuous strait or curved lines or segmented lines formed by a combination of strait and/or curved line portions.
- 10 The tracks of the second type forming the active shield are associated with a detection circuit configured to enable countermeasures in case of physical and/or electrical alteration such as cutting one or more tracks forming the active shield. The active shield tracks may carry variable electrical signals while the passive shield tracks may be at a constant potential such as for example $V_{dd} = 5$ Volt power supply
- 15 or ground $V_{ss} = 0$ Volt in CMOS technology.

According to an embodiment of the invention, the active shield tracks may be at a constant positive or negative potential and carry superimposed variable signals as well.

Brief description of the drawings

- 20 The present invention will be better understood thanks to the detailed description, which follows, and the accompanying drawings, which are given as non-limiting examples of embodiments of the invention, namely:

Figure 1 showing a top view of two superimposed layers of conductive tracks completely covering the top surface of a chip, each layer comprising tracks of an active shield mixed within tracks of a power grid.

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Figure 2 showing a sectional view of an integrated circuit chip provided with the protection according to the invention.

Detailed description of the invention

In security critical integrated circuit chips, some security countermeasures are implemented to provide safety of the critical information against reverse engineering techniques or physical and/or electrical alterations including analysis of the circuit hardware during operating. Some of these alterations aimed at obtaining the information in an unauthorized way are known as live physical attacks since they require physical access to the inner layers of the integrated circuit chip. These attack techniques include probing the critical information by making connections to the conductive tracks of the integrated circuit chip, faulting the integrated circuit chip by forcing electrical signals from these outside connections and changing the connections of the internal conductive tracks permanently by using Focused Ion Beam (FIB) or by using Fault attacks such as laser attacks.

According to an exemplary configuration, a shield comprising a plurality of metal tracks may cover the whole surface of the integrated circuit chip by forming a top metal layer. All or part of these metal tracks may be supplied with a predefined or random analog or digital test signal produced by at least one transmitter of at least one detection circuit and observed with at least one associated receiver located at certain points of the integrated circuit. The receiver is also supplied internally with a reference test signal similar to the test signal on the metal tracks. The receiver verifies the integrity of the top layer metal tracks by comparing the test signal with the reference test signal and enables countermeasures if a result of the comparison shows a difference between the reference test signal and the test signal produced by the transmitter.

Since any physical and/or electrical attack will disturb the integrity of these metal tracks by making them open or short circuit, the receiver does not receive the correct test signal pattern from the tracks, thus detects the physical and/or electrical attack.

A shield rendered active by supplying a test signal used to detect any physical and/or electrical attack is still vulnerable to physical modification. Since the top layer metal tracks of the active shield have fixed interconnections, it is possible to make shortcut connections between the tracks and remove the parts covering the whole integrated

circuit chip or a part of it, to perform the actual attack without being detected by the detection circuits associated to the active shield tracks.

To overcome this problem, an efficient and low cost solution consists in fact of a so-called obfuscation of the active shield tracks among passive shield tracks of a power grid for example. In this way, active shield tracks cannot be differentiated from passive shield tracks, in particular when both kinds of tracks are arranged according to a similar layout forming a given pattern or are arranged according to at least similar enough layouts to be indistinguishable from each other.

The active shield tracks, i.e. the second type of conductive tracks may be made of a material identical to the material of the passive shield tracks, i.e. the first type of conductive tracks. For example, both types of tracks may be made of material such as for example, gold, silver, copper, aluminum, or any other metal or alloy presenting a high electrical conductivity. The material of the active shield tracks is thus visually undistinguishable or indiscernible, by an observation device, from the material of the passive shield tracks.

According to an embodiment, the first type and the second type of tracks may look the same but they each may be composed by different alloys of gold, silver, copper, aluminum, etc. in condition to be visually indistinguishable from each other.

The protection circuit disclosed by document US2008/313746A1 does not include the feature regarding material and layout resemblance of grid check lines, (active shield tracks) and unchecked power grid lines (passive shield tracks). In this case, if the checked and unchecked lines (the active and passive shield tracks) can be differentiated, it may possible to make shortcut connections between the checked lines for performing a physical attack without being detected by the detection circuits associated to the checked lines.

The power grid represented schematically by figure 1 may cover the entire top surface of the chip that is substantially planar, or according to an embodiment, the power grid may extend only on one or more selected zones thereof where an enhanced protection is required for security purposes. The conductive tracks, i.e. metal tracks, forming the power grid may be arranged in any way on the top surface

depending on the structure and contacts arrangements of the semiconductor components integrated in the chip.

The power grid of figure 1 is made up of a layer M4 including a row of parallel tracks distributed on the entire top surface of the chip CH. The row comprises standard
5 power grid tracks M4P and active shield tracks M4A that are mixed within the power grid tracks. Furthermore, the power grid may be completed by an additional layer M5 including a row of parallel tracks where each track is perpendicular to the tracks of the lower layer M4 to form a grid having a given track density. As in the lower layer M4, the row comprises standard power grid tracks M5P and active shield tracks
10 M5A.

The active shield tracks M4A, M5A, which are independent from the power grid tracks M4P, M5P are connected to one or more detection circuits configured to monitor physical integrity of these tracks. For example, each active shield track or groups of them may be monitored by a specific detection circuit or all active shield
15 tracks may be monitored by a same detection circuit.

The power grids placed at different levels power the chip in a redundant way so that when one or more tracks are cut, the chip remains powered. The detection circuits, connected only to the active shield tracks, may measure variations of electrical signals, potential or current as well as cuts of these active shield tracks occurring at
20 physical and/or electrical attacks on the chip and may enable countermeasures such as resetting or disabling all or part of the chip's functionalities.

The grid arrangement of the tracks shows advantageous since the probability to cut an active shield track increases with the density of the grid, i.e. with the number of tracks per millimeter in each direction and the number of active shield tracks
25 arranged within the passive shield tracks.

According to a preferred embodiment, the active shield tracks are supplied with a similar potential, i.e. a substantially equal potential as the one of the power grid tracks in order to improve obfuscation in relation to the power grid tracks.

Electrical measurements by probing or imaging by using tools such as Scanning
30 Electron Microscopy to observe voltage contrast or FIB Focused Ion Beam, will thus

give a similar result than same measurements on the power grid tracks. In these conditions, an attacker may not recognize an active shield track from conventional power grid tracks so that bypassing the layers M4, M5 becomes very difficult without being detected.

- 5 For example, in a configuration represented by the sectional view of figure 2, the chip comprises a substrate S supporting semiconductor components CP, a surface including contacts CT covered by a stack of 5 successive layers M1, M2, M3, M4, M5 each separated by an insulating layer made up for example of silicon oxide, nitride or carbide.
- 10 Each layer M1, M2, M3, M4 M5 includes conductive tracks T extending on all or part of the chip surface. The conductive tracks T thus distributed in one or more layers M1, M2, M3, M4, M5, may further be connected each other and/or to the contacts CT of the components or circuits such as detection circuits arranged at the bottom of the stack by traversing the layers thanks to vias V.
- 15 Each layer M1, M2, M3, M4, M5 may comprise conductive tracks T supplied by a different potential or signal or, in certain cases, a same potential or signal may be applied to tracks of two or more layers depending of the integrated circuit chip configuration.

Some tracks T comprised in these layers M1, M2, M3, M4, M5 may constitute an active shield monitored by one or more detection circuits preferably integrated in the chip CH near other circuits. The active shield thus protects all or only the critical parts of the chip as well as the detection circuit themselves thereby preventing any direct tampering by disabling these detection circuits.

If detection circuits could be neutralized by an attacker, the active shield may be cut or removed without enabling the countermeasures foreseen in case of physical alteration thereof. To solve this problem, the chip comprises a set of detection circuits comprising fake and real detection circuits. The additional fake circuits or cells have an identical or almost identical layout to the real detection circuits, which may also be positioned at different places on the chip in order to obfuscate localization of the real detection circuits. Preferably, the fake detection circuits may be arranged according to a layout indiscernible, by an observation device, from the

layout of the real detection circuit. The fake detection circuits may be an imitation of the real detection circuits.

The active shield tracks and their associated detection circuits may be implemented in a chip in an efficient way at reduced cost during manufacturing of the chip because it uses existing metallic layers also used as shields and/or power grids. The active shield tracks do not only have to be inserted in the top layer, but may also be inserted in the different intermediate semiconductor layers of the chip.

CLAIMS

1. A chip comprising at least one semiconductor layer including semiconductor components and conductive tracks, said chip comprising at least one layer formed by a first type of conductive tracks extending over all or part of a surface of the chip and at least one second type of conductive track associated with at least one detection circuit configured to detect an alteration of the at least one second type of conductive track, the at least one first type of conductive track and the at least one second type of conductive track being made of a material including metal or alloy presenting a high electrical conductivity are arranged according to a predefined layout on the at least one layer, the chip is characterized in that the at least one first type of conductive track is mixed within the at least one second type of conductive track, the material and the layout of at least one second type of conductive track being indiscernible, by an observation device, from the material and the layout of the at least one first type of conductive track.
2. The chip according to claim 1, characterized in that the at least one second type of conductive track is made of a material identical to the material of the first type of conductive tracks.
3. The chip according to claim 1 or 2, characterized in that the at least one detection circuit is configured to enable countermeasures at detection of an alteration comprising physical or electrical alteration of the at least one second type of conductive track, the countermeasures comprising resetting or disabling all or part of functionalities of the chip.
4. The chip according to anyone of claim 1 to 3, characterized in that the at least one second type of conductive track is mixed within the first type of conductive tracks forming a substantially planar power grid covering a top surface of the chip, each first type of conductive track being supplied by a predetermined potential.
5. The chip according to claim 3, characterized in that the at least one second type of conductive track is supplied with a potential substantially equal to the potential of the first type of conductive tracks.

6. The chip according to claim 4 or 5, characterized in that the at least one second type of conductive track is mixed within the first type of conductive tracks additionally forming a shield against external electromagnetic perturbations or electromagnetic radiation produced by the chip activity.

7. The chip according to anyone of claim 1 to 6, characterized in that the at least one detection circuit comprises at least one transmitter configured to produce a test signal in the at least one second type of conductive track and at least one receiver associated to the transmitter configured to verify integrity of the second type of conductive track by comparing the test signal with a reference test signal and to enable the countermeasures if a result of the comparison shows a difference between the reference test signal and the test signal produced by the transmitter.

8. The chip according to anyone of claim 1 to 7 further comprising a set of detection circuits comprising fake and real detection circuits positioned at different places on the chip, the fake detection circuits being arranged according to a layout indiscernible, by an observation device, from the layout of the real detection circuit.

9. A method for protecting a chip against alterations, the chip comprising at least one semiconductor layer including semiconductor components and conductive tracks, said chip comprising at least one layer formed by a first type of conductive tracks extending over all or part of a surface of the chip, comprising:

- forming at least one second type of conductive track in a predefined material and arranging the at least one second type of conductive track according to a predefined layout,
- mixing the at least one second type of conductive track within the first type of conductive tracks,
- connecting the at least one second type of conductive track to at least one detection circuit configured to detect an alteration of the at least one second type of conductive track.

the method is characterized in that the material and the layout of the at least one second type of conductive track are selected to be indiscernible, by an observation device, from the material and the layout of the at least one first type of conductive track.

10. The method according to claim 9, characterized in that the at least one detection circuit enables countermeasures at detection of an alteration comprising physical or electrical alteration of the at least one second type of conductive track, the countermeasures comprising reset or disabling all or part of functionalities of the chip.

11. The method according to claim 9 or 10, characterized in that the at least one second type of conductive track is mixed within the first type of conductive tracks forming a substantially planar power grid covering a top surface of the chip, each first type of conductive track being supplied by a potential which is substantially equal to a predetermined potential.

12. The method according to claim 11, characterized in that the at least one second type of conductive track is supplied with a potential substantially equivalent to the potential of the first type of conductive tracks.

13. The method according to claim 11 or 12, characterized in that the at least one second type of conductive track is placed in a way to be mixed within the first type of conductive tracks additionally forming a shield against external electromagnetic perturbations or electromagnetic radiation produced by the integrated circuit chip activity.

14. The method according to anyone of claim 9 to 13, characterized in that the at least one detection circuit comprises at least one transmitter producing a test signal in the at least one second type of conductive track and at least one receiver associated to the transmitter verifying integrity of the second type of conductive track by comparing the test signal with a reference test signal and enabling the countermeasures if a result of the comparison shows a difference between the reference test signal and the test signal produced by the transmitter.

15. The method according to anyone of claim 9 to 14 characterized in that the chip comprises a set of detection circuits including fake and real detection circuits positioned at different places on the chip, the fake detection circuits being arranged according to a layout indiscernible, by an observation device, from the layout of the real detection circuit.

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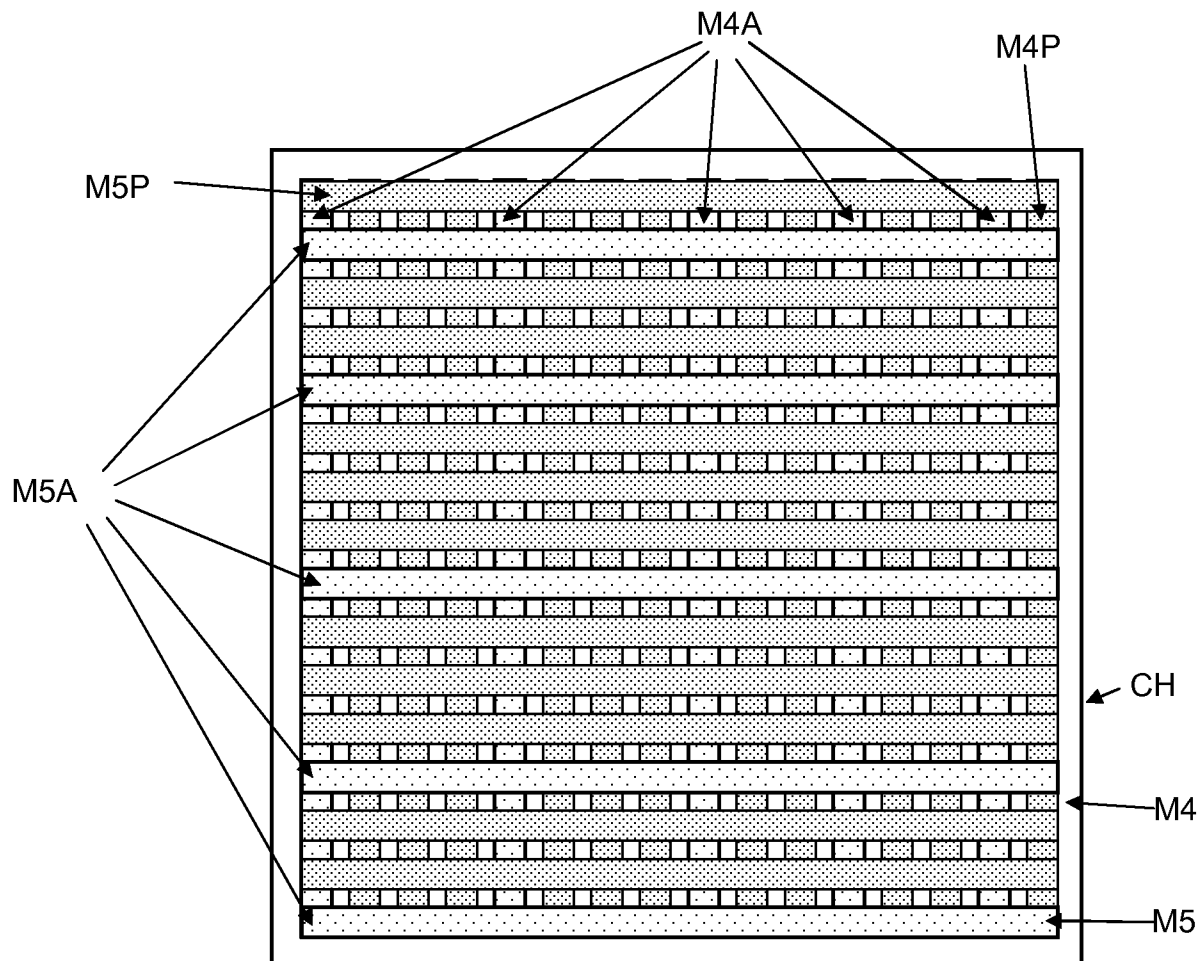


Fig. 1

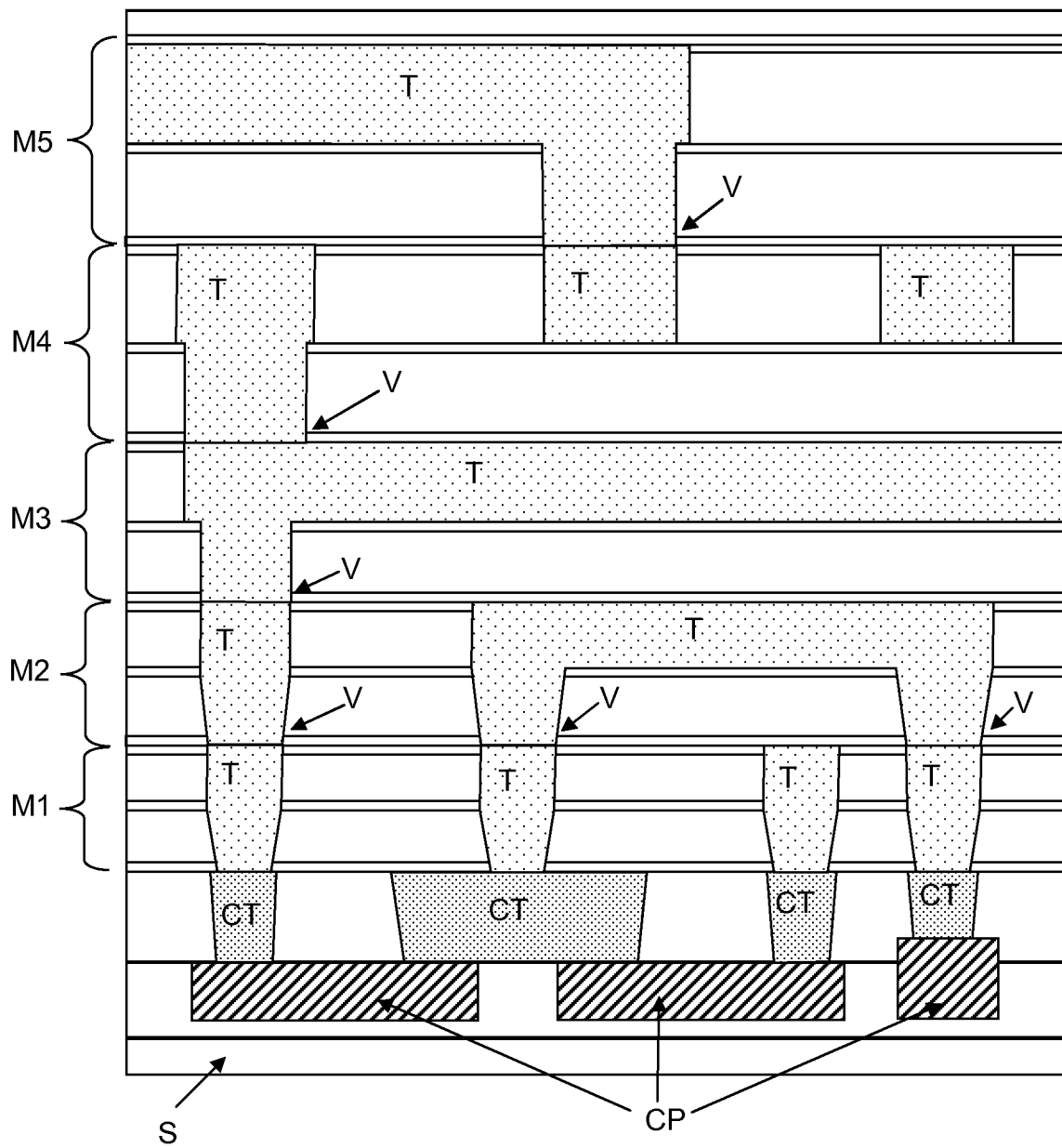


Fig. 2

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2016/060910

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06K19/073
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2008/313746 A1 (DOI BRYAN CARY [US]) 18 December 2008 (2008-12-18) paragraph [0029] - paragraph [0036]; claims 1-20; figures 1-2 -----	1-15



Further documents are listed in the continuation of Box C.



See patent family annex.

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A1-Hazam, Lorens

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2016/060910

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008313746 A1	18-12-2008	EP 2158606 A1	03-03-2010
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