Abstract: A method of manufacture and device for a dual-gate CMOS structure. The structure includes a first plate (106a-d) in an insulating layer (100) and a second plate (110a-d) above the insulating layer electrically corresponding to the first plate. An isolation structure (108a-d) is between the first plate and the second plate.
INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC: HOI/21/84(2006.01),27/108(2006.01)

USPC: 438/155.210;257/300
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S.: 438/155, 210, 241; 257/296, 300

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
</table>

D. Further documents are listed in the continuation of Box C. See patent family annex.

Date of the actual completion of the international search
30 January 2007 (30.01.2007)

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Form PCT/ISA/210 (second sheet) (April 2005)