



(51) International Patent Classification:

H01L 21/60 (2006.01) H01L 21/50 (2006.01)

(21) International Application Number:

PCT/CN2019/070143

(22) International Filing Date:

02 January 2019 (02.01.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicant: **YANGTZE MEMORY TECHNOLOGIES CO., LTD.** [CN/CN]; Room 7018, No. 18, Huaguang Road, Guandong Science and Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN).

(72) Inventors: **LIU, Mengyong**; Room 7018, No. 18, Huaguang Road, Guandong Science and Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **DING, Tao Tao**; Room 7018, No. 18, Huaguang Road, Guandong Science and Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **LIU, Wu**; Room 7018, No. 18, Huaguang Road, Guandong Science and Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN). **XING, Rui Yuan**; Room 7018, No. 18, Huaguang Road, Guandong Science and Technology Industrial Park, East

Lake Development Zone, Wuhan, Hubei 430074 (CN). **CHEN, Guoliang**; Room 7018, No. 18, Huaguang Road, Guandong Science and Technology Industrial Park, East Lake Development Zone, Wuhan, Hubei 430074 (CN).

(74) Agent: **NTD UNIVATION INTELLECTUAL PROPERTY AGENCY LTD.**; 10th Floor, Tower C, Beijing Global Trade Center, 36 North Third Ring Road East, Dongcheng District, Beijing 100013 (CN).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,

(54) Title: PLASMA ACTIVATION TREATMENT FOR WAFER BONDING

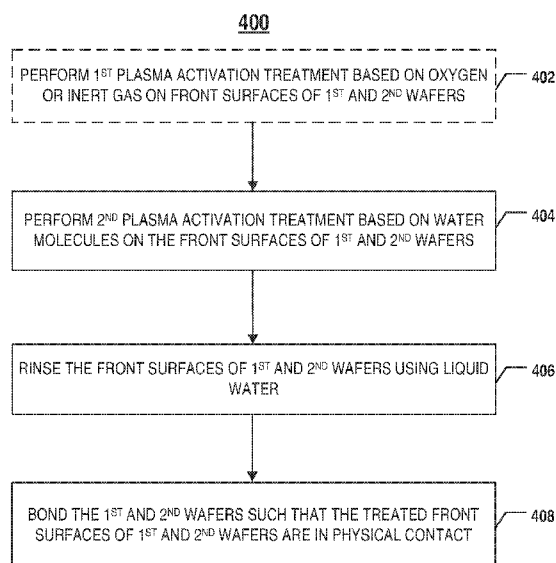


FIG. 4

(57) Abstract: Wafer bonding methods (400) comprise: a first plasma activation treatment based on oxygen or an inert gas is performed on a front surface of a first wafer (202) and a front surface of a second wafer (204) (402). After the first plasma activation treatment, a second plasma activation treatment based on water molecules is performed on the front surface of the first wafer (202) and the front surface of the second wafer (204) (404). After the second plasma activation treatment, the first wafer (202) and the second wafer (204) are bonded such that the treated front surface of the first wafer (202) is in physical contact with the treated front surface of the second wafer (204) (408).

EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

PLASMA ACTIVATION TREATMENT FOR WAFER BONDING

BACKGROUND

- [0001] Embodiments of the present disclosure relate to wafer bonding methods.
- [0002] Planar semiconductor devices, such as memory cells, are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the semiconductor devices approach a lower limit, planar process and fabrication techniques become challenging and costly. A three-dimensional (3D) device architecture can address the density limitation in some planar semiconductor devices, for example, Flash memory devices.
- [0003] A 3D semiconductor device can be formed by stacking semiconductor wafers or dies and interconnecting them vertically using, for instance, through-silicon vias (TSVs) or copper-to-copper (Cu-Cu) connections, so that the resulting structure acts as a single device to achieve performance improvements at reduced power and smaller footprint than conventional planar processes. Among the various techniques for stacking semiconductor wafers, direct bonding, a process where two separate wafer surfaces are brought into physical contact and are bonded without any intermediate adhesives or external forces, is recognized as one of the promising techniques.

SUMMARY

- [0004] Embodiments of wafer bonding methods are disclosed herein.
- [0005] In one example, a method for wafer bonding is disclosed. A first plasma activation treatment based on oxygen or an inert gas is performed on a front surface of a first wafer and a front surface of a second wafer. After the first plasma activation treatment, a second plasma activation treatment based on water molecules is performed on the front surface of the first wafer and the front surface of the second wafer. After the second plasma activation treatment, the first wafer and the second wafer are bonded such that the treated front surface of the first wafer is in physical contact with the treated front surface of the second wafer.
- [0006] In another example, a method for wafer bonding is disclosed. A plasma activation treatment based on water molecules is performed on a front surface of a first wafer and a front surface of a second wafer. The front surface of the first wafer and the front surface

of the second wafer are free from another plasma activation treatment based on oxygen or an inert gas. After the plasma activation treatment, the first wafer and the second wafer are bonded such that the treated front surface of the first wafer is in physical contact with the treated front surface of the second wafer.

[0007] In still another example, a method for wafer bonding is disclosed. A plasma activation treatment is performed on a front surface of a first silicon wafer and a front surface of a second silicon wafer to form hydroxyl groups on the front surface of the first silicon wafer and the front surface of the second silicon wafer. After the plasma activation treatment, the first silicon wafer and the second silicon wafer are bonded such that the treated front surface of the first silicon wafer is in physical contact with the treated front surface of the second silicon wafer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0009] FIG. 1A illustrates a cross-section of an exemplary bonded semiconductor device, according to some embodiments of the present disclosure.

[0010] FIG. 1B illustrates a cross-section of another exemplary bonded semiconductor device, according to some embodiments of the present disclosure.

[0011] FIGs. 2A–2D illustrate an exemplary fabrication process for wafer bonding, according to some embodiments of the present disclosure.

[0012] FIG. 3 illustrates an exemplary surface modification for wafer bonding, according to some embodiments of the present disclosure.

[0013] FIG. 4 is a flowchart of an exemplary method for wafer bonding, according to some embodiments of the present disclosure.

[0014] FIG. 5 is a flowchart of an exemplary method for a plasma activation treatment based on water molecules, according to some embodiments of the present disclosure.

[0015] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0016] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0017] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0018] In general, terminology may be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term “based on” may be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0019] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

[0020] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0021] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0022] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which interconnect lines and/or via contacts are formed) and one or more dielectric layers.

[0023] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term

“about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0024] As used herein, the term “3D memory device” refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND memory strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0025] As used herein, the term “front surface” of a structure refers to the surface of the structure at which a device is formed or will be subsequently formed.

[0026] Plasma activation bonding is a direct wafer bonding method. Plasma activation bonding method includes surface activation using oxygen or inert gas plasma, surface cleaning using deionized water, followed by preliminary bonding, and finally a heat treatment to bond the two wafers. Plasma activation bonding relies on van der Waals forces and hydrogen bonding in the hydroxyl groups to achieve preliminary bonding prior to the heat treatment. During the heat treatment, water molecules are removed in condensation reactions to form covalent bonds between front surfaces of the first and second wafers to achieve a stabilized bonding. However, low hydroxyl content in deionized water used in the surface cleaning process may not be sufficient to achieve stable covalent bonding, causing wafer debonding in some cases.

[0027] Various embodiments in accordance with the present disclosure provide improved plasma activation bonding methods that can achieve stable and strong covalent bonding by increasing the amount of hydroxyl groups on the bonding surfaces of the wafers prior to the bonding. Water molecules can be ionized to form hydroxyl groups and bombarded onto the wafer bonding surface by a plasma activation process. As a result, wafer bonding methods disclosed herein can provide, among other things, benefits of (i) sufficient hydroxyl groups on bonding surfaces during the bonding process to improve wafer bonding strength; (ii) providing a larger process window for subsequent processes; (iii) improving device structure stability and reliability to streamline fabrication process; and (iv) reducing production cost and improving device quality.

[0028] FIG. 1A illustrates a cross-section of an exemplary bonded semiconductor device 100, according to some embodiments of the present disclosure. Bonded semiconductor

device 100 represents an example of a non-monolithic 3D memory device. The term “non-monolithic” means that the components of bonded semiconductor device 100 (e.g., peripheral devices and memory array devices) can be formed separately on different substrates and then bonded to form a bonded semiconductor device. Bonded semiconductor device 100 can include a substrate 108, which can include silicon (e.g., single crystalline silicon), silicon germanium (SiGe), gallium arsenide (GaAs), germanium (Ge), silicon on insulator (SOI), or any other suitable materials. For ease of description, bonded semiconductor device 100 will be described as a non-monolithic 3D memory device. However, it is understood that bonded semiconductor device 100 is not limited to a 3D memory device and can include any suitable semiconductor devices that have stable and strong covalent bonds at its bonding interface using the plasma activation bonding methods described below in detail. It is understood that bonded semiconductor devices formed using the plasma activation bonding methods disclosed herein are not limited to the examples shown in FIGs. 1A–1B and can include any other suitable semiconductor devices, such as logic devices (e.g., central processing unit (CPU) and graphical processing unit (GPU)), volatile memory devices (e.g., dynamic random-access memory (DRAM) and static random-access memory (SRAM)), and non-volatile memory devices (e.g., Flash memory), in a 2D, 2.5D, or 3D architecture.

[0029] Bonded semiconductor device 100 can include two semiconductor structures (referred to herein as “wafers” as well), i.e., a memory array device chip 102 (a first wafer) and a peripheral device chip 104 (a second wafer) bonded on top of memory array device chip 102 in a face-to-face manner at a bonding interface 106. In some embodiments, bonding interface 106 is disposed between memory array device chip 102 and peripheral device chip 104 as a result of hybrid bonding (also known as “metal/dielectric hybrid bonding”), which is a direct bonding technology (e.g., forming bonding between surfaces without using intermediate layers, such as solder or adhesives) and can obtain metal-metal bonding and dielectric-dielectric bonding simultaneously. In some embodiments, bonding interface 106 is the place at which memory array device chip 102 and peripheral device chip 104 meet and are bonded. In practice, bonding interface 106 can be a layer with a certain thickness that includes the top surface of memory array device chip 102 and the bottom surface of peripheral device chip 104.

[0030] It is noted that x and y axes are included in FIG. 1A to further illustrate the spatial relationship of the components in bonded semiconductor device 100 having substrate 108. Substrate 108 includes two lateral surfaces (e.g., a top surface and a bottom surface) extending laterally in the x -direction (i.e., the lateral direction). As used herein, whether one component (e.g., a layer or a device) is “on,” “above,” or “below” another component (e.g., a layer or a device) of a semiconductor device (e.g., bonded semiconductor device 100) is determined relative to the substrate of the semiconductor device (e.g., substrate 108) in the y -direction (i.e., the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the y -direction. The same notion for describing spatial relationship is applied throughout the present disclosure.

[0031] In some embodiments, memory array device chip 102 is a NAND Flash memory device in which memory cells are provided in the form of an array of NAND memory strings 110 in a memory array device layer 134. Memory array device layer 134 can be disposed on substrate 108. In some embodiments, each NAND memory string 110 extends vertically through a plurality of pairs each including a conductor layer and a dielectric layer (referred to herein as “conductor/dielectric layer pairs”). The stacked conductor/dielectric layer pairs are collectively referred to herein as a “memory stack” 112 in memory array device layer 134. The conductor layers and dielectric layers in memory stack 112 can stack alternately in the vertical direction. Each NAND memory string 110 can include a semiconductor channel and a composite dielectric layer (also known as a “memory film”) including a tunneling layer, a storage layer (also known as a “charge trap/storage layer”), and a blocking layer (not shown). In some embodiments, memory array device layer 134 further includes a gate line slit (“GLS”) 114 that extends vertically through memory stack 112. GLS 114 can be used to form the conductor/dielectric layer pairs in memory stack 112 by a gate replacement process and can be filled with conductive materials for electrically connecting an array common source (ACS).

[0032] In some embodiments, memory array device chip 102 also includes an array interconnect layer 136 above memory array device layer 134 for transferring electrical signals to and from NAND memory strings 110. As shown in FIG. 1A, array interconnect layer 136 can include a plurality of interconnects (also referred to herein as “contacts”), including vertical interconnect access (via) contacts 116 and lateral

interconnect lines 118. As used herein, the term “interconnects” can broadly include any suitable types of interconnects, such as middle-end-of-line (MEOL) interconnects and back-end-of-line (BEOL) interconnects. Array interconnect layer 136 can further include one or more interlayer dielectric (ILD) layers (also known as “intermetal dielectric (IMD) layers”) in which interconnect lines 118 and via contacts 116 can form.

[0033] As shown in FIG. 1A, memory array device chip 102 can further include a bonding layer 138 at bonding interface 106 and above array interconnect layer 136 and memory array device layer 134. Bonding layer 138 can include a plurality of bonding contacts 130 and dielectrics electrically isolating bonding contacts 130. Bonding contacts 130 can include conductive materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), silicides, or any combination thereof. The remaining area of bonding layer 138 can be formed with dielectrics including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, low-k dielectrics, or any combination thereof. Bonding contacts 130 and surrounding dielectrics in bonding layer 138 can be used for hybrid bonding.

[0034] Peripheral device chip 104 can include a plurality of transistors 122 in a peripheral device layer 140 disposed below a semiconductor layer 120, such as a thinned substrate. In some embodiments, peripheral device layer 140 can include any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of bonded semiconductor device 100. For example, peripheral device layer 140 can include one or more of a page buffer, a decoder (e.g., a row decoder and a column decoder), a sense amplifier, a driver, a charge pump, a current or voltage reference, or any active or passive components of the circuits (e.g., transistors, diodes, resistors, or capacitors).

[0035] Similar to memory array device chip 102, peripheral device chip 104 can also include a peripheral interconnect layer 142 disposed below peripheral device layer 140 for transferring electrical signals to and from transistors 122. Peripheral interconnect layer 142 can include a plurality of interconnects, including interconnect lines 126 and via contacts 124 in one or more ILD layers. In some embodiments, peripheral device chip 104 also includes via contacts 128 (e.g., through silicon vias (TSVs) if semiconductor layer 120 is a thinned silicon substrate) extending vertically through semiconductor layer 120. In some embodiments, peripheral device chip 104 further includes a BEOL interconnect layer (not shown) above transistors 122 and semiconductor layer 120. In

some embodiments, the BEOL interconnect layer includes any suitable BEOL interconnects and contact pads that can transfer electrical signals between bonded semiconductor device 100 and external circuits.

[0036] As shown in FIG. 1A, peripheral device chip 104 can further include a bonding layer 144 at bonding interface 106 and below peripheral interconnect layer 142 and peripheral device layer 140. Bonding layer 144 can include a plurality of bonding contacts 132 and dielectrics electrically isolating bonding contacts 132. Bonding contacts 132 can include conductive materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. The remaining area of bonding layer 144 can be formed with dielectrics including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, low-k dielectrics, or any combination thereof. Bonding contacts 132 and surrounding dielectrics in bonding layer 144 can be used for hybrid bonding.

[0037] FIG. 1B illustrates a cross-section of another exemplary bonded semiconductor device 101, according to some embodiments of the present disclosure. Similar to bonded semiconductor device 100 described above in FIG. 1A, bonded semiconductor device 101 represents an example of a non-monolithic 3D memory device in which two semiconductor structures, i.e., a peripheral device chip 103 (a first wafer) and a memory array device chip 105 (a second wafer) are formed separately and bonded in a face-to-face manner at a bonding interface 107. In some embodiments, bonding interface 107 is the place at which memory array device chip 105 and peripheral device chip 103 meet and are bonded. In practice, bonding interface 107 can be a layer with a certain thickness that includes the top surface of peripheral device chip 103 and the bottom surface of memory array device chip 105. Different from bonded semiconductor device 100 described above in FIG. 1A in which peripheral device chip 104 is above memory array device chip 102, bonded semiconductor device 101 in FIG. 1B includes peripheral device chip 103 disposed below memory array device chip 105. It is understood that the details of similar structures (e.g., materials, fabrication process, functions, etc.) in both bonded semiconductor devices 100 and 101 may not be repeated below.

[0038] Peripheral device chip 103 can include a plurality of transistors 111 in a peripheral device layer 135 disposed on and/or in a substrate 109. In some embodiments, peripheral device layer 135 can include any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of bonded semiconductor device 101. For

example, peripheral device layer 135 can include one or more of a page buffer, a decoder (e.g., a row decoder and a column decoder), a sense amplifier, a driver, a charge pump, a current or voltage reference, or any active or passive components of the circuits (e.g., transistors, diodes, resistors, or capacitors). Peripheral device chip 103 can also include a peripheral interconnect layer 137 above peripheral device layer 135 for transferring electrical signals to and from transistors 111. Peripheral interconnect layer 137 can include a plurality of interconnects, including interconnect lines 115 and via contacts 113 in one or more ILD layers. As shown in FIG. 1B, peripheral device chip 103 further includes a bonding layer 139 at bonding interface 107 and above peripheral interconnect layer 137 and peripheral device layer 135. Bonding layer 139 can include a plurality of bonding contacts 131 and dielectrics electrically isolating bonding contacts 131.

[0039] In some embodiments, memory array device chip 105 is a NAND Flash memory device in which memory cells are provided in the form of an array of NAND memory strings 121 in a memory array device layer 141 disposed below a semiconductor layer 119 (e.g., a thinned substrate). In some embodiments, each NAND memory string 121 extends vertically through a memory stack 117 in memory array device layer 141. Each NAND memory string 121 can include a semiconductor channel and a composite dielectric layer (also known as a “memory film”) including a tunneling layer, a storage layer (also known as a “charge trap/storage layer”), and a blocking layer (not shown). In some embodiments, memory array device chip 105 further includes a GLS 123 that extends vertically through memory stack 117. GLS 123 can be used to form the conductor/dielectric layer pairs in memory stack 117 by a gate replacement process and can be filled with conductive materials for electrically connecting an array common source ACS.

[0040] Memory array device chip 105 can also include an array interconnect layer 143 below memory array device layer 141 for transferring electrical signals to and from NAND memory strings 121. Array interconnect layer 143 can include a plurality of interconnects, including interconnect lines 129 and via contacts 127 in one or more ILD layers. Memory array device chip 105 can also include semiconductor layer 119 and a BEOL interconnect layer (not shown) above NAND memory strings 121. In some embodiments, the BEOL interconnect layer includes any suitable BEOL interconnects and contact pads that can transfer electrical signals between bonded semiconductor device

101 and external circuits. In some embodiments, memory array device chip 105 further includes one or more through array contacts (TACs) 125 that extend vertically through the entirety of memory stack 117 and at least part of semiconductor layer 119. The upper end of TAC 125 can contact an interconnect in the BEOL interconnect layer (not shown), and the lower end of TAC 125 can contact another interconnect 127 or 129 in array interconnect layer 143. TAC 125 can thus make an electrical connection between peripheral interconnect layer 137 and the BEOL interconnect layer and carry electrical signals from peripheral device chip 103 to the BEOL interconnects of bonded semiconductor device 101. As shown in FIG. 1B, memory array device chip 105 can further include a bonding layer 145 at bonding interface 107 and below array interconnect layer 143 and memory array device layer 141. Bonding layer 145 can include a plurality of bonding contacts 133 and dielectrics electrically isolating bonding contacts 133.

[0041] FIGs. 2A–2D illustrate an exemplary fabrication process for wafer bonding, according to some embodiments of the present disclosure. FIG. 4 is a flowchart of an exemplary method 400 for wafer bonding, according to some embodiments of the present disclosure. FIGs. 2A–2D and 4 will be described together. It is understood that the operations shown in method 400 are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. Further, some of the operations may be performed simultaneously, or in a different order than shown in FIG. 4.

[0042] Referring to FIG. 4, method 400 starts at operation 402, in which a first plasma activation treatment is performed based on oxygen or an inert gas on a front surface of a first wafer and a front surface of a second wafer. In some embodiments, the inert gas includes nitrogen, argon, any other suitable inert gas, or any combination thereof. Each of the first wafer and second wafer can include silicon. That is, each of the first and second wafers is a silicon wafer, according to some embodiments. The first plasma activation treatment is also known as a surface activation process that can break the bonds of silicon oxide molecules formed by native oxidation or thermal oxidation on the front surfaces of silicon wafers.

[0043] As illustrated in FIG. 2A, the first plasma activation treatment is performed on the front surfaces of a first wafer 202 and a second wafer 204. In some embodiments, at least one of first and second wafers 202 and 204 includes a device formed on the front surface,

i.e., not a bare wafer. In one example, first wafer 202 and second wafer 204 can be memory array device chip 102 and peripheral device chip 104 illustrated in FIG. 1A, respectively. In another example, first wafer 202 and second wafer 204 can be peripheral device chip 103 and memory array device chip 105 illustrated in FIG. 1B, respectively. It is understood that one or both of first and second wafers 202 and 204 can be bare wafers without any device formed thereon. In some embodiments, first wafer 202 and second wafer 204 can include silicon, germanium, an III-V semiconductor, silicon carbide, silicon on insulating substrate, or any suitable combination thereof.

[0044] In some embodiments, at least part of the front surface of first wafer 202 and at least part of the front surface of second wafer 204 include a dielectric layer of oxides, nitrides, carbides, or a combination thereof. For example, each of first and second wafers 202 and 204 can be a silicon wafer that includes silicon, and the front surfaces of first and second wafers 202 and 204 can include silicon oxide, silicon nitride, or a nitrogen-doped silicon carbide. Fabrication methods to form the dielectric layer include, but not limited to, lithography, etching, deposition, thermal oxidation, filling, polishing, or a combination thereof. In some embodiments, in preparation for wafer bonding prior to subsequent first plasma activation treatment, at least part of the front surfaces of first and second wafers 202 and 204 is formed with silicon oxide, and then planarized using, for example, a chemical-mechanical polishing (CMP) technique. In some embodiments, the first and second wafers 202 and 204 to be bonded are not limited to those with extrinsically deposited silicon oxide layers, but can also include surfaces having intrinsic silicon oxide, such as glass substrates or native oxide layers.

[0045] Plasma activation (also known as “plasma functionalization”) is a method of surface modification employing plasma processing, which can modify the chemical and/or physical properties of the surface of a wafer. In some embodiments, plasma gases used by the first plasma activation treatment include, but not limited to, oxygen (O_2), an inert gas (e.g., nitrogen (N_2) or argon (Ar_2)), or a combination thereof. In one example, the plasma gas can be oxygen. In another example, the plasma gas can be nitrogen. The plasma gas can further include other suitable gases, such as hydrogen (H_2). Concentration of plasma gases is less than about 5%, such as less than 5%, according to some embodiments. In some embodiments, the first plasma activation treatment is performed with a pressure between about 0.05 mbar and about 0.5 mbar, such as between

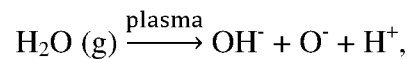
0.05 mbar and 0.5 mbar. The first plasma activation treatment can be performed with a discharge power between about 10 watts and about 100 watts, such as between 10 watts and 100 watts. In some embodiments, the first plasma activation treatment is performed with a high frequency discharge power between about 40 watts and about 100 watts, such as between 40 watts and 100 watts. In some embodiments, the first plasma activation treatment is performed with a low frequency discharge power between about 10 watts and about 40 watts, such as between 10 watts and 40 watts. In some embodiments, the first plasma activation treatment is performed for a duration between about 5 seconds and about 50 seconds, such as between 5 seconds and 50 seconds. In some embodiments, the first plasma activation treatment is performed with a flow rate between about 30 standard cubic centimeters per minute (sccm) and about 80 sccm, such as between 30 sccm and 80 sccm. In some embodiments, a chemical activation treatment is also be performed.

[0046] Method 400 proceeds to operation 404, as illustrated in FIG. 4, in which, after the first plasma activation treatment, a second plasma activation treatment based on water molecules is performed on the front surface of the first wafer and the front surface of the second wafer. Different from the first plasma activation treatment in which the plasma gas is oxygen or an inert gas, the plasma gas used by the second plasma activation includes water vapor, according to some embodiments. The water vapor can be ionized by the plasma processing to become hydroxyl groups, which can be bombarded onto the front surfaces of the first and second wafers. In some embodiments in which the first and second wafers include silicon, the hydroxyl groups are bonded on the silicon to form silanol groups on the front surfaces (i.e., bonding surfaces). The plasma processing can facilitate the formation of the silanol groups as well. As an operation dedicated for forming hydroxyl groups on the bonding surfaces, the second plasma activation treatment does not use oxygen or an inert gas as the plasma gas, according to some embodiments.

[0047] As illustrated in FIG. 2B, the second plasma activation treatment based on water molecules (H_2O) is performed on the front surface of first wafer 202 and the front surface of second wafer 204. Hydroxyl groups can be formed on the front surfaces of first and second wafers 202 and 204 by the second plasma activation treatment. For example, FIG. 5 is a flowchart of an exemplary method 500 for a plasma activation treatment based on water molecules, according to some embodiments of the present disclosure. It is understood that the operations shown in method 500 are not exhaustive and that other

operations can be performed as well before, after, or between any of the illustrated operations. Further, some of the operations may be performed simultaneously, or in a different order than shown in FIG. 5.

[0048] Starting at operation 502, liquid water is vaporized to form water vapor. Water vapor can be produced from the evaporation or boiling of liquid water. At operation 504, the water vapor is used as the plasma gas for the second plasma activation treatment. In some embodiments, water vapor is supplied to the plasma chamber and ionized in the plasma chamber under the conditions described below in detail to form hydroxyl groups (-OH). The ionization of water molecules in water vapor by plasma can be described as following:



where water molecules in the gaseous phase are ionized by plasma to become hydroxyl groups, oxygen ions, and hydrogen ions.

[0049] The second plasma activation treatment can be performed with a discharge power between about 10 watts and about 100 watts, such as between 10 watts and 100 watts (e.g., 10 watts, 20 watts, 30 watts, 40 watts, 50 watts, 60 watts, 70 watts, 80 watts, 90 watts, 100 watts, any range bounded by the lower end by any of these values, or any range defined by any two of these values). In some embodiments, the second plasma activation treatment is performed with a high frequency discharge power between about 40 watts and about 100 watts, such as between 40 watts and 100 watts (e.g., 40 watts, 45 watts, 50 watts, 55 watts, 60 watts, 65 watts, 70 watts, 75 watts, 80 watts, 85 watts, 90 watts, 95 watts, 100 watts, any range bounded by the lower end by any of these values, or any range defined by any two of these values). In some embodiments, the second plasma activation treatment is performed with a low frequency discharge power between about 10 watts and about 40 watts, such as between 10 watts and 40 watts (e.g., 10 watts, 15 watts, 20 watts, 25 watts, 30 watts, 35 watts, 40 watts, any range bounded by the lower end by any of these values, or any range defined by any two of these values).

[0050] In some embodiments, the second plasma activation treatment is performed with a pressure between about 0.05 mbar and about 0.5 mbar, such as between 0.05 mbar and 0.5 mbar (e.g., 0.05 mbar, 0.06 mbar, 0.07 mbar, 0.08 mbar, 0.09 mbar, 0.1 mbar, 0.2 mbar, 0.3 mbar, 0.4 mbar, 0.5 mbar, any range bounded by the lower end by any of these values, or any range defined by any two of these values). In some embodiments, the

second plasma activation treatment is performed for a duration between about 5 seconds and about 50 seconds, such as between 5 seconds and 50 seconds (e.g., 5 seconds, 10 seconds, 15 seconds, 20 seconds, 25 seconds, 30 seconds, 35 seconds, 40 seconds, 45 seconds, 50 seconds, any range bounded by the lower end by any of these values, or any range defined by any two of these values). In some embodiments, the second plasma activation treatment is performed with a flow rate between about 30 sccm and about 80 sccm, such as between 30 sccm and 80 sccm (e.g., 30 sccm, 40 sccm, 50 sccm, 60 sccm, 70 sccm, 80 sccm, any range bounded by the lower end by any of these values, or any range defined by any two of these values).

[0051] In some embodiments, the processing conditions of the first and second plasma activation treatments are nominally the same except for the different plasma gases. For example, at least one of a pressure, a discharge power, or a duration of the first plasma activation treatment is the same as a respective one of a pressure, a discharge power, or a duration of the second plasma activation treatment.

[0052] At operation 506, the hydroxyl groups ionized from the water vapor are formed on the front surfaces of first and second wafers 202 and 204 (e.g., silicon wafers) by the second plasma activation treatment. The hydroxyl groups are bombarded onto the front surfaces of first and second wafers 202 and 204 by the plasma processing, according to some embodiments. For example, as illustrated in FIG. 3, layers of hydroxyl groups 302 ionized from the water vapor are formed on the front surface of first silicon wafer 202 and the front surface of second silicon wafer 204. Referring back to FIG. 5, at operation 508, bonding of hydroxyl groups and silicon is facilitated by the second plasma activation treatment to form silanol groups (Si-OH). For example, as illustrated in FIG. 3, hydroxyl groups 302 on the front surfaces of first and second silicon wafers 202 and 204 can bond on silicon atoms by ionic bonds to form silanol groups. The plasma processing also facilitates the formation of silanol groups, for example, by increasing the amount of hydroxyl groups 302 bonded on silicon atoms, according to some embodiments.

[0053] Referring back to FIG. 4, in some embodiments, operation 402 is optional and can be skipped. That is, only one plasma activation treatment is performed on the front surfaces of the first and second wafers, which is based on water molecules, according to some embodiments. In some embodiments, operation 404 is performed on the front surfaces of the first and second wafers, which are free from another plasma activation

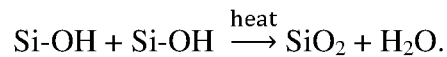
treatment based on oxygen or an inert gas, e.g., operation 402. In one example, the single plasma activation treatment can use water vapor as the plasma gas without oxygen or an inert gas. In another example, the single plasma activation treatment can use water vapor as well as at least one of oxygen or an inert gas as the mixed plasma gases. The processing conditions of the single plasma activation treatment are nominally the same as those of the second plasma activation treatment described above, according to some embodiments, which are not repeated.

[0054] Method 400 proceeds to operation 406, as illustrated in FIG. 4, in which, after the second plasma activation treatment, the front surface of the first wafer and the front surface of the second wafer are rinsed using liquid water. As illustrated in FIG. 2C, the front surfaces of first and second wafers 202 and 204 are rinsed using deionized water, which can clean the bonding surfaces prior to the bonding and further increase the amount of hydroxyl groups (from the free hydroxyl groups in the liquid water) on the bonding surfaces of first and second wafers 202 and 204. In some embodiments in which first and second wafers 202 and 204 are silicon wafers, after plasma activation treatment(s) and water rinsing, front surfaces of first and second silicon wafers 202 and 204 can be mainly terminated by silanol groups as shown in FIG. 3.

[0055] Method 400 proceeds to operation 408, as illustrated in FIG. 4, in which, after the water rinsing, the first wafer and the second wafer are bonded such that the treated front surface of the first wafer is in physical contact with the treated front surface of the second wafer. In some embodiments, the bonding includes hybrid bonding. For hybrid bonding, silanol groups are not formed on the entire front surfaces of first and second wafers, but instead formed only on the dielectric layers (e.g., silicon oxide layers).

[0056] As illustrated in FIG. 2D, first wafer 202 is flipped upside down and held in a face-to-face manner toward second wafer 204 by a bond chuck 206. In some embodiments, mechanical locking mechanisms and/or vacuum suction are used to hold first and second wafers 202 and 204 in a face-to-face manner after alignment. An electric field is applied to first and second wafers 202 and 204 through electrodes in bond chuck 206, according to some embodiments. Pressure can be applied through bond chuck 206 to initiate the bonding process (e.g., as a preliminary bonding process). In some embodiments, the pressure brings the bonding surfaces of first and second wafers 202 and 204 into physical contact. As shown in FIG. 3, during this operation, van der Waals

bonds and hydrogen bonds of hydroxyl groups 302 can be formed between the front surface of first silicon wafer 202 and the front surface of second silicon wafer 204, opposite to one another. A heat treatment process can then be applied through heating elements in bond chuck 206 on first and second silicon wafers 202 and 204. As shown in FIG. 3, a condensation reaction of silanol groups on the front surfaces of first and second wafers 202 and 204 can occur during the heat treatment, which results in formation of covalent Si-O-Si bonds 304 at the bonding interface between the front surfaces of first and second silicon wafers 202 and 204, thereby bonding first and second silicon wafers 202 and 204 together. In addition, the condensation reaction can also remove water molecules from the bonding interface. The condensation reaction can be described as following:



[0057] In some embodiments, the heat treatment can include thermally annealing first and second wafers 202 and 204 under nitrogen atmosphere, with an annealing temperature between about 200 °C and about 450 °C, such as between 200 °C and 450 °C. In some embodiments, the heat treatment duration is between about 1 hour and about 2 hours, such as between 1 hour and 2 hours.

[0058] According to one aspect of the present disclosure, a method for wafer bonding is disclosed. A first plasma activation treatment based on oxygen or an inert gas is performed on a front surface of a first wafer and a front surface of a second wafer. After the first plasma activation treatment, a second plasma activation treatment based on water molecules is performed on the front surface of the first wafer and the front surface of the second wafer. After the second plasma activation treatment, the first wafer and the second wafer are bonded such that the treated front surface of the first wafer is in physical contact with the treated front surface of the second wafer.

[0059] In some embodiments, after the second plasma activation treatment and prior to the bonding, the treated front surface of the first wafer and the treated front surface of the second wafer are rinsed using liquid water.

[0060] In some embodiments, to perform the second plasma activation treatment, liquid water is vaporized to form water vapor, and the water vapor is used as a plasma gas.

[0061] In some embodiments, the second plasma activation treatment is performed with a pressure between about 0.05 mbar and about 0.5 mbar. In some embodiments, the second

plasma activation treatment is performed with a discharge power between about 10 watts and about 100 watts. In some embodiments, the second plasma activation treatment is performed for a duration between about 5 seconds and about 50 seconds.

[0062] In some embodiments, at least one of a pressure, a discharge power, or a duration of the first plasma activation treatment is the same as a respective one of a pressure, a discharge power, or a duration of the second plasma activation treatment.

[0063] In some embodiments, the bonding includes hybrid bonding.

[0064] In some embodiments, hydroxyl groups are formed on the front surface of the first wafer and the front surface of the second wafer by the second plasma activation treatment. Each of the first and second wafers includes silicon, and the hydroxyl groups are bonded on the silicon to form silanol groups, according to some embodiments. In some embodiments, the second plasma activation treatment facilitates the bonding between the hydroxyl groups and the silicon.

[0065] According to another aspect of the present disclosure, a method for wafer bonding is disclosed. A plasma activation treatment based on water molecules is performed on a front surface of a first wafer and a front surface of a second wafer. The front surface of the first wafer and the front surface of the second wafer are free from another plasma activation treatment based on oxygen or an inert gas. After the plasma activation treatment, the first wafer and the second wafer are bonded such that the treated front surface of the first wafer is in physical contact with the treated front surface of the second wafer.

[0066] In some embodiments, after the plasma activation treatment and prior to the bonding, the treated front surface of the first wafer and the treated front surface of the second wafer are rinsed using liquid water.

[0067] In some embodiments, to perform the plasma activation treatment, liquid water is vaporized to form water vapor, and the water vapor is used as a plasma gas.

[0068] In some embodiments, the plasma activation treatment is performed with a pressure between about 0.05 mbar and about 0.5 mbar. In some embodiments, the plasma activation treatment is performed with a discharge power between about 10 watts and about 100 watts. In some embodiments, the plasma activation treatment is performed for a duration between about 5 seconds and about 50 seconds.

[0069] In some embodiments, the bonding includes hybrid bonding.

- [0070] In some embodiments, hydroxyl groups are formed on the front surface of the first wafer and the front surface of the second wafer by the plasma activation treatment. Each of the first and second wafers includes silicon, and the hydroxyl groups are bonded on the silicon to form silanol groups, according to some embodiments. In some embodiments, the plasma activation treatment facilitates the bonding between the hydroxyl groups and the silicon.
- [0071] According to still another aspect of the present disclosure, a method for wafer bonding is disclosed. A plasma activation treatment is performed on a front surface of a first silicon wafer and a front surface of a second silicon wafer to form hydroxyl groups on the front surface of the first silicon wafer and the front surface of the second silicon wafer. After the plasma activation treatment, the first silicon wafer and the second silicon wafer are bonded such that the treated front surface of the first silicon wafer is in physical contact with the treated front surface of the second silicon wafer.
- [0072] In some embodiments, the hydroxyl groups are bonded on silicon to form silanol groups. In some embodiments, the plasma activation treatment facilitates the bonding between the hydroxyl groups and the silicon.
- [0073] In some embodiments, to perform the plasma activation treatment, liquid water is vaporized to form water vapor, and the water vapor is used as a plasma gas.
- [0074] In some embodiments, prior to performing the plasma activation treatment, another plasma activation treatment is performed based on oxygen or an inert gas on the front surface of the first silicon wafer and the front surface of the second silicon wafer.
- [0075] In some embodiments, the front surface of the first silicon wafer and the front surface of the second silicon wafer are free from another plasma activation treatment based on oxygen or an inert gas.
- [0076] In some embodiments, after the plasma activation treatment and prior to the bonding, the treated front surface of the first silicon wafer and the treated front surface of the second silicon wafer are rinsed using liquid water.
- [0077] In some embodiments, the bonding includes hybrid bonding.
- [0078] The foregoing description of the specific embodiments will so reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present

disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0079] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0080] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0081] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A method for wafer bonding, comprising:
performing a first plasma activation treatment based on oxygen or an inert gas on a front surface of a first wafer and a front surface of a second wafer;
after the first plasma activation treatment, performing a second plasma activation treatment based on water molecules on the front surface of the first wafer and the front surface of the second wafer; and
after the second plasma activation treatment, bonding the first wafer and the second wafer such that the treated front surface of the first wafer is in physical contact with the treated front surface of the second wafer.
2. The method of claim 1, further comprising, after the second plasma activation treatment and prior to the bonding, rinsing the treated front surface of the first wafer and the treated front surface of the second wafer using liquid water.
3. The method of claim 1 or 2, wherein performing the second plasma activation treatment comprises:
vaporizing liquid water to form water vapor; and
using the water vapor as a plasma gas.
4. The method of any one of claims 1-3, wherein the second plasma activation treatment is performed with a pressure between about 0.05 mbar and about 0.5 mbar.
5. The method of any one of claims 1-4, wherein the second plasma activation treatment is performed with a discharge power between about 10 watts and about 100 watts.
6. The method of any one of claims 1-5, wherein the second plasma activation treatment is performed for a duration between about 5 seconds and about 50 seconds.

7. The method of any one of claims 1-3, wherein at least one of a pressure, a discharge power, or a duration of the first plasma activation treatment is the same as a respective one of a pressure, a discharge power, or a duration of the second plasma activation treatment.

8. The method of any one of claims 1-7, wherein the bonding includes hybrid bonding.

9. The method of any one of claims 1-8, wherein hydroxyl groups are formed on the front surface of the first wafer and the front surface of the second wafer by the second plasma activation treatment.

10. The method of claim 9, wherein
each of the first and second wafers comprises silicon; and
the hydroxyl groups are bonded on the silicon to form silanol groups.

11. The method of claim 10, wherein the second plasma activation treatment facilitates the bonding between the hydroxyl groups and the silicon.

12. A method for wafer bonding, comprising:
performing a plasma activation treatment based on water molecules on a front surface of a first wafer and a front surface of a second wafer, the front surface of the first wafer and the front surface of the second wafer being free from another plasma activation treatment based on oxygen or an inert gas; and

after the plasma activation treatment, bonding the first wafer and the second wafer such that the treated front surface of the first wafer is in physical contact with the treated front surface of the second wafer.

13. The method of claim 12, further comprising, after the plasma activation treatment and prior to the bonding, rinsing the treated front surface of the first wafer and the treated front surface of the second wafer using liquid water.

14. The method of claim 12 or 13, wherein performing the plasma activation treatment comprises:

vaporizing liquid water to form water vapor; and
using the water vapor as a plasma gas.

15. The method of any one of claims 12-14, wherein the plasma activation treatment is performed with a pressure between about 0.05 mbar and about 0.5 mbar.

16. The method of any one of claims 12-15, wherein the plasma activation treatment is performed with a discharge power between about 10 watts and about 100 watts.

17. The method of any one of claims 12-16, wherein the plasma activation treatment is performed for a duration between about 5 seconds and about 50 seconds.

18. The method of any one of claims 12-17, wherein the bonding includes hybrid bonding.

19. The method of any one of claims 12-18, wherein hydroxyl groups are formed on the front surface of the first wafer and the front surface of the second wafer by the plasma activation treatment.

20. The method of claim 19, wherein
each of the first and second wafers comprises silicon; and
the hydroxyl groups are bonded on the silicon to form silanol groups.

21. The method of claim 20, wherein the plasma activation treatment facilitates the bonding between the hydroxyl groups and the silicon.

22. A method for wafer bonding, comprising:
performing a plasma activation treatment on a front surface of a first silicon wafer and a front surface of a second silicon wafer to form hydroxyl groups on the front surface of the first silicon wafer and the front surface of the second silicon wafer; and

after the plasma activation treatment, bonding the first silicon wafer and the second silicon wafer such that the treated front surface of the first silicon wafer is in physical contact with the treated front surface of the second silicon wafer.

23. The method of claim 22, wherein the hydroxyl groups are bonded on silicon to form silanol groups.

24. The method of claim 23, wherein the plasma activation treatment facilitates the bonding between the hydroxyl groups and the silicon.

25. The method of any one of claims 22-24, wherein performing the plasma activation treatment comprises:

vaporizing liquid water to form water vapor; and
using the water vapor as a plasma gas.

26. The method of any one of claims 22-25, further comprising, prior to performing the plasma activation treatment, performing another plasma activation treatment based on oxygen or an inert gas on the front surface of the first silicon wafer and the front surface of the second silicon wafer.

27. The method of any one of claims 22-25, wherein the front surface of the first silicon wafer and the front surface of the second silicon wafer are free from another plasma activation treatment based on oxygen or an inert gas.

28. The method of any one of claims 22-27, further comprising, after the plasma activation treatment and prior to the bonding, rinsing the treated front surface of the first silicon wafer and the treated front surface of the second silicon wafer using liquid water.

29. The method of any one of claims 22-28, wherein the bonding includes hybrid bonding.

100

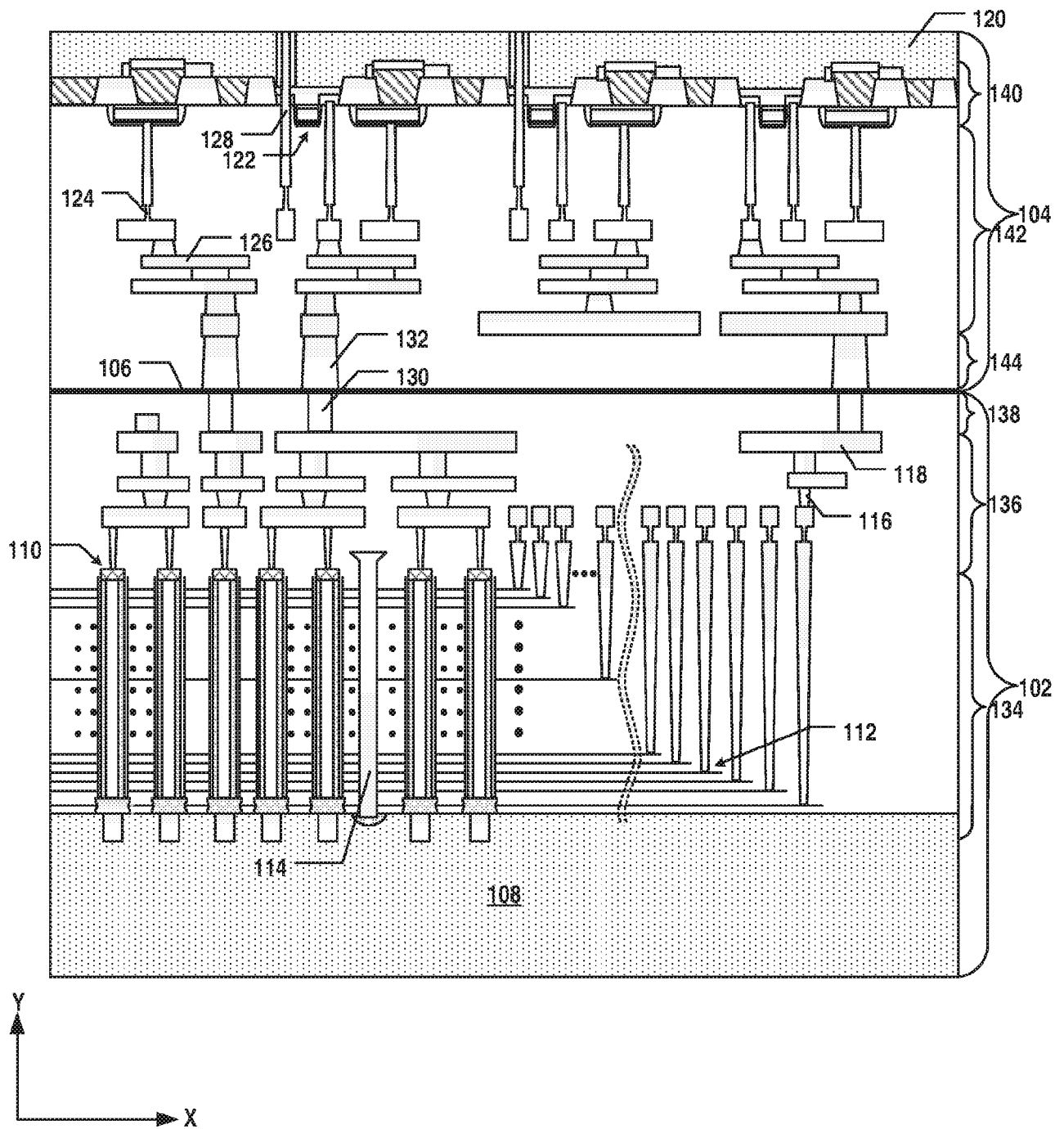


FIG. 1A

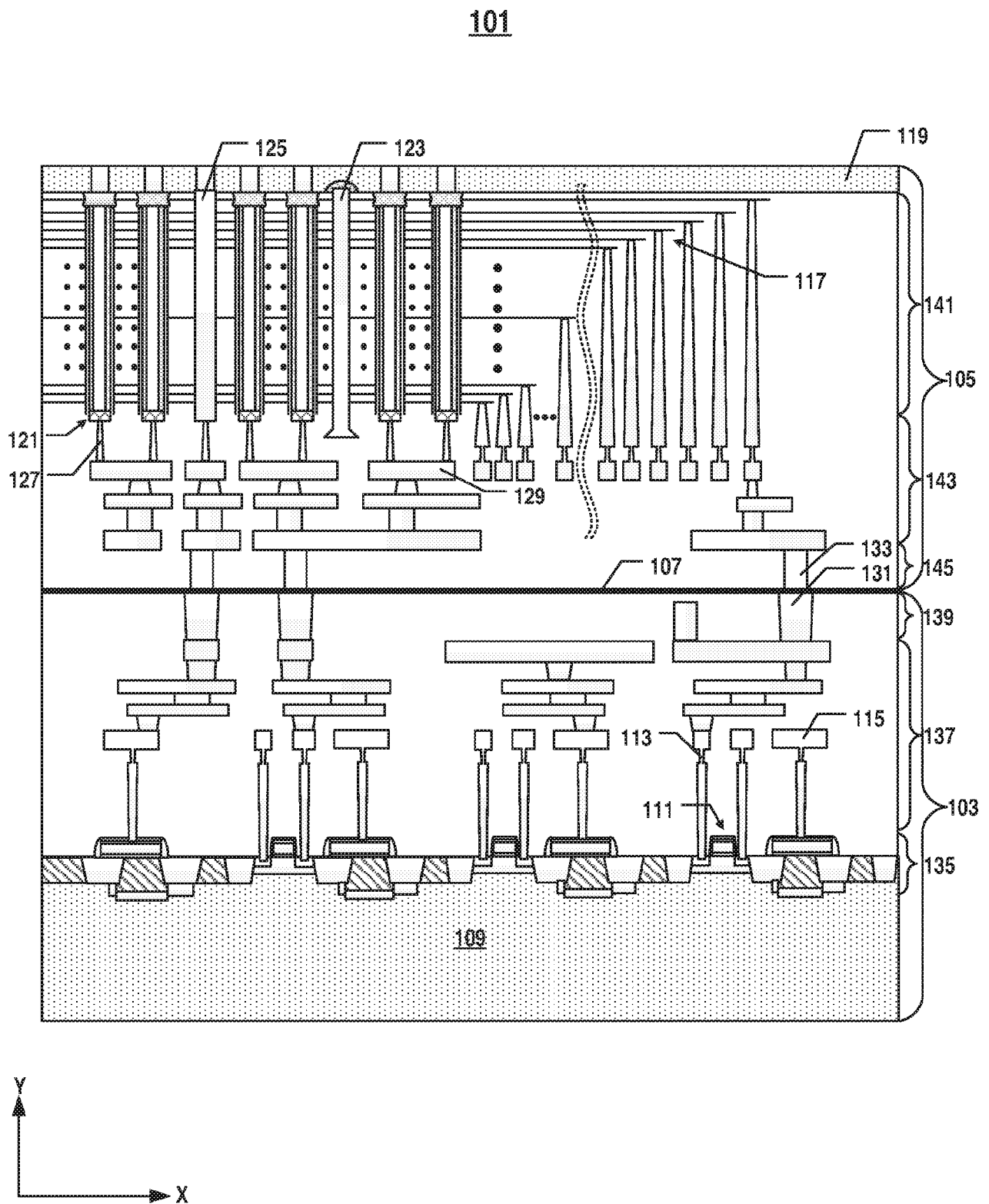


FIG. 1B

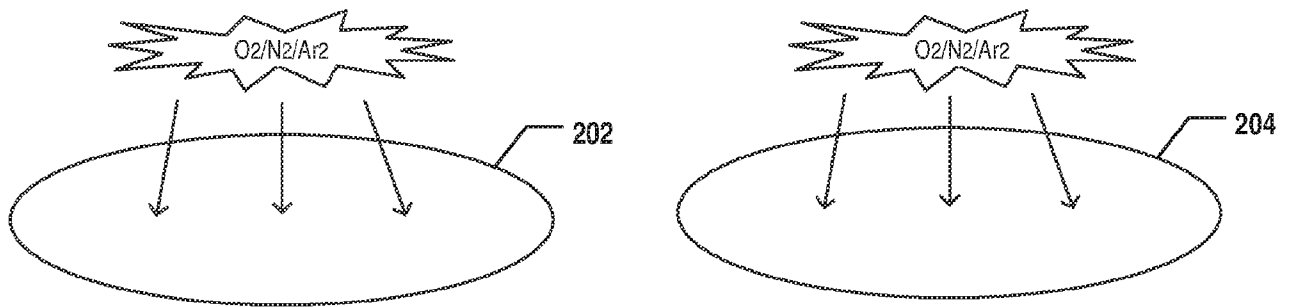


FIG. 2A

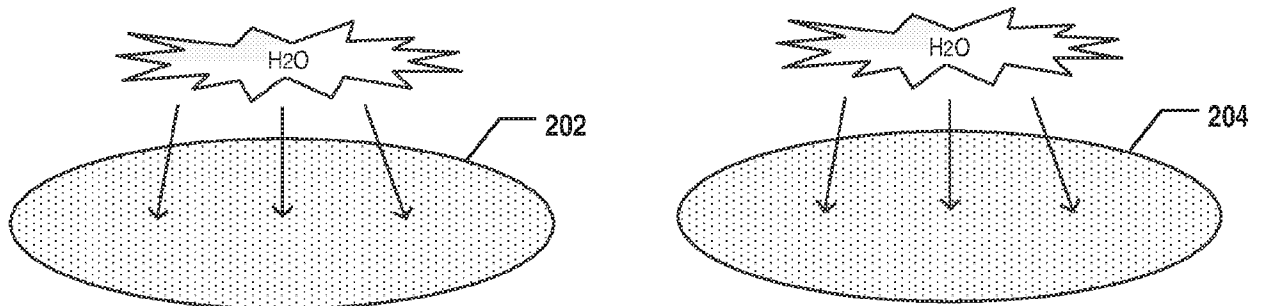


FIG. 2B

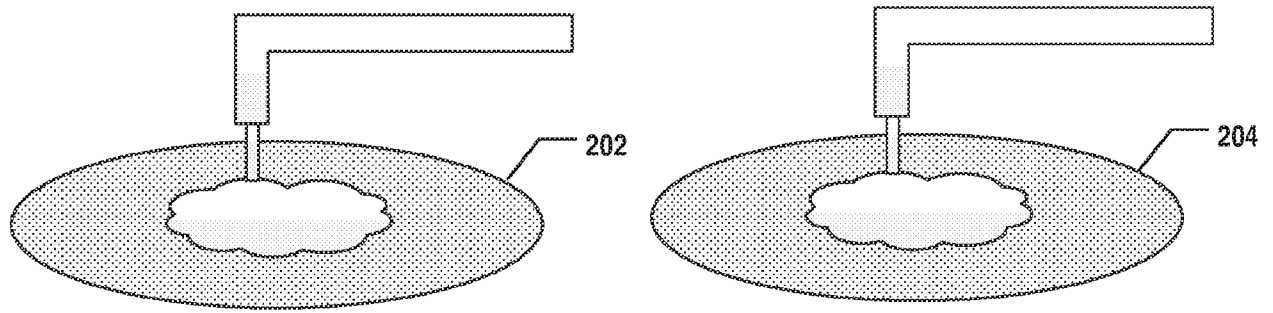


FIG. 2C

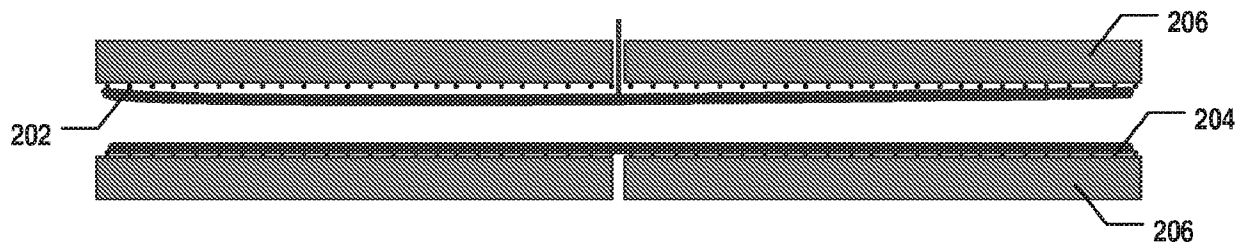


FIG. 2D

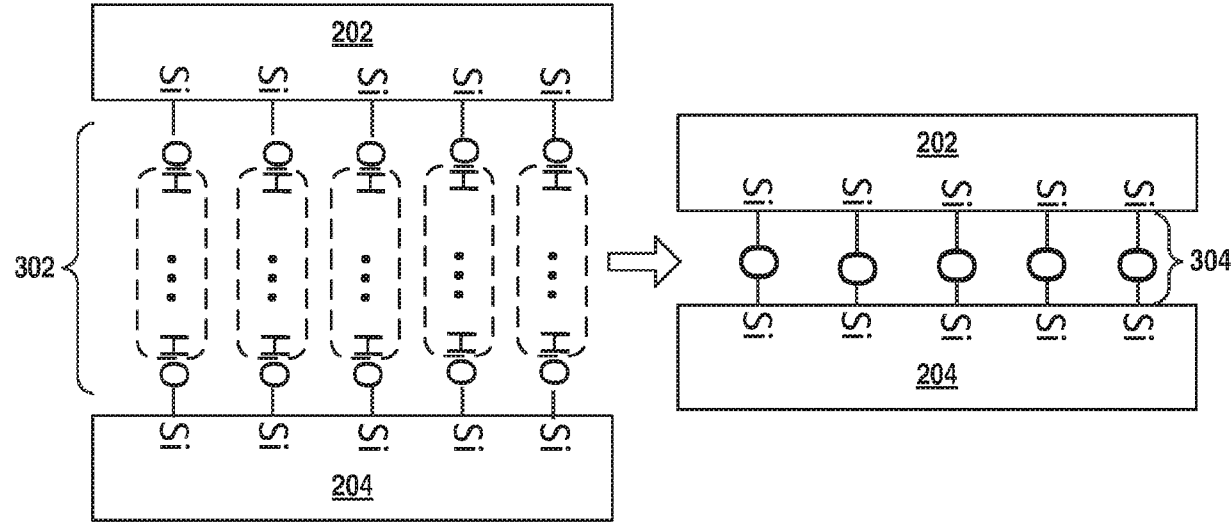


FIG. 3

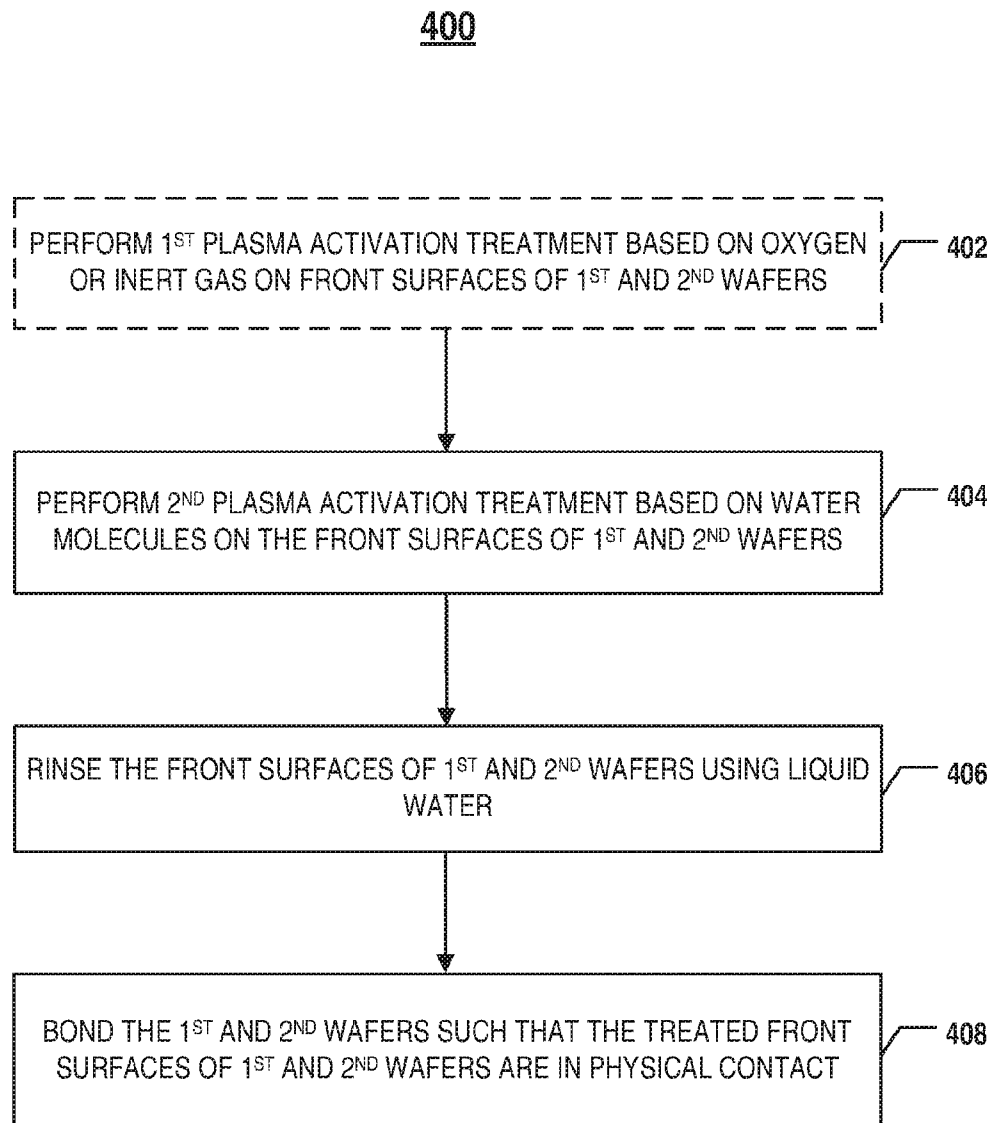
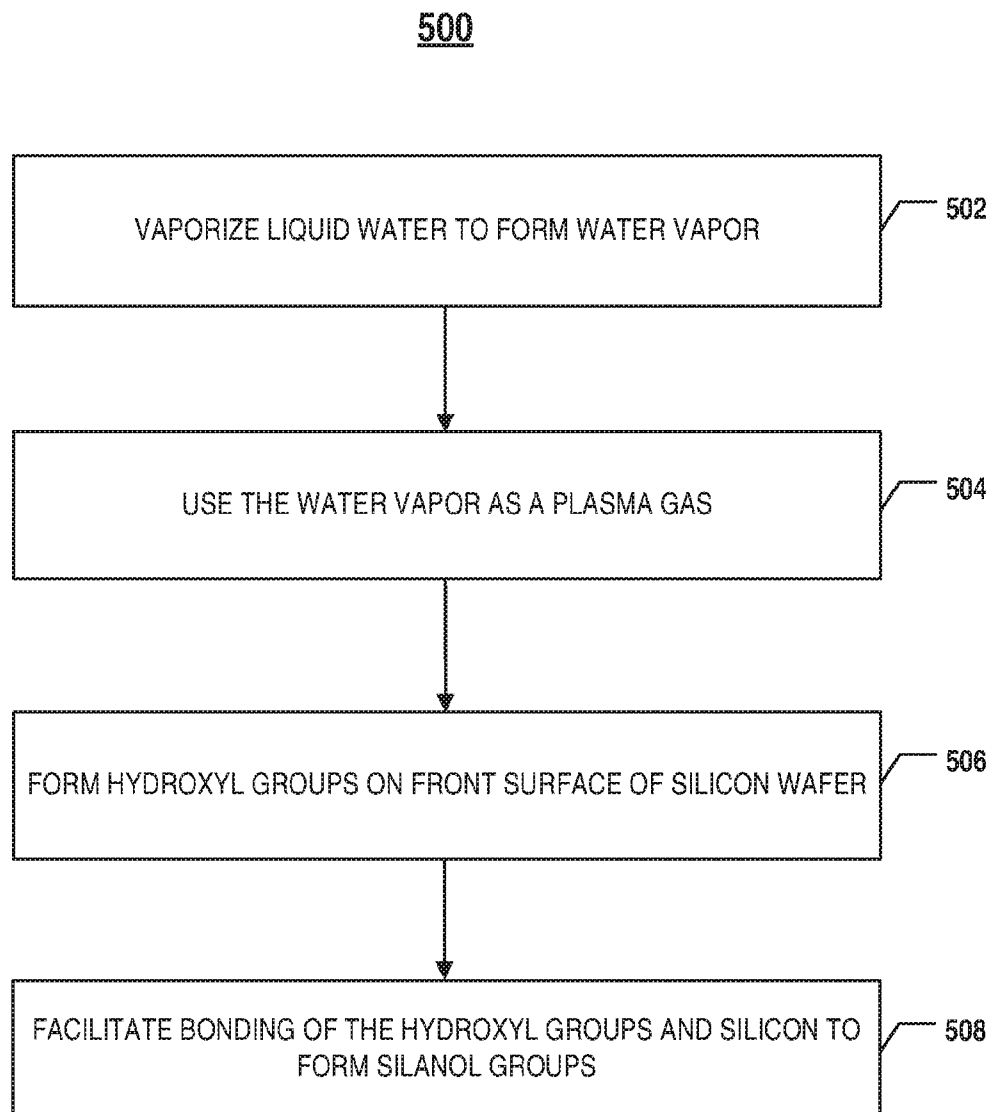


FIG. 4

**FIG. 5**

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/070143

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/60(2006.01)i; H01L 21/50(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,WPI,EPODOC,CNKI:YMTC, wafer, plasma, activat+, functionaliz+, oxygen, inert, gas, front, surface, water, rins, vaporiz+, increase, facilitate, hydroxyl, group, silicon, silanol, treatment, enhance, modification, hydrophilization, join

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5421953 A (NIPPONDENSO CO., LTD.) 06 June 1995 (1995-06-06) description, column 2 line 37-column 3 line 3, column 10 lines 32-61, and figures 1A-2D, 8	1-29
X	US 2006032582 A1 (CHEN, CHIEN-HUA ET AL.) 16 February 2006 (2006-02-16) description, paragraphs [0018]-[0043] and figures 2-5C	1-29
A	CN 107633997 A (YANGTZE MEMORY TECHNOLOGIES CO., LTD.) 26 January 2018 (2018-01-26) the whole document	1-29
A	CN 106571334 A (SHANGHAI IC R&D CENTER CO., LTD.) 19 April 2017 (2017-04-19) the whole document	1-29
A	CN 105197880 A (SEMICONDUCTOR MANUFACTURING INTERNATIONAL SHANGHAI CORPORATION) 30 December 2015 (2015-12-30) the whole document	1-29
A	JP 2017079316 A (BONDTECH INC.) 27 April 2017 (2017-04-27) the whole document	1-29
A	US 2007111471 A1 (BONDTECH INC.) 17 May 2007 (2007-05-17) the whole document	1-29

☒ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

10 September 2019

Date of mailing of the international search report

10 October 2019

Name and mailing address of the ISA/CN

National Intellectual Property Administration, PRC
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
100088
China

Authorized officer

WEI,Yanyan

Facsimile No. (86-10)62019451

Telephone No. 86-(10)-53962512

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/070143

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2014141560 A1 (RENESAS ELECTRONICS CORPORATION) 22 May 2014 (2014-05-22) the whole document	1-29

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/070143

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	5421953	A	06 June 1995	JP	H06302486	A	28 October 1994
				JP	2701709	B2	21 January 1998
				DE	4404931	A1	18 August 1994
US	2006032582	A1	16 February 2006	EP	1787322	A2	23 May 2007
				US	2006033188	A1	16 February 2006
				WO	2006020439	A2	23 February 2006
				US	7261793	B2	28 August 2007
				US	2007272349	A1	29 November 2007
				EP	1787322	B1	29 June 2011
				TW	200607751	A	01 March 2006
				JP	2008513975	A	01 May 2008
				TW	I372723	B	21 September 2012
				JP	5026267	B2	12 September 2012
CN	107633997	A	26 January 2018	TW	201911365	A	16 March 2019
				WO	2019029237	A1	14 February 2019
				CN	107633997	B	29 January 2019
				CN	109671614	A	23 April 2019
				US	2019051524	A1	14 February 2019
CN	106571334	A	19 April 2017	WO	2018076700	A1	03 May 2018
				US	2019214257	A1	11 July 2019
CN	105197880	A	30 December 2015	CN	105197880	B	20 March 2018
JP	2017079316	A	27 April 2017	JP	6544722	B2	17 July 2019
US	2007111471	A1	17 May 2007	WO	2005054147	A1	16 June 2005
				US	7645681	B2	12 January 2010
				JP	4695014	B2	08 June 2011
				JP	2006248895	A	21 September 2006
				JP	3820409	B2	13 September 2006
				JP	2005187321	A	14 July 2005
US	2014141560	A1	22 May 2014	JP	2014103291	A	05 June 2014
				US	9608034	B2	28 March 2017
				US	2016118437	A1	28 April 2016
				US	9263497	B2	16 February 2016