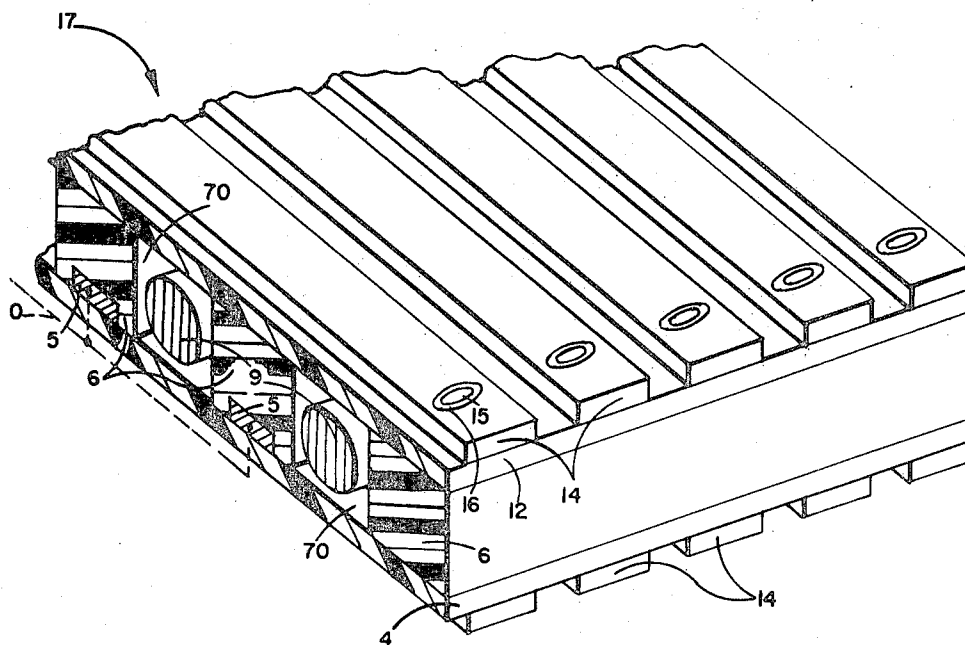


- [56] **References Cited**
- UNITED STATES PATENTS**
- 3,567,533 3/1971 Chiang et al. 156/3
- Primary Examiner*—Jacob H. Steinberg
Attorney—L. Lee Humphries, H. Fredrick Hamann
and Martin E. Gerry

A series of processes are described for making mats to accommodate plated wire memory conductors. Certain of these mats also include interstitial conductors. Outer layers of metal are etched to form word-straps. These word-straps are orthogonal to the tunnels in the mats, which tunnels accommodate the plated wires. Interstitial conductors used, are generally connected to a common point. In order to provide ready access to these tunnels or channels for easy insertion of the plated wires therein, molds are made by either of two special processes, which molds have cavities therein for retaining resin to be molded into walls forming the aforesaid tunnels. The molds provided results in both instances when used in a molding machine and/or in a press, in the final product, wherein the tunnels are blocked off at either end by the plastic material which is also used to form the top and bottom of tunnels. This is done in order to prevent accumulations within the tunnels of undesired matter and thereby prevent blocking of the tunnels and prevent inhibiting the insertion of the plated wires. Therefore, by cutting off an end strip of the plastic material covering the tunnel entrances at both ends after completing of molding or forming operations, the tunnels thus provided are free and clear of undesired foreign matter.

9 Claims, 34 Drawing Figures



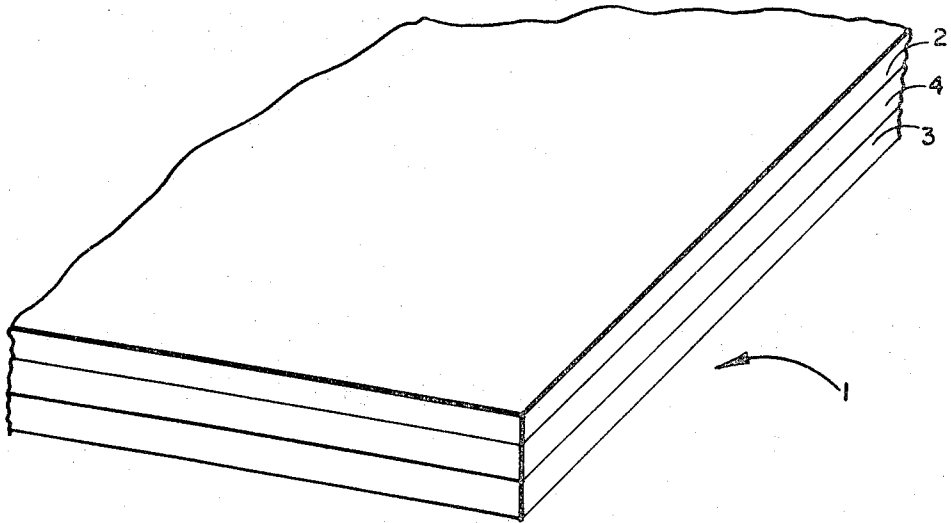


FIG. 1

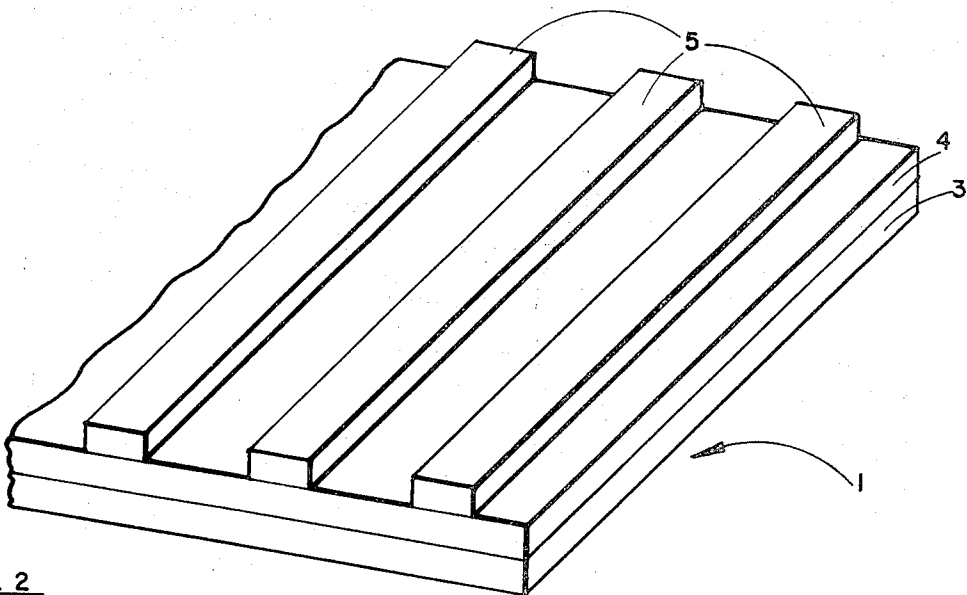
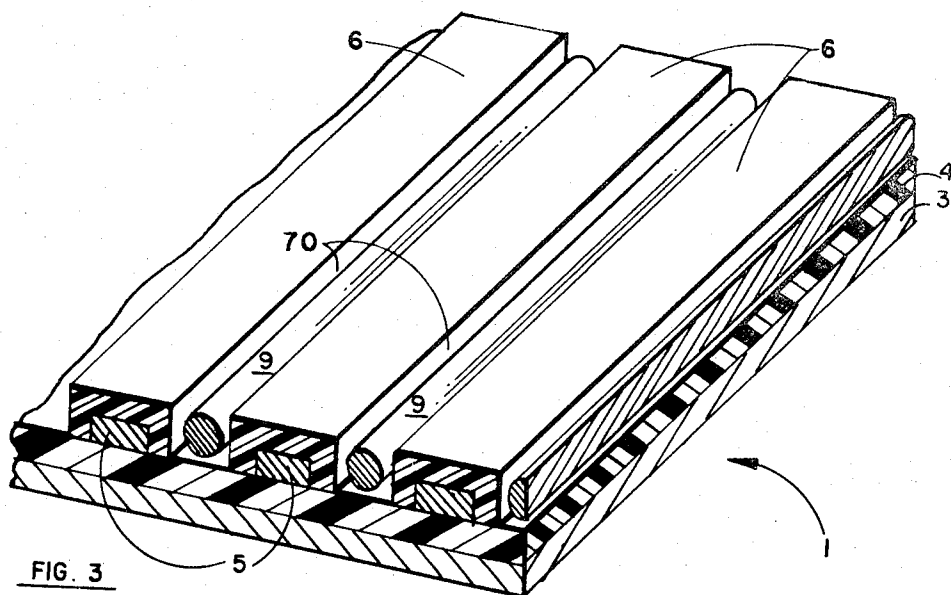
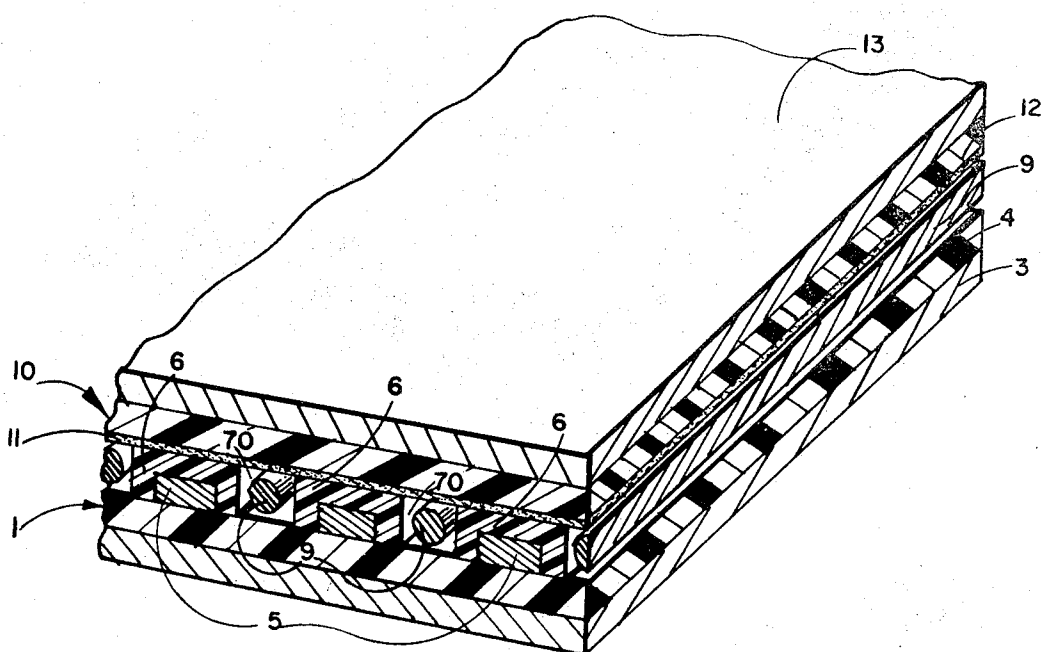


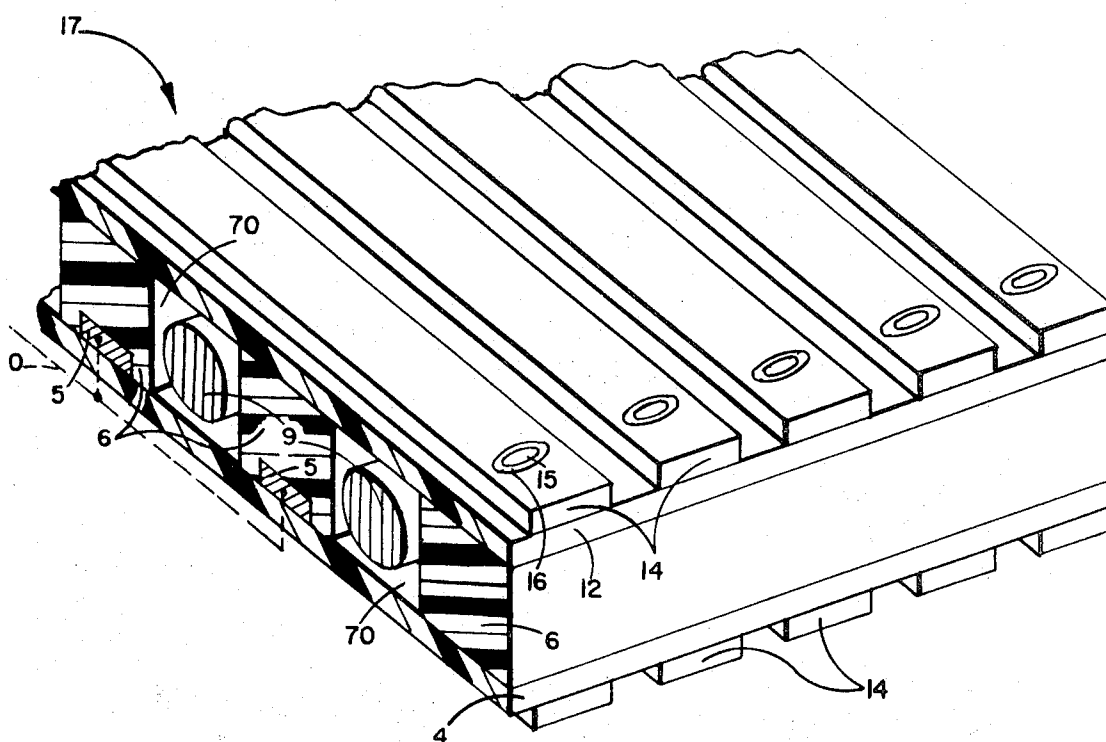
FIG. 2

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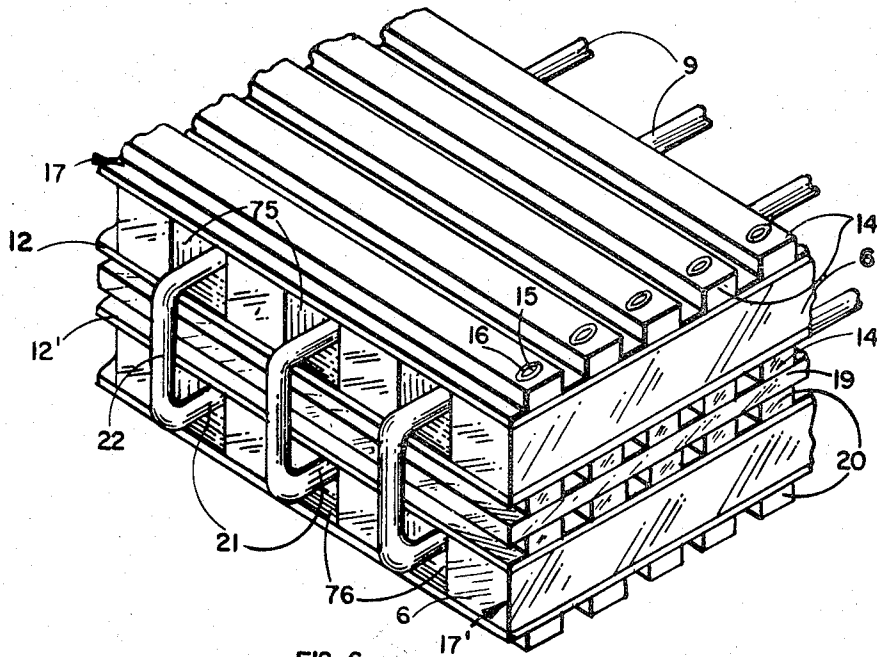


FIG. 6

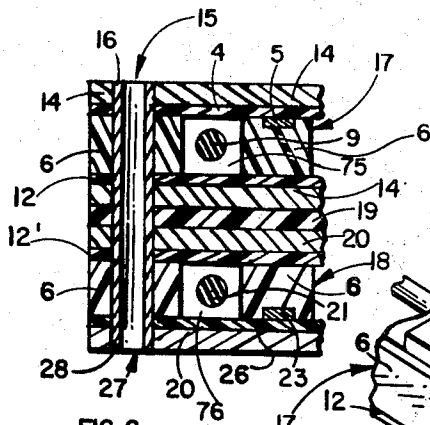


FIG. 8

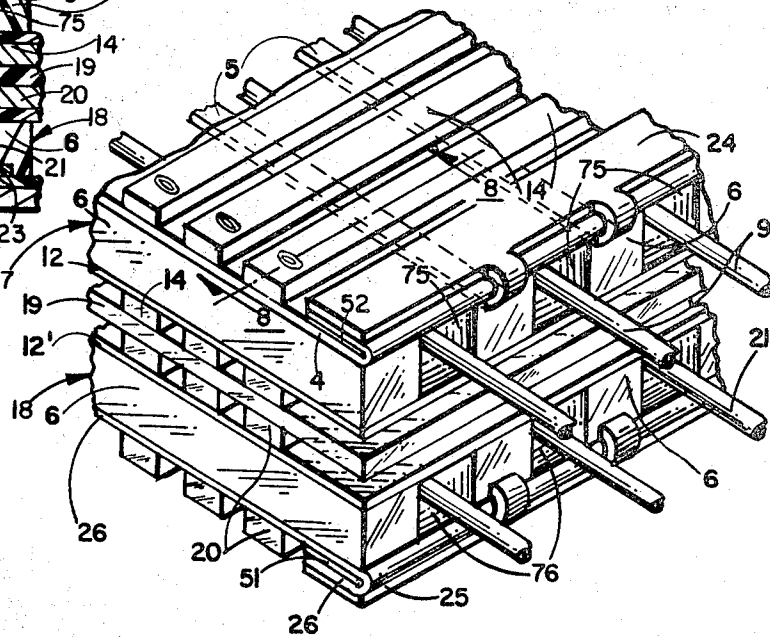


FIG. 7

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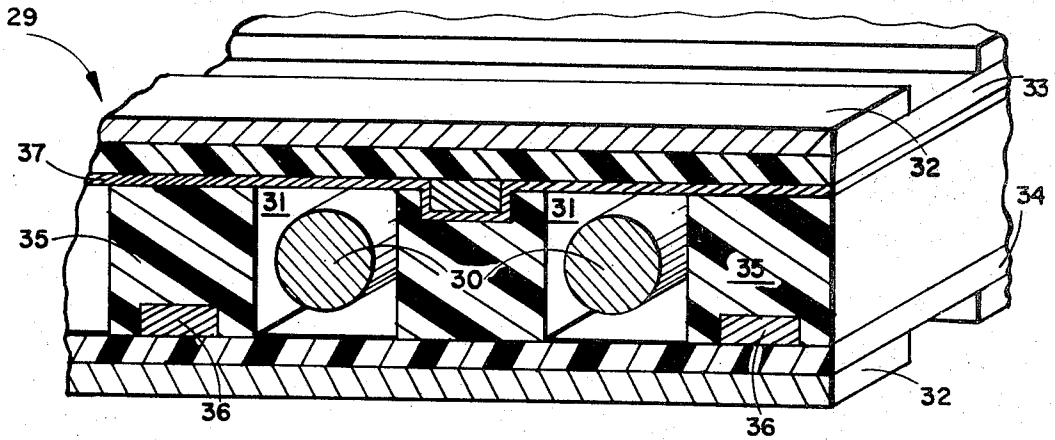


FIG. 9

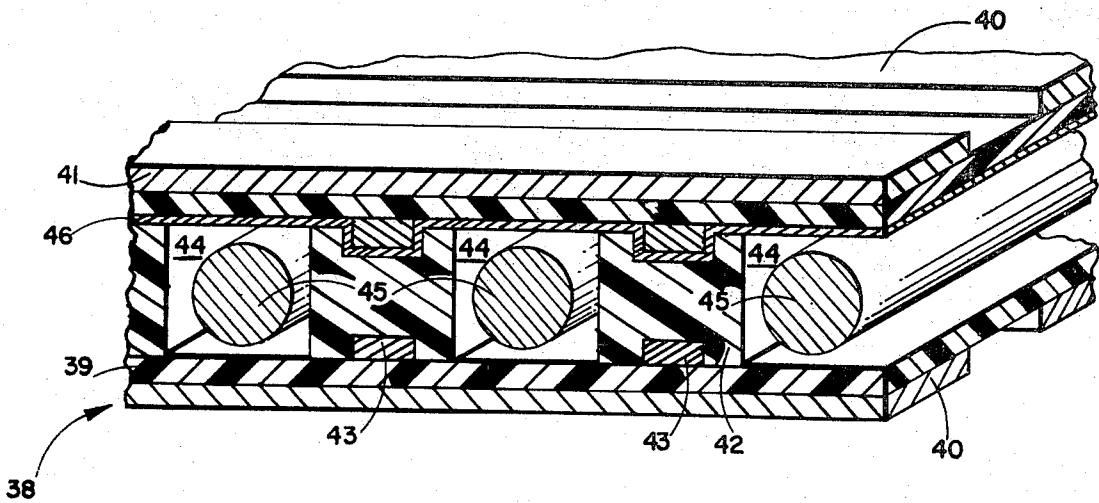


FIG. 10

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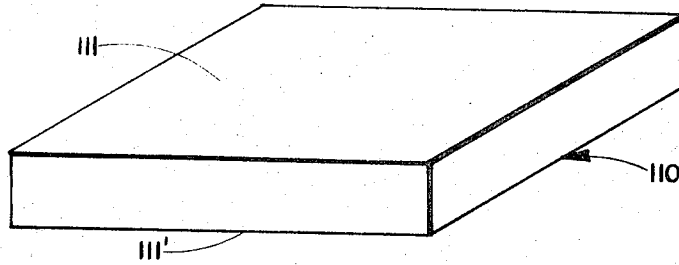


FIG. 11

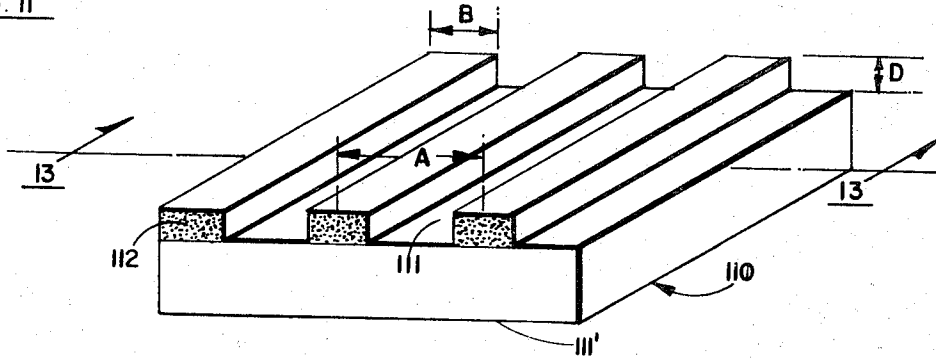


FIG. 12

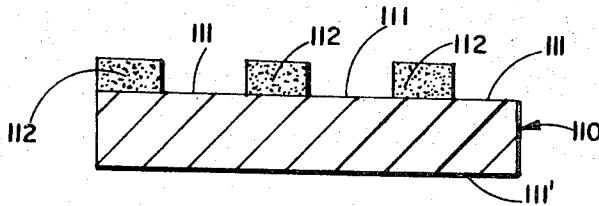


FIG. 13

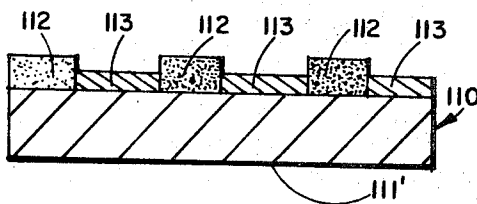


FIG. 14

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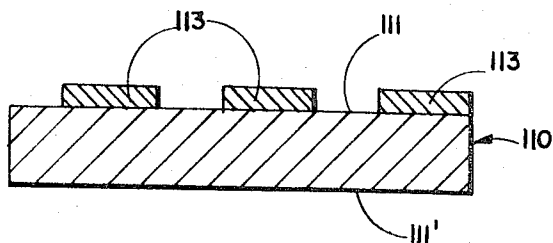


FIG. 15

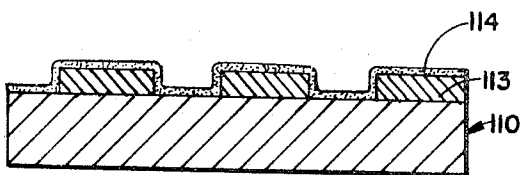


FIG. 16

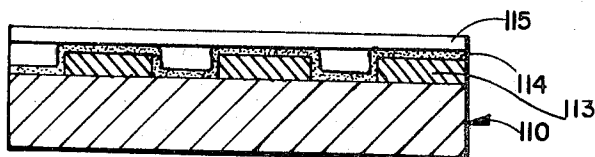


FIG. 17

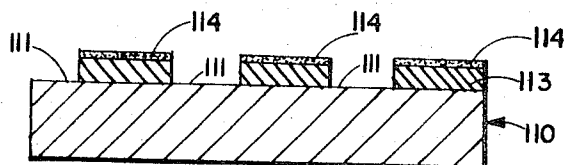


FIG. 18

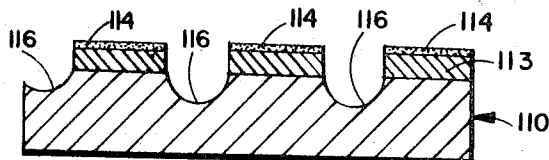


FIG. 19

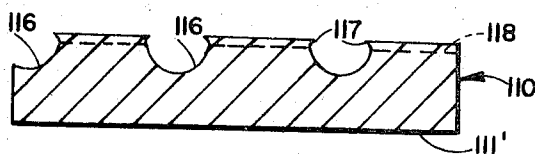


FIG. 20

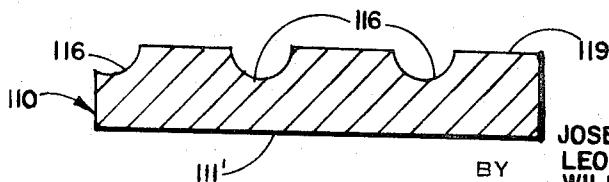


FIG. 21

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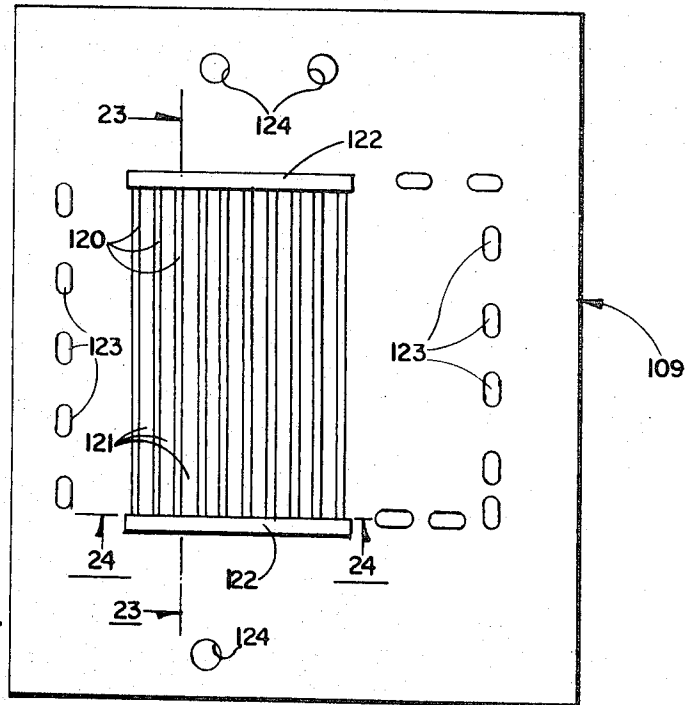


FIG. 22

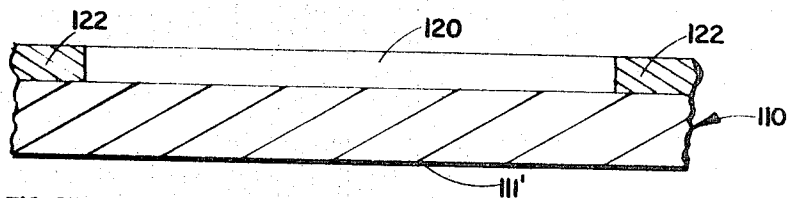


FIG. 23

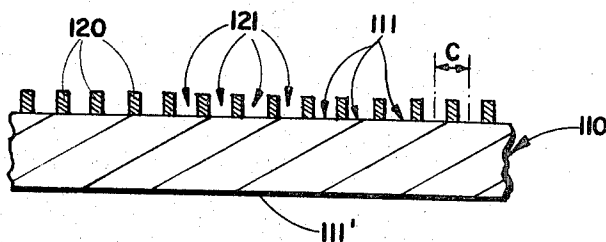


FIG. 24

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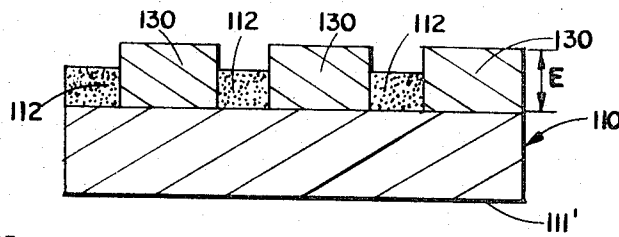


FIG. 25

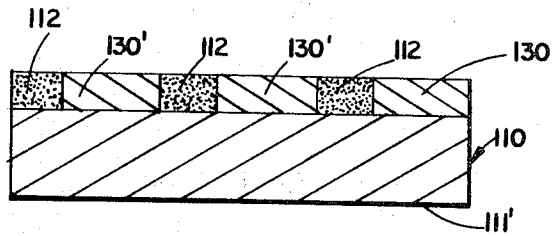


FIG. 26

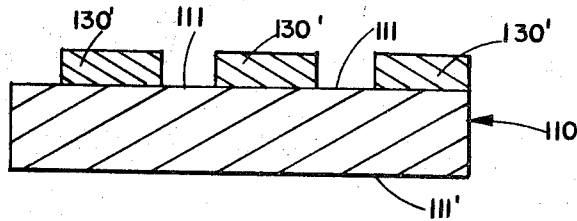


FIG. 27

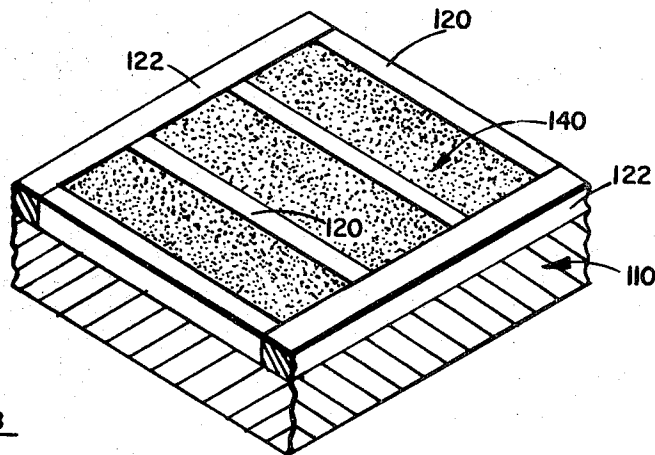


FIG. 28

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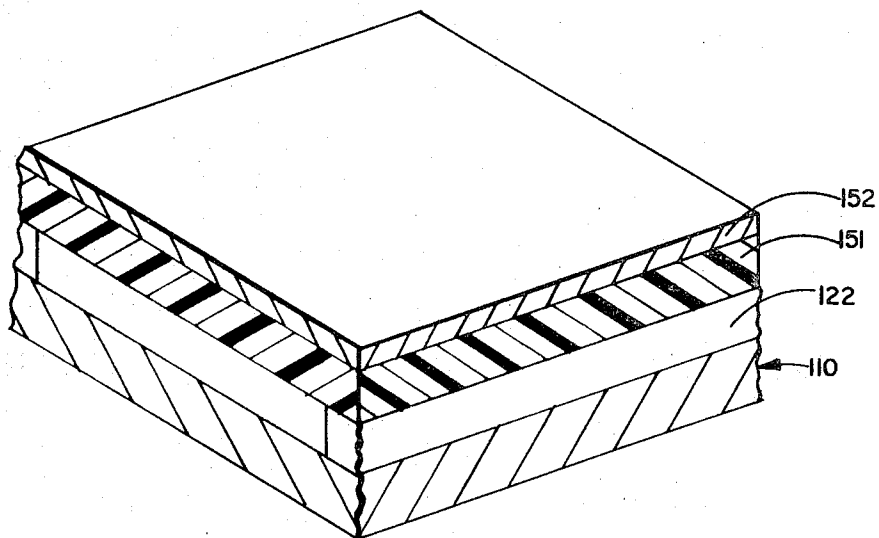


FIG. 29

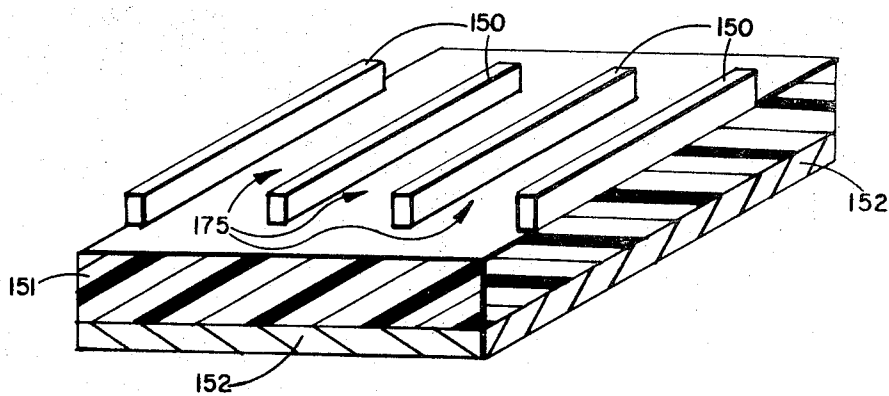


FIG. 30

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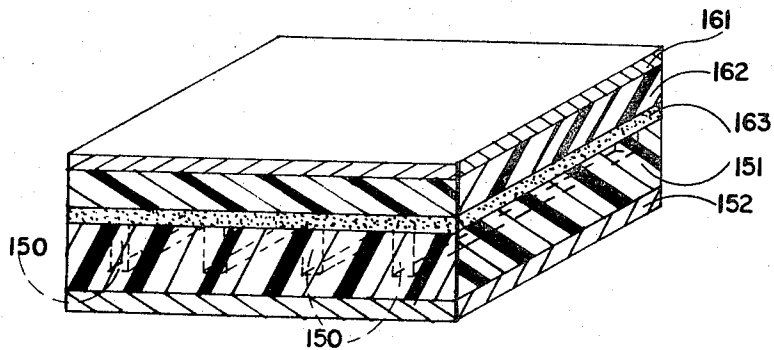


FIG. 31

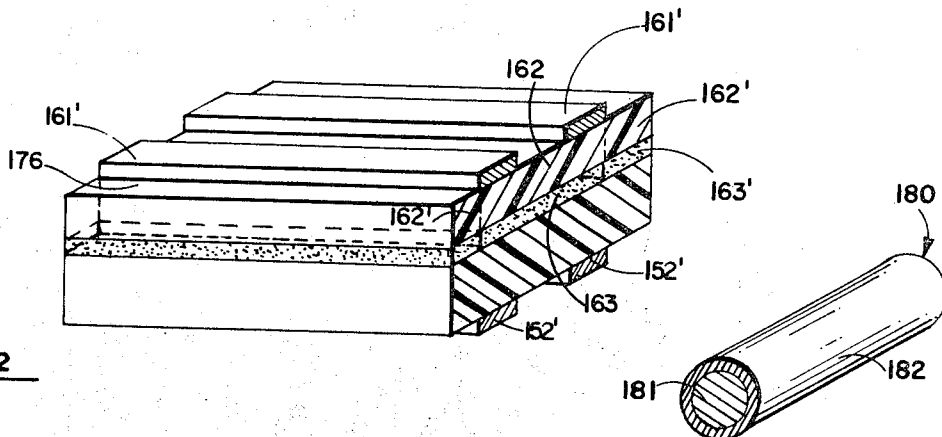


FIG. 32

FIG. 34

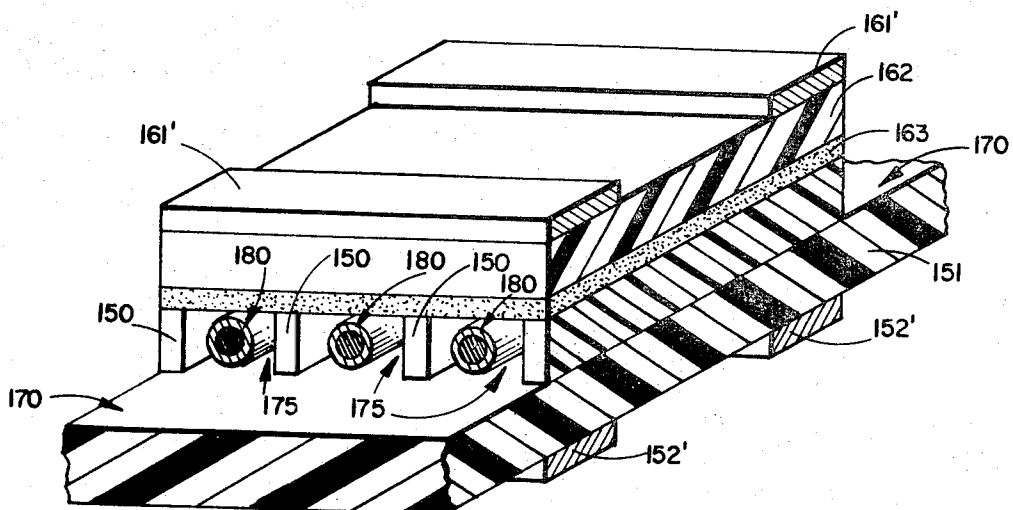


FIG. 33

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METHOD FOR MAKING A MOLD FOR CASTING OPEN TUNNELS IN PLATED WIRE MATS

BACKGROUND OF THE INVENTION

The invention relates to interstitial conductors between tunnels of a plated wire memory mat and more particularly to interstitial conductors which are covered by insulating layers to form tunnels for plated memory wires free of undesired matter within the tunnels.

U.S. Pat. No. 3,501,830, issued Mar. 24, 1970 to T. F. Bryzinski et al., for Methods of Making a Filamentary Magnetic Memory Using Flexible Sheet Metal teaches and shows a process for forming channels for accommodating plated memory wires called filaments. In one process, polystyrene is molded into layers for forming a channel structure. Copper clad flexible sheets are formed on the both sides of the polystyrene layers to complete the plated wire memory structure. Filaments are inserted into the channels before the tunnel structure is formed. The filaments are replaced by magnetically coated filaments subsequently. The patent also shows how electrical connections are made to the plated memory wires.

It is pointed out, however, that U.S. Pat. No. 3,501,830 does not teach or show interstitial conductors between each of the plated memory wires. The process disclosed in the U.S. Pat. No. 3,501,830 also requires that removable wires (filaments) be inserted into the tunnel structure as the tunnel structure is being formed. A process is preferred in which the tunnels can be formed without the necessity for using removable wires as taught by the patent. Interstitial conductors are necessary to reduce the electrical field between plated memory wires during the operation of the structure as a plated wire memory. If the electrical interference between wires can be reduced, the plated memory wires can be placed closer together for increasing the density of the plated wire memory.

The prior art does not disclose unique methods of making molds so as to prevent tunnels in which plated wires are inserted from being blocked by accumulation of undesired matter therein during the molding process, the tool or mold itself, nor the resultant product free from such undesired accumulations.

SUMMARY OF THE INVENTION

In accordance with the invention, a method is provided for making a mold for casting open tunnels for memory mats consists of applying a first photoresist material to a metallic plate having oppositely disposed major surfaces which are substantially parallel to each other wherein the first step of major surfaces has a first photoresist film applied thereto. The first photoresist film is then exposed to a predetermined line pattern in a first photographic plate and the exposed portion of the first photoresist film is then developed which results in strips of photoresist material on the first major surface of the metallic plate.

Metallic portions of the first major surface of the metallic plate thus exposed, are plated, such plating occurring between the strips of the first photoresist material. The first photoresist material is then stripped off.

A second photoresist material film is then applied to the exposed portions of the first of the major surfaces onto the plated portions thereon. The second photoresist film is then photographically exposed through a

second photographic plate having a pattern with lines therein, the pattern is then developed and the exposed second photoresist film results in removal of a portion thereof that was applied to the portions of the first major surfaces, while retaining the second photoresist material on the surfaces of the plated portions.

The exposed portions of the first major surfaces of the metallic plate are then etched to a predetermined depth thereby forming depressions in such exposed portions for enabling the creation of cavities in the mold. The remaining portions of the second photoresist film are then removed along with the plating, thereby resulting in a series of parallel cavities in the first major surface, such cavities having burred edges. To remove the burred edges the first major surface is flash-etched resulting in the finished mold.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a single metal clad dielectric board.

FIG. 2 is a perspective view of the FIG. 1 embodiment showing conducting metal strips etched in the metal layers.

FIG. 3 is a perspective view of the FIG. 2 embodiment showing dielectric layers over the conducting metal strips to form channels and plated memory wires inserted in the channels between the dielectric strips.

FIG. 4 is a perspective view of the FIG. 3 board showing the channels covered by a single metal clad dielectric board for forming plated wire memory tunnels. The metal layer is on the outside of the single clad board.

FIG. 5 is a perspective view of the FIG. 4 embodiment showing other metal layers etched into conducting strips to form word-straps for the plated wire memory structure. The word straps are interconnected at one edge of the board by through-hole plating.

FIG. 6 is a perspective view of the plated wire memory structure showing two of the FIG. 5 plated wire memory mats separated by an insulating substrate and the connection of the plating memory wires by hairpin terminations at one edge of the structure.

FIG. 7 is a perspective view of an opposite edge of the FIG. 6 plated wire memory showing one embodiment of how the interstitial conductors are interconnected at a common point to form a ground plane for the plated wire memory.

FIG. 8 is a cross-sectional view taken along plane 8-8 of the FIG. 7 structure showing one embodiment of how the word-straps of the plated wire memory are interconnected by through-hole plating techniques.

FIG. 9 is a cross-sectional view of a different embodiment of a plated wire memory having staggered interstitial conductors between plated memory wires.

FIG. 10 is a cross-sectional view of another embodiment of a plated wire memory having dual interstitial conductors between plated memory wires.

FIG. 11 is a perspective view of a block of metal used to make the mold in the first and second exemplary methods of making the mold.

FIG. 12 is a perspective view showing photoresist material strips having been formed on the mold block in accordance with the first and second exemplary methods of making the mold.

FIG. 13 is a cross-section view taken at plane 13-13 of FIG. 12, common to both exemplary methods of making the mold.

FIG. 14 is a cross-section view of the mold as made by the first method, with the photoresist material strips and layers of metallic acid resistant metal layers between the photoresist strips.

FIG. 15 is a cross-section view of the mold as made by the first method, with the photoresist material removed therefrom and with only the metallic acid resistant metal layers remaining.

FIG. 16 is a cross-section view, similar to FIG. 15, except for an overlay film of photoresist material attached to the upper surface of the mold block and the exposed side walls and upper surfaces of the acid resistant metal layers of the partially completed mold by the first method.

FIG. 17 is a view partially in cross-section showing the use of a photographic plate with a predetermined pattern therein positioned on top of the photoresist layer for photographic processing and image transfer by optical or photographic process of the predetermined pattern to portions of the photoresist layer in the partially completed mold by the first method.

FIG. 18 is a cross-section view of the partially completed mold by the first method with the photoresist material between the acid-resistant metal layers removed by a developing solution or by etching.

FIG. 19 is a cross-section view of the partially completed mold by the first method showing the mold block having been etched below its upper surface.

FIG. 20 is a cross-section view of the partially completed mold by the first method showing the photoresist and acid resistant metal strips having been removed and resulting in undesired edges or rough burrs along the length of the troughs etched below the upper mold block surface. This figure also shows a portion of the upper mold block surface including the burred or rough edges to be removed so as to remove the undesired rough edges in the troughs.

FIG. 21 is a cross-section view of the mold block after the layer containing the rough edges in the troughs has been removed.

FIG. 22 is a plan view of the finished mold showing the resulting troughs which become the portion of the mold to make the tunnel walls in the finished product, and also showing the end portions at the troughs which enable the closing of the tunnels during formation or molding of the product so as to make possible keeping these tunnels free of undesired obstructions and contaminants. This view also shows alignment apertures and mold stops. This view is common to the mold made by either the first or the second method.

FIG. 23 is a cross-section view of part of the finished mold taken at plane 23—23 of FIG. 22.

FIG. 24 is a cross-section view of part of the finished mold taken at plane 24—24 of FIG. 22.

FIG. 25 is the next view subsequent to FIG. 13, shown in cross-section, as a step in the process of making the mold by the second method, wherein layers of copper or nickel are provided between the layers of photoresist material.

FIG. 26 is a cross-section view showing the removal of excess copper or nickel layers so that these layers are parallel to the upper and lower surfaces of the mold block and are also parallel to the photoresist layers, used in fabrication of the mold by the second method.

FIG. 27 is a cross-section view showing the removal of the photoresist material between the copper or nickel layers thereby forming the channels between the

layers of copper or nickel to obtain the mold shown in FIGS. 22—24 as the last step in the second method of making such mold.

FIG. 28 is a perspective view partially in cross-section of a portion of the finished mold made by either method and utilized herein for fabrication of the product to achieve trim channels which are those end portions blocking the tunnels of the wire mat so as to prevent contamination and undesired blockage thereof. This mold shows resin material inserted in its cavities.

FIG. 29 is a perspective view showing the mold of FIG. 28 with a laminate of plastic-copper thereover after molding operation is completed.

FIG. 30 is a perspective view showing the product resulting after molding the lower portion of the wire mat, showing the walls formed by the molded resin and providing tunnels therebetween.

FIG. 31 is a perspective view of the product resulting after a second laminate with adhesive binder has been placed over the resin walls of product as shown as FIG. 30 and the second plastic sheet pressed against the top of the walls, and closing off the ends or tunnels of the resin walls as well.

FIG. 32 is a perspective view of the product resulting when the upper and lower copper layers of the laminates are etched into word-straps.

FIG. 33 is the final product after the trim channels or end portions of the plastic layer with its adhesive undercoating has been cut with a razor blade and removed, exposed clean tunnels without contaminants therein ready for insertion of the plated wires, which plated wires are shown inserted therein.

FIG. 34 is a perspective view of one of the plated wires showing an internal magnetic core with an outer plating of electrically conductive material or conversely an internal electrically conductive core plated externally with magnetic material.

EXEMPLARY EMBODIMENTS

PLATED WIRE MATS WITHOUT TRIM CHANNELS

A wire mat product results from the application of a process for forming interstitial conductors separated by tunnels for plated memory wires by initially forming conducting metal strips between plated wire tunnels of a plated wire memory mat on one surface of a dielectric substrate. Dielectric layers are formed over the conducting metal strips to form channels therebetween. The channels are covered by a second dielectric substrate to form tunnels for accommodating plated memory wires.

Word-straps orthogonal to the tunnels are then formed on the outer surfaces of both substrates. The word-straps on both surfaces are interconnected to complete an electrical path around the tunnels.

The conducting metal strips comprising the interstitial conductors are interconnected at a common point to provide electrical continuity between all of the interstitial conductors. Plated memory wires are inserted into the tunnels.

The plated memory wires and the word-straps may be inserted into an electrical connector for providing power, electrical ground connections, input and output signals. The common connection of the interstitial conductors is connected to electrical ground. In one embodiment, a second plated wire memory mat can be produced and placed in registration with the first mat

to increase the capacity of the resulting memory. The mats would be separated by a dielectric substrate. The plated memory wires of both mats would also be connected.

FIG. 1 is a perspective view of a double metal clad dielectric board 1 comprising copper layers 2 and 3 laminated to an epoxy-glass layer 4. As a specific example, the copper layers are 0.0005 inch and the epoxy-glass layer is approximately 0.0025 inches in thickness.

Other metals and dielectric materials can be used in place of copper and epoxy-glass although copper and epoxy-glass are most often used. Nickel on a polyimide layer individually or in combination with an epoxy-glass layer are also usable. As will be indicated subsequently, it is preferred if the dielectric is somewhat flexible. However, the flexibility is not necessary.

The copper layer 2 is masked and etched into parallel copper strips identified generally by the numeral 5 in FIG. 2. As will be described in more detail subsequently the copper strips become interstitial conductors between plated memory wires. Standard photore-sist techniques and etchants such as FeCl_3 can be used to form the copper strips on the layer 4.

In one embodiment, an epoxy resin material is placed in a mold and cast over the copper strips 5 to form resin strips identified generally by the numeral 6 in FIG. 3. The mold is subjected to a temperature and pressure to cause an adherence between the resin and the epoxy-glass substrate 4.

An epoxy resinous material such as polyamide is preferred for forming the strips 6. However, other materials can also be used. For example, epoxy polyols or amine cured epoxies may also be used. The polyamide resin readily adheres to the surface of the epoxy glass layer 4.

The space identified by the numeral 7 between the resin strips 6 comprises channels 8 for accommodating plated memory wires 9. Although the wires 9 are shown in the channels in FIG. 3, in most embodiments, the wires are inserted during the last step of the process. In one example, the plated memory wires may be described as having a beryllium copper core coated by a layer of nickel-iron alloy. The wire may also be coated in an organic insulating layer, if preferred.

Referring to FIG. 4, a single metal clad dielectric board 10 is placed over the top of the FIG. 3-board for sealing channel 8 so that the channels become tunnels 70 for the plated memory wires 9. An adhesive layer 11 is applied to the surface of epoxy-glass layer 12 of board 10. The adhesive layer includes a gelling agent to reduce its flowing characteristics.

An epoxy adhesive or other commercial adhesive may be used on the surface of dielectric layer 12 for achieving adhesion between layer 12 and the top surface of strips 6. A relatively low flow adhesive is preferred in order to prevent contamination of the plated wire memory tunnels. The particular adhesive should be selected in view of the temperatures and pressures to which the board is subjected during the laminating steps of the process. Copper layer 13 is laminated to the outside surface of epoxy-glass layer 12.

After the board 10 has been placed over the channels, the combination of board 10, board 1 and the intervening strips 6 is subjected to heat and pressure for fusing the combination together. Pressures and temperatures necessary to achieve a fusion of the dielectric layers together are known to persons skilled in the art.

For example, pressures of 100psi and temperatures of 350° Fahrenheit may be used to fuse the structure together.

Referring to FIG. 5, it is noted that after the boards have been laminated together as shown in FIG. 4, the outside copper layers 3 and 13 of the resulting structure are masked and etched into word-straps identified generally by the numeral 14. The word-straps 14 are orthogonal to the tunnels for the plated memory wires 9. For convenience the adhesive layer 11 is not shown.

In addition, holes are drilled, either mechanically or chemically, through the word-straps on the upper surface of the FIG. 5 structure, layers 12, 6, 4, and the word-straps 14 on the bottom surface of the FIG. 5 structure. The holes are plated by well-known plating techniques for providing electrical continuity between the word-straps. The holes are identified generally by the numeral 15 and the plated layer on the inside of the holes is identified by the numeral 16. The resulting plated wire memory mat is shown at 17.

It is necessary to electrically connect the word-straps at one edge of the FIG. 5 structure in order to complete an electrical path around the plated memory wires 9. It is pointed out that other techniques may be used to electrically connect the word-straps. Plated through holes are used to illustrate one example of how the electrical connection can be achieved.

In one embodiment of the invention, the copper strips, or interstitial conductors 5 may also be electrically connected at one edge of the board by plating techniques. The dotted line 50 illustrates a plated interconnection between the interstitials.

For example, when the resin strips 6 were molded over the copper strips 5, a recess could have been provided at one edge of the structure. Subsequently, during the through hole plating process, a conductive layer (illustrated by dotted line 50) could have been plated between the strips 5 for interconnecting the interstitials at a common point. The common point is connected to electrical ground during operation to provide a ground plane for the memory mat 17. For that embodiment, it is necessary that an insulating layer be provided over the plated layer between the strips 5 to prevent electrical contact between plated memory wires and the interconnected interstitials. FIG. 7 or 8 show the preferred method and structure for interconnecting the copper strips 5.

In one embodiment the epoxy resin strips 6 are molded over the etched copper strips 5. However, in another embodiment, the FIG. 5 plated wire memory 17 can be produced by molding or otherwise forming, the epoxy resin strips 6 on the surface of epoxy-glass layer 12. After the strips 6 are fused to the epoxy-glass layer 12, the combination is then placed over the strips 5 and laminated together as indicated above, to produce the same structure as shown in FIG. 5. In other words, the resinous strips 6 can be molded to either board 10 or over the copper strips of board 1. When the two boards are assembled together, the resulting structure appears as shown in FIG. 5.

Referring to FIG. 6, and notwithstanding that in FIG. 5 plated wire memory mat 17 can be used, in some cases it is preferred to increase the capacity of the plated wire memory by adding an additional plated wire memory mat 17'. The new combination of wire mats is comprised of plated wire memory 17 and plated wire memory mat 17', separated by substrate 19. The

substrate 19 may be an epoxy-glass layer. The plated wire memory mat 17' is formed in a manner similar to that indicated for the formation of the FIG. 5 plated wire memory mat 17. The two plated wire memory mats 17 and 17' are placed on the surfaces of substrate 19 so that the word-straps 14 and 20 of mats 17 and 17' respectively are in registration. The plated memory wires 9 and 21 of the respective mats are also in registration, and are shown inserted in their respective channels 75 and 76. The plated memory wires of the mats are interconnected by the hairpin interconnectors 22. The hairpins may be connected to the plated memory wires inside the tunnels by soldering, welding, etc. In the preferred embodiment, the plated wires may be formed in the configuration shown and inserted into the tunnel structure without the necessity for welding the hairpin connectors 22. The interstitials are not shown in FIG. 6 since in the usual case the resinous material covers the ends of the interstitials on the side of the structure. Epoxy layer 12 is the same as in FIG. 5, and epoxy layer 12' is the same as epoxy layer 12. Epoxy resin strips 6 are the same as in FIG. 5.

After the plated wire memory mats 17 and 17' have been assembled on the substrate 19, the entire assembly is fused together. Heat and pressure are applied so that the structures fuse to each other. A temperature of, for example, 200° F and a pressure of, for example, 100psi may be used to fuse the structure together. An adhesive layer (not shown) may also be applied to the top surface of the word-straps which contact the surfaces of substrate 19. Alternately, the structures may be fused together at room temperature by the use of pressure alone.

Referring to FIGS. 7 and 8, the preferred interconnection of the interstitial conductors 5 of plated wire memory mat 17 and interstitial conductor 23 of plated wire memory mat 18 are shown at common connections. The common connection for mats 17 and 18 are plates 24 and 25 respectively. As shown in FIGS. 7 and 8 the interstitial conductors 5 for plated wire memory mat 17 and the interstitial conductors 23 for the plated memory wire mat 18 are formed with protruding plate 24 and 25 respectively. The substrates 4 and 26 each have a portion which extends under the plates 24 and 25.

It is preferred if the substrates 4 and 25 are relatively flexible for enabling the extended portions to be easily folded back on top of the outside surfaces of the memory mats 17 and 18 respectively. In order to maintain a relatively planar surface on both sides of the memory, it is preferred if plate 24 and the thickness of the folded portion of substrate 4 are equal to the thickness of the word-straps 14. The same characteristics are also preferred for plate 25 and substrate 26 relatively to word-straps 20. However, it should be pointed out that the planar characteristics are not necessary. As a result, the plates may be secured to the top surfaces of the plated wire memory without the necessity for folding back a portion of the substrate 4, and similarly for substrate 26. Epoxy layers 12 and 12' serve the same purpose as in FIG. 6, and epoxy resin strips 6 for embedding interstitial conductors are the same as in FIG. 5.

In addition, the interconnection of the interstitials at the common point represented by the plates may be achieved by electrodeposition techniques without necessity for etching the plates. The folded over technique is used to illustrate one example of a method for

interconnecting the interstitials at a common point and for securing that common point to a plate which is usable as a ground plane for the interstitials. The folded portions may be secured to the outer surfaces by an adhesive with or without heat and pressure. The adhesive layers are identified by the numerals 51 and 52.

In operation, the word-straps 14 in FIGS. 5 and 6, word-straps 14 and 20 in FIGS. 7 and 8, word-straps 32 in FIG. 9 and word-straps 40 in FIG. 10 receive input and output signals as appropriate for operating the structure as a plated wire memory. The plates 24 and 25 are connected to electrical ground. Ordinarily, the word-straps and plated memory wires as well as the plates 24 and 25 are provided with connector terminations which insert into receptacles (not shown). Since such structure is well-known to persons skilled in the art the details are not shown in FIG. 7.

FIG. 8 is a cross-sectional view taken along plane 8—8 of the FIG. 7 plated wire memory 18 showing the interconnection of the word-straps of both plated wire memory mats. As shown in FIG. 8, plated through hole 15 including plated copper layer 16 interconnects the word-straps 14 of plated wire memory mat 17. Substrate 19 is shown separating the two plated wire memory mats. Plated through hole 27 with copper layer 28 interconnects the word-straps 20 of plated wire memory mat 18. Plated memory wires 9 and 21 are also shown.

FIG. 9 is an illustration of a different embodiment of the FIG. 5 plated wire memory mat 17. The embodiment is designated at 29. Plated memory wires 30 are shown in tunnels 31. Word-straps 32 on both surfaces of the structure are orthogonal to the plated memory wires 30. The word-straps are secured to dielectric substrates 33 and 34. The resinous strips 35 form the walls of the tunnels 31 for housing the plated wires 30. Dielectric or epoxy-glass layer 33 has adhesive coating 37 thereon for attaching to resinous strips 35.

The difference between the FIG. 9 and FIG. 5 structures is the position of the interstitial conductors 36. As indicated by FIG. 9, the interstitials are formed alternately on substrate 33 and on substrate 34 such that every other interstitial conductor is in a different plane. Adhesive layer 37 is shown securing substrate 33 to the tops of resinous strips 35.

FIG. 10 is also a different embodiment of the plated wire memory mat shown in FIG. 5. The FIG. 10 plated memory mat 38 is comprised of lower substrate 39 on which word-straps 40 are formed and upper substrate 41 which also includes word-straps 40.

Upper substrate 41 is fused to the top surface of resinous strips 42 by the adhesive layer 46. Interstitial conductors 43 are shown disposed on the inner surface of substrate 41 and on the inner surface of substrate 39. As a result, parallel interstitial conductors 43 exist between each of the tunnels 44 for the plated memory wires 45. The process details for forming the FIG. 10 embodiment are substantially the same as the process details described in connection with the previous embodiments.

In operation, information is written into a selected memory bit location along a plated memory wire by passing a current down a selected word-strap in coincidence with a bit current being passed down a plated memory wire. The polarity of the bit current determines whether a logic "1" and/or a logic "0" is written at the intersection of the word-strap and the plated

wire. The interstitials prevent the electrical field in one plated wire from causing information to be written into the adjacent bit portions on either side of the selected plated wire, carried by other adjacent wires.

It would be possible to avoid the interference between plated memory wires by extending the distance between the wires. However, it is preferred to have an increased storage capacity without increasing the size of the plated wire memory. This relatively increases the capacity without the necessity for increasing the size of the plated wire memory mat.

It is pointed out that operatively, the use of the wires in the tunnels may be structured in the form of iron coated or magnetically coated copper wire, or conversely may be wire of an iron core center with copper plated on its exterior. In using the assemblies above described as a memory device, two conditions of writing and reading need be considered, and the sense of, or polarities of the pulses constituting the currents in the word-straps and in the plated wires in the tunnels. For writing, the word-strap pulse polarities will always be positive as contemplated, and for reading, these pulses will either be positive or be absent. The wire pulse polarities will be either positive or negative in writing usage, and in reading usage will not have any pulses at all. Therefore, the resultant logic obtained can be seen from the following table:

Writing Condition		
Pulse Polarity On Wires positive(+) negative(-)	Pulse Polarity On Word-Straps positive (+) positive (+)	Logic Result 1 0
Reading Condition		
Pulse Polarity On Wires none used none used	Pulse Polarity On Word-Straps positive (+) no current	Logic Result 1 0

In order to bring out the novel features of this invention, FIGS. 11-32 can be shown to illustrate the inventive concept mold, process for making the mold, and product made, which figures differ from FIGS. 1-5 in that a trim channel is provided in the product to be hereinafter described in terms of the product itself, in the process for making the product, and in the mold used in the process for making the product. Similar structures to that shown in FIGS. 1-5, and also applying to the more complex version of interstitial mats, are shown in FIGS. 6-10, but with the added feature of providing ready access to the channels, such as channels 70 of FIG. 5, channels 75 and 76 of FIGS. 6, 7 and 8, channels 31 of FIG. 9 and channels 44 of FIG. 10.

FIRST EXEMPLARY METHOD OF MAKING THE MOLD FOR CASTING OPEN TUNNELS FOR PLATED WIRE MATS

Referring to FIGS. 11-24, in the fabrication of cast resin plated wire mat structures, a mold as shown at 109 is required. The mold is conventionally made by machining steel. This is a very expensive method for providing tooling. An inexpensive method for producing this tool is achieved by chemically etching the required configuration in a brass or other metal body 110. This method is permissive of enabling several molds to be made of one configuration or different configurations depending upon the requirement, at relatively low cost.

The method for making the mold is described as follows:

Step 1: Surfaces of a 0.5 inch thick brass plate 110 is ground so that both major surfaces 111 and 111' are parallel, and have a minimum of a 20 microinch finish, as shown in FIG. 11.

Step 2: Apply photoresist film and expose a positive pattern from a photographic plate of lines on pre-established centers A such as 0.025 inches, each line having a width, B of 0.012 inches and develop photographically the exposed image, resulting in strips of photoresist material 112, as shown in FIG. 12 and in its cross-section view FIG. 13.

Step 3: Plate the exposed brass surfaces with an acid resistant metal 113, such as solder plate, as shown in FIG. 14.

Step 4: Strip photoresist 112 in methylethylketone solvent, the result being shown in FIG. 15.

Step 5: Apply photoresist film 114 to surfaces of solder plate 113 and brass surface 111, as shown in FIG. 16.

Step 6: Expose the photoresist film 114 to a negative pattern of lines in a photographic plate 115 and develop the image so that the solder plated surfaces are protected, as shown first in FIG. 17 and then in FIG. 18.

Step 7: As shown in FIG. 18, etch the uncoated area of brass 111 to a predetermined depth of at least 0.002 inches, usual depths varying between 0.004-0.009 inches, in a solution of chromic-sulfuric acid which will not etch the solder 113. This acid solution consists of chromic acid of 50-200 grams/liter and sulfuric acid of 50-200 milliliters per liter. The depressions 116 formed in this manner are rounded and provide a casting with a rounder surface. This is most suitable for subsequent processing; such depressions are shown in FIG. 19.

Step 8: Remove photoresist 114 in a methylethylketone solution and strip solder 113 in a solution of fluoroboric acid of 30-50 percent by volume and hydrogen peroxide of 7-10 percent by volume, the effect shown in FIG. 20, which results in undesired edges 117.

Step 9: Flash etch in chromic sulfuric acid, the surface 111 approximately 0.001 to remove "metal overhangs" left on the walls due to the undercutting action of the etchant, which removes the 0.001 inch thickness designated as 118 in FIG. 20, resulting in clean surface 119 shown in FIG. 21.

The Finished Mold: The mold at 109 as shown in plan view FIG. 22 and in its cross-section view FIG. 23 taken along plane 23-23 of FIG. 22 and another cross-section view FIG. 24 taken along plane 24-24 of FIG. 22 which view is in a plane perpendicular to the view of FIG. 23, depicts the finished product in the form of a mold used to make the plated wire memory mats or retainer shown in FIGS. 1-5, but may also be used to fabricate the more complex configuration of wire mat represented by FIGS. 6-10.

Here, there is shown the finished mold at 109 resulting from the process of making the mold, above described, having raised walls 120 and mold channels 121 between walls 120, the channels 121 and mold walls 120 terminating at either end in raised strips 122 so that in the molding process such strips will form ends that can be removed to expose molded tunnels formed

to enable wires to be inserted in the formed tunnels. Mold tabs 123 are provided for enabling the uniform casting of resin in the final product made by this mold, and mold alignment holes 124 are provided to align the mold so that the word-straps 14 of the product shown in FIG. 5 are aligned perpendicular to tunnels 70 as shown in FIG. 5, or similarly for tunnels 75 and 76 in FIGS. 6, 7, and 8, tunnels 31 in FIG. 9 and tunnels 44 in FIG. 10.

SECOND EXEMPLARY METHOD OF MAKING THE MOLD FOR CASTING OPEN TUNNELS FOR PLATED WIRE MATS

In the fabrication of cast resin plated wire mat structures a mold is required. The mold is conventionally made by machining steel. This is a very expensive method for providing tooling. In addition, the center to center locations C of mold channels similar to mold channels 121 of FIGS. 22 and 24, are 0.020 inches. This is very difficult to achieve by machining and therefore the resultant product is even more expensive using conventional methods. A satisfactory tool can be made by electrochemical deposition of the required configuration on a brass plate or other metal plate through the use of a photosensitive material. Such mold made by this process will result in the configuration shown in FIGS. 22-24.

The method for making such a mold, is as follows:

Step 1: A $\frac{1}{2}$ inch thick brass plate 110 is ground so that both surfaces 111 and 111' are parallel and a minimum of a 20 microinch finish is provided. This is shown at FIG. 11.

Step 2: Apply 0.010 inch thick film illustrated by dimension D of photosensitive material 112, such heights may also be as low as 0.002 inches, and expose a positive or negative pattern of a photographic plate of lines in pre-established center to center dimension A such as 0.020 inches, each line having a width B, which is at least 0.002 inches and typically being of 0.012 inches and develop photographically the exposed image, which results in FIG. 12 and cross-section thereof shown as FIG. 13.

Step 3: Electroplate as shown in FIG. 25, the non-exposed grooves 111 resulting in layers 130 therein of a thickness E greater than 0.010 inches; layers 130 being a metal such as copper or nickel.

Step 4: Machine the plated layers 130 parallel to the base surface 111' and to a height 0.008 inches, the upper surfaces of resulting layers 130' after machining, being parallel to the upper and exposed surfaces of layers 112, as shown in FIG. 26.

Step 5: Remove photoresist material 112 previously shown in FIG. 26, using a solvent such as dichloromethane, resulting in FIG. 27.

The Finished Mold: The mold at 109 as shown in plan view FIG. 22 and in its cross-section view FIG. 23 taken along plane 23-23 of FIG. 22 and another cross-section view FIG. 24 taken along plane 24-24 of FIG. 22 which view is in a plane perpendicular to the view of FIG. 23, depicts the finished product in the form of a mold used to make the plated wire memory mats or retainer shown in FIGS. 1-5, but may also be used to fabricate the more complex configuration of wire mat represented by FIGS. 6-10.

Here, there is shown the finished mold at 109 resulting from the process of making the mold, above de-

scribed, having raised walls 120 and mold channels 121 between walls 120, the channels 121 and mold walls 120 terminating at either end in raised strips 122 so that in the molding process such strips will form ends that can be removed to expose molded tunnels formed to enable wires to be inserted in the formed tunnels. Mold tabs 123 are provided for enabling the uniform casting of resin in the final product made by this mold, and mold alignment holes 124 are provided to align the mold so that the word-straps 14 of the product shown in FIG. 5 are aligned perpendicular to tunnels 70 as shown in FIG. 5, or similarly for tunnels 75 and 76 in FIGS. 6, 7 and 8, tunnels 31 in FIG. 9 and tunnels 44 in FIG. 10.

PLATED WIRE MATS WITH TRIM CHANNELS DESCRIBING METHOD OF PRODUCING AND PRODUCT BEING PRODUCED

Having described in connection with FIGS. 1-10 the wire mats that do not have the benefit of being fabricated by the use of trim channels, and having described two molds and methods for making such molds in connection with FIGS. 11-27 to enable these wire mats to have trim channels at two ends thereof, the following description is addressed to the method of casting open tunnels with trim channels for such plated wire mats.

Conventionally, cutting tunnels for plated wire loading results in contamination of tunnels and makes wire insertion therein troublesome. This problem is resolved by designing and fabricating a cast resin parallel set of tunnels which have trim channels at both ends of the set of tunnels by use of the aforescribed molds. This is achieved as follows:

Step 1: Starting with the mold as above described but also shown in FIG. 28 in perspective view, the cavities formed by portions 120 and 122 are loaded with resin material 140.

Step 2: The mold is then covered with a laminate consisting of a plastic material 151 such as an epoxy-glass which is prelaminate to a copper layer 152. The mold with the laminate as shown in FIG. 29 are inserted in a molding press which heats the mold to the required temperature to cause resin material 140 to flow and then cool and set. The result obtained when the laminate 151-152 is removed from the mold is shown in FIG. 30 wherein it is obvious that the resin 140 has set to the shape of the cavities in the mold forming rectangular bar-like parallel walls 150 of the set resin which are attached to the free major surface of the plastic material 151, and forming channel 175 between walls 150.

Step 3: Laminate consisting of plastic material 162 attached to copper sheet 161 is then positioned over the wall portions 150 as shown in FIG. 30. One surface of plastic material 162 has an adhesive material 163 attached hereto which is used to make contact with wall portions 150. The laminate 161-162-163 together with the assembly as shown in FIG. 30 is inserted into a press which by pressure and the effect of the adhesive material 163 causes walls 150 to be attached and adhere to plastic material 162, walls 150 embedding themselves into plastic material 162 so that plastic material 162 completely covers the openings to tunnels 175 at both ends of such tunnels. This is shown in FIG. 31.

Step 4: The configuration of FIG. 31 will therefore have a lower copper plate 152 and an upper copper plate 161. Word-straps as shown in FIG. 32, consisting of copper straps 152' and 161' are etched by etching plates 152 and 162 with suitable protective masks in an acid solution such as chromic-sulfuric acid, and are made in a similar manner as word-straps were made in conjunction with word-straps 14 of FIGS. 5, 6, 7, 8 or word-straps 32 of FIG. 9 or word-straps 40 of FIG. 10. As a result, the closing of ends of the tunnels by plastic material 162 and its corresponding adhesive 163 at the ends of the tunnels, such portions forming there are designated as 162' for the plastic material and 163' for the adhesive portion. Portions 162'-163' necessarily need to be removed in order to expose tunnels 175.

Step 5: Referring to FIG. 32, a razor blade or sharp knife is run along line 176 deep enough to sever portions 162'-163' at either end of the molded product. Portions 162'-163' can then be easily peeled-off and lifted from such assembly exposing at both ends openings to tunnels 175 to permit easy insertion of wires 180 therein. Such wires as inserted in tunnels which openings have been freed by removal of strips 162'-163' are shown in FIG. 33. Details for connection of word-straps used in connection with these mats, and manner in which wires 180 are used have been described in detail in connection with FIGS. 3-10, above, and need not be repeated here. Upon removal of strips 162'-163', area of plastic material 151 becomes larger by an area as at 170 as compared with the area of plastic material 162. As shown in FIG. 34, wire 180 may comprise a magnetic core 181 with an outer plating layer 182 of electrically conductive material for preventing attenuation of fast pulses which generally behave in a skin-effect manner, the conductive current at the outer surface of the wire, or the core represented by 181 may be of conventional copper wire with an outer plating represented by 182 of magnetizable material.

It should be noted that the FIGS. 30-33 representing the product, with trim channel portion 162' are formed by the exertion of pressure of the press used to cause adhesion of the plastic material to the upper edges of molded walls 150 and to the ends of these walls, since it must be remembered that these figures represent only a portion of the laminate materials used, additional portions of such plastic material 162 and its adhesive undercoating 163 extending beyond the tunnel area are now shown in these drawings. Therefore, such abundance of material overlaps the ends of the molded walls when pressure is exerted by the forming press, but inasmuch as this plastic material does not flow too readily, and the width or distance between two parallel walls 150 is extremely small, there is very little material on top of the walls 150 to fill in the tunnels 175. It must be remembered that the widths in question across tunnels 175 are only several mils wide.

We claim:

1. A method for making a mold, comprising the steps of:

- applying a first photoresist film to one surface of a metallic plate;
- exposing said first photoresist film through a predetermined line pattern;
- developing the exposed first photoresist film;
- removing the unexposed portions of said first photoresist film thereby to produce strips of photoresist material on said one surface of said metallic plate;
- plating said one surface of said metallic plate which is exposed between the strips of said first photoresist material with an acid resistant metal; stripping the first photoresist material from said one surface of said metallic plate;
- applying a second photoresist film to said one surface of said metallic plate including the exposed portions thereof and the plated portions thereon;
- exposing said second photoresist film through a second predetermined line pattern;
- developing the exposed second photoresist film;
- removing the unexposed portions of said first photoresist film thereby to remove that portion of said second photoresist film that was applied to said one surface of said metallic plate while retaining said second photoresist material on the surfaces of the plated portions;
- etching the exposed portions of said one surface with an acid which attacks the material of said metallic plate but not the plated portion thereby forming depressions in said one surface;
- removing the remaining portions of said second photoresist film and said acid resistant metal thereby resulting in a plurality of cavities in said one surface, and
- flash etching the first major surface of the mold to thereby remove burred edges, if any, thereby resulting in the finished mold.
2. The invention as stated in claim 1, wherein: the depth of etching the exposed portions of the first of said major surfaces being at least 0.002 inches.
3. The invention as stated in claim 1, wherein: the etched depressions in the exposed portions of the first of said major surfaces are arc-shaped.
4. The invention as stated in claim 1, wherein: said metallic plate is brass.
5. The invention as stated in claim 1, wherein: the step of plating is accomplished by applying solder on the exposed surface of said metallic plate.
6. The invention as stated in claim 1, wherein: methylethylketone compound is used for stripping the first photoresist material.
7. The invention as stated in claim 1, wherein: the step of etching is accomplished by applying chromic sulfuric acid to said metallic plate.
8. The invention as stated in claim 1, wherein: the step of removing the remaining portion of said second photoresist material is accomplished by the use of methylethylketone and the plated material is removed by the use of a fluoroboric acid and hydrogen peroxide mixture.
9. The invention as stated in claim 1, wherein: the step of flash etching is accomplished by the use of chromic sulfuric acid.

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