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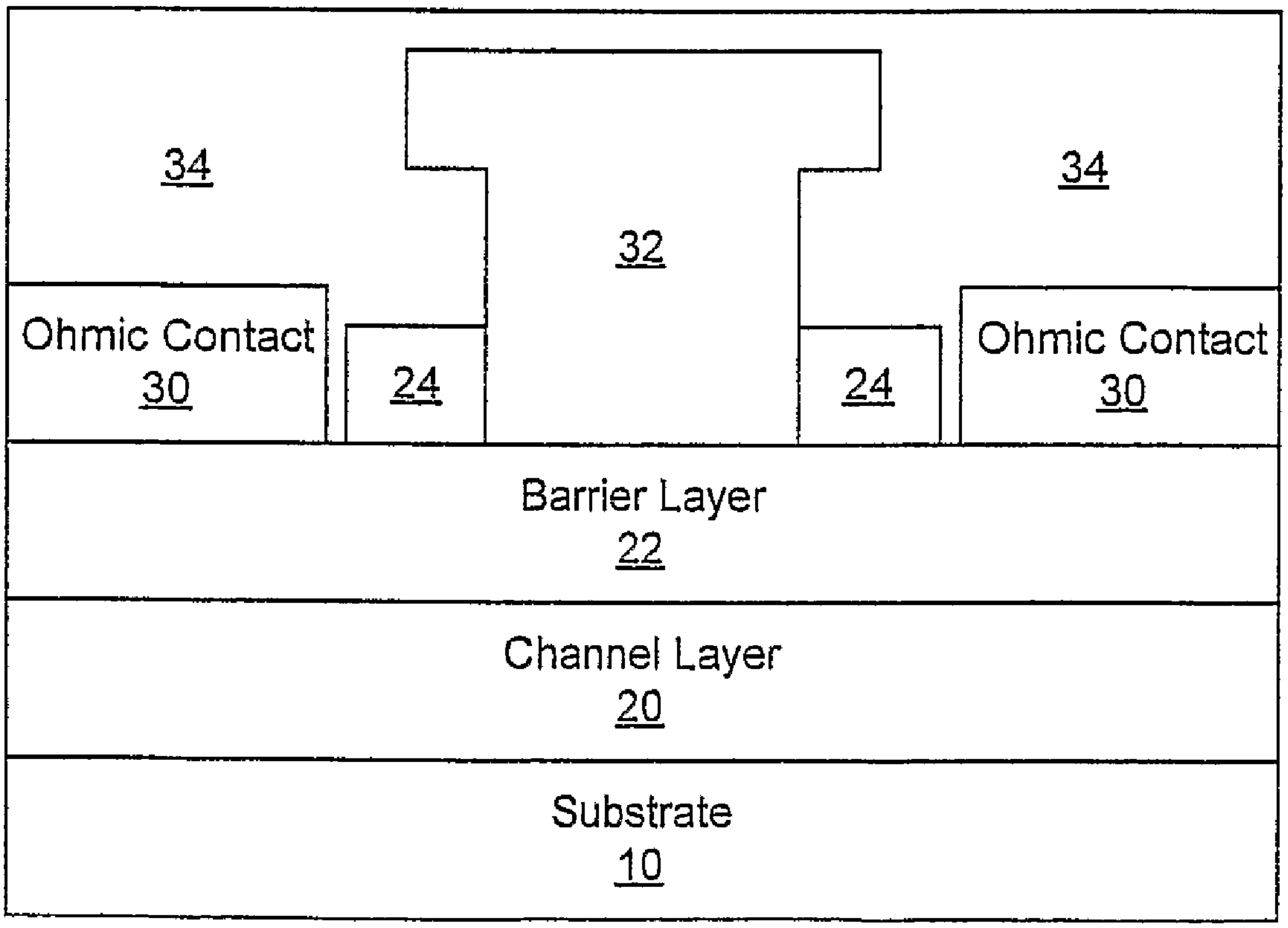
(54) Titre : TRANSISTORS A BASE DE NITRURE POURVUS D'UNE COUCHE PROTECTRICE ET D'UN EVIDEMENT FORME SANS TROP DE DOMMAGE, ET LEURS PROCEDES DE FABRICATION
(54) Title: NITRIDE-BASED TRANSISTORS WITH A PROTECTIVE LAYER AND A LOW-DAMAGE RECESS AND METHODS OF FABRICATION THEREOF



(57) Abrégé/Abstract:
Transistors are fabricated by forming a nitride-based semiconductor barrier layer on a nitride-based semiconductor channel layer and forming a protective layer on a gate region of the nitride-based semiconductor barrier layer. Patterned ohmic contact metal regions are formed on the barrier layer and annealed to provide first and second ohmic contacts. The annealing is carried out with

(57) **Abrégé(suite)/Abstract(continued):**
the protective layer on the gate region. A gate contact is also formed on the gate region of the barrier layer. Transistors having protective layer in the gate region are also provided as are transistors having a barrier layer with a sheet resistance substantially the same as an as-grown sheet resistance of the barrier layer.

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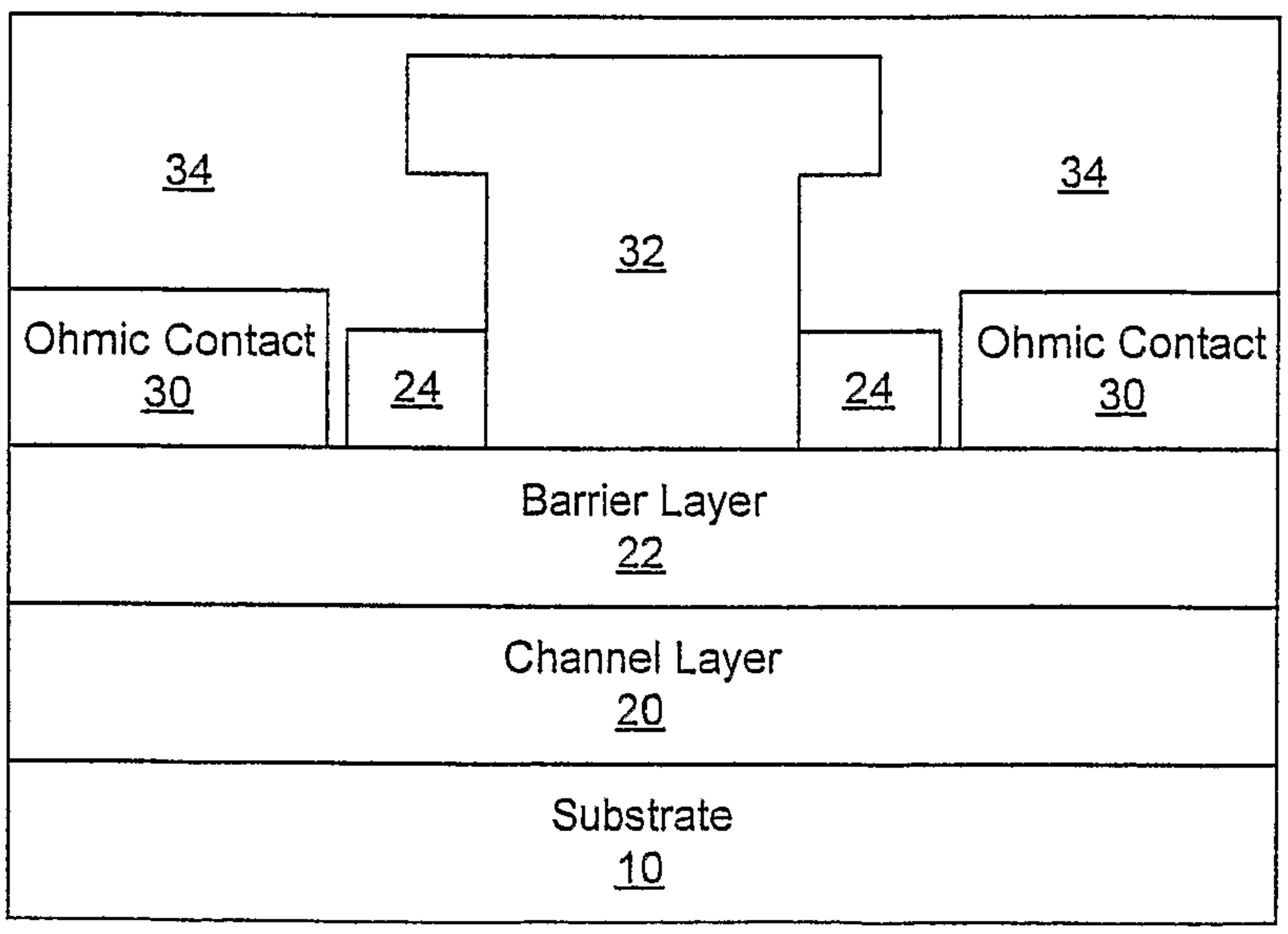

(57) Abstract: Transistors are fabricated by forming a nitride-based semiconductor barrier layer on a nitride-based semiconductor channel layer and forming a protective layer on a gate region of the nitride-based semiconductor barrier layer. Patterned ohmic contact metal regions are formed on the barrier layer and annealed to provide first and second ohmic contacts. The annealing is carried out with the protective layer on the gate region. A gate contact is also formed on the gate region of the barrier layer. Transistors having protective layer in the gate region are also provided as are transistors having a barrier layer with a sheet resistance substantially the same as an as-grown sheet resistance of the barrier layer.

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NITRIDE-BASED TRANSISTORS WITH A PROTECTIVE LAYER AND A LOW-DAMAGE RECESS AND METHODS OF FABRICATION THEREOF

STATEMENT OF GOVERNMENT INTEREST

This invention was made with Government support. The Government has certain rights in this invention.

FIELD OF THE INVENTION

The present invention relates to semiconductor devices and, more particularly, to transistors that incorporate nitride-based active layers.

BACKGROUND

Materials such as silicon (Si) and gallium arsenide (GaAs) have found wide application in semiconductor devices for lower power and (in the case of Si) lower frequency applications. These, more familiar, semiconductor materials may not be well suited for higher power and/or high frequency applications, however, because of their relatively small bandgaps (*e.g.*, 1.12 eV for Si and 1.42 for GaAs at room temperature) and/or relatively small breakdown voltages.

In light of the difficulties presented by Si and GaAs, interest in high power, high temperature and/or high frequency applications and devices has turned to wide bandgap semiconductor materials such as silicon carbide (2.996 eV for alpha SiC at room temperature) and the Group III nitrides (*e.g.*, 3.36 eV for GaN at room temperature). These materials, typically, have higher electric field breakdown strengths and higher electron saturation velocities as compared to gallium arsenide and silicon.

A device of particular interest for high power and/or high frequency applications is the High Electron Mobility Transistor (HEMT), which is also known as a modulation doped field effect transistor (MODFET). These devices may offer operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher doped"), smaller bandgap material and can contain a very high sheet electron concentration in excess of, for example, 10^{13} carriers/cm^2. Additionally, electrons that originate in the wider-bandgap semiconductor transfer to the 2DEG, allowing a high electron mobility due to reduced ionized impurity scattering.

This combination of high carrier concentration and high carrier mobility can give the HEMT a very large transconductance and may provide a strong performance advantage over metal-semiconductor field effect transistors (MESFETs) for high-frequency applications.

High electron mobility transistors fabricated in the gallium nitride/aluminum gallium nitride (GaN/AlGaN) material system have the potential to generate large amounts of RF power because of the combination of material characteristics that includes the aforementioned high breakdown fields, their wide bandgaps, large conduction band offset, and/or high saturated electron drift velocity. A major portion of the electrons in the 2DEG is attributed to polarization in the AlGaN. HEMTs in the GaN/AlGaN system have already been demonstrated. U.S. Patents 5,192,987 and 5,296,395 describe AlGaN/GaN HEMT structures and methods of manufacture. U.S. Patent No. 6,316,793, to Sheppard et al., which is commonly assigned and is incorporated herein by reference, describes a HEMT device having a semi-insulating silicon carbide substrate, an aluminum nitride buffer layer on the substrate, an insulating gallium nitride layer on the buffer layer, an aluminum gallium nitride barrier layer on the gallium nitride layer, and a passivation layer on the aluminum gallium nitride active structure.

One step in the fabrication of nitride-based transistors is the formation of ohmic contacts for such transistors. The formation of ohmic contacts has, typically, required high annealing temperatures (*e.g.* 900 °C). Such high annealing temperatures may damage the materials and/or the device.

For example, in conventional devices utilizing high annealing temperatures when forming ohmic contacts, the sheet resistance of a gate region (defined as the active device region between the two contacts) of AlGaN and/or GaN layers typically increases in comparison to sheet resistances of the AlGaN and/or GaN layers as-grown. Such an increase in sheet resistance is believed to detrimentally affect the device.

Embodiments of the present invention provide for fabricating a transistor by forming a nitride-based semiconductor barrier layer on a nitride-based semiconductor channel layer and forming a protective layer on a gate region of the nitride-based semiconductor barrier layer. Patterned ohmic contact metal regions are formed on the barrier layer and annealed to provide first and second ohmic contacts. The annealing is carried out with the protective layer on the gate region. A gate contact is also formed on the gate region (*e.g.*, the active device region between the first and second ohmic contacts) of the barrier layer.

In further embodiments of the present invention, the protective layer is removed subsequent to annealing the patterned ohmic contact metal. The protective layer may be an aluminum nitride layer. The protective layer may be removed utilizing a low damage etching technique. For example, the low damage etching technique may include wet removal with a strong base, such as KOH. After removing the protective layer a passivation layer may be formed on exposed portions of the barrier layer. In these embodiments, the gate contact may be formed by etching a recess in the passivation layer utilizing a low damage etch technique to expose a portion of the gate region of the barrier layer and forming the gate contact in the recess in the passivation layer.

In additional embodiments of the present invention, the passivation layer is formed on exposed portions of the barrier layer and the protective layer. In these embodiments, the gate contact may be provided by forming a gate contact that extends through the passivation layer and the protective layer to contact the barrier layer.

In yet other embodiments of the present invention, forming a protective layer includes forming a patterned protective layer on the barrier layer. The patterned protective layer covers a first portion of the barrier layer corresponding to the gate region and exposes adjacent second portions of the barrier layer corresponding to the first and second ohmic contacts. The patterned ohmic contact metal regions are provided by forming patterned ohmic contact metal regions on the second portions of the barrier layer. The patterned ohmic contact metal regions are adjacent and spaced apart from the patterned protective layer.

In still further embodiments of the present invention, forming the patterned protective layer includes blanket depositing a protective layer material on the barrier material, the mask having windows corresponding to locations of the first and second ohmic contacts, etching the blanket-deposited protective layer through the windows utilizing a low damage etching technique and removing the mask. The windows corresponding to locations of the first and second ohmic contacts may be larger than an area of the first and second ohmic contacts. The low damage etching technique may be one or more of RIE, ECR, downstream plasma and/or ICP using CF_4/O_2, NF_3/O_2 and/or other fluorinated species.

Forming the gate contact may include etching a recess in the patterned protective layer that exposes a portion of the first portion of the barrier layer and depositing a gate contact in the recess. Forming a recess may include forming a mask on the patterned protective layer, the mask having a window corresponding to location of the recess, etching the patterned protective layer through the window utilizing a low damage etching technique and removing the mask. The low damage etching technique utilized to etch the patterned protective layer may include RIE, ECR, downstream plasma and/or ICP using CF_4/O_2, NF_3/O_2 and/or other fluorinated species.

In particular embodiments of the present invention, the protective layer includes SiN, AlN and/or SiO_2. The SiN, AlN and/or SiO_2 may be non-stoichiometric and can have compressive or tensile strain. The protective layer may be deposited using physical vapor deposition (PVD) and/or chemical vapor deposition (CVD).

In yet additional embodiments of the present invention, a passivation layer is formed on the patterned protective layer so as to substantially fill gaps between the patterned protective layer and the first and second ohmic contacts. The patterned protective layer and the passivation layer may be the same or different materials. For example, the patterned protective layer may be aluminum nitride and the passivation layer may be silicon nitride. Alternatively, the patterned protective layer and the passivation layer may be silicon nitride.

In still other embodiments of the present invention, the patterned protective layer is removed so as to expose the first portion of the barrier layer. Removing the patterned protective layer may be followed by forming a passivation layer on exposed portions of the barrier layer. In such embodiments, the patterned protective layer may be aluminum nitride and the passivation layer may be silicon nitride.

is preceded by forming the passivation layer. The gate contact is provided by forming a recess in the passivation layer that exposes a portion of the first portion of the barrier layer and forming a gate contact in the recess. Forming the recess may include forming a mask on the passivation layer. The mask has a window corresponding to location of the recess. The passivation layer is etched through the window utilizing a low damage etching technique and the mask is then removed.

In particular embodiments of the present invention, the nitride-based channel layer and the nitride-based semiconductor barrier layer are Group III-nitride layers. For example, the channel layer may have a composition of $Al_xGa_{1-x}N$ wherein $0 \leq x < 1$, where the bandgap of the channel layer is less than the bandgap of the barrier layer. The channel layer could also be aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN) and the barrier layer could be aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN. The barrier layer and/or the channel layer may be multiple layers. A buffer layer may also be formed on a substrate and the channel layer formed on the buffer layer to provide the nitride-based channel layer. The channel layer and the barrier layer may be configured to provide a High Electron Mobility Transistor (HEMT). The nitride-based channel layer may be provided on a SiC substrate.

In still further embodiments of the present invention, the formation of the gate contact is preceded by the formation of a passivation layer. The formation of the gate contact the includes forming a recess in the passivation layer and the patterned protective layer that exposes a portion of the first portion of the barrier layer and forming a gate contact in the recess.

In particular embodiments of the present invention, the protective layer is formed to a thickness of at least about a thickness of the ohmic contact material. The protective layer may also have a thickness of at least about two monolayers. In particular, the protective layer may have a thickness of from about 1 nm to about 500 nm.

In yet other embodiments of the present invention, a high electron mobility transistor includes a nitride-based channel layer on a substrate and a nitride-based semiconductor barrier layer on the nitride-based channel layer. The channel of that is substantially the same as an as-grown sheet resistance of the nitride-based HEMT channel. Ohmic contacts and a gate contact are provided on the barrier layer.

The high electron mobility transistor may further include a protective layer disposed on the barrier layer that is adjacent and spaced apart from the ohmic contacts and that the gate contact extends through. A passivation layer may also be provided on the protective layer and that substantially fills a gap between the ohmic contacts and the protective layer. The passivation layer may also be on the protective layer and the gate contact may extend through the protective layer and the passivation layer. The gate contact may be also be provided directly on the protective layer. The passivation layer on the barrier layer may substantially fill a gap between the ohmic contacts and the gate contact.

In particular embodiments of the present invention, the nitride-based channel layer and the nitride-based semiconductor barrier layer each include a Group III-nitride layer. The channel layer may have a lower bandgap than the barrier layer. The channel layer may include an undoped layer having a thickness of greater than about 20 Å. The channel layer may also include a superlattice and/or a combination of Group III-nitride layers. The channel layer may include aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN). The barrier layer may include aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN. For example, the barrier layer may include $Al_xGa_{1-x}N$ wherein $0 < x < 1$. The barrier layer may include multiple layers. A buffer layer may also be provided on the substrate, where the nitride-based channel layer is disposed on the buffer layer.

In still further embodiments of the present invention, the protective layer has a thickness of at least about a thickness of the ohmic contacts. The ohmic contacts may also have a contact resistance of less than about 1 Ω-mm.

In yet other embodiments of the present invention, a high electron mobility transistor includes a nitride-based channel layer on a substrate, a nitride-based semiconductor barrier layer on the nitride-based channel layer, a protective layer on the barrier layer, ohmic contacts on the barrier layer, adjacent and spaced apart from the protective layer so as to provide a gap between the ohmic contacts and the protective layer and a gate contact on the barrier layer and extending through the that substantially fills the gap between the ohmic contacts and the protective layer.

In still further embodiments of the present invention, fabrication of a transistor includes forming a nitride-based semiconductor barrier layer on a nitride-based semiconductor channel layer and forming a protective layer on a gate region of the nitride-based semiconductor barrier layer. Patterned ohmic contact metal regions are formed on the barrier layer. The patterned ohmic contact metal is annealed to provide first and second ohmic contacts, for example, source and drain contacts. A recess is etched in the protective layer in a gate region of the barrier layer utilizing a low damage etch technique to expose a portion of the gate region of the barrier layer. The gate contact is formed in the recess in the passivation layer.

In particular embodiments of the present invention, the protective layer comprises a passivation layer. The protective layer may, for example, be an aluminum nitride layer, a silicon nitride layer and/or a silicon dioxide layer or layers. The low damage etching technique may be a wet etch using a strong base. In certain embodiments of the present invention, annealing the patterned ohmic contact metal to provide first and second ohmic contacts is carried out prior to forming a protective layer. In other embodiments of the present invention, annealing the patterned ohmic contact metal to provide first and second ohmic contacts is carried out subsequent to forming a protective layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1F are schematic drawings illustrating fabrication of a transistor according to embodiments of the present invention.

Figures 2A and **2B** are schematic drawings illustrating operations in the fabrication of a transistor according to further embodiments of the present invention.

Figure 3 is a schematic illustration of an alternative fabrication step according to embodiments of the present invention.

Figure 4 is a schematic illustration of a transistor according to further embodiments of the present invention.

Figure 5 is a schematic illustration of a transistor according to further embodiments of the present invention.

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. Furthermore, the various layers and regions illustrated in the figures are illustrated schematically. Accordingly, the present invention is not limited to the relative size, spacing and alignment illustrated in the accompanying figures. As will also be appreciated by those of skill in the art, references herein to a layer formed "on" a substrate or other layer may refer to the layer formed directly on the substrate or other layer or on an intervening layer or layers formed on the substrate or other layer. It will also be appreciated by those of skill in the art that references to a structure or feature that is disposed "adjacent" another feature may have portions that overlap or underlie the adjacent feature.

Embodiments of the present invention utilize a protective layer and/or a low damage recess fabrication technique to reduce gate leakage and/or provide a high quality Schottky contact in a semiconductor device, such as a transistor. The use of a protective layer may reduce damage to the semiconductor in the gate region of the transistor that may occur during an anneal of ohmic contacts of the device. Thus, high quality gate and ohmic contacts may be provided with reduced degradation of the gate region that may result from formation of the ohmic contacts.

Embodiments of the present invention may be particularly well suited for use in nitride-based HEMTs such as Group III-nitride based devices. As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In). The term also refers to ternary and quaternary compounds such as AlGaN and AlInGaN. As is well understood by those in this art, the Group III elements can combine with nitrogen to form binary (*e.g.*, GaN), ternary (*e.g.*, AlGaN, AlInN), and quaternary (*e.g.*, AlInGaN) compounds. These compounds all have empirical formulas in which one mole of nitrogen is combined with a total of

$0 \leq x \leq 1$ are often used to describe them.

Suitable structures for GaN-based HEMTs that may utilize embodiments of the present invention are described, for example, in commonly assigned U.S. Patent 6,316,793 and U.S. Patent Publication No. 2002/0066908A1 filed July 12, 2001 and published June 6, 2002, for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," U.S. provisional application serial no. 60/290,195 filed May 11, 2001 for "GROUP III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER," United States Patent Publication No. 2002/0167023A1 to Smorchkova *et al.*, published November 14, 2002, entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" and United States Patent Application Serial No. 10/617,843 filed July 11, 2003 for "NITRIDE-BASED TRANSISTORS AND METHODS OF FABRICATION THEREOF USING NON-ETCHED CONTACT RECESSES," the disclosures of which are hereby incorporated herein by reference in their entirety.

Fabrication of embodiments of the present invention is schematically illustrated in **Figures 1A-1E**. As seen in **Figure 1A**, a substrate **10** is provided on which nitride based devices may be formed. In particular embodiments of the present invention, the substrate **10** may be a semi-insulating silicon carbide (SiC) substrate that may be, for example, 4H polytype of silicon carbide. Other silicon carbide candidate polytypes include the 3C, 6H, and 15R polytypes. The term "semi-insulating" is used descriptively rather than in an absolute sense. In particular embodiments of the present invention, the silicon carbide bulk crystal has a resistivity equal to or higher than about $1x10^5$ Ω-cm at room temperature.

Optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate **10**. For example, an AlN buffer layer may be provided to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. Additionally, strain balancing transition layer(s) may also be provided as described, for example, in commonly assigned United States Patent Publication 2003/0102482A1, filed July 19, 2002 and published

TRANSISTORS AND METHODS OF FABRICATING STRAIN BALANCED NITRIDE HETEROJUNCTION TRANSISTORS, and United States Provisional Patent Application Serial No. 60/337,687, filed December 3, 2001 and entitled "STRAIN BALANCED NITRIDE HETEROJUNCTION TRANSISTOR," the disclosures of which are incorporated herein by reference as if set forth fully herein.

Silicon carbide has a much closer crystal lattice match to Group III nitrides than does sapphire (Al_2O_3), which is a very common substrate material for Group III nitride devices. The closer lattice match may result in Group III nitride films of higher quality than those generally available on sapphire. Silicon carbide also has a very high thermal conductivity so that the total output power of Group III nitride devices on silicon carbide is, typically, not as limited by thermal dissipation of the substrate as in the case of the same devices formed on sapphire. Also, the availability of semi-insulating silicon carbide substrates may provide for device isolation and reduced parasitic capacitance. Appropriate SiC substrates are manufactured by, for example, Cree, Inc., of Durham, N.C., the assignee of the present invention, and methods for producing are described, for example, in U. S. Patent Nos. Re. 34,861; 4,946,547; 5,200,022; and 6,218,680, the contents of which are incorporated herein by reference in their entirety. Similarly, techniques for epitaxial growth of Group III nitrides have been described in, for example, U. S. Patent Nos. 5,210,051; 5,393,993; 5,523,589; and 5,292,501, the contents of which are also incorporated herein by reference in their entirety.

Although silicon carbide may be used as a substrate material, embodiments of the present invention may utilize any suitable substrate, such as sapphire, aluminum nitride, aluminum gallium nitride, gallium nitride, silicon, GaAs, LGO, ZnO, LAO, InP and the like. In some embodiments, an appropriate buffer layer also may be formed.

Returning to **Figure 1A**, a channel layer **20** is provided on the substrate **10**. The channel layer **20** may be deposited on the substrate **10** using buffer layers, transition layers, and/or nucleation layers as described above. The channel layer **20** may be under compressive strain. Furthermore, the channel layer and/or buffer nucleation and/or transition layers may be deposited by MOCVD or by other techniques known to those of skill in the art, such as MBE or HVPE .

III-nitride, such as $Al_xGa_{1-x}N$ where $0 \leq x < 1$, provided that the energy of the conduction band edge of the channel layer **20** is less than the energy of the conduction band edge of the barrier layer **22** at the interface between the channel and barrier layers. In certain embodiments of the present invention, x = 0, indicating that the channel layer **20** is GaN. The channel layer **20** may also be other Group III-nitrides such as InGaN, AlInGaN or the like. The channel layer **20** may be undoped ("unintentionally doped") and may be grown to a thickness of greater than about 20 Å. The channel layer **20** may also be a multi-layer structure, such as a superlattice or combinations of GaN, AlGaN or the like.

A barrier layer **22** is provided on the channel layer **20**. The channel layer **20** may have a bandgap that is less than the bandgap of the barrier layer **22** and the channel layer **20** may also have a larger electron affinity than the barrier layer **22**. The barrier layer **22** may be deposited on the channel layer **20**. In certain embodiments of the present invention, the barrier layer **22** is AlN, AlInN, AlGaN or AlInGaN with a thickness of between about 0.1 nm and about 10 nm. Examples of layers according to certain embodiments of the present invention are described in United States Patent Publication No. 2002/0167023A1, to Smorchkova *et al.*, entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosure of which is incorporated herein by reference as if set forth fully herein. In particular embodiments of the present invention, the barrier layer **22** is thick enough and has a high enough Al composition and doping to induce a significant carrier concentration at the interface between the channel layer **20** and the barrier layer **22** through polarization effects when the barrier layer **22** is buried under ohmic contact metal. Also, the barrier layer **22** should be thick enough to reduce or minimize scattering of electrons in the channel due to ionized impurities deposited at the interface between the barrier layer **22** and a second cap layer **24** (**Fig. 1B**).

The barrier layer **22** may be a Group III-nitride and has a bandgap larger than that of the channel layer **20** and a smaller electron affinity than the channel layer **20**. Accordingly, in certain embodiments of the present invention, the barrier layer **22** is AlGaN, AlInGaN and/or AlN or combinations of layers thereof. The barrier layer **22** may, for example, be from about 0.1 nm to about 10 nm thick, but is not so thick as to present invention, the barrier layer **22** is undoped or doped with an n-type dopant to a concentration less than about 10^{19} cm^{-3}. In some embodiments of the present invention, the barrier layer **22** is $Al_xGa_{1-x}N$ where $0 < x < 1$. In particular embodiments, the aluminum concentration is about 25%. However, in other embodiments of the present invention, the barrier layer **22** comprises AlGaN with an aluminum concentration of between about 5% and about 100%. In specific embodiments of the present invention, the aluminum concentration is greater than about 10%.

Figure 1B illustrates formation of a protective layer **24** on the barrier layer **22.** The protective layer **24** may be silicon nitride (Si_xN_y), aluminum nitride (AlN) and/or other suitable protective material, such as silicon dioxide (SiO_2) and/or an oxynitride. Other materials may also be utilized for the protective layer **24** as long as the material may be removed without damaging the underlying barrier layer **22.** For example, the protective layer **24** could also include magnesium oxide, scandium oxide, aluminum oxide and/or aluminum oxynitride. Furthermore, the protective layer **24** may be a single layer or multiple layers of uniform and/or non-uniform composition.

In particular embodiments of the present invention, the protective layer **24** is SiN. The SiN may be formed by PVD and/or CVD and may be non-stoichiometric in compressive or tensile strain. For example, the protective layer may have a stress of between about -100 MPa and about 100 MPa. In certain embodiments of the present invention, the SiN protective layer has an index of refraction at a 633 nm wavelength of from about 1.6 to about 2.2. In particular embodiments, the index of refraction of the SiN protective layer is 1.98 ± 0.05.

In certain embodiments, the protective layer **24** may be AlN. The AlN may be formed by PVD and/or CVD and may be non-stoichiometric in compressive or tensile strain. For example, the protective layer may have a stress of between about -100 MPa and about 100 MPa. In certain embodiments of the present invention, the AlN protective layer has an index of refraction at a 633 nm wavelength from about 1.8 to about 2.1. In particular embodiments, the index of refraction of the AlN protective layer is 1.85 ± 0.05.

The protective layer **24** may also be SiO_2. The SiO_2 may be formed by PVD and/or CVD and may be non-stoichiometric in compressive or tensile strain. For example, the protective layer may have a stress of between about -100 MPa and about has an index of refraction at a 633 nm wavelength of from about 1.36 to about 1.56. In particular embodiments, the index of refraction of the SiO_2 protective layer is 1.46 ± 0.03.

The protective layer **24** is blanket formed on the barrier layer **22** and may be formed by deposition. For example, a silicon nitride layer may be formed by high quality sputtering and/or PECVD. Typically, the protective layer **24** may have a thickness of about 30 nm, however, other thickness layers may also be utilized. For example, the protective layer should be sufficiently thick so as to protect the underlying layer during a subsequent anneal of ohmic contacts. Layers as thin as two or three monolayers may be sufficient for such purposes. However, in general, the protective layer **24** may have a thickness of from about 10 nm to about 500nm. Also, a high quality SiN protective layer may be grown in-situ with the MOCVD growth of the group III nitride layers.

As illustrated in **Figure 1C**, windows are opened in the protective layer **24** for formation of ohmic contacts **30**. The windows may be formed utilizing a patterned mask and a low damage etch with respect to the barrier layer **22** to expose the underlying barrier layer **22**. Examples of low damage etch techniques include etching techniques other than reactive ion etching, such as inductively coupled plasma or electron cyclotron resonance (ECR) or downstream plasma etching with no DC component to the plasma. For SiO_2, a low damage etch could be a wet etch with buffered hydrofluoric acid. A selective etch of SiN and/or SiO_2 to an etch stop layer, such as ITO, SCO, MgO or the like, followed by a low damage removal of the etch stop layer could also be performed. For SiN, SiO_2 may be used as an etch stop layer. In such embodiments, the protective layer **24** may include the SiN, AlN and/or SiO_2 layer as well as the etch stop layer. Thus, in certain embodiments of the present invention, the protective layer **24** may include multiple layers.

As is further illustrated in **Figure 1C**, with a subsequent photolithography step and evaporation, ohmic metal is patterned to provide the ohmic contacts **30**. The ohmic contacts **30** are patterned so as to be smaller than the window in the protective layer **24** such that the edges of the ohmic contacts **30** are spaced apart from the protective layer **24**. For example, the edges of the ohmic contacts **30** may be spaced apart from the protective layer **24** by a distance of from about 0.1 to about 0.2 μm. The ohmic contacts **30** should be spaced apart from the protective layer **24** a distance of the ohmic contact metal. If the ohmic contact metal contacts the protective layer **24**, the metal may diffuse into the protective layer **24** during subsequent heating steps which may result in a short between a gate contact and the ohmic contact(s) **30**. However, the gap between the ohmic contacts **30** and the protective layer **24** should not be so large as to defeat the protective purpose of the protective layer **24** and, thereby, substantially degrade the performance of the device but should not be so small to risk random contact of ohmic material to the protective layer. Thus, for example, in certain embodiments of the present invention, the gap may be from about 0.1 μm to about 0.5 μm.

The ohmic contact material is annealed to provide the ohmic contacts **30**. The anneal may be a high temperature anneal. For example, the anneal may be an anneal at a temperature of greater than about 900 °C. Through the use of an ohmic contact anneal, the resistance of the ohmic contacts may be reduced from a high resistance to less than about 1 Ω-mm. Thus, as used herein, the term "ohmic contact" refers to a non-rectifying contact that has a contact resistance of less than about 1 Ω-mm. The presence of the protective layer during the high temperature process steps may inhibit damage to the barrier layer **22** that may be caused by such steps. Thus, for example, the sheet resistance of the gate region **21** after the high temperature ohmic contact anneal may be substantially the same as the sheet resistance of the gate region **21** as-grown (*i.e.* before the contact anneal).

Figure 1D illustrates the formation of a gate window. As seen in **Figure 1D**, a mask **26** is formed on the ohmic contacts and the protective layer **24** and patterned to form a window that exposes a portion of the protective layer **24**. A recess is then formed through the protective layer **24** to expose a portion of the barrier layer **22**. The recess is formed using the mask **26** and a low damage etch process as described above. In particular embodiments where the ohmic contacts **30** provide source and drain contacts, the recess may be offset between the source and drain contacts such that the recess, and subsequently the gate contact **32**, is closer to the source contact than the drain contact.

As seen in **Figure 1E**, a gate contact **32** is formed in the recess and contacts the exposed portion of the barrier layer **22**. The gate contact may be a "T" gate as illustrated in **Figure 1E** and may be fabricated using conventional fabrication techniques. Suitable gate materials may depend on the composition of the barrier

Schottky contact to a nitride based semiconductor material may be used, such as Ni, Pt, $NiSi_x$, Cu, Pd, Cr, W and/or WSiN. Although it may be undesirable, it is possible that a small gap between the protective layer **24** and the gate contact **32** may arise as a result of, for example, anisotropy of the low-damage etch, resulting in an exposed surface of the barrier layer **22** between the protective layer **24** and the gate contact **32**.

Figure 1F illustrates the formation of a passivation layer **34**. The passivation layer may be blanket deposited on the structure of **Figure 1E**. In particular embodiments, the passivation layer **34** is deposited so as to substantially fill the gap between the protective layer **24** and the ohmic contacts **30** and also the gap between the protective layer **24** and the gate contact **32**, if such gap exists. In certain embodiments of the present invention, the passivation layer **34** may be silicon nitride, aluminum nitride, silicon dioxide and/or an oxynitride. Furthermore, the passivation layer **34** may be a single or multiple layers of uniform and/or non-uniform composition.

While embodiments of the present invention have been described with reference to a two mask process for forming opening gate contact windows and forming gate contacts with a gap to the protective layer **24**, **Figures 2A** and **2B** illustrate operations for forming the ohmic contact windows and the ohmic contacts with a single mask. As seen in **Figure 2A**, a mask **200**, such as a photoresist, with a negative bevel may be formed on the protective layer **24**. The negative bevel of the mask **200** corresponds to the gap distance between the subsequently formed ohmic contacts **30** and the patterned protective layer **24**. The protective layer **24** is isotropically etched using a low damage etch process as described above to provide the contact windows. Thus, the contact windows will be defined by the bottom dimension of the mask **200**. A mask layer without a negative bevel could also be used if the etch is isotropic and the low-damage etch is substantially over etched to provide a lateral undercut to the desired spacing.

As seen in **Figure 2B**, ohmic contact metal **300** is evaporated on the resulting structure. The overhang of the mask **200** defines the location where metal is deposited on the exposed barrier layer **22**. Thus, the contact metal **300** is spaced apart from the patterned protective layer **24**. The mask **200** and the metal **300** on the mask **200** are removed to provide the structure of **Figure 1C**.

known to those of skill in the art. Furthermore, while the mask **200** is shown as having a bevel, in other embodiments of the present invention, the mask may have a step or other such configuration that provides a mask with two different apparent window sizes for the etch of the protective layer **24** and the deposition of contact material. Thus, for example, multi-layer photoresists are available that have different exposure sensitivity such that a single exposure may provide a mask with an overhang or step such that the window provided by the layer of photoresist proximate the protective layer **24** is large than a window provided by the layer of photoresist spaced apart from the protective layer **24**.

Figure 3 illustrates fabrication of transistors according to further embodiments of the present invention. As seen in **Figure 3**, the formation of the protective layer **24** prior to ohmic metal deposition may be omitted and the ohmic metal may be deposited and patterned on the barrier layer **22** to provide ohmic contact material regions **30** on the barrier layer **22**. A protective layer **40** is then formed on the gate region of the barrier layer **22** and the ohmic contact material. In particular embodiments of the present invention, the protective layer **40** may be aluminum nitride that is blanket deposited by sputtering. The protective layer **40** may also be materials such as described above with reference to the protective layer **24**.

The anneal of the ohmic contact material regions **30** is carried out with the protective layer **40** in place. The protective layer **40** may then be removed, for example, using a low damage etching technique such as those described above. The gate contact **32** may then be formed, before or after formation of a passivation layer **34**. For example, a layer of silicon nitride could be deposited by sputtering. A gate recess could then be etched, for example, using a low damage etch process as described above, into the passivation layer and the gate formed in the recess. Such a process may provide for the silicon nitride passivation layer maintaining its full thickness to the edge of the "T" gate. Thus, a transistor having a structure such as that illustrated in **Figure 4** may be provided.

Alternatively, the structure illustrated in **Figure 4** may be provided utilizing the fabrication steps illustrated in **Figures 1A-1F**, however, the protective layer **24** may be removed either prior to or subsequent to the formation of the gate contact **32**. In such a case, the protective layer **24** should be removed using low damage etching techniques such as those described above.

protective layer **24** is formed to at least about as thick as the ohmic contacts **30**. As seen in **Figure 5**, in such embodiments, the wings of the gate contact **34** may be formed directly on the protective layer **24**. For example, the protective layer **24** may be formed to a thickness of from about 500 to about 5000 Å. A low damage etch through the protective layer **24** would be carried out and the "T" gate **32** formed directly on and through the protective layer **24**. Subsequent overlayer passivation **34** may also be provided, for example, to improve environmental protection of the device.

While embodiments of the present invention have been described herein with reference to particular HEMT structures, the present invention should not be construed as limited to such structures. For example, additional layers may be included in the HEMT device while still benefiting from the teachings of the present invention. Such additional layers may include GaN cap layers, as for example, described in Yu et al., "Schottky barrier engineering in III–V nitrides via the piezoelectric effect," Applied Physics Letters, Vol. 73, No. 13, 1998, or in U.S. Patent Publication No. 2002/0066908A1 filed July 12, 2001 and published June 6, 2002, for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," the disclosures of which are incorporated herein by reference as if set forth fully herein. In some embodiments, insulating layers such as SiNx, or relatively high quality AlN may be deposited for making a MISHEMT and/or passivating the surface. The additional layers may also include a compositionally graded transition layer or layers.

Furthermore, the barrier layer **22** may also be provided with multiple layers as described in United States Patent Publication No. 2002/0167023A1, to Smorchkova *et al.*, entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosure of which is incorporated herein by reference as if set forth fully herein. Thus, embodiments of the present invention should not be construed as limiting the barrier layer to a single layer but may include, for example, barrier layers having combinations of GaN, AlGaN and/or AlN layers. For example, a GaN, AlN structure may be utilized to reduce or prevent alloy scattering. Thus, embodiments of the layers may include AlGaN based barrier layers, AlN based barrier layers and combinations thereof.

In the drawings and specification, there have been disclosed typical embodiments of the invention, and, although specific terms have been employed, they have been used in a generic and descriptive sense only and not for purposes of limitation.

THAT WHICH IS CLAIMED IS:

1. A method of fabricating a transistor, comprising:

forming a nitride-based semiconductor barrier layer on a nitride-based semiconductor channel layer;

forming a protective layer on a gate region of the nitride-based semiconductor barrier layer;

forming patterned ohmic contact metal regions on the barrier layer;

removing the protective layer;

annealing the patterned ohmic contact metal to provide first and second ohmic contacts, wherein the annealing is carried out with the protective layer on the gate region; and

forming a gate contact on the gate region of the barrier layer.

2. The method of Claim 1, wherein the protective layer comprises an aluminum nitride layer, a silicon nitride (SiN) layer and/or a silicon dioxide (SiO_2) layer.

3. The method of Claim 1, wherein removing the protective layer comprises removing the protective layer utilizing a low damage etching technique.

4. The method of Claim 3, wherein the low damage etching technique comprises a wet etch using a strong base.

5. The method of Claim 1, wherein removing the protective layer is followed by forming a passivation layer on exposed portions of the barrier layer.

6. The method of Claim 5, wherein forming a gate contact comprises:

etching a recess in the passivation layer utilizing a low damage etch technique to expose a portion of the gate region of the barrier layer; and

forming the gate contact in the recess in the passivation layer.

7. The method of Claim 5, wherein forming a gate contact comprises forming a gate contact that extends through the passivation layer to contact the barrier layer.

8. The method of Claim 1, wherein forming a protective layer comprises forming a patterned protective layer on the barrier layer, the patterned protective layer covering a first portion of the barrier layer corresponding to the gate region and exposing adjacent second portions of the barrier layer corresponding to the first and second ohmic contacts; and

wherein forming patterned ohmic contact metal regions comprises forming patterned ohmic contact metal regions on the second portions of the barrier layer, the patterned ohmic contact metal regions being adjacent and spaced apart from the patterned protective layer.

9. The method of Claim 8, wherein forming a patterned protective layer comprises:

blanket depositing a protective layer material on the barrier layer;

forming a mask on the blanket deposited protective layer material, the mask having windows corresponding to locations of the first and second ohmic contacts;

etching the blanket deposited protective layer through the windows utilizing a low damage etching technique; and

removing the mask.

10. The method of Claim 9, wherein the windows corresponding to locations of the first and second ohmic contacts are larger than an area of the first and second ohmic contacts.

11. The method of Claim 9, wherein forming patterned ohmic contact metal regions on the second portions of the barrier layer, the patterned ohmic contact metal regions being adjacent and spaced apart from the patterned protective layer is carried out prior to removing the mask.

12. The method of Claim 5, wherein the passivation layer comprises silicon nitride.

13. The method of Claim 1, further comprising

forming a Group III-nitride layer to provide the nitride-based channel layer; and

wherein forming a nitride-based semiconductor barrier layer comprises forming a Group III-nitride layer.

14. The method of Claim 13, wherein the channel layer has a composition of $Al_xGa_{1-x}N$ wherein $0 \leq x < 1$, and wherein the bandgap of the channel layer is less than the bandgap of the barrier layer.

15. The method of Claim 14:

wherein the channel layer comprises aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN); and

wherein the barrier layer comprises aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN.

16. The method of Claim 1, wherein the barrier layer comprises multiple layers.

17. The method of Claim 1 further comprising:

forming a buffer layer on a substrate; and

forming a Group III-nitride channel layer on the buffer layer to provide the nitride-based channel layer.

18. The method of Claim 1, where the channel layer and the barrier layer are configured to provide a High Electron Mobility Transistor (HEMT).

19. The method of Claim 1, wherein the nitride-based channel layer is provided on a SiC substrate.

20. The method of Claim 1, wherein the protective layer is formed to a thickness of at least about a thickness of the ohmic contact material.

21. The method of Claim 1, wherein the protective layer has a thickness of at least about two monolayers.

22. The method of Claim 1, wherein the protective layer has a thickness of from about 5.0 nm to about 500 nm.

23. The method of Claim 5, wherein forming a passivation layer is performed in-situ.

24. The method of Claim 23, wherein forming the passivation layer comprises growing the passivation layer using MOCVD growth.

25. A high electron mobility transistor comprising:

a nitride-based channel layer on a substrate;

a nitride-based semiconductor barrier layer on the nitride-based channel layer, the nitride based semiconductor barrier layer having a sheet resistance that is substantially the same as an as-grown sheet resistance of the nitride-based semiconductor barrier layer;

ohmic contacts on the barrier layer; and

a gate contact on the barrier layer.

26. The high electron mobility transistor of Claim 25, further comprising a protective layer disposed on the barrier layer that is adjacent and spaced apart from the ohmic contacts and that the gate contact extends through.

27. The high electron mobility transistor of Claim 26, further comprising a passivation layer on the protective layer and that substantially fills a gap between the ohmic contacts and the protective layer.

28. The high electron mobility transistor of Claim 27, wherein the passivation layer is also on the protective layer and wherein the gate contact extends through the protective layer and the passivation layer.

29. The high electron mobility transistor of Claim 27, wherein at least a portion of the gate contact is directly on the protective layer and a portion of the gate contact is directly on the barrier layer.

30. The high electron mobility transistor of Claim 25, further comprising a passivation layer on the barrier layer that substantially fills a gap between the ohmic contacts and the gate contact.

31. The high electron mobility transistor of Claim 41:

wherein the nitride-based channel layer comprises a Group III-nitride layer; and

wherein the nitride-based semiconductor barrier layer comprises a Group III-nitride layer.

32. The high electron mobility transistor of Claim 25, wherein the channel layer has a lower bandgap than the barrier layer.

33. The high electron mobility transistor of Claim 25, wherein the channel layer comprises an undoped layer having a thickness of greater than about 20 Å.

34. The high electron mobility transistor of Claim 25, wherein the channel layer comprises a superlattice and/or a combination of Group III-nitride layers.

35. The high electron mobility transistor of Claim 25:

wherein the channel layer comprises aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN); and

wherein the barrier layer comprises aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN.

36. The high electron mobility transistor of Claim 25, wherein the barrier layer comprises $Al_xGa_{1-x}N$ wherein $0 < x < 1$.

37. The high electron mobility transistor of Claim 25, wherein the barrier layer comprises multiple layers.

38. The high electron mobility transistor of Claim 25, further comprising a buffer layer on the substrate, and wherein the nitride-based channel layer is disposed on the buffer layer.

39. The high electron mobility transistor of Claim 26, wherein the protective layer has a thickness of at least as thick as the ohmic contacts.

40. The high electron mobility transistor of Claim 25, wherein the ohmic contacts have a contact resistance of less than about 1 Ω-mm.

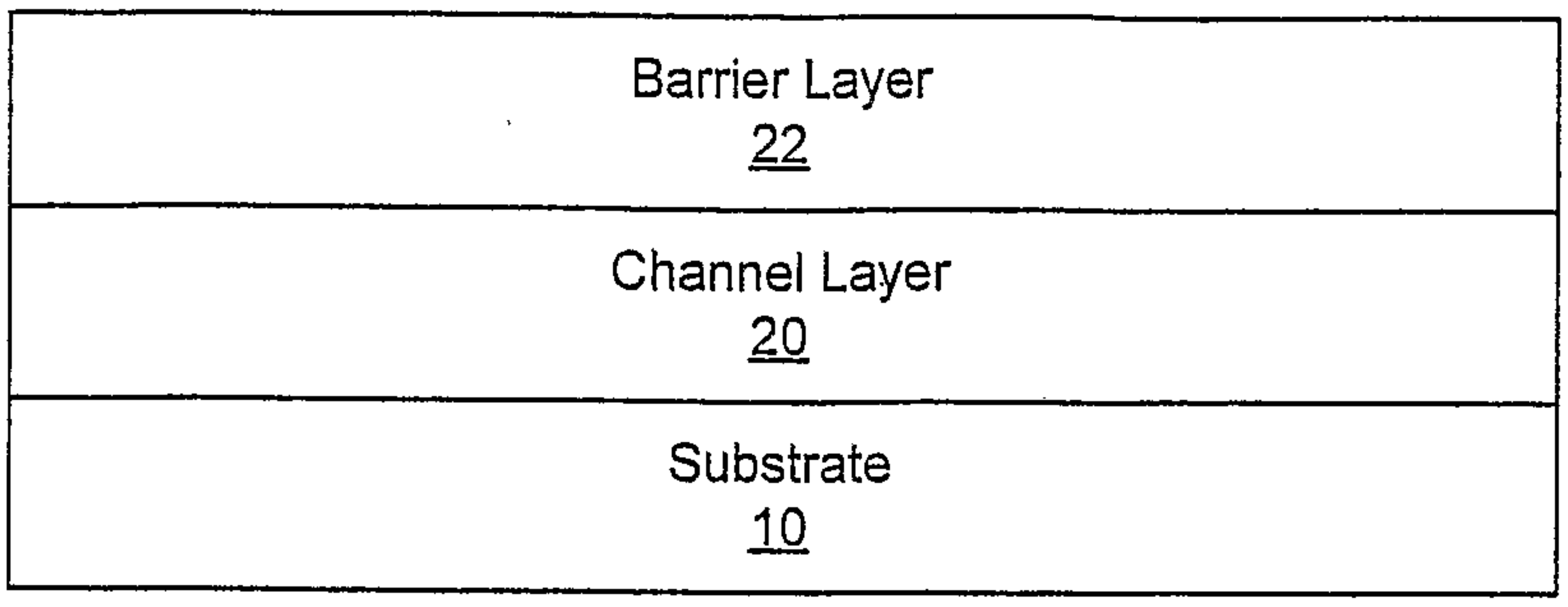


Figure 1A

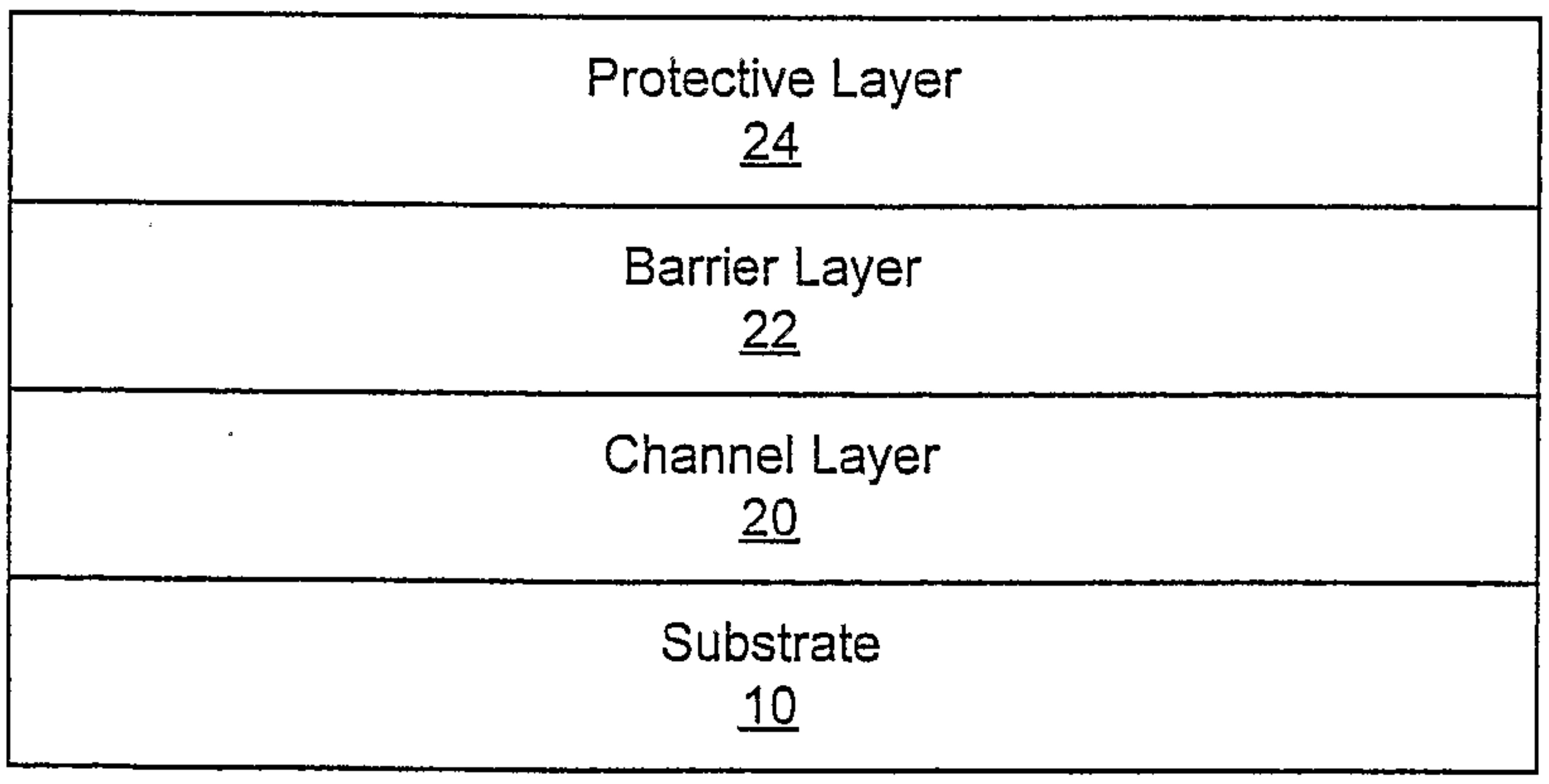


Figure 1B

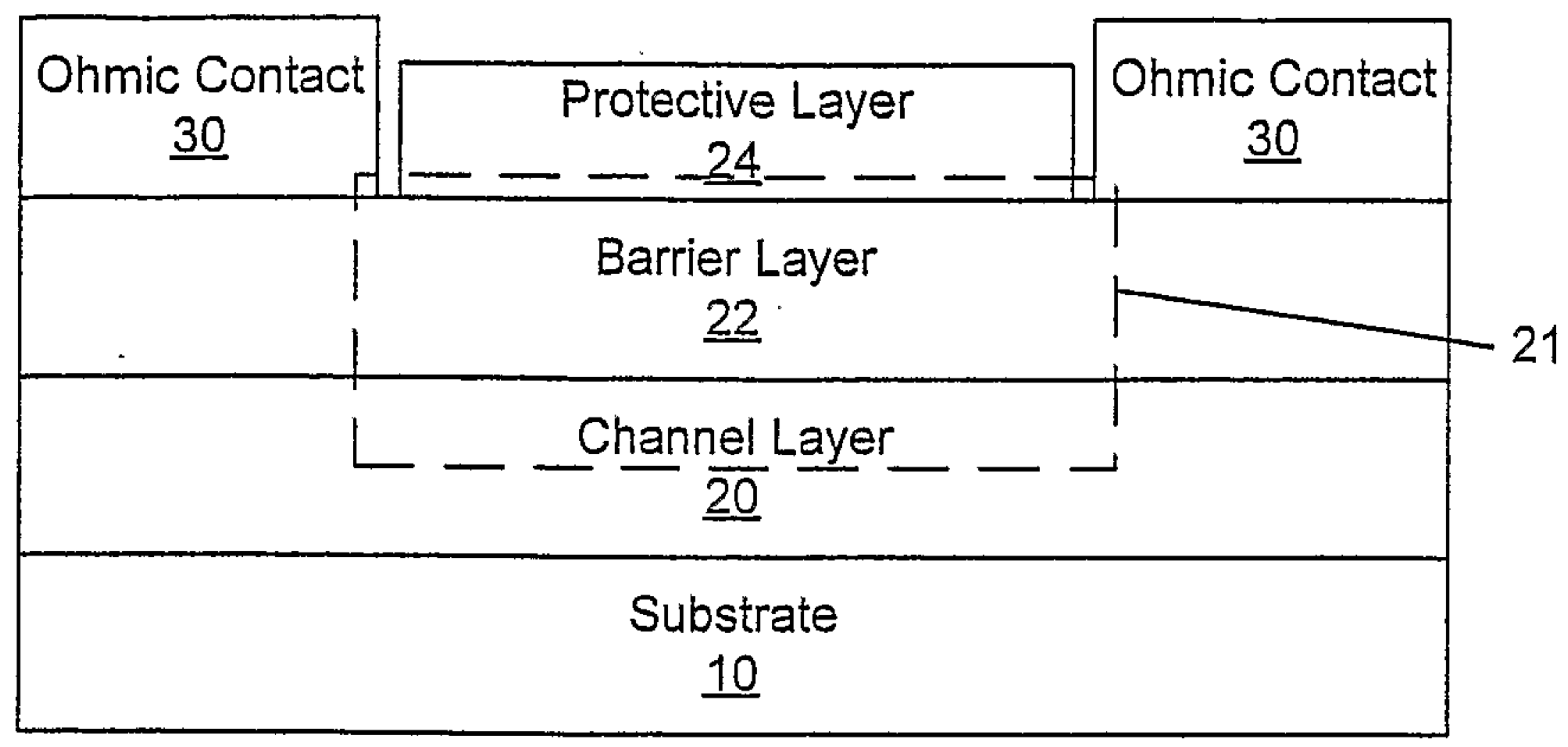


Figure 1C

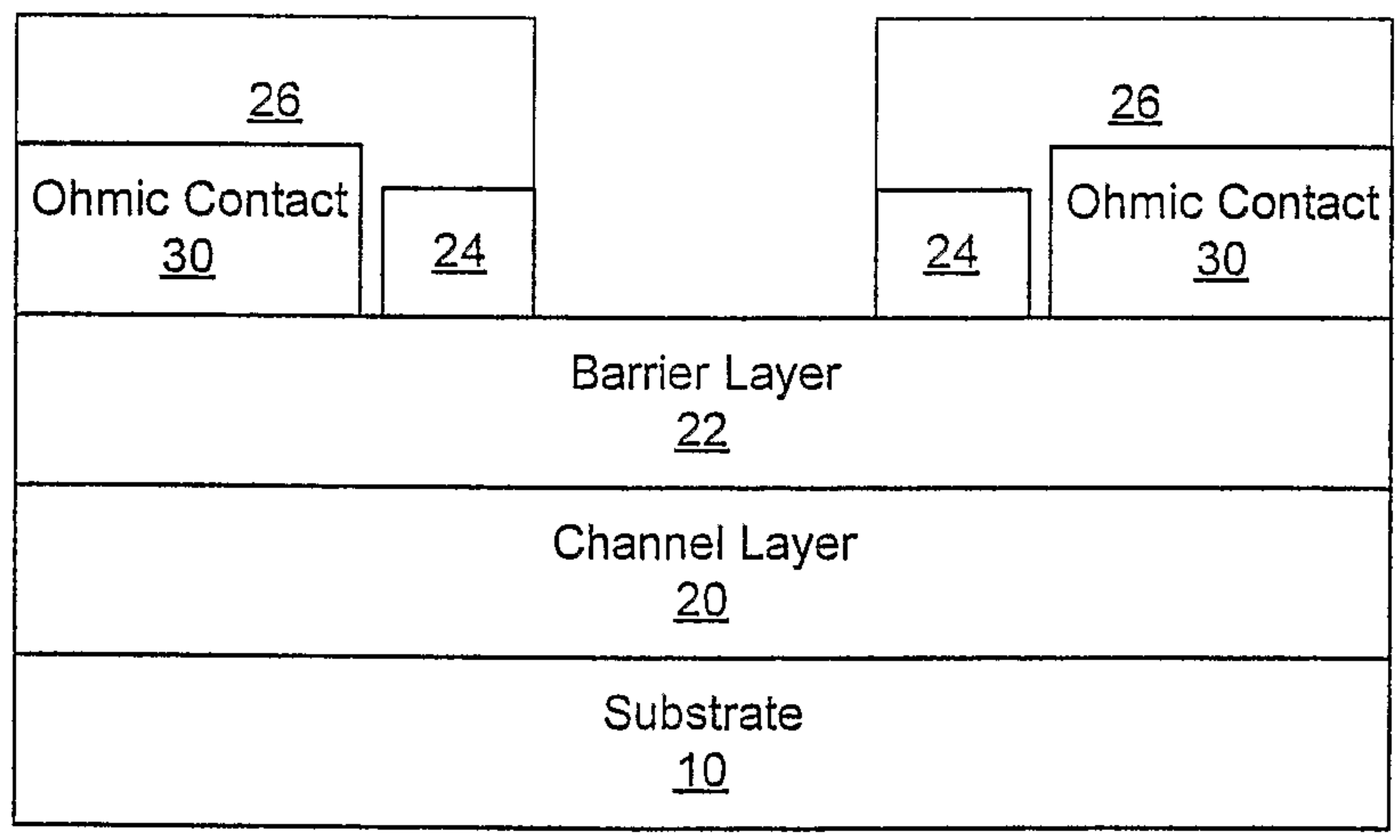


Figure 1D

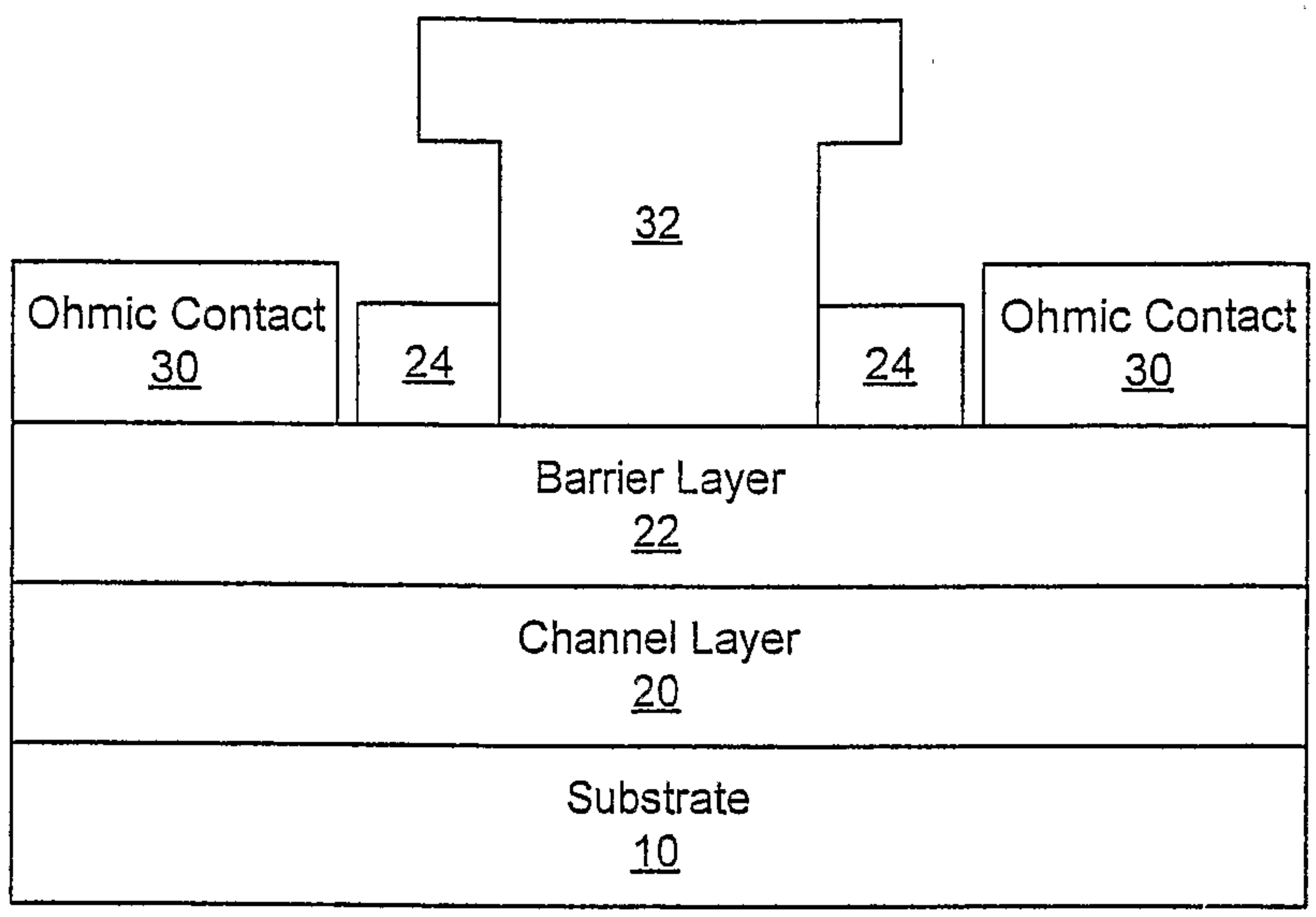


Figure 1E

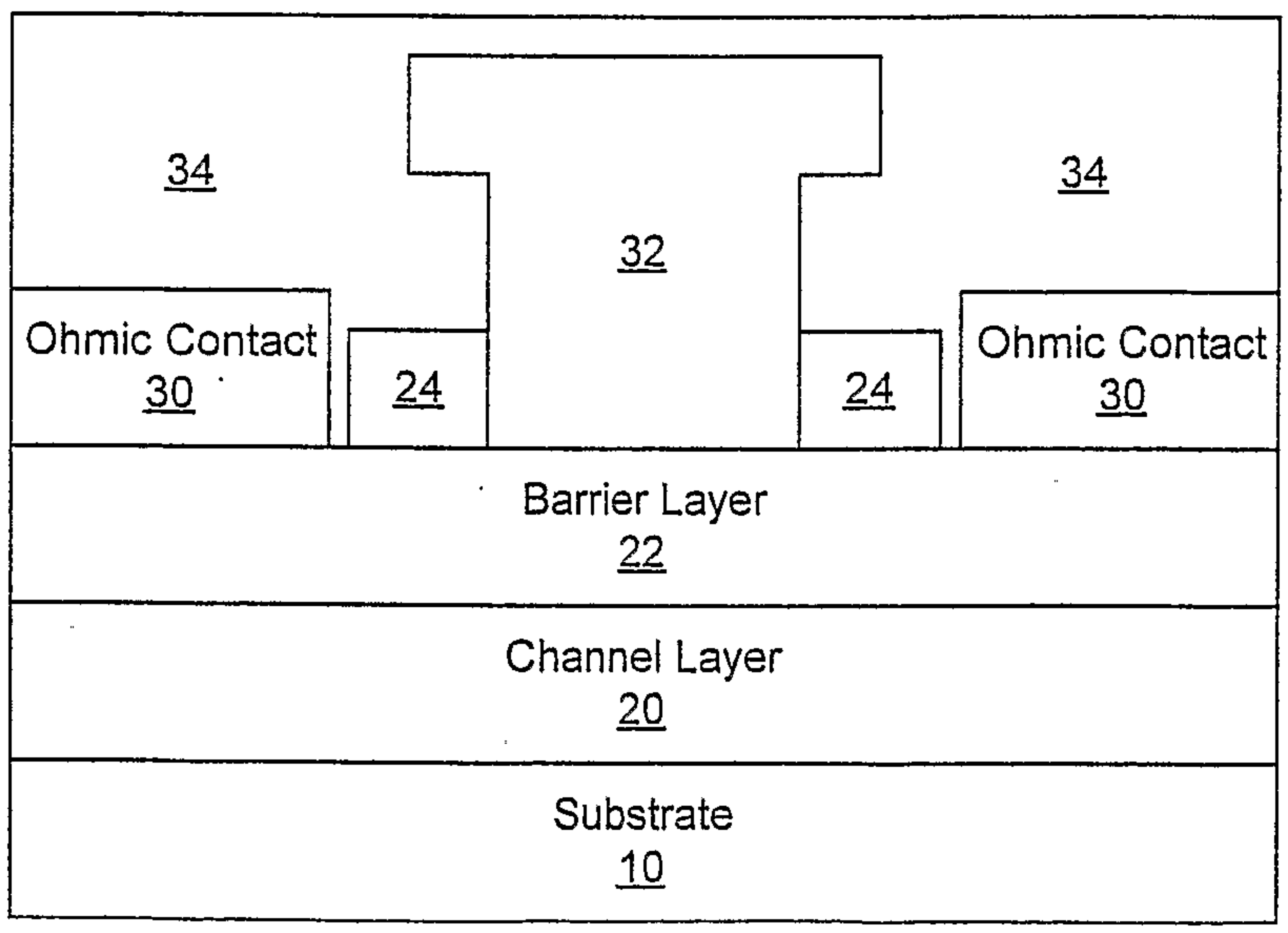


Figure 1F

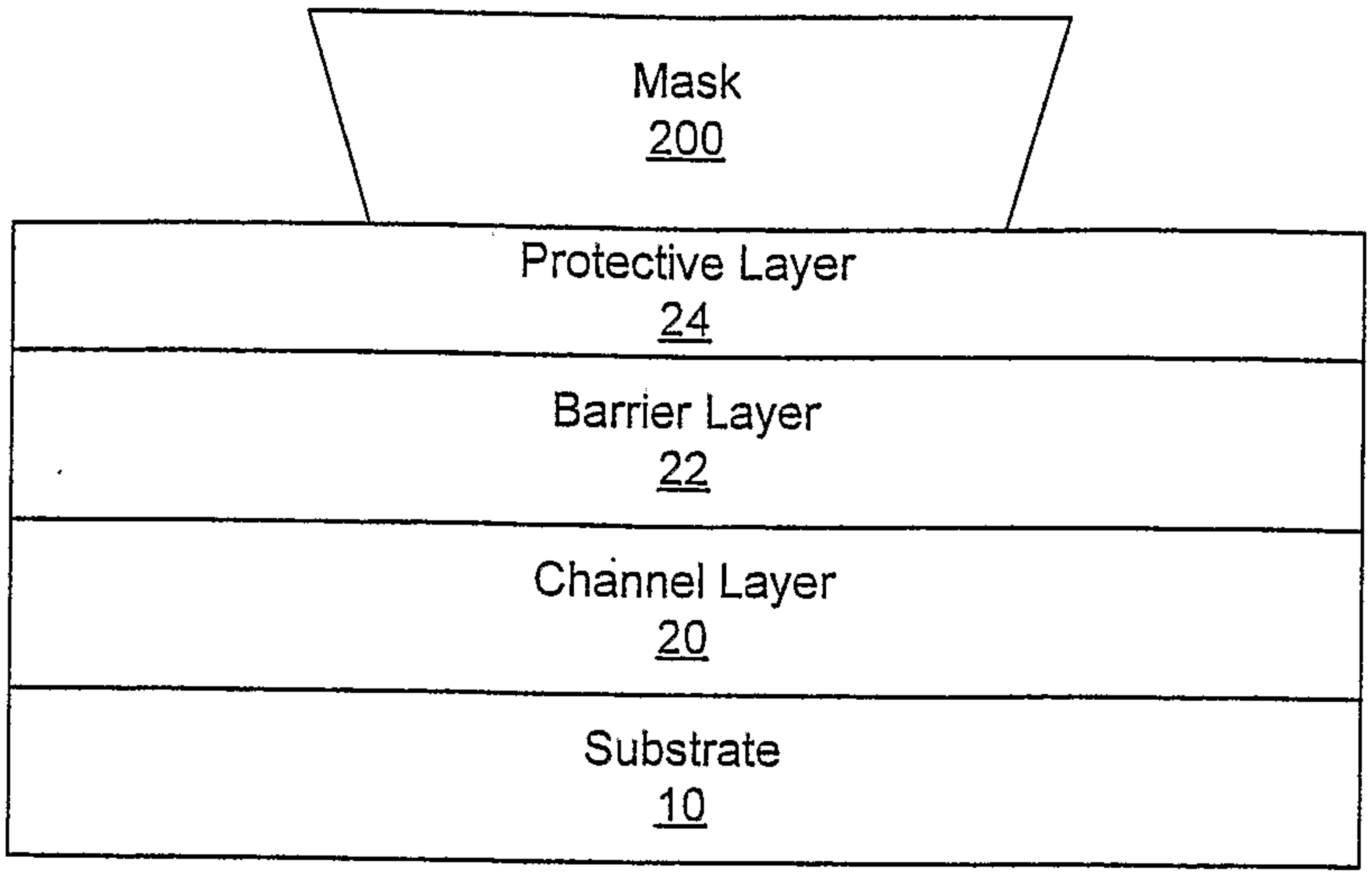


Figure 2A

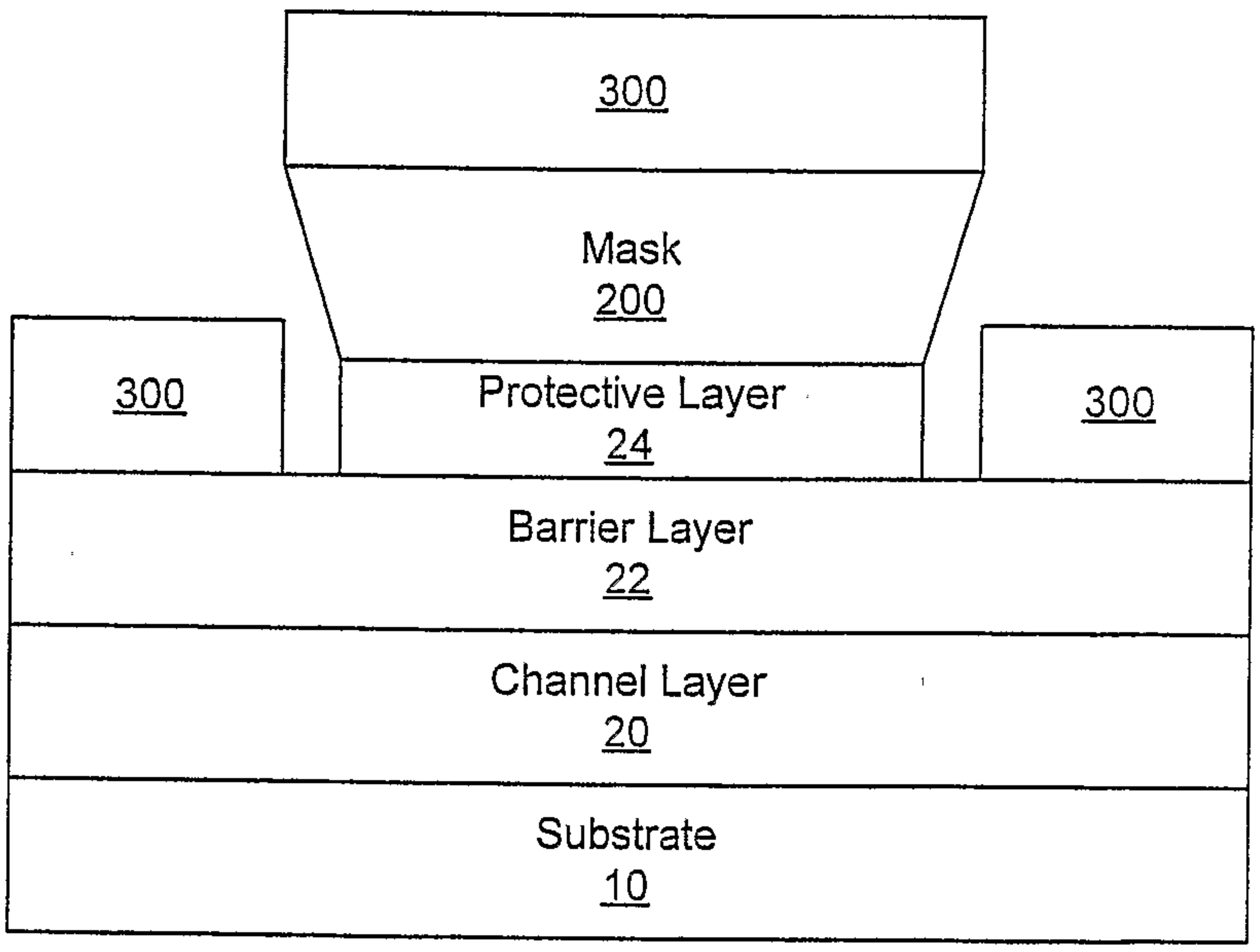


Figure 2B

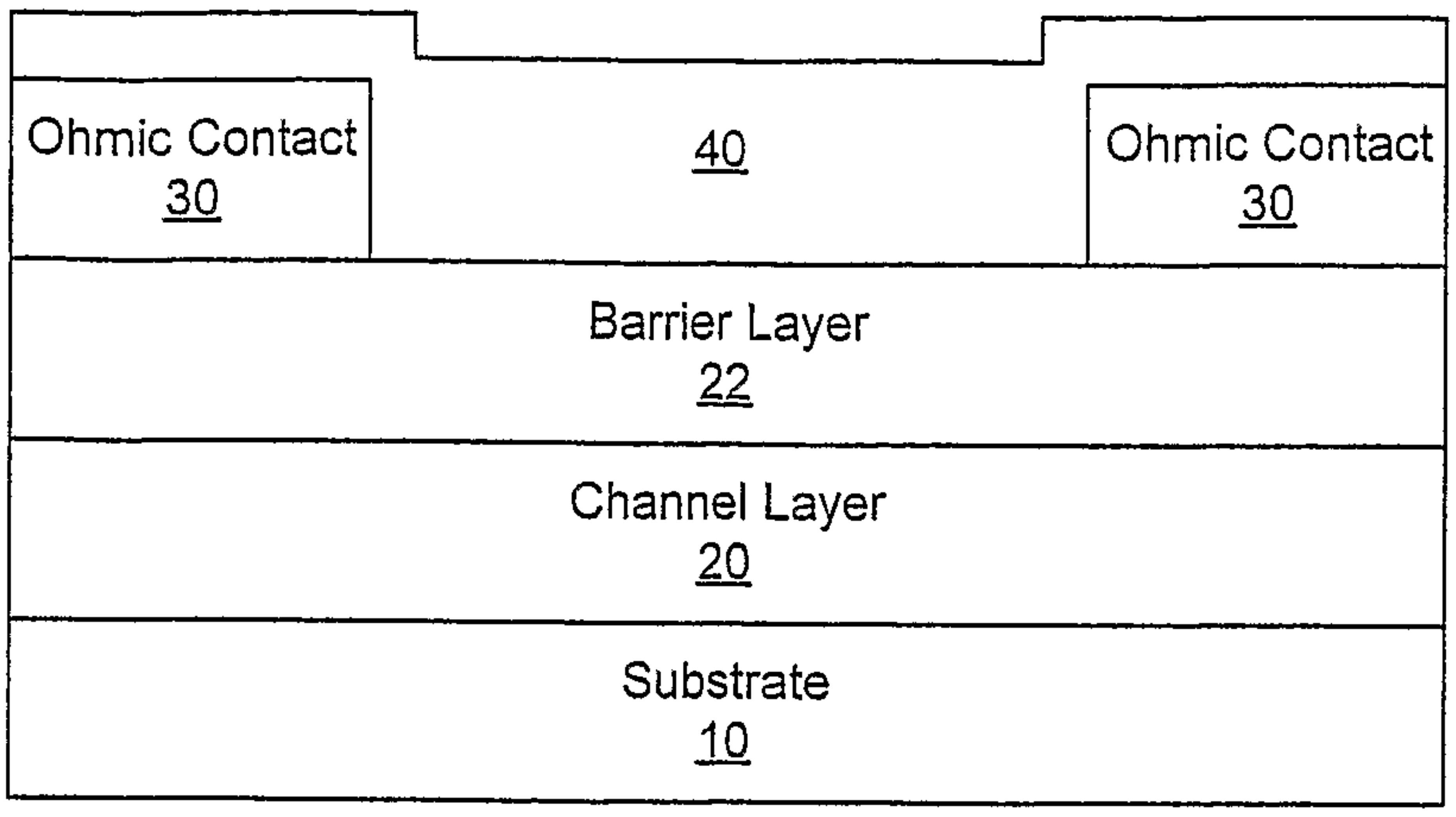


Figure 3

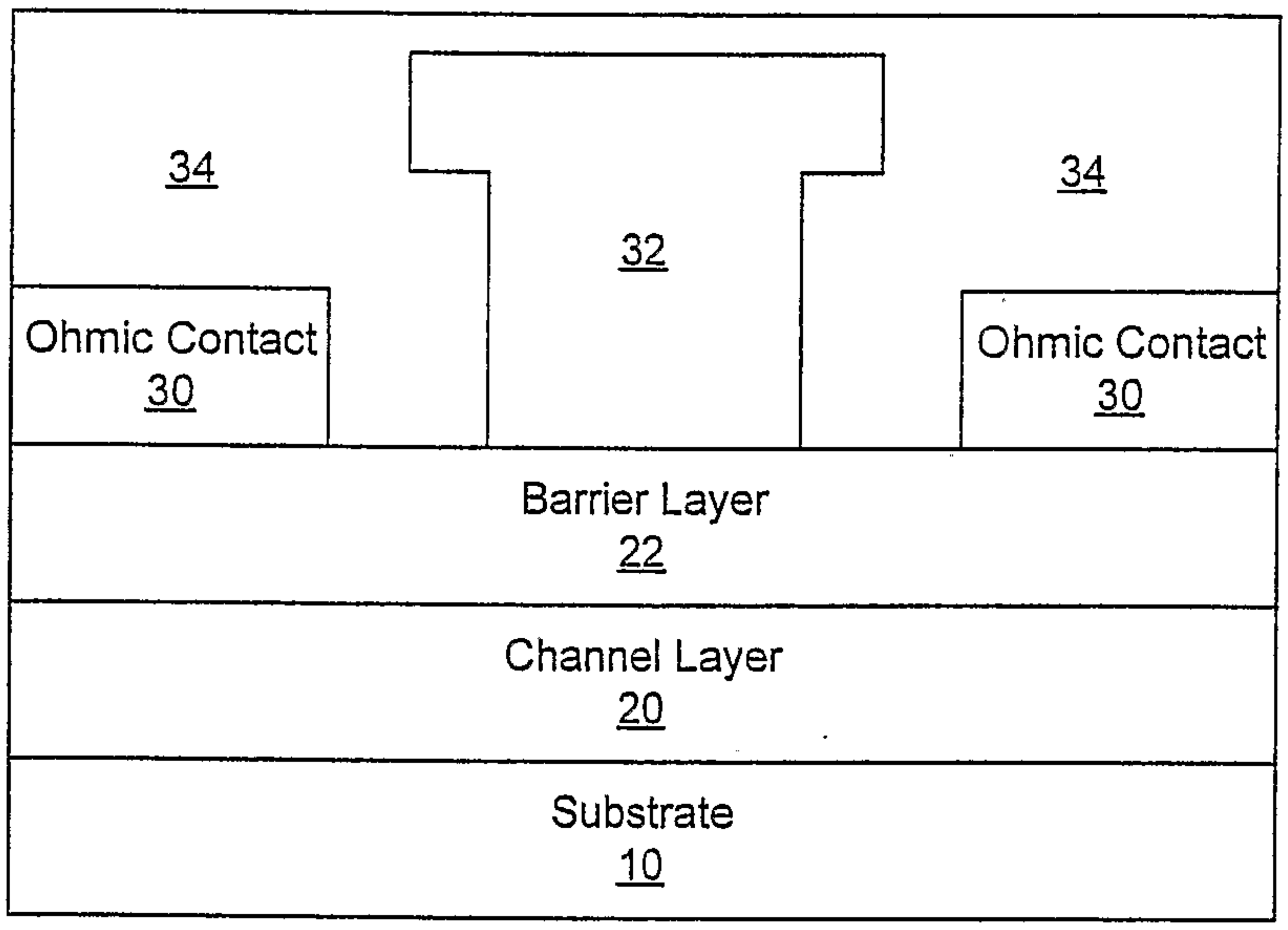


Figure 4

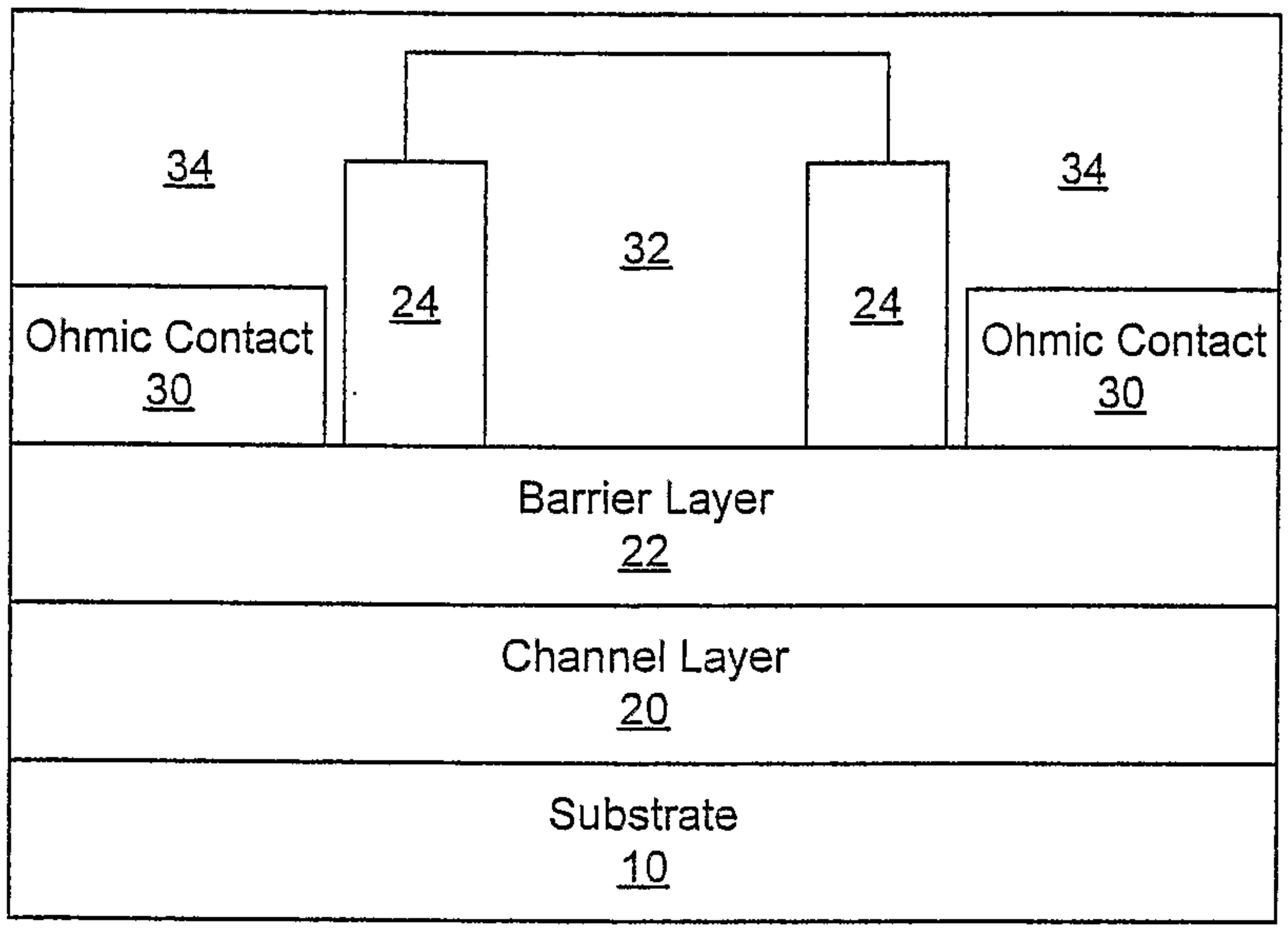
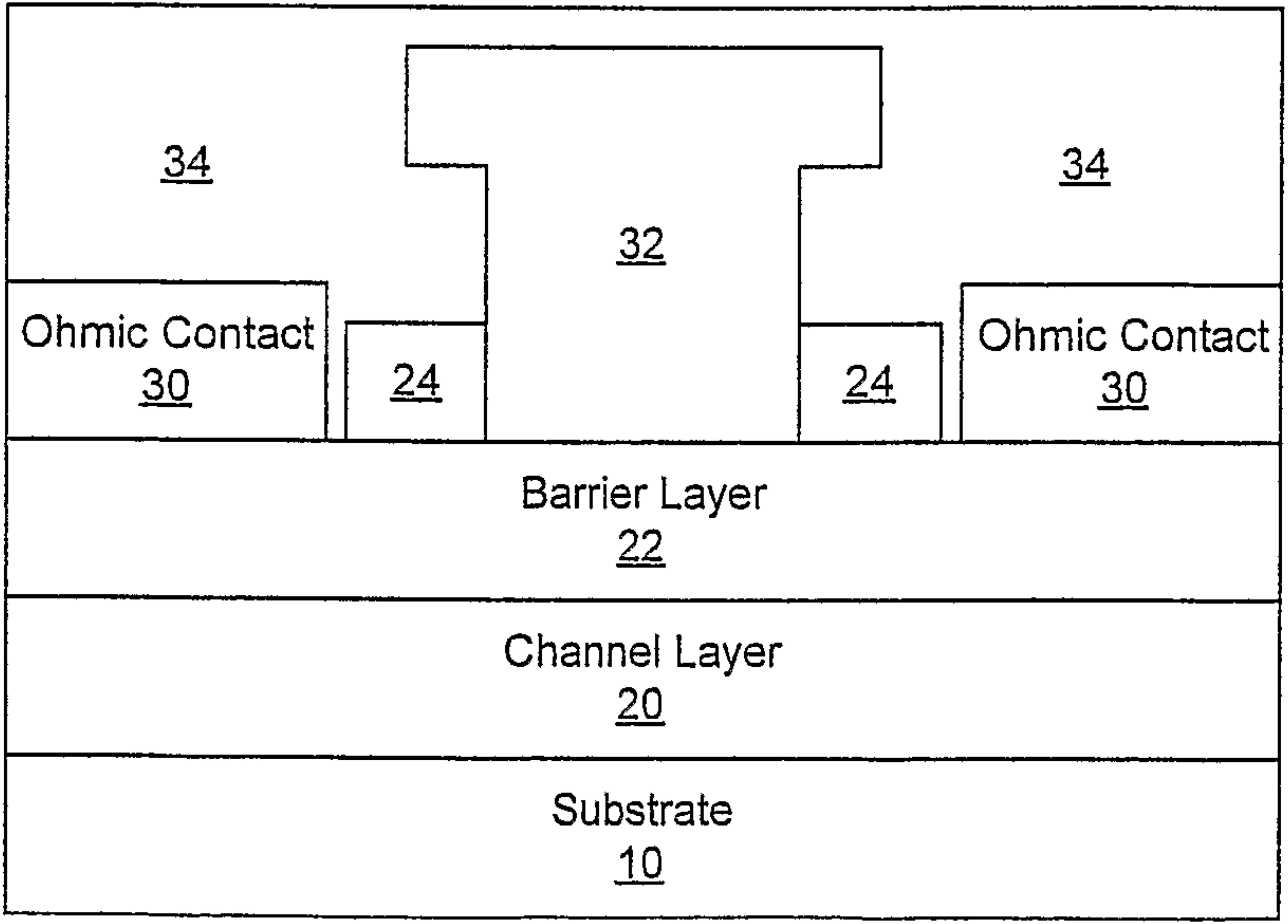

34
34
32
24
24
Ohmic Contact
30
Ohmic Contact
30
Barrier Layer
22
Channel Layer
20
Substrate
10

Figure 5


34
32
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Ohmic Contact
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Ohmic Contact
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Channel Layer
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Substrate
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