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(54) Title: POROUS SILICON STRUCTURES AND LASER MACHINING METHODS FOR SEMICONDUCTOR WAFER PROCESSING

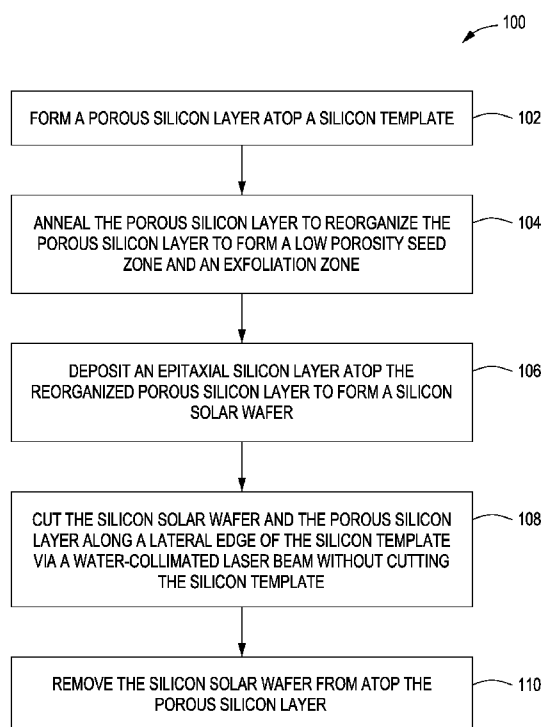


FIG. 1

(57) Abstract: In some embodiments, a method of separating a silicon solar wafer from atop a silicon template includes: (a) forming a porous silicon layer atop a silicon template; (b) annealing the porous silicon layer to reorganize the porous silicon layer to form a low porosity seed zone and an exfoliation zone; (c) depositing an epitaxial silicon layer atop the reorganized porous silicon layer to form a silicon solar wafer; (d) cutting the silicon solar wafer and the reorganized porous silicon layer along a lateral edge of the silicon template via a water-collimated laser beam without cutting the silicon template; and (e) separating the silicon solar wafer from atop the reorganized porous silicon layer.



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POROUS SILICON STRUCTURES AND LASER MACHINING METHODS FOR SEMICONDUCTOR WAFER PROCESSING

FIELD

[0001] Embodiments of the present disclosure pertain to the field of semiconductor processing and, in particular, to methods of separating silicon solar cells and dicing semiconductor wafers.

BACKGROUND

[0002] In semiconductor wafer processing, integrated circuits and solar cells are formed on a wafer (also referred to as a substrate). Each wafer is processed to form a large number of individual solar cells or individual regions containing integrated circuits known as dice. Following the integrated circuit formation process or the solar cell formation process, the wafer is singulated to separate individual dies or individual solar cells from one another. Typical methods that are used for singulation are scribing and sawing. One problem with either scribing or sawing is that chips and gouges can form along the severed edges of the singulated piece. In addition, cracks can form and propagate from the edges of the dice into the substrate and render the integrated circuit inoperative.

[0003] Thus, the inventors have provided improved methods for separating silicon solar cells and dicing semiconductor wafers.

SUMMARY

[0004] In some embodiments, a method of separating a silicon solar wafer from atop a silicon template includes: (a) forming a porous silicon layer atop a silicon template; (b) annealing the porous silicon layer to reorganize the porous silicon layer to form a low porosity seed zone and an exfoliation zone; (c) depositing an epitaxial silicon layer atop the reorganized porous silicon layer to form a silicon solar wafer; (d) cutting the silicon solar wafer and the reorganized porous silicon layer along a lateral edge of the silicon template via a water-collimated laser beam without cutting the silicon template; and (e) separating the silicon solar wafer from atop the reorganized porous silicon layer.

[0005] In some embodiments, a method of dicing a semiconductor wafer comprising a plurality of integrated circuits includes: (a) forming porous silicon in device perforation areas between integrated circuits on the semiconductor wafer; (b) applying a thin polyvinyl alcohol (PVA) mask atop the plurality of integrated circuits; (c) cutting the semiconductor wafer to singulate the plurality of integrated circuits.

[0006] In some embodiments, a method of dicing a semiconductor wafer comprising a plurality of integrated circuits, includes: (a) laser scribing the semiconductor wafer to form trenches partially into but not through the semiconductor wafer between the plurality of integrated circuits; (b) cutting the semiconductor wafer via a water-collimated laser beam through the trenches to form corresponding trench extensions and singulate the plurality of integrated circuits.

[0007] Other embodiments and variations of the present disclosure are discussed below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Embodiments of the present disclosure, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative embodiments of the disclosure depicted in the appended drawings. The appended drawings illustrate only typical embodiments of the disclosure and are therefore not to be considered limiting of the scope, for the disclosure may admit to other equally effective embodiments.

[0009] Figure 1 is a flow diagram of a method for separating a silicon solar wafer from atop a silicon template in accordance with some embodiments of the present disclosure.

[0010] Figures 2A-2E are illustrative cross-sectional views of a substrate during different stages of the method of Figure 1 in accordance with some embodiments of the present disclosure.

[0011] Figures 3A-3D are illustrative cross-sectional views of a substrate during different stages of the method of Figure 1 in accordance with some embodiments of the present disclosure.

[0012] Figure 4 is a flow diagram of a method for dicing a semiconductor wafer comprising a plurality of integrated circuits in accordance with some embodiments of the present disclosure.

[0013] Figures 5A-5C are illustrative cross-sectional views of a substrate during different stages of the method of Figure 4 in accordance with some embodiments of the present disclosure.

[0014] Figure 6 is a flow diagram of a method for dicing a semiconductor wafer comprising a plurality of integrated circuits in accordance with some embodiments of the present disclosure.

[0015] Figures 7A-7B are illustrative cross-sectional views of a substrate during different stages of the method of Figure 6 in accordance with some embodiments of the present disclosure.

[0016] Figure 8 is a flow diagram of a method 800 for processing a substrate in accordance with some embodiments of the present disclosure.

[0017] Figures 9A-9D are illustrative cross-sectional views of a substrate during different stages of the processing sequence of Figure 8 in accordance with some embodiments of the present disclosure.

[0018] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. Elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0019] Embodiments of methods for separating silicon solar cells and dicing semiconductor wafers are provided herein. In at least some embodiments, the inventive methods described herein may advantageously facilitate silicon solar wafer separation using a single water collimated laser cutting process. The water collimated laser advantageously enables solar cell manufacturing with templates and wafers of equal size and without complex and costly focal length adjustment. In at least some embodiments, the inventive methods described herein may also

advantageously facilitate die singulation using porous silicon and a water-collimated laser. Use of the porous silicon in die in device perforation areas advantageously reduces chipping and edge cracking along the edges of the integrated circuits during dicing. Furthermore, the water-collimated laser is advantageously material and equipment compatible with back end packaging which makes the water-collimated laser more production worthy than chemical etching for separating a plurality of integrated circuits.

[0020] Figure 1 is a flow diagram of a method 100 for separating a silicon solar wafer from atop a silicon template in accordance with some embodiments of the present disclosure. Figures 2A-2E are illustrative cross-sectional views of a substrate during different stages of the processing sequence of Figure 1 in accordance with some embodiments of the present disclosure.

[0021] The method 100 begins at 102, as depicted in Figure 2A, by forming a porous silicon layer 200 atop a silicon template 202. In some embodiments, the porous silicon layer 200 is formed by submerging the silicon template 202 in an electrolyte solution and applying an anodic current. Silicon atoms on the surface of the silicon template 202 facing the negative electrode are etched leaving nanometer-scale pores. The thickness and porosity of the porous silicon layer 200 are controlled by the direction and magnitude of the anodic current passing through the thickness of the silicon template 202. The porous silicon layer 200 may have a thickness between about 0.1 micron and about 3 microns and may have porosity between about 25 percent and about 75 percent. In some, embodiments, the porous silicon layer may be formed using two or more sequential steps with different anodic current and time settings to form a shallow zone with low porosity and a deeper zone with high porosity. For example, the silicon template 202 may first be subjected to a first anodic current for a first period of time to form a shallow zone with low porosity and then subjected to a second anodic current for a second period of time to form a deeper zone with high porosity.

[0022] The porous silicon layer 200 consists of one or more zones with low porosity and one or more zones with high porosity. As described above, in some embodiments, the porous silicon layer 200 comprises a shallow zone, proximate the upper surface 206 of the porous silicon layer 200, with a low porosity, for example

about 25 percent porosity, and a deeper zone with a high porosity, for example about 75 percent porosity. At 104, and as depicted in Figure 2B, the porous silicon layer 200 is annealed 204. Annealing the porous silicon layer 200 reorganizes the porous silicon layer 200 in zones with low porosity to produce a low porosity seed zone. The low porosity seed zone has a crystalline structure to enhance epitaxial growth of subsequently deposited silicon layer 208 described at 106 below. The anneal process also consolidates the pores in the high porosity zone (i.e. the exfoliation zone) into large voids to assist with wafer separation as described at 110 below. In some embodiments, the seed zone has a thickness of less than about 1 micron. In some embodiments, the exfoliation zone has a thickness of about 1 to about 3 microns. The anneal process occurs in a hydrogen environment at a suitable temperature and for suitable amount of time to reorganize the upper surface 206 of the porous silicon layer 200. For example, in some embodiments, the anneal process occurs at a temperature of about 1100 to about 1200 degrees Celsius for about 5 to about 30 minutes.

[0023] Next, at 106, as depicted in Figure 2C, a silicon layer 208 is deposited atop the reorganized surface 210 of the porous silicon layer 200 to form a silicon substrate. In some embodiments, the silicon layer 208 formed atop the reorganized surface 210 of the porous silicon layer 200 (e.g., the silicon substrate) is a solar wafer. In some embodiments, the silicon layer 208 is about 40 to about 160 microns thick, for example about 100 microns thick. In some embodiments, the silicon layer 208 is deposited atop the reorganized surface 210 of the porous silicon layer 200 via any suitable epitaxial deposition process known in the art.

[0024] Next, at 108, as depicted in Figure 2D, a water-collimated laser beam 212 from a water-collimated laser is used to cut the silicon layer 208 and the porous silicon layer 200 along a lateral edge 214 of the silicon template 202 without cutting the silicon template 202. In some embodiments, the water-collimated laser beam 212 is used to cut a bevel 216 along the lateral edge 214 having an angle of about 45 degrees or greater and less than about 90 degrees from a horizontal surface 218 of the silicon layer 208.

[0025] In some embodiments, the water-collimated laser produces a water-collimated laser beam 212 using a liquid source comprising a mixture of water and

solvent. The purpose of the solvent is to reduce the surface tension of the water. In some embodiments, the mixture comprises about 5 to about 100 percent solvent, for example about 5 vol. % solvent and the balance water. In some embodiments, the solvent is isopropanol, toluene, or the like. In some embodiments, the mixture reduces the water column diameter to about 5 to about 25 microns, for example about 15 microns.

[0026] Conventional silicon solar wafer separation utilizes a first IR laser beam having a first wavelength to define a window on the perimeter of a silicon solar cell formed atop a silicon template. The silicon solar cell is then separated from the silicon template. A second laser, having a second wavelength different from the first wavelength, is used to trim the edges of the silicon solar cell to a final controlled dimension. The silicon template can be reclaimed for example via a chemical treatment or ultrasonic treatment.

[0027] The inventors have observed that the method 100 advantageously uses a single laser cutting process to separate a silicon solar wafer instead of the conventional dual laser separation processes described above. The use of the water collimated laser also advantageously enables solar cell manufacturing with templates and wafers of equal size instead of using oversized templates as in the conventional process described above.

[0028] In addition, directing the water-collimated laser along the lateral edge of the silicon template (*i.e.*, off the field defined by the template), minimizes epitaxial silicon redeposition, which improves silicon solar cell yield. Another advantage of the method 100 described above is that the water-collimated laser minimizes the heat affected zone which reduces epitaxial silicon redeposition on the template surface and also reduces cracking at the laser edge, providing significant yield enhancement. Minimizing the heat affected zone also advantageously prevents the porous silicon from fusing to the template which improves the exfoliation yield. Another advantage of the method 100 described above is that the water-collimated laser does not utilize complex and costly focal length adjustment typically used for conventional lasers.

[0029] Next, at 110, as depicted in Figure 2E, the silicon layer 208 (e.g., the solar wafer) is lifted or peeled from atop the porous silicon layer 200 using for example a vacuum process.

[0030] In some embodiments, at 102, as depicted in Figure 3A, the porous silicon layer 200 encompasses an outer surface 300 of the silicon template 202. The porous silicon layer 200 is formed as described above with respect to Figure 2A. The porous silicon layer 200 is annealed, as described at 104 above, to reorganize the surface of the porous silicon layer 200. In some embodiments, at 106 and as depicted in Figure 3B, the silicon layer 208 is formed to encompass an outer surface 302 of the reorganized porous silicon layer 200. In some embodiments, at 108 and as depicted in Figure 3C, the silicon layer 208 and the porous silicon layer 200 are cut via a water-collimated laser beam 212 along the lateral edge 214 of the silicon template 202. The water-collimated laser beam 212 is applied perpendicular to a horizontal surface 218 of the silicon layer 208. At 110 and as depicted in Figure 3D, the silicon layer 208 (i.e. the solar wafer) is lifted or peeled from atop the porous silicon layer 200 using for example a vacuum process.

[0031] Figure 4 is a flow diagram of a method 400 for dicing a semiconductor wafer comprising a plurality of integrated circuits in accordance with some embodiments of the present disclosure. Figures 5A-5D are illustrative cross-sectional views of a substrate during different stages of the processing sequence of Figure 4 in accordance with some embodiments of the present disclosure.

[0032] The method 400 begins at 402, as depicted in Figure 5A, by forming porous silicon in device perforation areas 506 that separate a plurality of integrated circuits 504.

[0033] The device perforation areas 506 do not contain integrated circuits 504 and are designated as locations along which the semiconductor wafer 502 will be diced. In some embodiments, the device perforation areas 506 are selectively electrochemically etched to form porous silicon. Selective electrochemical etching can be done by using a grid of platinum wire electrodes aligned to the device perforation areas 506. In some embodiments, the porous silicon is formed in the device perforation areas 506 by masking the integrated circuits 504 with a patterned mask layer to prevent acid in the electrolyte solution from contacting the integrated

circuits 504. The patterned mask layer may be any suitable mask layer such as a hard mask or photoresist layer. The patterned mask layer may be formed by any process suitable to form a patterned mask layer capable of providing an adequate template for defining a pattern. For example, in some embodiments, the patterned mask layer may be formed via a patterned etch process.

[0034] In an embodiment, semiconductor wafer 502 is composed of a material suitable to withstand a fabrication process and upon which semiconductor processing layers may suitably be disposed. For example, in one embodiment, semiconductor wafer 502 is composed of a group IV-based material such as, but not limited to, crystalline silicon, germanium or silicon/germanium. In a specific embodiment, providing semiconductor wafer 502 includes providing a monocrystalline silicon substrate. In a particular embodiment, the monocrystalline silicon substrate is doped with impurity atoms. In another embodiment, semiconductor wafer 502 is composed of a III-V material such as, e.g., a III-V material substrate used in the fabrication of light emitting diodes (LEDs).

[0035] In an embodiment, semiconductor wafer 502 has disposed, as a portion of the integrated circuits 504, an array of semiconductor devices. Examples of such semiconductor devices include, but are not limited to, memory devices or complimentary metal-oxide-semiconductor (CMOS) transistors fabricated in a silicon substrate and encased in a dielectric layer. A plurality of metal interconnects may be formed above the devices or transistors, and in surrounding dielectric layers, and may be used to electrically couple the devices or transistors to form the integrated circuits 504. Materials making up the device perforation areas 506 may be similar to or the same as those materials used to form the integrated circuits 504. For example, device perforation areas 506 may be composed of layers of dielectric materials, semiconductor materials, and metallization. In one embodiment, one or more of the device perforation areas 506 includes test devices similar to the actual devices of the integrated circuits 504.

[0036] Next, at 404, and depicted in 5A, a thin polyvinyl alcohol (PVA) film 500 is applied to the semiconductor wafer 502 to cover the integrated circuits 504. In some embodiments, the thickness of the thin PVA film 500 is about 1 to about 2 microns.

The purpose of the thin PVA mask is to protect the underlying integrated circuits from damage during the dicing process.

[0037] Next, at 406, and as depicted at Figure 5B, the semiconductor wafer 502 is cut at the device perforation areas 506 to singulate the plurality of integrated circuits 504. In some embodiments, the semiconductor wafer 502 is cut via any suitable dicing method such as a dicing saw, conventional laser, or a water-collimated laser beam. As depicted in 5C, the thin PVA film 500 is removed following the singulation process. The inventors have observed that the method 400 advantageously improves die yield. The conversion from silicon to porous silicon in the device perforation areas 506 advantageously reduces chipping and edge cracking along the edges of the integrated circuits 504 during dicing.

[0038] Figure 6 is a flow diagram of a method 600 for dicing a semiconductor wafer comprising a plurality of integrated circuits in accordance with some embodiments of the present disclosure. Figures 7A-7D are illustrative cross-sectional views of a substrate during different stages of the processing sequence of Figure 6 in accordance with some embodiments of the present disclosure.

[0039] The method 600 begins at 602, as depicted in Figure 7A, laser scribing the semiconductor wafer 700 to form trenches 702 partially into but not through the semiconductor wafer between the plurality of integrated circuits 704. In some embodiments, the laser scribing is to a depth at least lower than device layers on the substrate (e.g., oxide and nitride device layers) and into an underlying bulk silicon. In some embodiments, laser scribing is performed using a laser having a pulse width in the femtosecond range. Specifically, a laser with a wavelength in the visible spectrum plus the ultra-violet (UV) and infra-red (IR) ranges (totaling a broadband optical spectrum) may be used to provide a femtosecond-based laser, i.e., a laser with a pulse width on the order of the femtosecond (e.g., about 10–15 femtoseconds). Next at 604, and as depicted in Figure 7B, the semiconductor wafer is cut via a water-collimated laser beam 706 through the trenches 702 to form corresponding trench extensions and singulate the plurality of integrated circuits 704. In some embodiments, a thin PVA film can be applied to the semiconductor wafer 700 to cover the integrated circuits 704. In some embodiments, the laser scribing at 602 and cutting the semiconductor wafer at 604 are each performed at

atmospheric pressure (e.g., not at vacuum). The inventors have observed that the method 600 advantageously improves die yield. Cuts via a water-collimated laser beam 706 have minimal edge cracking, minimal recast, and minimal heat effects on edges between integrated circuits. Furthermore, the water-collimated laser method is material and equipment compatible with back end packaging which makes the water-collimated laser more production worthy than chemical etching for separating a plurality of integrated circuits. For example, the water-collimated laser method has a negligible heat affected zone and therefore does not use a thick PVA mask which reduces the risk of fluorine and carbon contamination.

[0040] Figure 8 is a flow diagram of a method 800 for processing a substrate in accordance with some embodiments of the present disclosure. Figures 9A-9D are illustrative cross-sectional views of a substrate during different stages of the processing sequence of Figure 8 in accordance with some embodiments of the present disclosure.

[0041] Embodiments of the method 800 generally relate to methods for processing substrates, and may be useful in processing thin semiconductor substrates. For example and without limitation, the method may be useful for generating silicon substrates, silicon germanium (SiGe) substrates, or gallium arsenide (GaAs) substrates. Embodiments of the disclosed method may be useful in generating other substrates as well. In at least some embodiments, the inventive methods may advantageously affect production costs by reducing or eliminating waste as compared to some conventional processes used to form thin substrates. In some embodiments, a thin substrate is one with a thickness of about 300 μm or less. While not intending to be limiting in scope, the inventors have observed that the inventive methods may be particularly advantageous in the fabrication of monocrystalline silicon substrates which may be useful in, for example, solar cells.

[0042] The method begins at 802 by providing a starting double-sided template (template 900), as depicted in Figure 9A, upon which a silicon substrate, for example a solar cell, will be formed. In some embodiments, the template 900 is a monocrystalline (100) silicon wafer. The template 900 may be any shape suitable for forming a silicon substrate, such as circular, square, or rectangular. The template 900 may be formed from any process compatible material, including, as

non-limiting examples, silicon and gallium-arsenide. The template 900 may have a thickness suitable for forming a silicon substrate. The template 900 comprises a first surface 902, an opposing second surface 904, and an edge 906 connecting the first surface 902 and the second surface 904. The template 900 is a double sided template (e.g. suitable for forming a silicon substrate on the first surface 902 and the second surface 904). The first surface 902 and the second surface 904 are polished, non-textured surfaces. The first surface 902 and the second surface 904 can undergo double sided lapping or buffing processes to produce polished, or substantially polished, and texture-free surfaces.

[0043] Next at 804, and as depicted in Figure 9B, a porous silicon layer 908 is formed on the first surface 902, on the second surface 904, and on the edge 906. Forming the porous silicon layer 908 on the first surface 902 and also on the edge 906 (e.g. a “wrap-around” porous silicon layer 908) improves porous silicon quality near the edge of the template 900 and allows the process to be compatible with the epitaxial formation and laser scribing methods described above and depicted in Figures 3A-3D.

[0044] The porous silicon layer 908 is formed by electrochemical anodic etching of silicon on the first surface 902, on the second surface 904, and on the edge 906. In some embodiments, the electrochemical anodic etch is performed by immersing the template in a solution comprising hydrogen fluoride (HF), or hydrogen fluoride (HF) and an acetic acid, or hydrogen fluoride (HF) and isopropyl alcohol (IPA). In some embodiments, the solution consists of, or consists essentially of hydrogen fluoride (HF), or hydrogen fluoride (HF) and an acetic acid, or hydrogen fluoride (HF) and isopropyl alcohol (IPA). During the porous silicon formation, the electrical current polarity is periodically switched between positive and negative currents so that each side of the template 900 is successively etched in order to form a porous silicon structure on both template sides. In some embodiments, the current intensity is also adjusted to form a multilayer porous silicon layer having predetermined different porosities. For example, a high porosity (e.g. 40%-80%) first silicon layer can be formed on the template 900 (e.g. directly on the template 900) to facilitate releasing a subsequently formed semiconductor wafer due to the low-density physical connections and weak mechanical strength of the high porosity first silicon layer and

a low porosity (e.g. 15% to 30%) second silicon layer can be formed on the high porosity first silicon layer to act as a crystalline seed layer for subsequent high quality epitaxial silicon growth.

[0045] An exemplary apparatus for forming a “wrap-around” porous silicon layer 908 is described in commonly owned United States Patent Publication 2016/0298263, entitled “PROCESS GAS PREHEATING SYSTEMS AND METHODS FOR DOUBLE-SIDED MULTI-SUBSTRATE BATCH PROCESSING”, by Ishikawa, et al. Each template 900 is held at the second surface 904 proximate the edge 906. As described above, holding the templates 900 at the second surface 904 and not at the edge 906 allows for the formation of a “wrap-around” porous silicon layer 908. However, holding the template at the second surface 904 form an exclusion zone 910 which is an area of the second surface 904 proximate the edge 906 where the porous silicon layer does not form.

[0046] Returning to Figure 10, power supply 1002 provides power with current intensity control, time control, and polarity switching capability to electrodes 1004. The passage of electrical current creates porous silicon layers 908. One of ordinary skill will understand that different electrolyte volumes and concentrations, etch chamber sizes, distances between adjacent templates, current levels, and polarities may be used.

[0047] Next at 806, the template 900 having the porous silicon layer 908 is annealed. The template 900 is annealed at a temperature of about 1000 to about 1300 degrees Celsius. The template is annealed in a hydrogen (H₂) gas atmosphere. While annealing, the template 900 is subjected to a gettering process to remove metallic contamination from the template 900. Metallic impurities (e.g. platinum from the electrodes 1004; nickel, copper, and iron contamination from walls of the process chamber 1000) can contaminate the template 900 during the anodic etch process discussed at 804 above.

[0048] The gettering process exposes the template 900 to a sufficient temperature for a sufficient amount of time for the metallic impurities in the template 900 to become mobile. The metallic impurities migrate to a location where they are “gettered” (*i.e.* rendered electrically inactive or removed from the active region). In some embodiments, gettering of the template 900 is performed in an atmosphere

comprising, or in some embodiments consisting or consisting essentially of, hydrogen chloride (HCl) gas atmosphere at the anneal temperature described above, where the hydrogen chloride (HCL) reacts with metal impurities to form a volatile metal chloride species. In some embodiments, gettering of the template 900 is performed in an atmosphere comprising, or in some embodiments consisting or consisting essentially of, trichlorosilane (HCl_3Si) gas and hydrogen (H_2) gas at the anneal temperature described above. In some embodiments, gettering of the template 900 is performed in an atmosphere comprising, or in some embodiments consisting or consisting essentially of, silicon tetrachloride (SiCl_4) gas and hydrogen (H_2) gas at the anneal temperature described above.

[0049] Next at 808, and as depicted in Figure 9C, a silicon layer is epitaxially formed on the template 900. The epitaxial silicon layer 912 is formed on the porous silicon layer 908 at the first surface 902, the second surface 904 (except the exclusion zone 910 of the second surface 904 proximate the edge 906 where the susceptors support the template 900) and the edge 906. In some embodiments, the epitaxial silicon layer 912 is via any suitable epitaxial deposition process known in the art. In some embodiments, the epitaxial silicon layer 912 is formed to a thickness of about 140 to about 160 microns. At the thickness range discussed, the epitaxial silicon layer 912 can be removed from the template as discussed below without the need for reinforcement plates on the epitaxial silicon layer 912.

[0050] Next at 810, and as depicted in Figure 9D, the epitaxial silicon layer 912 is separated (e.g. exfoliated) from the template 900. As described above with respect to Figure 3C-3D, the epitaxial silicon layer 912 and the porous silicon layer 908 are cut via a water-collimated laser beam along the edge 906 of the template 900. The water-collimated laser beam is applied perpendicular to a horizontal surface of the epitaxial silicon layer 912. The epitaxial silicon layer 912 is lifted or peeled from atop the porous silicon layer 908 using for example a vacuum process.

[0051] In some embodiments, an anisotropic etch may be performed to clear residual reorganized porous silicon material proximate the edge 906 of the template 900 prior to exfoliation at 810 to prevent breakage of the epitaxial silicon layer 912 during exfoliation. The laser scribed epitaxial silicon layer 912 is placed in a reclamation chemistry and prior to initiating exfoliation which improves exfoliation

yield without the need for a separate etch bath. Thin epitaxial silicon layer 912 can be allowed to float in the reclamation chemistry after separation, and then mounted to an adhesive-backed film.

[0052] Next, at 812 the exfoliated epitaxial silicon layer 912 is textured via isotexture etching on one or both surfaces 914, 916 of the epitaxial silicon layer 912. The advantage of texturing the epitaxial silicon layer 912 after exfoliation is provide a smooth emitter-face and improved process control of the texture process.

[0053] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof.

Claims:

1. A method of separating a silicon substrate from atop a silicon template, comprising:
 - (a) forming a porous silicon layer atop a silicon template;
 - (b) annealing the porous silicon layer to reorganize the porous silicon layer to form a low porosity seed zone and an exfoliation zone;
 - (c) depositing an epitaxial silicon layer atop the reorganized porous silicon layer to form a silicon substrate;
 - (d) cutting the silicon substrate and the reorganized porous silicon layer along a lateral edge of the silicon template via a water-collimated laser beam without cutting the silicon template; and
 - (e) separating the silicon substrate from atop the reorganized porous silicon layer.
2. The method of claim 1, wherein forming the porous silicon layer further comprises forming a porous silicon layer atop an upper surface of the silicon template.
3. The method of claim 2, wherein cutting the epitaxial silicon layer and the porous silicon layer further comprises forming a bevel along the lateral edge having an angle of about 45 degrees or greater and less than about 90 degrees from a horizontal surface of the epitaxial silicon layer.
4. The method of claim 1, wherein forming the porous silicon layer further comprises forming a porous silicon layer encompassing an outer surface of the silicon template.
5. The method of claim 4, wherein forming the epitaxial silicon layer further comprises forming the epitaxial silicon layer encompassing an outer surface of the porous silicon layer.

6. The method of claim 5, wherein cutting the epitaxial silicon layer and the porous silicon layer further comprises applying a water-collimated laser beam along the lateral edge of the silicon template and perpendicular to a horizontal surface of the epitaxial silicon layer.
7. The method of claim 1, wherein the water-collimated laser beam uses a liquid source comprising a mixture of water and solvent.
8. The method of claim 7, wherein the mixture comprises about 5 to about 100 percent solvent and a balance water.
9. The method of claim 1, where in the silicon substrate is a silicon solar wafer.
10. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:
 - (a) forming porous silicon in device perforation areas between a plurality of integrated circuits on the semiconductor wafer;
 - (b) applying a thin polyvinyl alcohol (PVA) mask atop the plurality of integrated circuits; and
 - (c) cutting the semiconductor wafer to singulate the plurality of integrated circuits.
11. The method of claim 10, wherein cutting the semiconductor wafer further comprises cutting the semiconductor wafer via a dicing saw.
12. The method of claim 10, wherein cutting the semiconductor wafer further comprises cutting the semiconductor wafer via a water-collimated laser beam.
13. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:
 - (a) laser scribing the semiconductor wafer to form trenches partially into but not through the semiconductor wafer between the plurality of integrated circuits; and

(b) cutting the semiconductor wafer via a water-collimated laser beam through the trenches to form corresponding trench extensions and singulate the plurality of integrated circuits.

14. The method of claim 13, wherein the laser scribing and the cutting are performed at atmospheric pressure.

15. The method of claim 13, wherein the laser scribing is to a depth passing through device layers formed on the semiconductor wafer and partially into a bulk silicon of the semiconductor wafer.

1/8

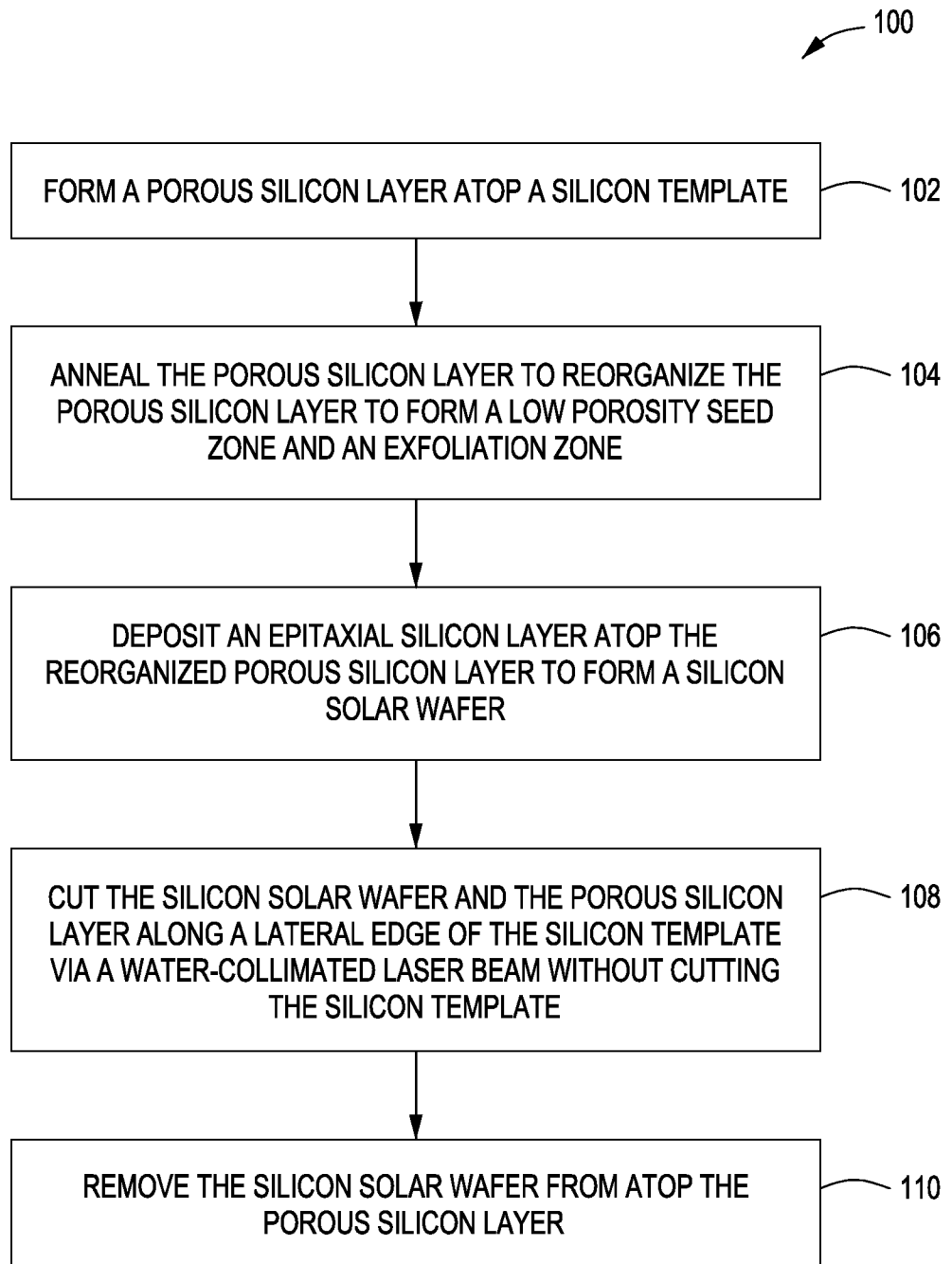


FIG. 1

2/8

FIG. 2A

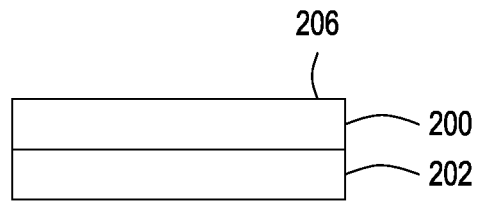


FIG. 2B

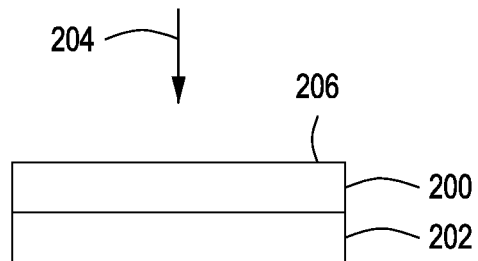


FIG. 2C

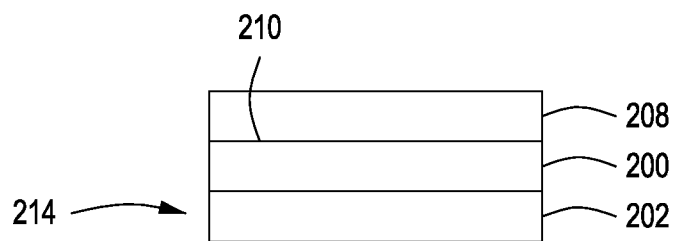


FIG. 2D

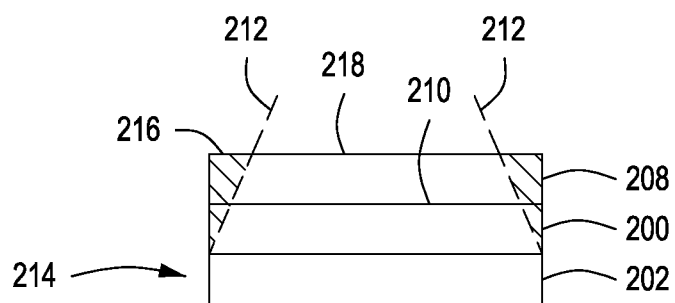
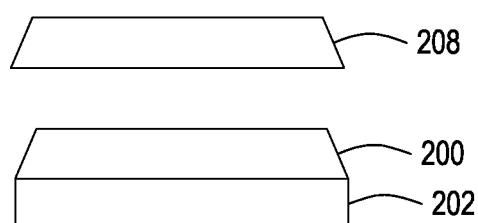


FIG. 2E



3/8

FIG. 3A

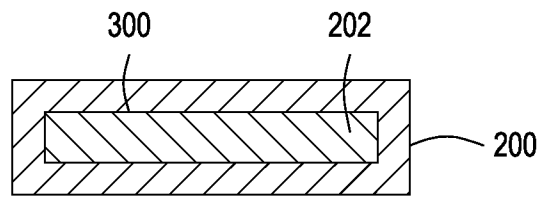


FIG. 3B

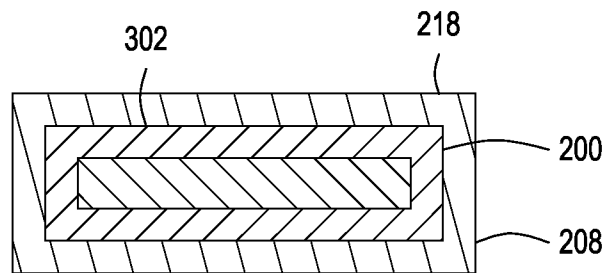


FIG. 3C

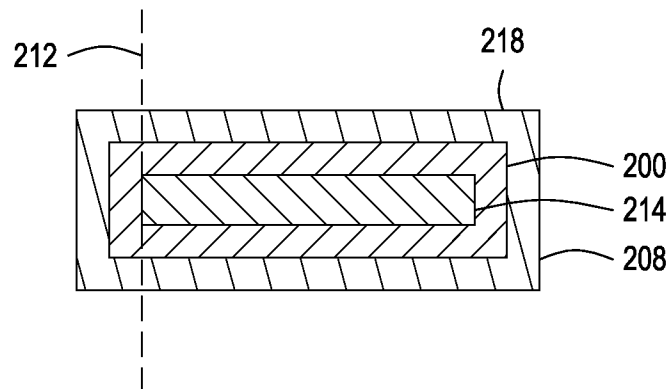
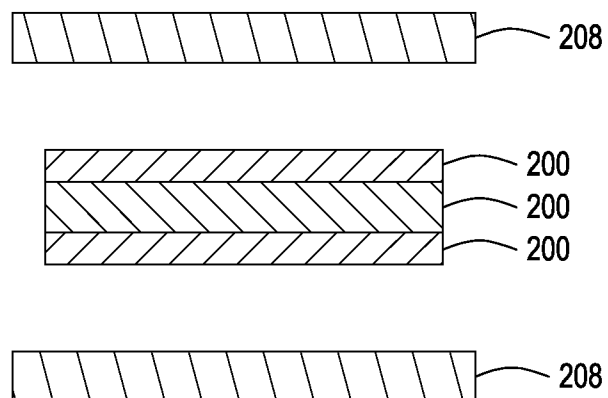


FIG. 3D



4/8

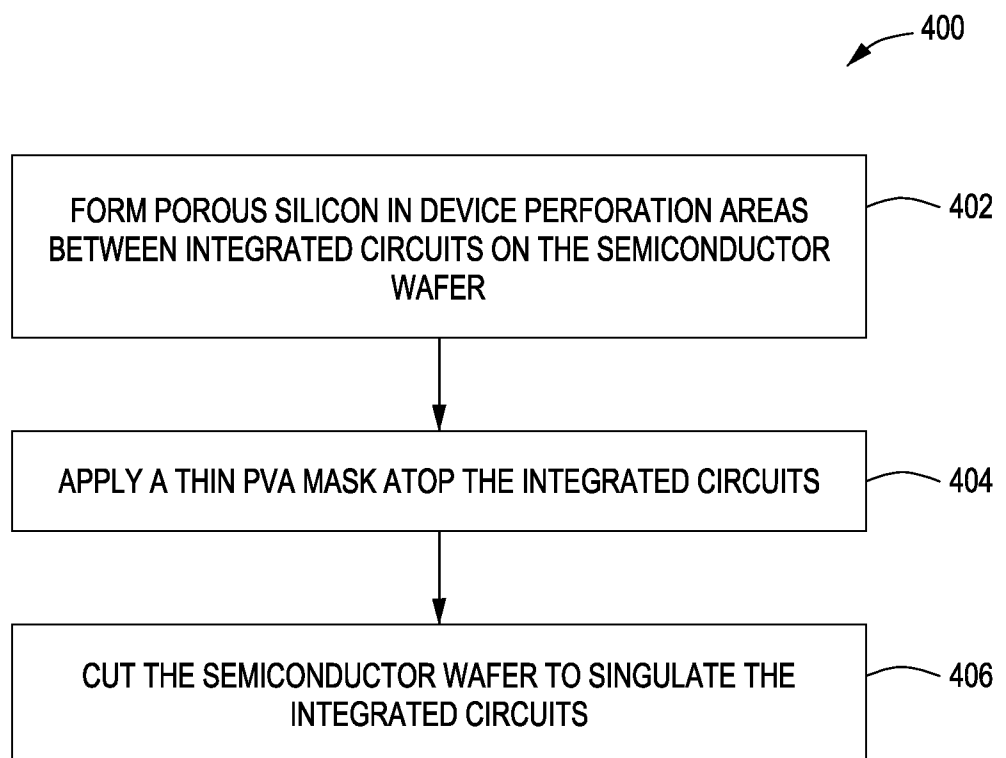


FIG. 4

5/8

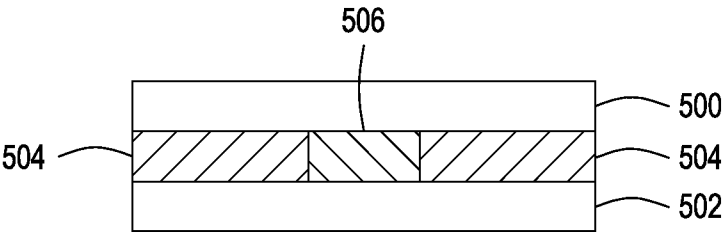


FIG. 5A

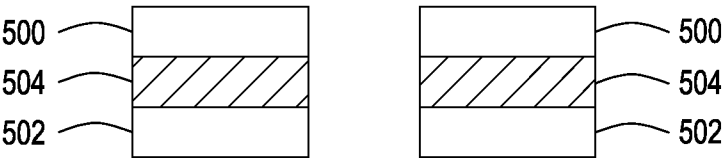


FIG. 5B

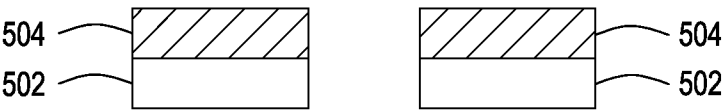


FIG. 5C

6/8

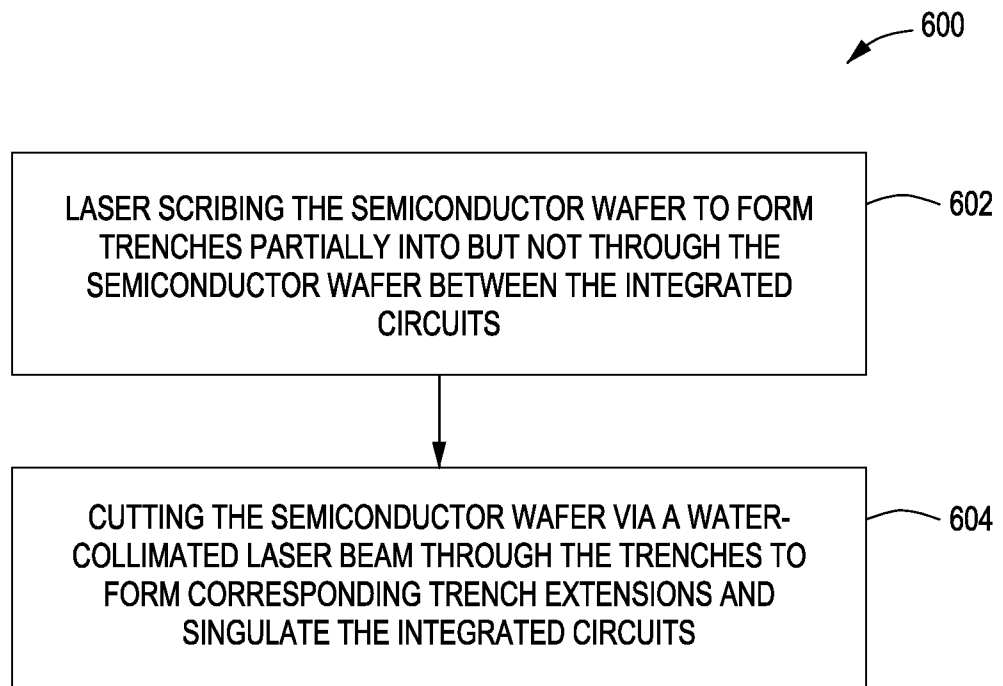


FIG. 6

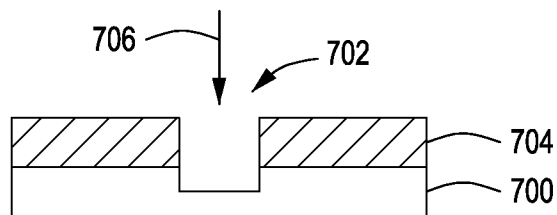


FIG. 7A

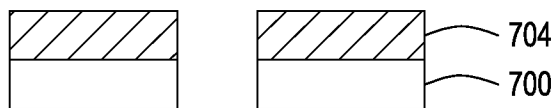


FIG. 7B

7/8

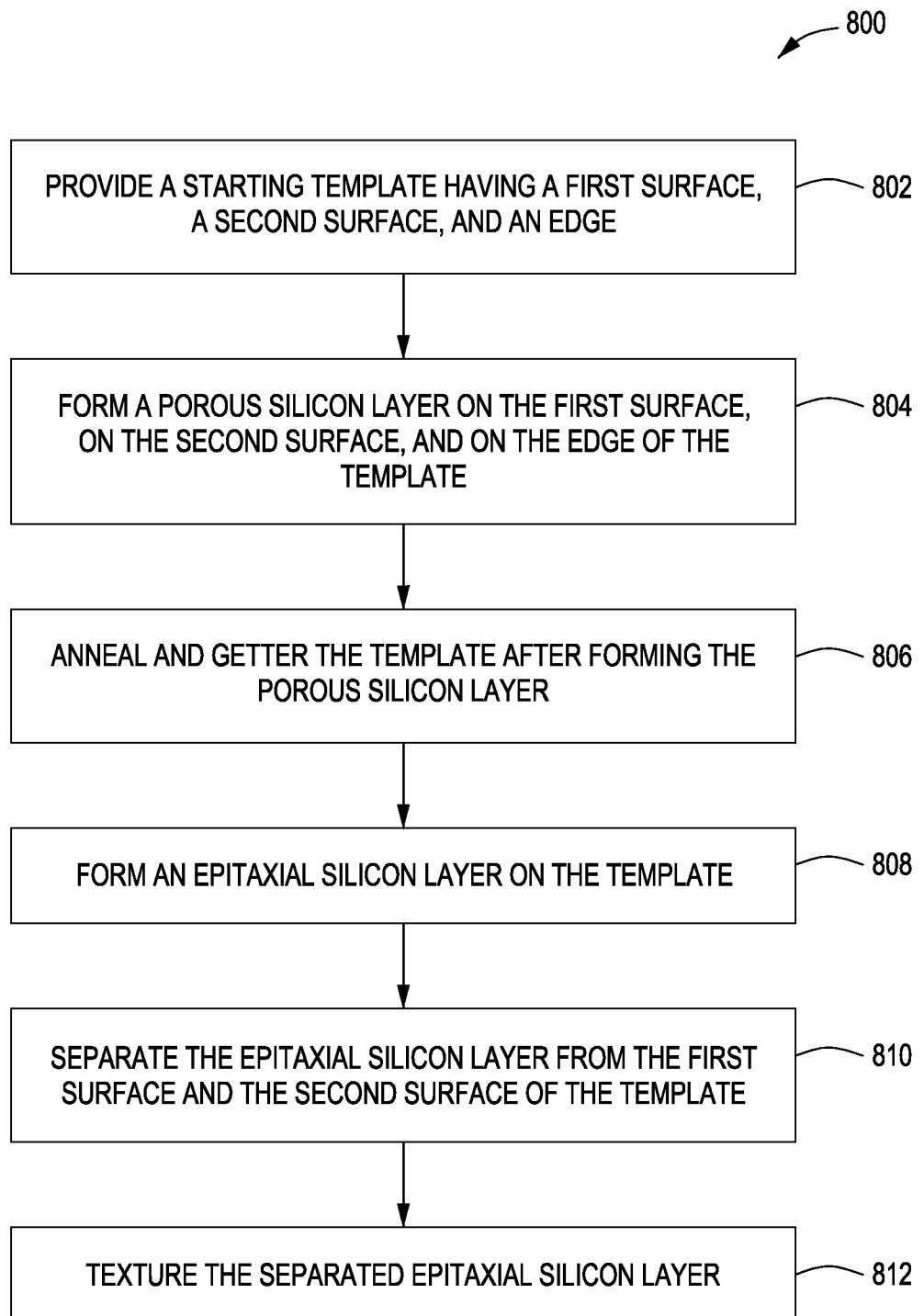


FIG. 8

8/8

FIG. 9A

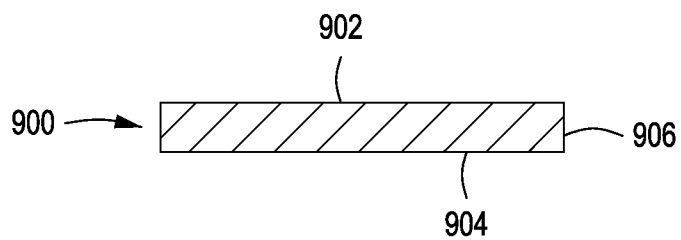


FIG. 9B

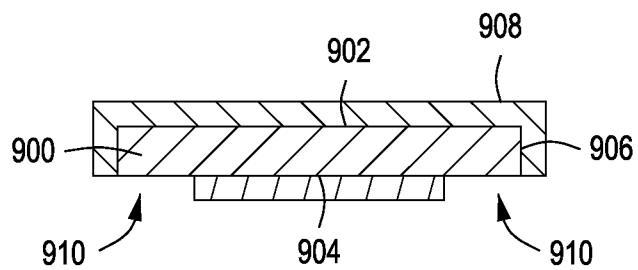


FIG. 9C

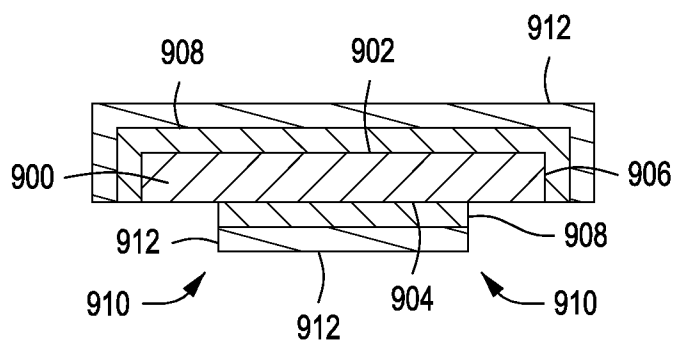
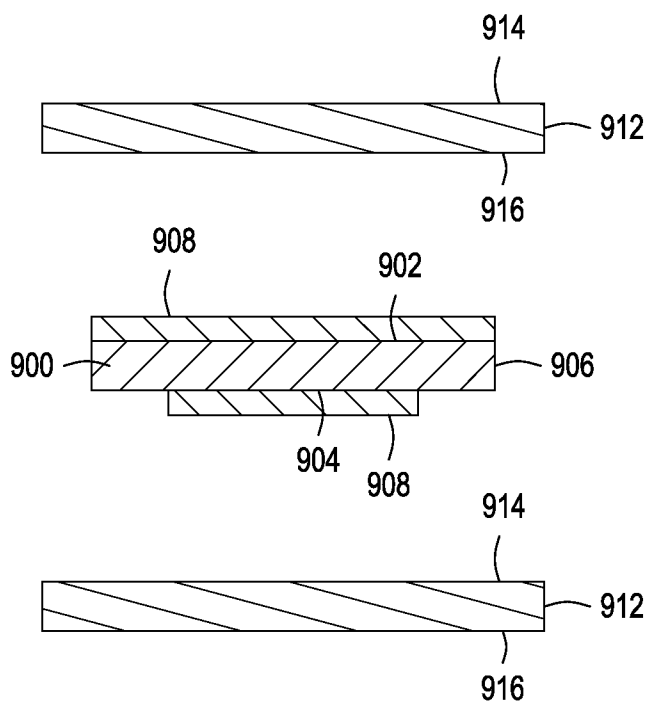


FIG. 9D



Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Group I: Claims 1-9 are directed to a method of separating a silicon substrate from atop a silicon template.

Group II: Claims 10-12 are directed to a method comprising: forming porous silicon in device perforation areas between a plurality of integrated circuits on a semiconductor wafer; and applying a thin polyvinyl alcohol (PVA) mask atop the plurality of integrated circuits.

Group III: Claims 13-15 are directed to a method comprising laser scribing a semiconductor wafer to form trenches partially into but not through the semiconductor wafer between a plurality of integrated circuits.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☒ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2017/016429**A. CLASSIFICATION OF SUBJECT MATTER****H01L 31/18(2006.01)i, H01L 31/0392(2006.01)i, H01L 21/78(2006.01)i, H01L 21/268(2006.01)i, H01L 21/324(2006.01)i, H01L 21/20(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 31/18; H01L 21/20; B23K 26/38; H01L 21/02; H01L 21/762; H01L 21/78; H01L 21/822; C04B 41/91; H01L 21/44; H01L 31/0392; H01L 21/268; H01L 21/324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: silicon template, porous silicon layer, cutting, dicing, semiconductor wafer, singulation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013-0137244 A1 (KARL-JOSEF KRAMER et al.) 30 May 2013 See paragraphs [0104]-[0112]; and claim 1.	1-9
A	WO 2010-034725 A2 (INSTITUT FUER SOLARENERGIEFORSCHUNG GMBH) 01 April 2010 See page 9, line 33 - page 10, line 36; claim 1; and figure 1.	1-9
A	JP 10-233352 A (CANON, INC.) 02 September 1998 See paragraphs [0085]-[0087]; claim 1; and figure 1.	1-9
X	US 2014-0015109 A1 (WEI-SHENG LEI et al.) 16 January 2014 See paragraphs [0006], [0032], [0035], [0043]; claims 1, 8; and figures 1, 4A, 4C.	10-12
A	US 2003-0100143 A1 (ROSE A. MULLIGAN et al.) 29 May 2003 See paragraphs [0030]-[0035]; and figures 1-5.	10-12
X	US 2014-0120697 A1 (APPLIED MATERIALS, INC.) 01 May 2014 See paragraphs [0053], [0057]-[0060]; claims 1, 6; and figures 9A-9D.	13-15
A	WO 03-002289 A1 (ELECTRO SCIENTIFIC INDUSTRIES, INC.) 09 January 2003 See paragraphs [0115]-[0117]; claim 1; and figure 15.	13-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

21 June 2017 (21.06.2017)

Date of mailing of the international search report

21 June 2017 (21.06.2017)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/016429

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013-0137244 A1	30/05/2013	KR 10-1289789 B1 KR 10-1384872 B1 KR 10-1389030 B1 US 2012-0125256 A1 US 2012-0167819 A1 WO 2012-021880 A2 WO 2012-021880 A3 WO 2012-099701 A1 WO 2012-162704 A2 WO 2012-162704 A3	26/07/2013 18/04/2014 29/04/2014 24/05/2012 05/07/2012 16/02/2012 10/05/2012 26/07/2012 29/11/2012 28/03/2013
WO 2010-034725 A2	01/04/2010	DE 102008048498 A1 WO 2010-034725 A3	08/04/2010 23/09/2010
JP 10-233352 A	02/09/1998	AU 1997-48462 B2 CA 2225131 A1 CA 2225131 C CN 1150594 C CN 1190248 A EP 0849788 A2 EP 0849788 A3 EP 0849788 B1 JP 2005-101630 A JP 3927977 B2 JP 3962465 B2 KR 10-0304161 B1 TW 410477 A US 2003-0203547 A1 US 6100166 A US 6534382 B1	24/01/2002 18/06/1998 01/01/2002 19/05/2004 12/08/1998 24/06/1998 10/02/1999 10/03/2004 14/04/2005 13/06/2007 22/08/2007 30/11/2001 01/11/2000 30/10/2003 08/08/2000 18/03/2003
US 2014-0015109 A1	16/01/2014	CN 104412368 A JP 2015-528211 A KR 10-2015-0030771 A TW 201405651 A US 2015-0102467 A1 US 8940619 B2 WO 2014-011378 A1	11/03/2015 24/09/2015 20/03/2015 01/02/2014 16/04/2015 27/01/2015 16/01/2014
US 2003-0100143 A1	29/05/2003	AU 2002-357722 A1 CN 1666332 A EP 1449250 A2 MY 129398 A US 6838299 B2 WO 03-046980 A2 WO 03-046980 A3	10/06/2003 07/09/2005 25/08/2004 30/03/2007 04/01/2005 05/06/2003 23/10/2003
US 2014-0120697 A1	01/05/2014	CN 102986006 A CN 102986006 B	20/03/2013 13/01/2016

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/016429

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 03-002289 A1	09/01/2003	CN 105428281 A	23/03/2016
		JP 2013-535114 A	09/09/2013
		JP 2015-057840 A	26/03/2015
		JP 2015-109450 A	11/06/2015
		JP 5688453 B2	25/03/2015
		KR 10-1511648 B1	13/04/2015
		KR 10-2013-0083381 A	22/07/2013
		KR 10-2014-0083065 A	03/07/2014
		KR 10-2015-0005670 A	14/01/2015
		TW 201205658 A	01/02/2012
		TW 201434084 A	01/09/2014
		TW 201508833 A	01/03/2015
		TW I488229 B	11/06/2015
		TW I520204 B	01/02/2016
		TW I547987 B	01/09/2016
		US 2011-0312157 A1	22/12/2011
		US 2014-0367041 A1	18/12/2014
		US 2016-0141210 A1	19/05/2016
		US 8642448 B2	04/02/2014
		US 8853056 B2	07/10/2014
		US 9245802 B2	26/01/2016
		WO 2011-163149 A2	29/12/2011
		WO 2011-163149 A3	12/04/2012
		AU 2001-49140 A1	02/04/2002
		AU 2001-93288 A1	02/04/2002
		CA 2436736 A1	08/08/2002
		CA 2449574 A1	19/12/2002
		CN 1516635 A	28/07/2004
		CN 1516635 C	08/02/2006
		CN 1527754 A	08/09/2004
		CN 1527754 C	21/02/2007
		CN 1788916 A	21/06/2006
		CN 1788916 B	25/07/2012
		EP 1365880 A1	03/12/2003
		GB 2389811 A	24/12/2003
		JP 2004-526575 A	02/09/2004
		JP 2004-528991 A	24/09/2004
		JP 4551086 B2	22/09/2010
		JP 4634692 B2	16/02/2011
		KR 10-0853827 B1	22/08/2008
		KR 10-0877936 B1	12/01/2009
		TW 525240 A	21/03/2003
		TW 583045 A	11/04/2004
		US 2002-0033558 A1	21/03/2002
		US 2002-0063361 A1	30/05/2002
		US 2002-0149136 A1	17/10/2002
		US 2002-0190435 A1	19/12/2002
		US 2006-0091126 A1	04/05/2006
		US 6676878 B2	13/01/2004

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/016429Patent document
cited in search reportPublication
datePatent family
member(s)Publication
date

US 7157038 B2	02/01/2007
WO 02-060636 A1	08/08/2002
WO 02-100587 A1	19/12/2002
WO 02-24395 A1	28/03/2002
WO 02-24396 A1	28/03/2002