Feb. 6, 1968 I. R. MARCUS 3,368,199

TWO-WIRE SETTING SYSTEM FOR ELECTRIC TIMERS

Filed Jan. 22, 1964 2 Sheets-Sheet 1

FIG. 1

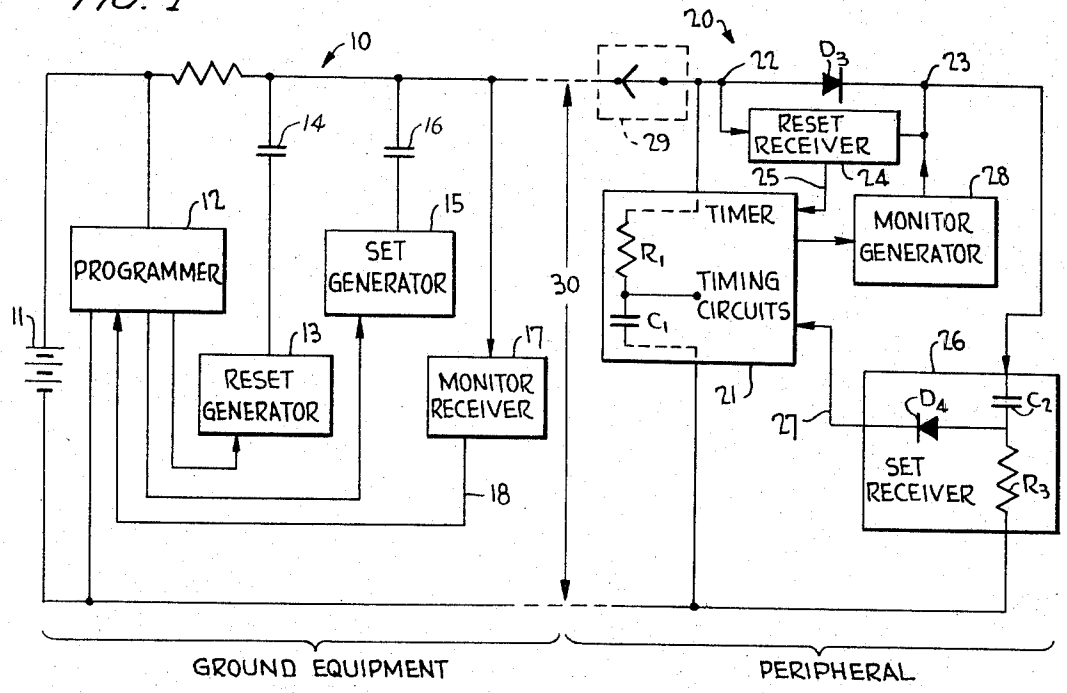
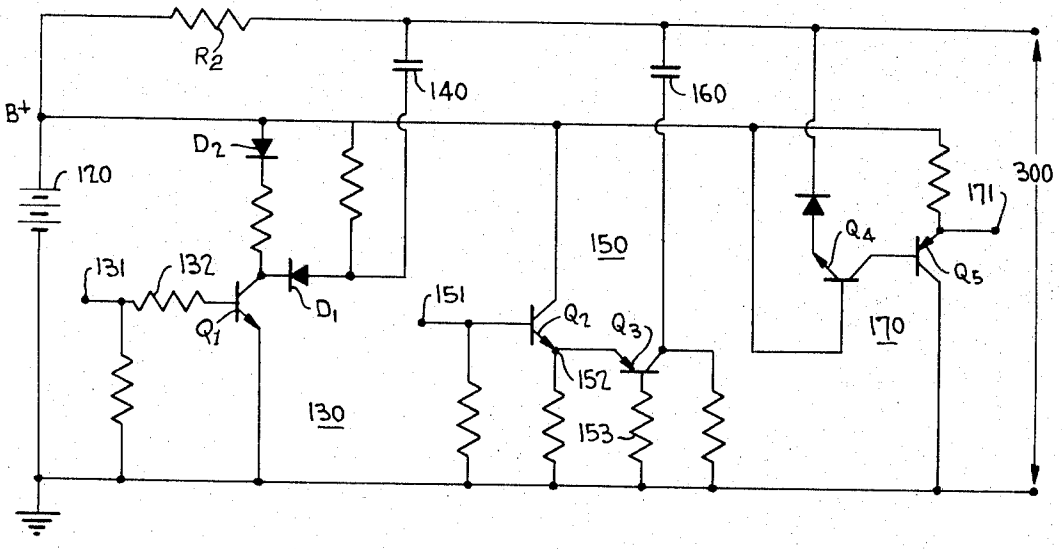


FIG. 2a



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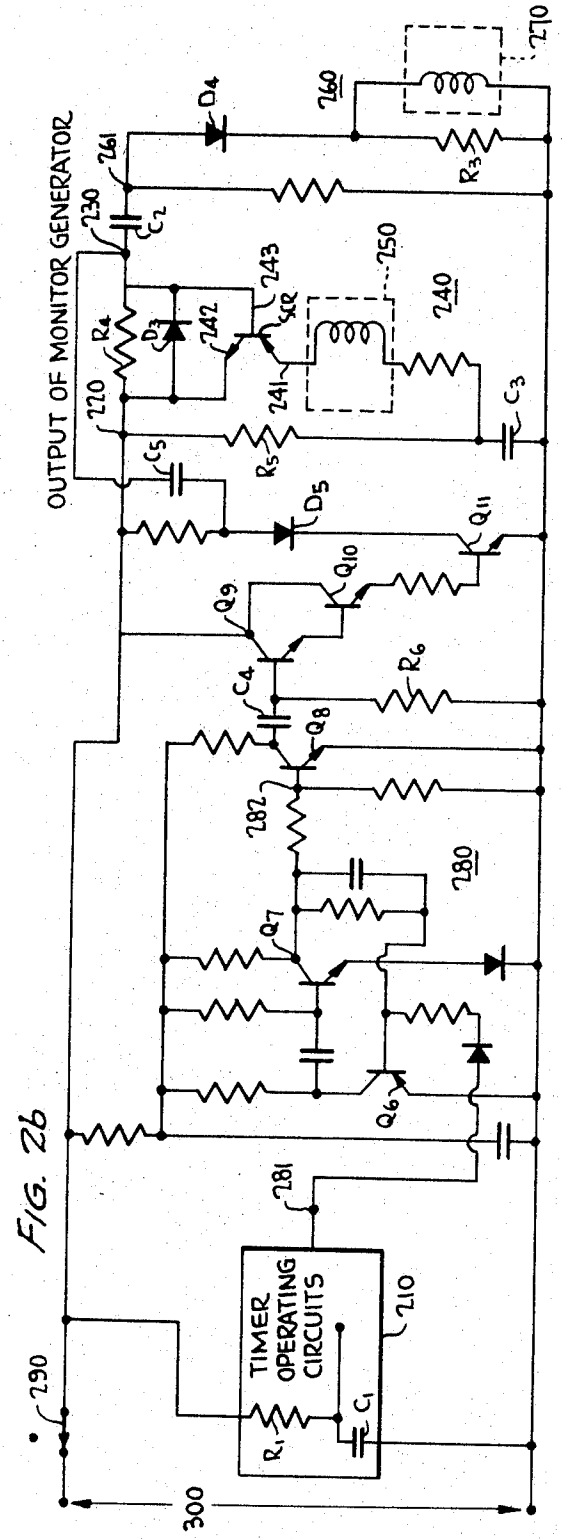

FIG. 2b

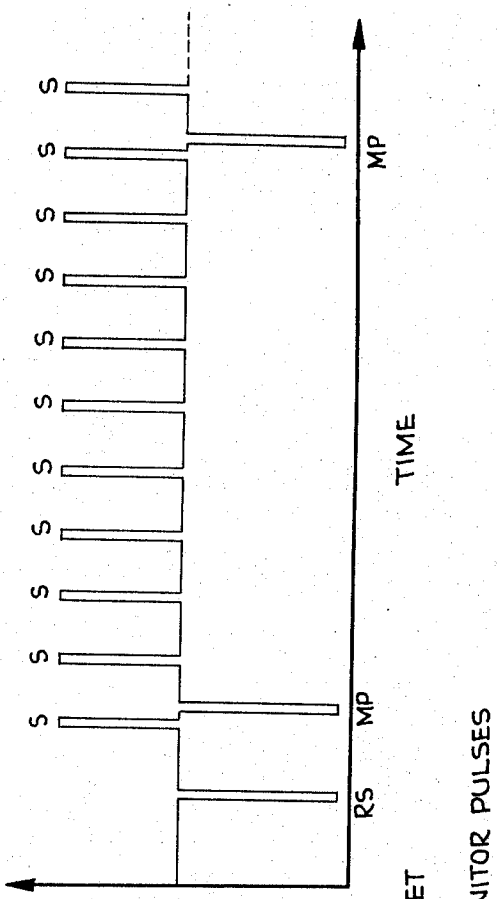

FIG. 3

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United States Patent Office 3,368,199
Patented Feb. 6, 1968

3,368,199

TWO-WIRE SETTING SYSTEM FOR ELECTRIC TIMERS

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Filed Jan. 22, 1964, Ser. No. 339,560
2 Claims. (Cl. 340—147)

ABSTRACT OF THE DISCLOSURE

A means for resetting, setting and monitoring a timer using only a two-wire communication line. Each phase of the operating cycle is controlled by a programmer. A reset generator transmits a pulse via the two wire line to a reset receiver which communicates the pulse to the timer. A set generator transmits a series of pulses of a predetermined number via the two wire line to a set pulse receiver which communicates these pulses to the timer for setting purposes. After the timer has received a predetermined number of set pulses a monitor generator is activated and a pulse emanating therefrom is transmitted to a monitor receiver via the two-wire communication line.

The invention described herein may be manufactured and used by or for the Government of the United States of America for governmental purposes without the payment to me of any royalty thereon.

This invention relates generally to two-wire communication systems and more particularly to a remote two-wire setting system for powering, resetting, setting and monitoring a timer.

Timers have applications in many types of control systems, and in such systems timers usually contain memory devices which may, for example, be cascaded counting circuits. It is necessary that the memory devices in a timer be set to the proper state initially to cause the outputs to occur at the proper time. It is often desirable and sometimes necessary to set the memory devices from some position remote from the timer.

In the past, two systems for setting the memory devices in timers have been used. In the first of these a wire from each device is brought out to an external switch which sets all the memory devices to the desired states simultaneously. This system has the advantage of allowing remote setting by a simple setting device. It has the disadvantages of requiring multipin connectors and a multiwire cable. The number of connector pins and cable wires severely limits the reliability of the setting system. A further disadvantage of this system is it does not permit dynamic monitoring of the timer to show that the timer has been correctly set and is functioning properly.

In the other setting system, the timer is reset, or in other words, set to its maximum value. Pulses are then sequentially applied to the timer until the memory devices achieve their desired set states. This system has the advantages of allowing remote setting by a lesser number of wires than the first described system and of permitting monitoring of the timer. It has the disadvantages of requiring a more complex setting device and additional wires for resetting and monitoring the timer and for supplying power to the timer.

It is an object of the invention to provide a highly reliable remote setting system for timers.

Another object of the invention is to provide a two-wire communication system for powering, resetting, setting and monitoring a timer.

Briefly described, a preferred embodiment of the present invention takes the form of a two-wire communication line having control and monitoring circuitry connected to the line. Circuitry responsive to the control circuitry for resetting and setting a timer and circuitry cooperative with the monitoring circuitry and responsive to the timer is connected to the line at a point remote from the control and monitoring circuitry. The communication line additionally has a source of power connected to it for supplying power to the timer while the timer is being set.

The specific nature of the invention as well as other objects, aspects, uses and advantages thereof, will clearly appear from the following description and from the accompanying drawings in which:

FIG. 1 is a generalized block diagram of the two-wire setting system of the present invention;

FIGS. 2*a* and 2*b* are schematic diagrams of the preferred embodiment of the two-wire setting system of the present invention; and

FIG. 3 is a timing diagram of the voltage pulses that occur on the two-wire communication line in the setting system of the present invention.

Referring now to the drawings, and more particularly to FIGURE 1 there is shown in block diagram form a first network **10** and a second network **20** interconnected by a two-wire communication line **30**. Additionally there is provided a D.C. power supply **11** for supplying voltage to the timer **21** by way of the communication line. The first network may be considered the ground equipment; and the second ntwork, the peripheral equipment. It is contemplated that the ground equipment and the peripheral equipment will be connected together by the communication line **30** and a two-pin connector, not shown. This would allow the ground equipment to be disconnected from the peripheral equipment. It would then be possible to use one unit of ground equipment to set several units of peripheral equipment by simply disconnecting the communication line from one unit of peripheral equipment and connecting it to another unit.

The ground equipment includes a programmer **12** connected across the power supply **11**. The programmer **12** is connected to and at a certain predetermined time activates a reset generator **13**. The reset generator at such time as it is activated by the programmer generates a negative pulse of short duration. This pulse is coupled to the communication line **30** by way of the capacitor **14**. Referring now to FIGURE 3 of the drawings where this pulse is shown as negative pulse RS, it can be seen that the effect of this pulse is to substantially short circuit the communication line **30**. Referring again to FIGURE 1, the negative pulse generated by the reset generator causes point **22** in the peripheral equipment **20** to assume ground potential. Point **23** is then positive with respect to point **22** since the charge on capacitor C_2 back biases diode D_3. Under this condition the reset receiver **24** is activated and generates a signal on the reset line **25** of the timer **21**.

The programmer **12** additionally is connected to and at certain predetermined times activates set generator **15** in the ground equipment **10**. The set generator at such times as it is activated by the programmer generates positive pulses of short duration. These pulses are coupled to the communication line **30** by way of capacitor **16**. Referring to FIGURE 3, these pulses are shown as positive pulses S over-riding the power supply voltage. Referring again to FIGURE 1, diode D_3 passes the positive pulses generated by the set generator in the ground equipment **10** to the set receiver **26** in the peripheral equipment **20**. The set receiver **26** is activated by the positive pulses and generates signals on the set line **27** of the timer **21**. Since the potential at point **23** is the same as the potential at point **22** for positive pulses appearing on the communication line **30**, the reset receiver **24** is not activated by pulses generated by the set generator **15**.

After the set receiver has received a predetermined number of set pulses, the timer 21 sends a signal to the monitor generator 23 in the peripheral equipment 20. The monitor generator generates a negative pulse delayed with respect to a corresponding set pulse when it receives a signal from the timer. This negative pulse is applied to point 23. This forward biases diode D_3 causing it to conduct, and the negative pulse appears on the communication line 30 at point 22. Referring to FIGURE 3, the monitor pulses are shown as negative pulses MP. Like the reset pulse, the effect of those pulses is to substantially short circuit the communication line. Referring again to FIGURE 1, the monitor receiver 17, in the ground equipment 10 is activated by negative pulses appearing on the communication line 30 and produces a signal on line 18. The programmer 12 performs a comparing function to determine if a monitor pulse is received after the predetermined number of set pulses have been generated by the set generator. If the monitor pulse is not received at the proper time it is an indication of a malfunction of timer 21 or a faulty connection of the communication line 30 to the peripheral equipment 20.

There is additionally shown in FIGURE 1 a line switch 29 in the peripheral equipment 20 which is connected in series with the communication line 30. This switch may be connected to a safety device, not shown, which responds to some condition in the peripheral equipment. It should be noted that the failure to receive a monitor pulse at the time expected may also be an indication that the line switch 29 is open.

The programmer 12, which is not shown in greater detail since the particular circuitry is not necessary to an understanding of the present invention, may simply comprise two manual push-button switches, one for reset and one for set, and a lamp. The switches are followed by suitable pulse forming circuitry which produce suitable signals for activating the reset generator and the set generator. The lamp is caused to light by suitable lamp driver circuitry in response to a pulse received by the monitor receiver. Alternatively, the programmer may be fully automatic requiring only minimual manual operation. For example, there is provided a preset counter driven by an astable multivibrator. The first pulse from the astable multivibrator is used to activate the reset generator. The succeeding pulses are used to activate the set generator and to cause the preset counter to count down to zero. When the counter has counted to zero, the pulses to the set generator are inhibited. At predetermined time intervals, as determined by a counter, a bistable multivibrator is set. If a monitor pulse is not received before the next set pulse is generated, the bistable multivibrator gates any suitable alarm to "on" and inhibits further operation of the programmer.

Reference is now made to FIGURES 2*a* and 2*b* which together show the circuitry of the preferred embodiment of the present invention. It is contemplated that the timers in the peripheral equipments will all have self-contained power supplies. These power supplies are not on during the setting process. An additional power supply 120 is then required for the timer during the setting process in order for the timer to respond to reset and set pulses. It is contemplated that the timer has a non-volatile memory which permits the timer to retain its setting in the absence of power. Such a memory may be, for example, a magnetic core counter. As explained with reference to the generalized block diagram shown in FIGURE 1, the reset and monitor pulses interrupt the voltage to the communication line 30 while the set pulses add to the voltage supplied to the timer 21. It is necessary that the voltage to the timer remain substantially constant to assure the proper operation of the timer during the setting operation. This is accomplished by a simple RC low-pass filter network identified as R_1 and C_1 in FIGURE 2*b*. C_1 is large enough so that the voltage supply across it and the timer does not fall appreciably when a reset or monitor pulse appears on the communication line 300. The time constant R_1C_1 is many times greater than the duration of any of the pulses appearing on the communication line. During reset and monitor pulses which represent substantially short circuit conditions of the communication line, it is necessary to limit the maximum current through the line. This is accomplished by resistance R_2 shown in FIGURE 2*a*. A more elaborate current limiter may be employed to limit the maximum current to approximately the current required by the timer. However, the simple resistor limiter shown limits the current to about two to four times the current used by the timer.

The programmer, shown in block form in FIGURE 1, first provides a positive pulse to input terminal 131 of the reset generator 130 shown in FIGURE 2*a*. The terminal 131 is connected by way of resistor 132 to the base of transistor Q_1. The positive pulse causes transistor Q_1 to conduct providing a conduction path for current through capacitor 140, diode D_1 and transistor Q_1 to ground. Thus there is generated on communication line 300 a negative pulse as shown in FIGURE 3. Diode D_1 isolates input terminal 131 of the reset generator from negative monitor pulses that appear on communication line 300. Positive set pulses raise the collecter voltage of transistor Q_1 but do not feed through to the input terminal 131. Diode D_2 isolates the B+ line from positive set pulses from the set generator.

The reset receiver shown in FIGURE 2*b* is pulsed when point 230 is positive with respect to point 220. This occurs when point 220 goes to ground. Silicon-controlled rectifier SCR normally has its anode 241 and cathode 242 at the same potential. When point 220 goes to ground potential during a reset pulse, the cathode 242 of silicon-controlled rectifier SCR goes to ground potential. The anode 241 of silicon-controlled rectifier remains at the power supply voltage due to the long R_5C_3 time constant and the short duration of the reset pulse. The gate, point 243, is positive with respect to the cathode, point 242, and the silicon-controlled rectifier SCR fires causing pulse current to flow through the reset line of timer 210. Neither set pulses nor monitor pulses allow point 230 to be positive with respect to point 220 due to the conduction of diode D_3 during these pulses thereby shunting resistor R_4.

The programmer then provides a series of positive pulses to input terminal 151 of the set generator 150 shown in FIGURE 2*a*. Terminal 151 is connected to the base of the transistor Q_2 which is connected as an emitter follower. The emitters of transistors Q_2 and Q_3 are connected together, and the base of transistor Q_3 is connected by way of resistor 153 to ground. The positive pulses provided at terminal 151 by the programmer appear at the common junction 152 of the emitters of transistors Q_2 and Q_3. Transistor Q_3 is therefore biased toward conduction, and the pulses appear at the collecter of transistor Q_3. These pulses are coupled to the communication line 300 by capacitor 160. This results in a series of voltage pulses over-riding the voltage on the communication line as shown in FIGURE 3. The purpose of transistor Q_3 is to isolate the set generator input terminal 151 from all negative pulses appearing on the communication line 300.

Due to the diode D_4 in the set receiver 260 shown in FIGURE 2*b*, the set receiver responds to positive pulses only. When a positive pulse appears at point 230, point 261 goes positive from ground causing pulse current to flow in the set line 270 of the timer 210.

After the timer 210 has received certain predetermined numbers of set pulses, the timer provides a pulse at input terminal 281 of the monitor generator 280 shown in FIGURE 2*b*. The first section of the monitor generator 280 generally comprising transistors Q_6 and Q_7 is a one-shot multivibrator. The pulse generated by the one-shot appearing at point 282 has a duration greater than the pulse duration of the set pulses but less than the time between the set pulses. The pulse is inverted by transistor Q_8, con-

nected in conventional common emitter fashion, and is differentiated by differentiation network R_6C_4. The resulting wave form appearing at the base of transistor Q_9 is a negative spike occurring at the time corresponding to the beginning of the pulse generated by the one-shot and a positive spike occurring at the time corresponding to the end of the pulse generated by the one-shot. The positive spike is amplified by transistors Q_9 and Q_{10} and applied at the base of transistor Q_{11}. This causes transistor Q_{11} to conduct thereby providing a conduction path by way of diode D_3, capacitor C_5, diode D_5 and transistor Q_{11} to ground. This results in a negative pulse which occurs between set pulses on communication line **300** as shown in FIGURE 3.

Transistor Q_4 in the monitor receiver **170** shown in FIGURE 2*a* is saturated since the B+ line is connected to the base of transistor Q_4. When a negative pulse appears on communication line **300**, the collector of transistor Q_4 goes to ground due to the conduction path provided by transistor Q_4 and diode D_6. This causes transistor Q_5 to conduct, thereby, providing monitor pulses at output terminal **171**. Note that as shown in the figure the monitor receiver will respond to the reset pulse. To make the monitor receiver non-responsive to the reset pulse a switch may be provided which would switch the base of Q_4 from the B+ line to ground during the reset pulse.

A remote two-wire setting system for a timer has been shown. It has the capability to power, reset, set and monitor the setting process and to check the line switch. It will be apparent that the embodiment shown is only exemplary and that various modifications can be made in construction and arrangement within the scope of the invention as defined in the appended claims.

I claim as my invention:

1. A remote two-wire setting system for resetting, setting and monitoring a timer, comprising:

(a) two wires with said timer being connected between said two wires;

(b) a D.C. power source connected across said two wires;

(c) a programming means;

(d) a reset generator connected to said programming means and to one of said two wires, said reset generator being activated after a predetermined time by said programming means to generate an output pulse which is communicated to said one of said two wires, said output pulse being capable of substantially short circuiting said two wires for the duration of said output pulse;

(e) a reset receiver means for generating a reset pulse and communicating said pulse to said timer in response only to said short circuit condition;

(f) a set generator connected to said programmer and, in response to a signal from said programmer, generates output pulses which are communicated to one of said two wires, said output pulses being of such a polarity that the voltage differential between said two wires is increased;

(g) a set receiver for receiving only said output pulses from said set generator and for generating set signals in response thereto and for communicating said set signals to said timer;

(h) a monitor generator connected to said timer and to one of said two wires for generating an output pulse coupled to said one of said two wires in response to a signal from said timer after said timer has received a predetermined number of pulses from said set generator;

(i) a monitor receiver connected to said one of said two wires and to said programming means for receiving said output pulse from said monitor generator and communicating a signal to said programming means in response thereto.

2. The remote two-wire setting system for timers of claim **1** in which there is a first section and a second section detachably connected by means of said two wires; said first section comprising: said D.C. power source, said programming means, said reset generator, said set generator and said monitor receiver; and said second section comprising: said timer, said reset receiver, said monitor generator and said set receiver; whereby one of said first sections may be used to reset, set and monitor each of a plurality of timers in each of a plurality of second sections.

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