(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
3 July 2014 (03.07.2014)

WIPO | PCT

(10) International Publication Number
WO 2014/106040 A1

(51) International Patent Classification:
G06F 17/50 (2006.01)

(21) International Application Number:
PCT/US2013/077975

(22) International Filing Date:
27 December 2013 (27.12.2013)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/747,982 31 December 2012 (31.12.2012) US
13/849,427 22 March 2013 (22.03.2013) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) Title: PATTERN-BASED POWER-AND-GROUND (PG) ROUTING AND VIA CREATION

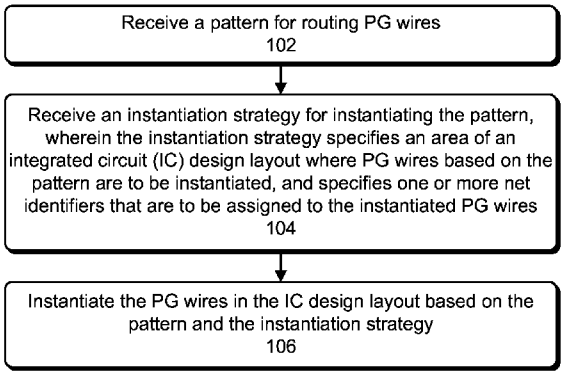


FIG. 1

(57) Abstract: Systems and techniques for pattern-based power-and-ground (PG) routing and via rule based via creation are described. A pattern for routing PG wires can be received. Next, an instantiation strategy may be received, wherein the instantiation strategy specifies an area of an integrated circuit (IC) design layout where PG wires based on the pattern are to be instantiated and specifies one or more net identifiers that are to be assigned to the instantiated PG wires. The PG wires can be instantiated in the IC design layout based on the pattern and the instantiation strategy. Additionally, a set of via rules can be received, wherein each via rule specifies a type of via that is to be instantiated at an intersection between two PG wires that are in two different metal layers. Next, one or more vias can be instantiated in the IC design layout based on the set of via rules.

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PATTERN-BASED POWER-AND-GROUND (PG) ROUTING AND VIA CREATION

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BACKGROUND

Technical Field

[0001] This disclosure relates to electronic design automation (EDA). More specifically, this disclosure relates to pattern-based power-and-ground routing and via creation.

Related Art

[0002] Power-and-ground (PG) nets refer to the nets in an integrated circuit that supply power and ground voltages to circuit elements. Conventional techniques typically create a PG net by individually creating and connecting a large number of wire segments. For example, conventional techniques typically create a PG net by using a script that individually creates each wire segment in the PG net, i.e., each wire segment that is created in the PG net corresponds to the execution of a command that creates a single wire segment.

[0003] Such conventional approaches have many drawbacks. In particular, the scripts that are used to create PG nets are becoming unmanageably complex due to the rapidly increasing size and complexity of circuit designs. It is not uncommon for a company to have a team of dedicated engineers for creating and maintaining these scripts. Furthermore, whenever a floorplan of a circuit design is modified, the script also usually needs to be modified. The process of modifying the script and then checking the modified script can take a long time. Due to these drawbacks conventional script-based approaches can easily add a few weeks to the total turn-around-time for modifying the circuit design floorplan.

[0004] Therefore, what are needed are systems and techniques for PG routing without the above-described problems.

SUMMARY

[0005] Some embodiments described herein provide systems and techniques for pattern-based PG routing. Specifically, a pattern for routing PG wires can be received. For example, a pattern-based PG routing application may read a file that contains a description of a pattern that

is defined using a pattern definition language. Next, the embodiment may receive an instantiation strategy that specifies an area of an integrated circuit (IC) design layout where PG wires based on the pattern are to be instantiated and specifies one or more net identifiers that are to be assigned to the instantiated PG wires. The instantiation strategy can also optionally specify PG blockages (i.e., areas in the IC design where PG wires are not allowed to be routed) and any extension requirements (e.g., so that the pattern can be electrically connected to one or more existing objects in the IC design). In some embodiments, a graphical user interface can be used to create a instantiation strategy. The PG wires can then be instantiated in the IC design layout based on the pattern and the instantiation strategy.

[0006] The pattern can be a hierarchical pattern that combines a set of two or more patterns. The pattern definition language may support a set of basic patterns (e.g., line pattern, ring pattern, etc.) and provide constructs to define hierarchical patterns.

[0007] Some embodiments described herein provide systems and techniques for pattern-based via creation. Specifically, a set of via rules can be received, wherein each via rule specifies a type of via that is to be instantiated at an intersection between two PG wires that are in two different metal layers. Next, one or more vias can be instantiated in the IC design layout based on the set of via rules. The process of instantiating one or more vias can involve: (1) detecting an intersection between a first PG wire in a first metal layer and a second PG wire in a second metal layer, (2) selecting a via rule in the set of via rules based on a first pattern that was used to create the first PG wire and a second pattern that was used to create the second PG wire, and (3) instantiating a via in the IC design layout at the intersection between the first PG wire and the second PG wire according to the selected via rule.

[0008] The logic for selecting a via rule can be arbitrarily complex. In some embodiments, the most specific via rule can be selected when multiple via rules match the pattern criteria. For example, upon detecting an intersection between PG wires that were created using a first pattern and a second pattern, an embodiment can select a pattern-specific via rule in the set of via rules that matches the first and second patterns. If none of the pattern-specific via rules match the criteria, then a pattern-type-specific via rule can be selected that matches pattern types corresponding to the first and second patterns. If none of the pattern-specific via rules match the criteria and also none of the pattern-type-specific via rules match the criteria, then a default via rule can be used.

BRIEF DESCRIPTION OF THE FIGURES

[0009] FIG. 1 presents a flowchart that illustrates a process for pattern-based PG routing in accordance with some embodiments described herein.

[0010] FIG. 2A illustrates examples of patterns in accordance with some embodiments described herein.

[0011] FIG. 2B illustrates an instantiation strategy for instantiating a pattern in accordance with some embodiments described herein.

[0012] FIG. 2C illustrates how a pattern can be instantiated in a given area without violating PG blockages in accordance with some embodiments described herein.

[0013] FIG. 3 illustrates a ring pattern in accordance with some embodiments described herein.

[0014] FIG. 4 presents a flowchart that illustrates a process for creating vias based on via rules in accordance with some embodiments described herein.

[0015] FIGs. 5A-5D illustrate how via rules can be used to create vias in accordance with some embodiments described herein.

[0016] FIG. 6 illustrates a computer system in accordance with some embodiments described in this disclosure.

DETAILED DESCRIPTION

[0017] The following description is presented to enable any person skilled in the art to make and use the invention, and is provided in the context of a particular application and its requirements. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the one or more inventions disclosed herein are not limited to the embodiments shown, but are to be accorded the widest scope consistent with the principles and features disclosed herein.

Overview of an electronic design automation (EDA) flow

[0018] An EDA flow can be used to create a circuit design. Once the circuit design is finalized, it can undergo fabrication, packaging, and assembly to produce integrated circuit chips. An EDA flow can include multiple steps, and each step can involve using one or more EDA software tools. Some EDA steps and software tools are described below. These examples of

EDA steps and software tools are for illustrative purposes only and are not intended to limit the embodiments to the forms disclosed.

[0019] Some EDA software tools enable circuit designers to describe the functionality that is desired to be implemented. These tools also enable circuit designers to perform what-if planning to refine functionality, check costs, etc. During logic design and functional verification, the HDL (hardware description language), e.g., SystemVerilog, code can be written and the design can be checked for functional accuracy, e.g., the design can be checked to ensure that it produces the correct outputs.

[0020] During synthesis and design for test, the HDL code can be translated to a netlist using one or more EDA software tools. Further, the netlist can be optimized for the target technology, and tests can be designed and implemented to check the finished chips. During netlist verification, the netlist can be checked for compliance with timing constraints and for correspondence with the HDL code.

[0021] During design planning, an overall floorplan for the chip can be constructed and analyzed for timing and top-level routing. During physical implementation, circuit elements can be positioned in the layout (placement) and can be electrically coupled (routing). PG routing can take place during physical implementation.

[0022] During analysis and extraction, the circuit's functionality can be verified at a transistor level and parasitics can be extracted. During physical verification, the design can be checked to ensure correctness for manufacturing, electrical issues, lithographic issues, etc.

[0023] During resolution enhancement, geometric manipulations can be performed on the layout to improve manufacturability of the design. During mask data preparation, the design can be taped-out to produce masks which are used during fabrication.

Pattern-based PG routing

[0024] FIG. 1 presents a flowchart that illustrates a process for pattern-based PG routing in accordance with some embodiments described herein.

[0025] The process can begin by receiving a pattern for routing PG wires (operation 102). The pattern can be a hierarchical pattern that combines a set of two or more patterns. Specifically, the pattern can be described using a pattern definition language that allows a user to define a pattern in terms of other patterns that are natively supported by the pattern definition language or that are defined elsewhere (e.g., either in the same file or in a different file). The pattern definition language may natively support a set of basic patterns which can then be used to create more complex patterns. For example, the set of basic patterns can include a single line, a

single segment, a line-and-space pattern, a ring pattern, macro/pad connection, standard cell rail, and/or any other patterns that are desired to be natively supported in the pattern definition language. The pattern definition language can provide constructs that enable a new pattern to be defined and created by combining one or more existing patterns.

[0026] This disclosure includes examples of patterns that are described using a particular pattern definition language. This pattern definition language has been used for illustration purposes only. The pattern definition examples presented in this disclosure are not intended to limit the embodiments to the forms disclosed.

[0027] In addition to the pattern, the process can also receive an instantiation strategy for instantiating the pattern, wherein the instantiation strategy includes an area of an IC design layout where PG wires based on the pattern are to be instantiated and one or more net identifiers that are to be assigned to the instantiated PG wires (operation 104). The area specified in the instantiation strategy can generally include a set of polygons in a given layer of the IC design layout. A set of PG blockages can also be specified in the instantiation strategy in addition to specifying the area where the PG wires are to be instantiated. A PG blockage can indicate one or more areas in the IC design where PG wires are not allowed to be instantiated.

[0028] The process can then instantiate the PG wires in the IC design layout based on the pattern and the instantiation strategy (operation 106). As mentioned above, if any PG blockages are specified, then the process can instantiate the PG wires in the area of the IC design layout that was specified in the instantiation strategy without violating the PG blockages (e.g., by avoiding the blocked areas) that were specified in the instantiation strategy.

[0029] FIG. 2A illustrates examples of patterns in accordance with some embodiments described herein. The three pattern examples illustrated in FIG. 2A are called pattern1, pattern2, and pattern3. In FIG. 2A, patterns pattern1 and pattern2 are basic patterns, i.e., these patterns are natively supported in the pattern description language. Pattern pattern3, on the other hand, is a pattern that is defined in terms of patterns pattern1 and pattern2.

[0030] Pattern pattern1 is a line with the following parameters: width = 1, layer = 1, and direction = v ("v" means "vertical"). As shown in FIG. 2A, pattern1 can be defined using the following statement in a pattern definition language: "pattern1 : (type = line, width = 1, layer = 1, direction = v)." Since pattern1 extends indefinitely in the vertical direction (this is illustrated in FIG. 2A by the arrows that extend out from the top and bottom edges of rectangle 202), the endpoints or length of rectangle 202 in the vertical direction is not specified.

[0031] Pattern pattern2 is a segment that can be defined using the following statement: "pattern2 : (type = segment, width = 1, layer = 2, direction = h, low = 0, high = 4)." Since

pattern2 is a segment, the ends of the pattern (or alternatively the length) need to be specified. The "low" value specifies the location of the left edge of rectangle 204, and the "high" value specifies the location of the right edge of rectangle 204. The direction parameter is "h," which stands for "horizontal."

[0032] Pattern pattern3 defines a mesh pattern (mesh 206 in FIG. 2A) based on patterns pattern1 and pattern2. As shown in FIG. 2A, the definition of patttern3 states that pattern3 is a combination of a repetition of pattern1 and a repetition of pattern2. The repetition of pattern1 begins at offset "m" and is repeated with pitch "p." The repetition of pattern2 begins at offset (xo, yo), and repeats with pitch "xp" in the horizontal direction and with pitch "yp" in the vertical direction. Since the lines corresponding to pattern1 extend indefinitely in the vertical direction, the offset and pitch in the vertical direction are not specified for pattern1.

[0033] The syntax and semantics of the pattern definition language shown in FIG. 2A is for illustration purposes only and is not intended to limit the embodiments to the forms disclosed. Many modifications and variations will be apparent to those skilled in the art. For example, instead of specifying the layer information in the pattern definition (e.g., the parameter assignment "layer = 1" in pattern1's definition), the layer information may be specified when a pattern is instantiated.

[0034] FIG. 2B illustrates an instantiation strategy for instantiating a pattern in accordance with some embodiments described herein. The instantiation strategy can specify area 224 in IC design layout 222 for instantiating a PG pattern and can specify that net identifier "n123" be assigned to the instantiated wires. In general, multiple net identifiers can be specified in an instantiation strategy. For example, the instantiation strategy may specify that horizontal wires be assigned net identifier "n1" and vertical wires be assigned net identifier "n2." PG blockages 226 can also be specified in the instantiation strategy, wherein PG blockages 226 are to be avoided while instantiating a PG pattern. PG blockages can generally be located anywhere in IC design layout 222, and a PG blockage may apply to one or more layers.

[0035] FIG. 2C illustrates how a pattern can be instantiated in a given area without violating PG blockages in accordance with some embodiments described herein. Instantiated pattern 228 in FIG. 2C is obtained when pattern3 shown in FIG. 2A is instantiated in area 224 shown in FIG. 2B while avoiding PG blockages 226 shown in FIG. 2B. The wires of instantiated pattern 228 are assigned net identifier "n123" (not shown in FIG. 2C) as was specified in the instantiation strategy. Note that pattern1 is on layer 1, and pattern2 is on layer 2. Therefore, the vertical lines in instantiated pattern 228 are on layer 1, and the horizontal segments in instantiated pattern 228 are on layer 2. In some embodiments, the instantiation strategy can also

specify how the wires in instantiated pattern 228 are to be extended. For example, an instantiation strategy may specific that one or more wires are to be extended so that the wires electrically connect one or more objects in IC design layout 222. The pattern-based PG routing tool may select one or more wires in instantiated pattern 228 (e.g., based on the location of the objects that need to be electrically connected), and then extend the selected wires in the appropriate direction (i.e., so that the extended wires electrically connect the objects that were specified in the instantiation strategy).

[0036] The pattern examples shown in FIG. 2A are for illustration purposes only, and are not intended to limit the embodiments described herein. Many variations and modifications to the illustrative examples disclosed herein will be apparent to those skilled in the art. For example, FIG. 3 illustrates a ring pattern in accordance with some embodiments described herein. As shown in FIG. 3, a ring pattern can be defined using the following statement: "pattern4: (type = ring, width = 1, xlen, ylen)." The parameter assignment "type = ring" indicates that the pattern is a ring pattern. Next, the parameter assignment "width = 1" specifies the width of the ring (i.e., the width of the shaded area in FIG. 3). The parameter "xlen" and "ylen" specify the dimensions of the ring as shown in FIG. 3.

[0037] When different patterns are instantiated on different layers (e.g., pattern1 on metal layer M1, pattern2 on metal layer M2, etc.), vias may need to be created to electrically connect the different patterns. A process for creating vias based on via rules is now described.

Via rules

[0038] FIG. 4 presents a flowchart that illustrates a process for creating vias based on via rules in accordance with some embodiments described herein. The process can begin with receiving a set of via rules, wherein each via rule specifies a type of via that is to be instantiated at an intersection between two PG wires that are in two different metal layers (operation 402). Next, one or more vias can be instantiated in the IC design layout based on the set of via rules (operation 404).

[0039] Instantiating one or more vias can include the following operations: (1) detecting an intersection between a first PG wire in a first metal layer and a second PG wire in a second metal layer, (2) selecting a via rule in the set of via rules based on a first pattern that was used to create the first PG wire and a second pattern that was used to create the second PG wire, and (3) instantiating a via in the IC design layout at the intersection between the first PG wire and the second PG wire based on the via rule.

[0040] A via rule can be specified at the pattern level (this type of via rule is called a "pattern-specific via rule" in this disclosure) or at the pattern-type level (this type of via rule is called a "pattern-type-specific via rule" in this disclosure). A pattern-specific via rule specifies two patterns (e.g., pattern1 and pattern2). The pattern-specific via rule can instantiate a via at the intersection between two PG wires that were created by the two patterns specified in the pattern-specific via rule. For example, if a pattern-specific via rule specifies patterns pattern1 and pattern2, then the via rule can instantiate a via at the intersection of a PG wire created by pattern1 in layer 1 and a PG wire created by pattern2 in layer 2. A pattern-type-specific via rule specifies two pattern-types (e.g., pattern-type "line" and pattern-type "ring"), and is used to create a via at the intersection between two PG wires that were created by two patterns belonging to the two pattern-types. For example, a pattern-type-specific via rule can be used to create a via at the intersection of a PG wire that was created by a line pattern and a PG wire that was created by a ring pattern.

[0041] If multiple via rules match the criteria for an intersection, then the process may select the most specific via rule or select a via rule that has the highest priority (assuming that the via rules have been assigned priorities). For example, suppose a pattern-specific via rule R1 states that a via is to be created at the intersection between PG wires that were created by patterns P1 and P2. Let patterns P1 and P2 belong to pattern types T1 and T2, respectively. Further, suppose a pattern-type-specific via rule R2 states that a via is to be created at the intersection between PG wires that were created by patterns of pattern types T1 and T2. In this example, both R1 and R2 would be applicable to an intersection between PG wires that were created using patterns P1 and P2. In some embodiments, since via rule R1 is more specific than via rule R2, the process may select via rule R1 for creating the via.

[0042] In some embodiments, each via rule may be associated with a priority, and the matching via rule with the highest priority may be selected for creating the via. If none of the via rules match an intersection, then the process may use a default via rule to create the via (assuming a default via rule has been defined).

[0043] Specifically, in some embodiments, the process for selecting a via rule for an intersection between two PG wires that were created using a first and second pattern may be stated as follows: (1) select a pattern-specific via rule in the set of via rules that matches the first and second patterns, (2) if a pattern-specific via rule cannot be selected, then select a pattern-type-specific via rule in the set of via rules that matches pattern types corresponding to the first and second patterns, and (3) if a pattern-specific via rule or a pattern-type-specific via rule cannot be selected, select a default via rule (assuming a default rule has been defined). These techniques

for selecting a via rule have been presented for illustration purposes only and are not intended to limit the embodiments to the forms disclosed.

[0044] FIGs. 5A-5D illustrate how via rules can be used to create vias in accordance with some embodiments described herein. FIG. 5A illustrates four different patterns (pat1, pat2, pat3, and pat4) and three different vias (via1, via2, and via3). Patterns pat1 and pat2 are vertical lines on layer 1, wherein the width of pattern pat2 is greater than the width of pattern pat1. Patterns pat3 and pat4 are horizontal lines on layer 2, wherein the width of pattern pat4 is greater than the width of pattern pat3. As shown in FIG. 5A, a single via at the center of the intersecting region is created in via1, a single via on the left end of the intersecting region is created in via2, and a 2 × 2 via array at the top left corner of the intersecting region is created in via3.

[0045] FIG. 5B illustrates a mesh pattern (mesh 502) that has been created using patterns pat1, pat2, pat3, and pat4 (e.g., mesh 502 may be created by specifying offset and pitch values for each of the patterns). Note that no vias have been created in FIG. 5B.

[0046] FIG. 5C illustrates a set of via rules that can be used to create vias in mesh 502. Specifically, via rules 504 include four via rules. The first via rule states that a via of type via1 is to be created when two PG wires created by patterns pat1 and pat3 intersect. The second via rule states that a via of type via2 is to be created when two PG wires created by patterns pat2 and pat3 intersect. The third via rule states that a via of type via3 is to be created when two PG wires created by patterns pat2 and pat4 intersect. The fourth via rule states that no vias are to be created when two PG wires created by patterns pat1 and pat4 intersect.

[0047] FIG. 5D illustrates the result of applying via rules 504 to mesh 502. As shown in FIG. 5D, the first via rule was used for the top-left intersection, the second via rule was used for the top-right intersection, the third via rule was used for the bottom-right intersection, and the fourth via rule was used for the bottom-left intersection.

Computer system

[0048] FIG. 6 illustrates a computer system in accordance with some embodiments described in this disclosure. Computer system 602 can include processor 604, memory 606, and storage device 608. Computer system 602 can be coupled to display device 614, keyboard 610, and pointing device 612. Storage device 608 can store operating system 616, application 618, and data 620. Data 620 can include input required by application 618 and/or output generated by application 618.

[0049] Computer system 602 may automatically (or with user input) perform one or more processes that are implicitly or explicitly described in this disclosure. For example, computer

system 602 can load application 618 into memory 606, and application 618 can then be used to perform pattern-based PG routing and/or via creation based on a set of via rules.

CONCLUSION

[0050] The above description is presented to enable any person skilled in the art to make and use the embodiments. Various modifications to the disclosed embodiments will be readily apparent to those skilled in the art, and the general principles defined herein are applicable to other embodiments and applications without departing from the spirit and scope of the present disclosure. Thus, the present invention is not limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

[0051] The data structures and code described in this disclosure can be partially or fully stored on a computer-readable storage medium and/or a hardware module and/or hardware apparatus. A computer-readable storage medium includes, but is not limited to, volatile memory, non-volatile memory, magnetic and optical storage devices such as disk drives, magnetic tape, CDs (compact discs), DVDs (digital versatile discs or digital video discs), or other media, now known or later developed, that are capable of storing code and/or data. Hardware modules or apparatuses described in this disclosure include, but are not limited to, application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), dedicated or shared processors, and/or other hardware modules or apparatuses now known or later developed.

[0052] The methods and processes described in this disclosure can be partially or fully embodied as code and/or data stored in a computer-readable storage medium or device, so that when a computer system reads and executes the code and/or data, the computer system performs the associated methods and processes. The methods and processes can also be partially or fully embodied in hardware modules or apparatuses, so that when the hardware modules or apparatuses are activated, they perform the associated methods and processes. Note that the methods and processes can be embodied using a combination of code, data, and hardware modules or apparatuses.

[0053] The foregoing descriptions of embodiments of the present invention have been presented only for purposes of illustration and description. They are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art. Additionally, the above disclosure is not intended to limit the present invention. The scope of the present invention is defined by the appended claims.

What Is Claimed Is:

1. A method for pattern-based power-and-ground (PG) routing, the method comprising:

receiving a pattern for routing PG wires, wherein the pattern is described using a pattern definition language;

receiving an instantiation strategy for instantiating the pattern, wherein the instantiation strategy specifies an area of an integrated circuit (IC) design layout where PG wires based on the pattern are to be instantiated and specifies one or more net identifiers that are to be assigned to the instantiated PG wires; and

instantiating the PG wires in the IC design layout based on the pattern and the instantiation strategy.

2. The method of claim 1, wherein the pattern is a hierarchical pattern that combines a set of two or more patterns.

3. The method of claim 1, wherein the method further comprises:

receiving a set of via rules, wherein each via rule specifies a type of via that is to be instantiated at an intersection between two PG wires that are in two different metal layers; and

instantiating one or more vias in the IC design layout based on the set of via rules.

4. The method of claim 3, wherein said instantiating one or more vias comprises:

detecting an intersection between a first PG wire in a first metal layer and a second PG wire in a second metal layer;

selecting a via rule in the set of via rules based on a first pattern that was used to create the first PG wire and a second pattern that was used to create the second PG wire; and

instantiating a via in the IC design layout at the intersection between the first PG wire and the second PG wire based on the via rule.

5. The method of claim 4, wherein selecting the via rule includes selecting a pattern-specific via rule in the set of via rules that matches the first and second patterns.

6. The method of claim 5, wherein selecting the via rule further includes, responsive to determining that no pattern-specific via rule matched, selecting a pattern-type-specific via rule in the set of via rules that matches pattern types corresponding to the first and second patterns

7. The method of claim 6, wherein selecting the via rule further includes, responsive to determining that no pattern-specific via rule and no pattern-type-specific via rule matched, selecting a default via rule

8. A non-transitory computer-readable storage medium storing instructions that, when executed by a computer, cause the computer to perform a method for pattern-based power-and-ground (PG) routing, the method comprising:

receiving a pattern for routing PG wires, wherein the pattern is described using a pattern definition language;

receiving an instantiation strategy for instantiating the pattern, wherein the instantiation strategy specifies an area of an integrated circuit (IC) design layout where PG wires based on the pattern are to be instantiated and specifies one or more net identifiers that are to be assigned to the instantiated PG wires; and

instantiating the PG wires in the IC design layout based on the pattern and the instantiation strategy.

9. The non-transitory computer-readable storage medium of claim 8, wherein the pattern is a hierarchical pattern that combines a set of two or more patterns.

10. The non-transitory computer-readable storage medium of claim 8, wherein the method further comprises:

receiving a set of via rules, wherein each via rule specifies a type of via that is to be instantiated at an intersection between two PG wires that are in two different metal layers; and

instantiating one or more vias in the IC design layout based on the set of via rules.

11. The non-transitory computer-readable storage medium of claim 10, wherein said instantiating one or more vias comprises:

detecting an intersection between a first PG wire in a first metal layer and a second PG wire in a second metal layer;

selecting a via rule in the set of via rules based on a first pattern that was used to create the first PG wire and a second pattern that was used to create the second PG wire; and

instantiating a via in the IC design layout at the intersection between the first PG wire and the second PG wire based on the via rule.

12. The non-transitory computer-readable storage medium of claim 11, wherein selecting the via rule includes selecting a pattern-specific via rule in the set of via rules that matches the first and second patterns.

13. The non-transitory computer-readable storage medium of claim 12, wherein selecting the via rule further includes, responsive to determining that no pattern-specific via rule matched, selecting a pattern-type-specific via rule in the set of via rules that matches pattern types corresponding to the first and second patterns.

14. The non-transitory computer-readable storage medium of claim 13, wherein selecting the via rule further includes, responsive to determining that no pattern-specific via rule and no pattern-type-specific via rule matched, selecting a default via rule

15. A method for creating vias during pattern-based power-and-ground (PG) routing, the method comprising:

receiving a set of via rules, wherein each via rule specifies a type of via that is to be instantiated at an intersection between two PG wires that are in two different metal layers;

detecting an intersection between a first PG wire in a first metal layer and a second PG wire in a second metal layer;

selecting a via rule in the set of via rules based on a first pattern that was used to create the first PG wire and a second pattern that was used to create the second PG wire; and

instantiating a via in the IC design layout at the intersection between the first PG wire and the second PG wire based on the selected via rule.

16. The method of claim 15, wherein selecting the via rule includes selecting a pattern-specific via rule in the set of via rules that matches the first and second patterns.

17. The method of claim 16, wherein selecting the via rule further includes, responsive to determining that no pattern-specific via rule matched, selecting a pattern-type-

specific via rule in the set of via rules that matches pattern types corresponding to the first and second patterns.

18. The method of claim 17, wherein selecting the via rule further includes, responsive to determining that no pattern-specific via rule and no pattern-type-specific via rule matched, selecting a default via rule.

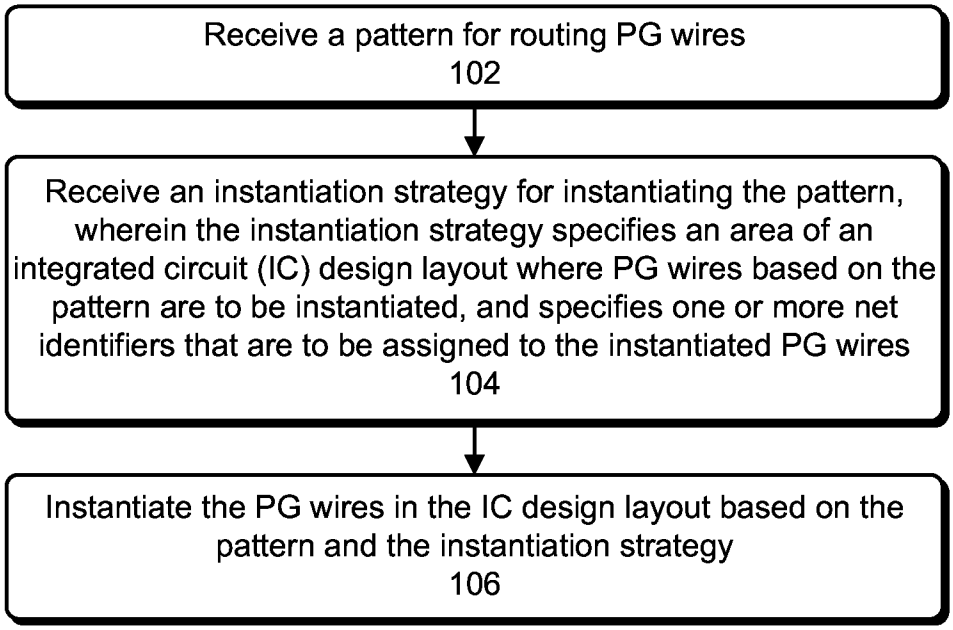

Receive a pattern for routing PG wires
102
Receive an instantiation strategy for instantiating the pattern, wherein the instantiation strategy specifies an area of an integrated circuit (IC) design layout where PG wires based on the pattern are to be instantiated, and specifies one or more net identifiers that are to be assigned to the instantiated PG wires
104
Instantiate the PG wires in the IC design layout based on the pattern and the instantiation strategy
106

FIG. 1

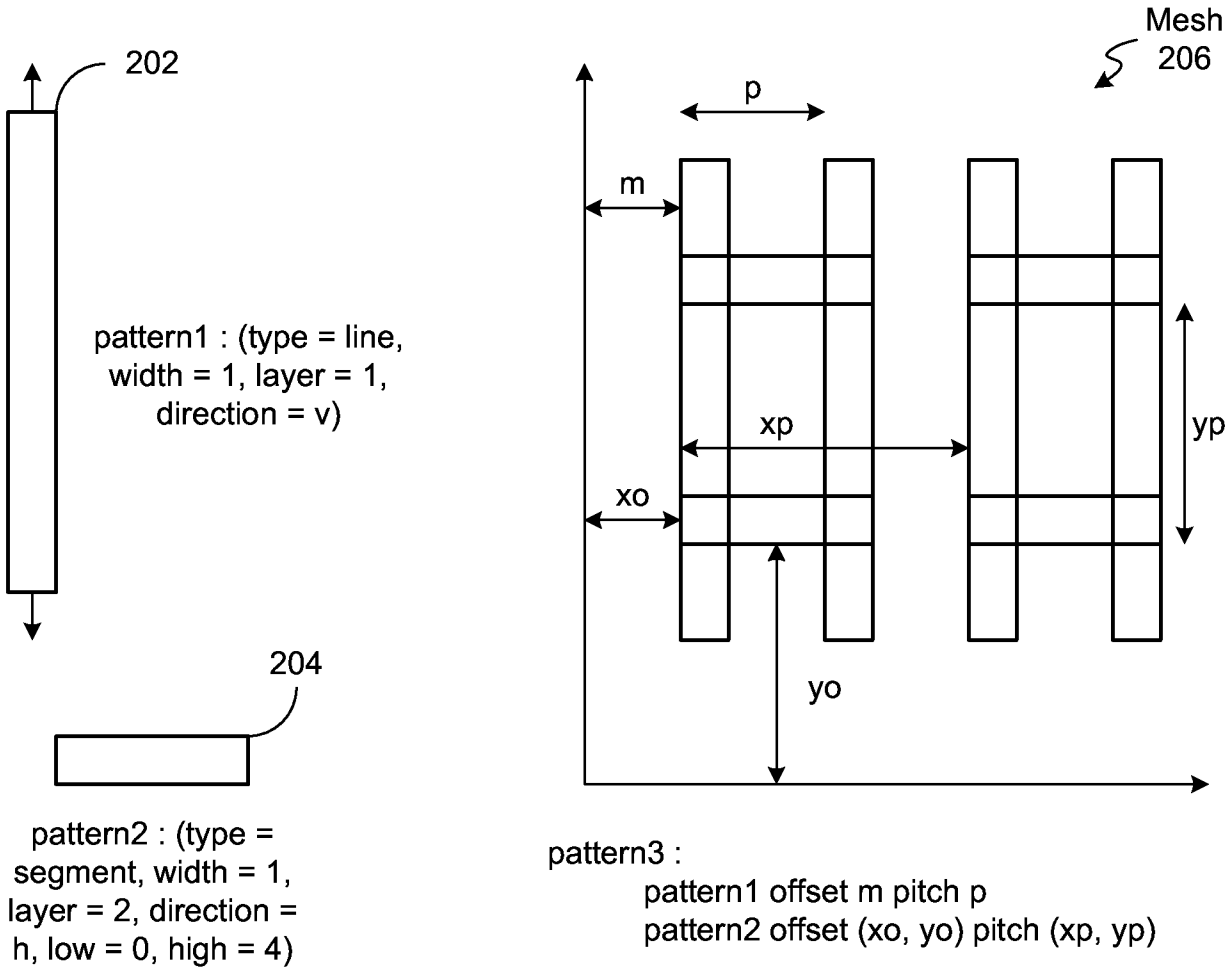

202
pattern1 : (type = line, width = 1, layer = 1, direction = v)
204
pattern2 : (type = segment, width = 1, layer = 2, direction = h, low = 0, high = 4)
Mesh
206
p
m
xp
xo
yp
yo
pattern3 :
pattern1 offset m pitch p
pattern2 offset (xo, yo) pitch (xp, yp)

FIG. 2A

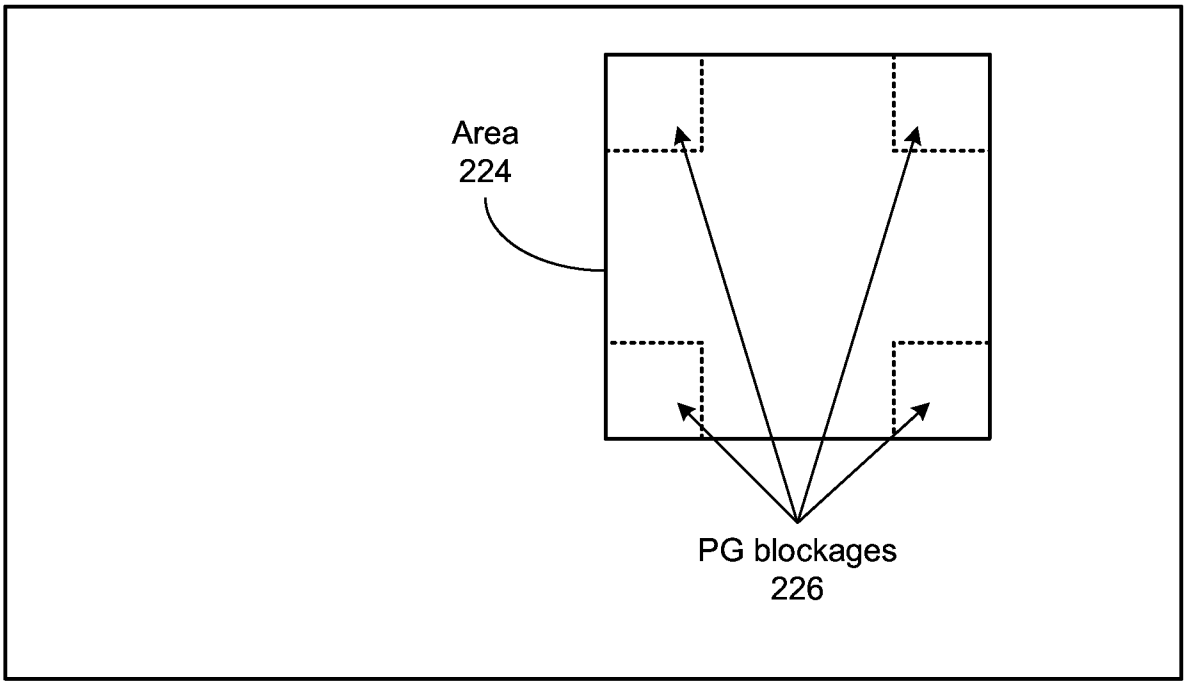

Area
224
PG blockages
226
IC design layout
222

FIG. 2B

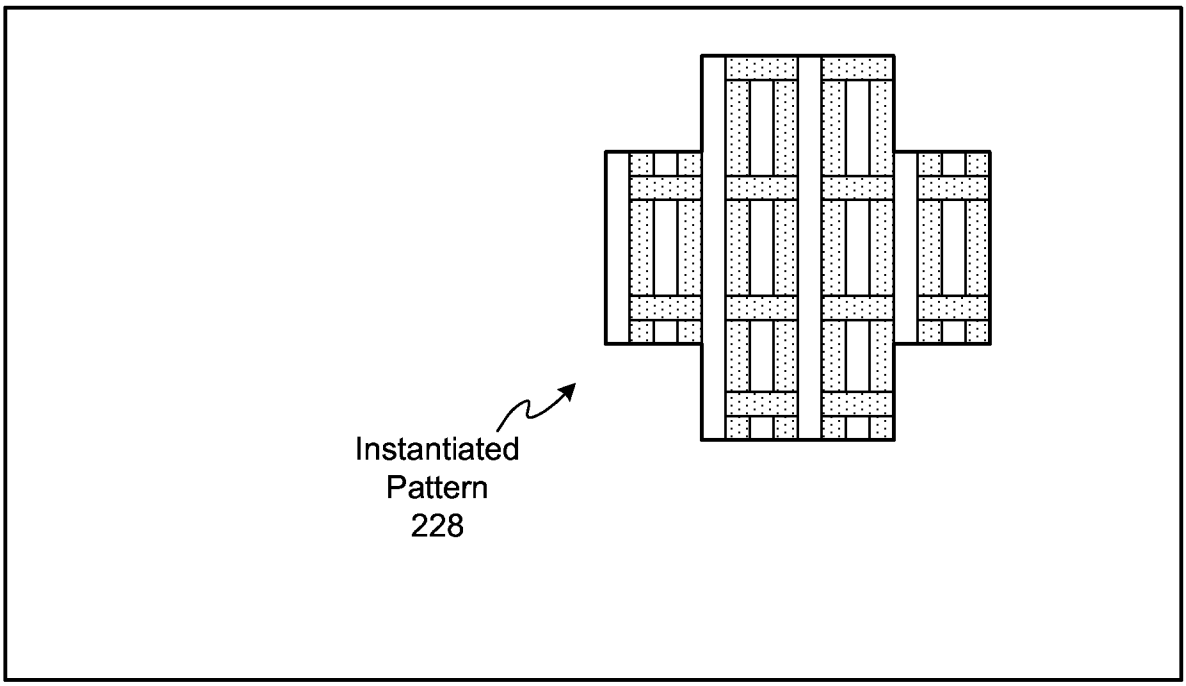

Instantiated
Pattern
228
IC design layout
222

FIG. 2C

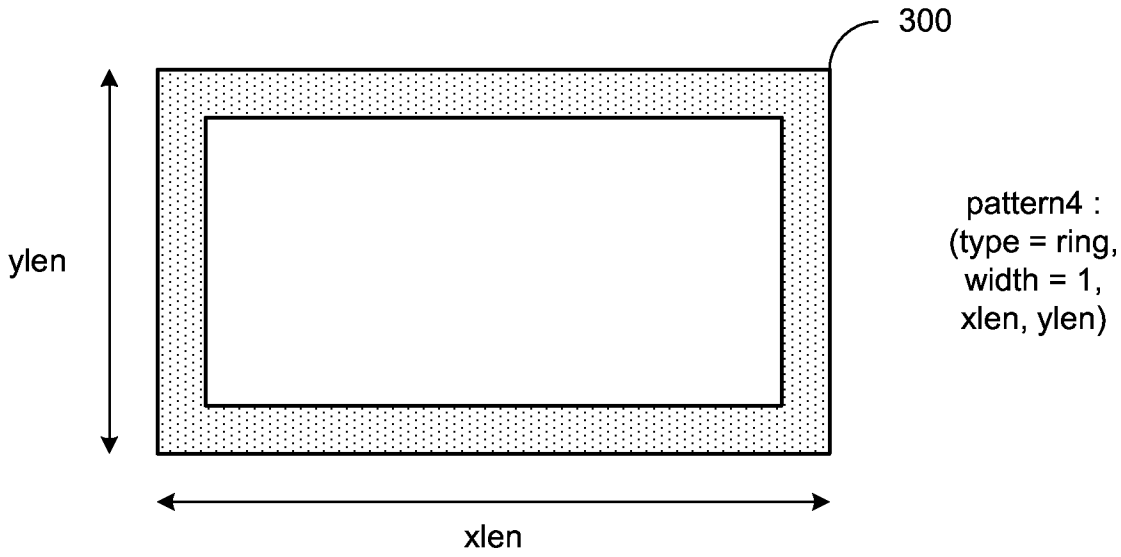

300
ylen
pattern4 :
(type = ring,
width = 1,
xlen, ylen)
xlen

FIG. 3

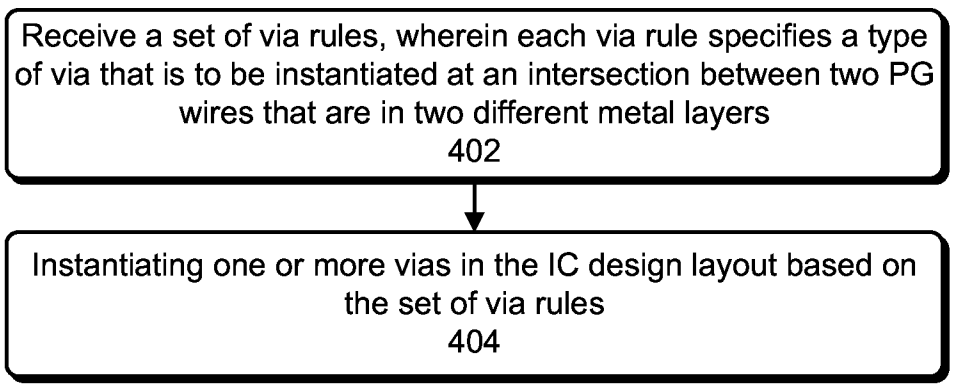

Receive a set of via rules, wherein each via rule specifies a type of via that is to be instantiated at an intersection between two PG wires that are in two different metal layers
402
Instantiating one or more vias in the IC design layout based on the set of via rules
404

FIG. 4

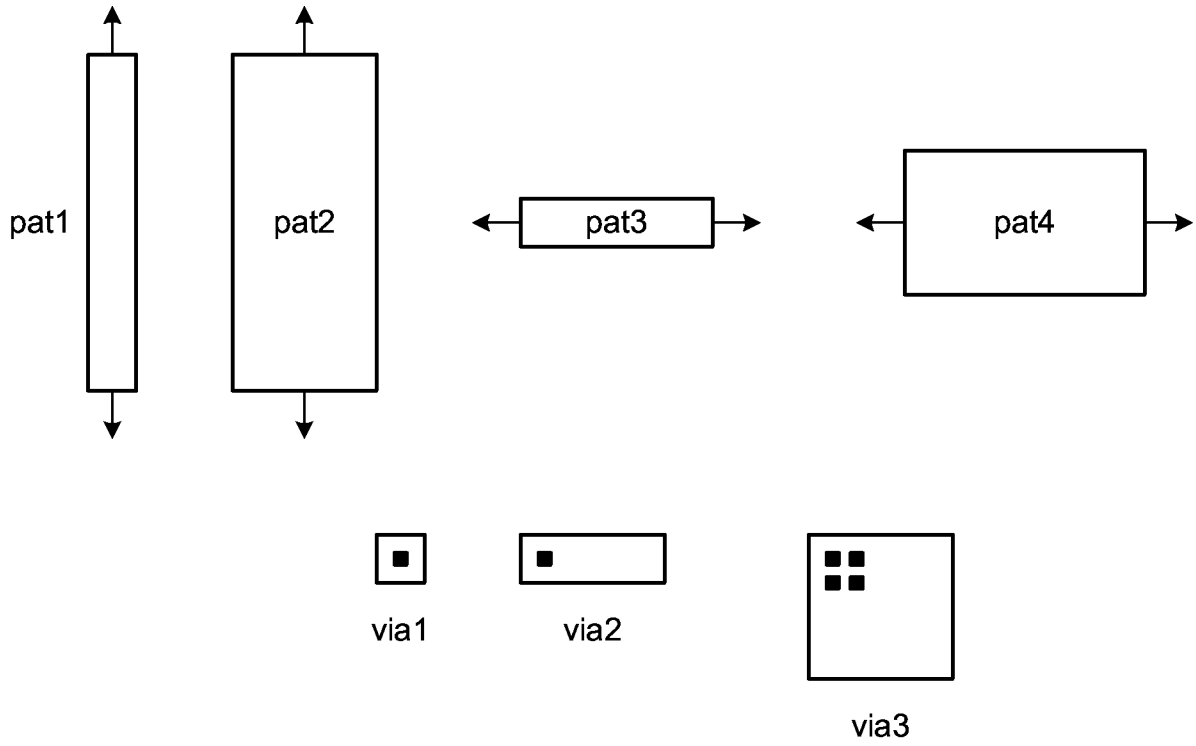


FIG. 5A

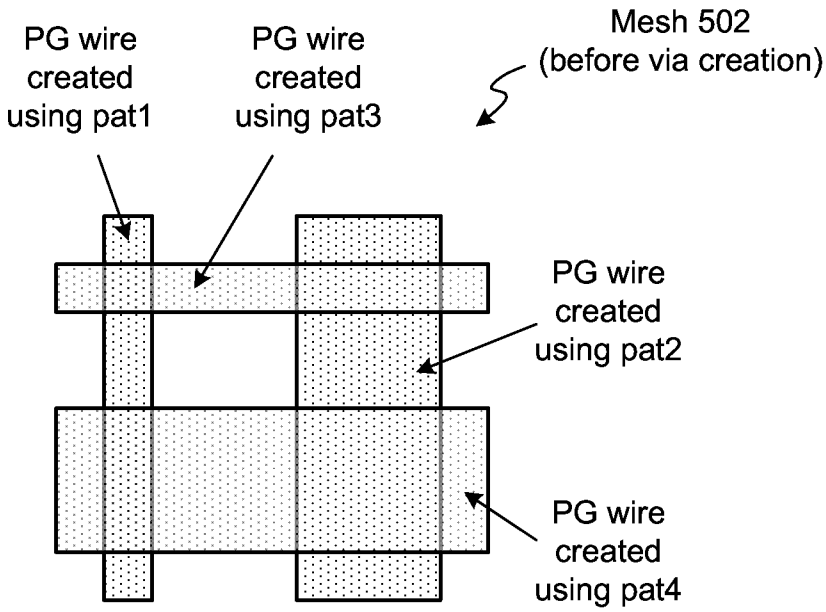


FIG. 5B

Via rules 504

```
via pat1 pat3 via1    #rule1
via pat2 pat3 via2    #rule2
via pat2 pat4 via3    #rule3
via pat1 pat4 nil     #rule4
```

FIG. 5C

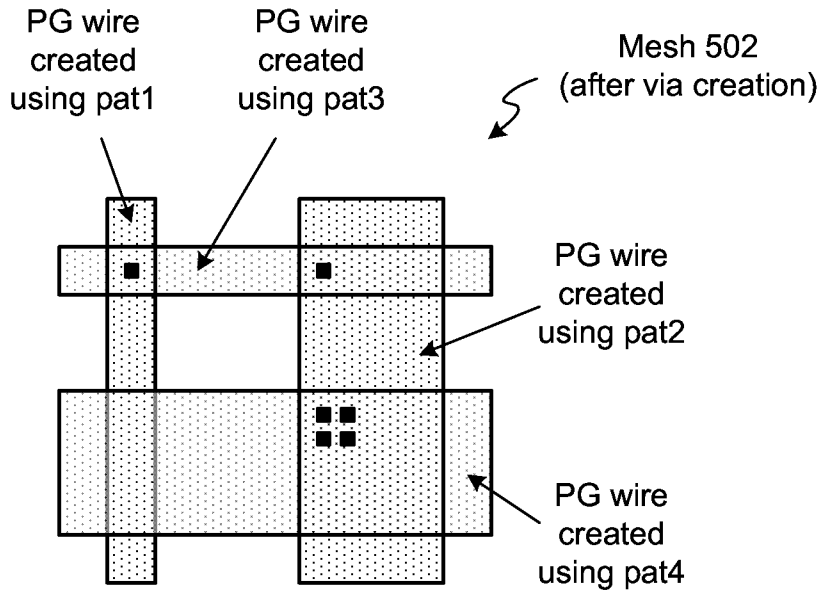

PG wire created using pat1
PG wire created using pat3
Mesh 502 (after via creation)
PG wire created using pat2
PG wire created using pat4

FIG. 5D

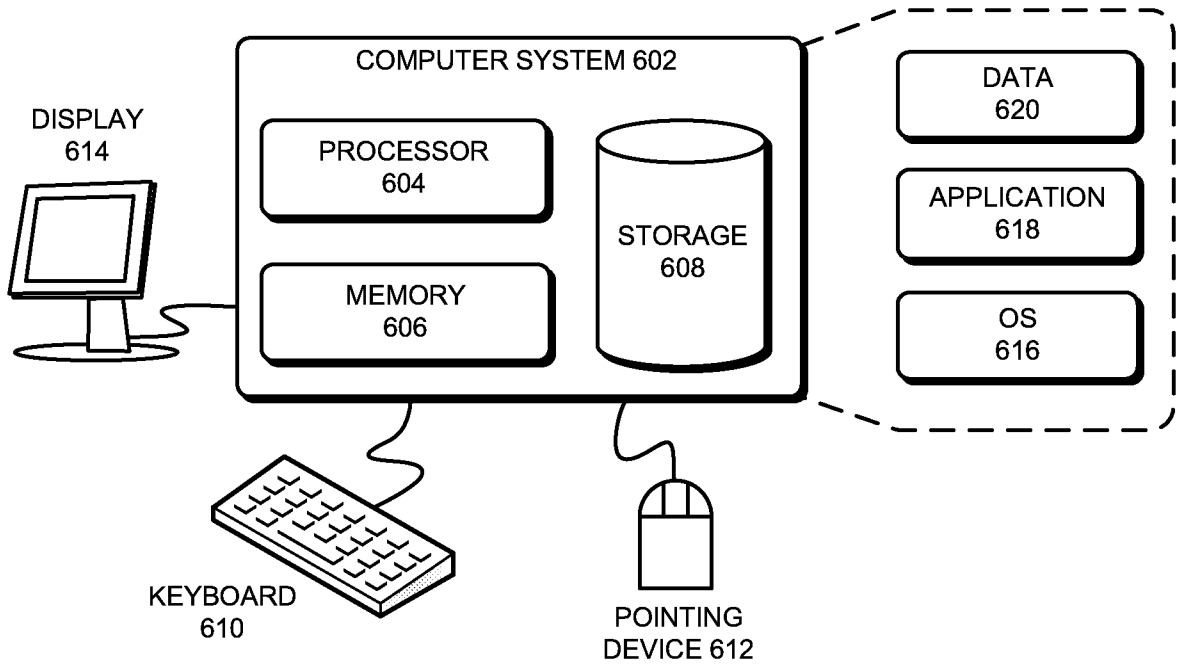

COMPUTER SYSTEM 602
DISPLAY 614
PROCESSOR 604
MEMORY 606
STORAGE 608
DATA 620
APPLICATION 618
OS 616
KEYBOARD 610
POINTING DEVICE 612

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/077975

A. CLASSIFICATION OF SUBJECT MATTER

G06F 17/50(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F 17/50; H01L 23/48; G06F 9/455; H01L 21/44

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: power ground routing, wire, pattern, via rule, intersection, layer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2012-0223368 A1 (DEEPAK D. SHERLEKAR et al.) 06 September 2012 See paragraphs [0009]-[0011], [0037]-[0047], [0055]-[0064]; and figures 5-10.	1-18
A	US 2012-0317531 A1 (KRISHNAKUMAR SUNDARESAN) 13 December 2012 See paragraphs [0007]-[0014], [0040-[0049]; and figure 4.	1-18
A	US 2011-0113398 A1 (JOACHIM KEINERT et al.) 12 May 2011 See paragraphs [0014]-[0017], [0030]-[0040], [0044]; and figures 1a, 4.	1-18
A	US 2009-0132980 A1 (SUBARNAREKHA SINHA et al.) 21 May 2009 See paragraphs [0010]-[0011], [0055]-[0062], [0075]; and figures 2E, 3B-3C.	1-18
A	US 2006-0080630 A1 (TA-CHENG LIN) 13 April 2006 See paragraphs [0003]-[0011], [0026]-[0030], [0036]-[0044]; claim 1; and figures 1, 7-8.	1-18

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 April 2014 (11.04.2014)	**16 April 2014 (16.04.2014)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2013/077975

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US 2005-0172252 A1	04/08/2005
		US 7603641 B2	13/10/2009
		WO 2005-045711 A2	19/05/2005
		WO 2005-045711 A3	04/08/2005