United States Patent [19]

Snook et al.

[11] **3,717,872**

[45] **Feb. 20, 1973**

[54] HIGH FIDELITY SYMBOL DISPLAY THROUGH LIMITED BANDWIDTH SYSTEM

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[22] Filed: **June 1, 1970**

[21] Appl. No.: **57,847**

[52] **U.S. Cl.**.....**343/5 EM**, 315/18, 340/324 A

[51] **Int. Cl.**.....**G01s 7/22**

[58] **Field of Search**.....343/5 EM, 17; 315/18; 340/324 A

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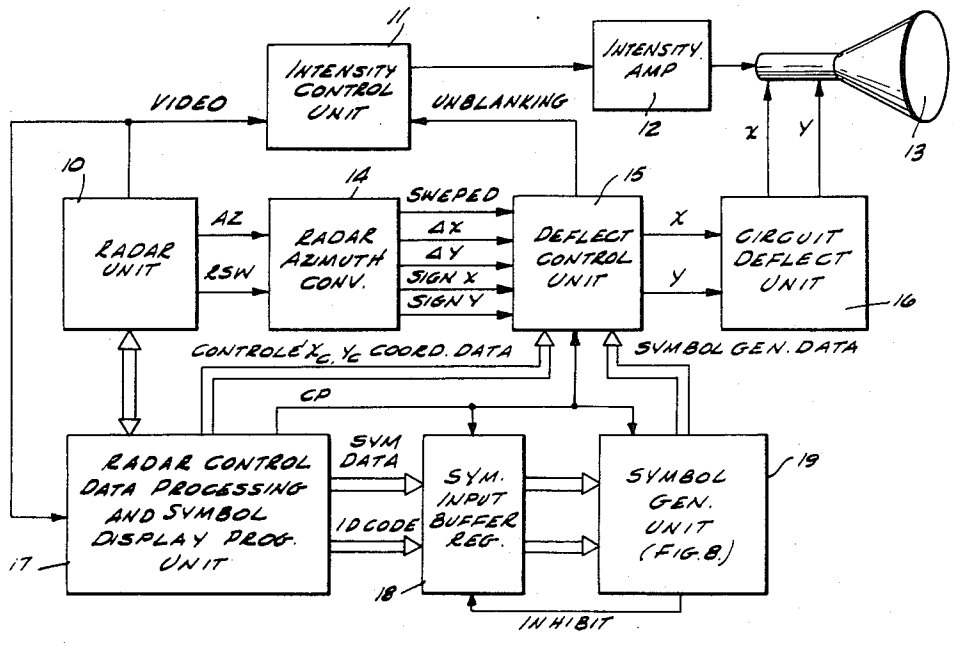
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[57] **ABSTRACT**

A symbol display system is disclosed which uses short strokes to form a symbol. The strokes proceed from point to point, each stroke being defined by cumulative changes in X and Y coordinates from a designated starting point. Each change from one point to another is sequentially read from a storage unit addressed by a symbol select matrix and a time counter. To maximize the speed of the strokes without distortion at corners of more than about 45°, a zero change is stored as the next change following a change leading to the corner point. More than one symbol may be programmed for display on a line. A program counter controls a sequencer to address the symbols to be displayed in sequence through the symbol display matrix, and to initiate displacement of the starting point for the next symbol a predetermined distance from the starting point of the last symbol.

9 Claims, 9 Drawing Figures



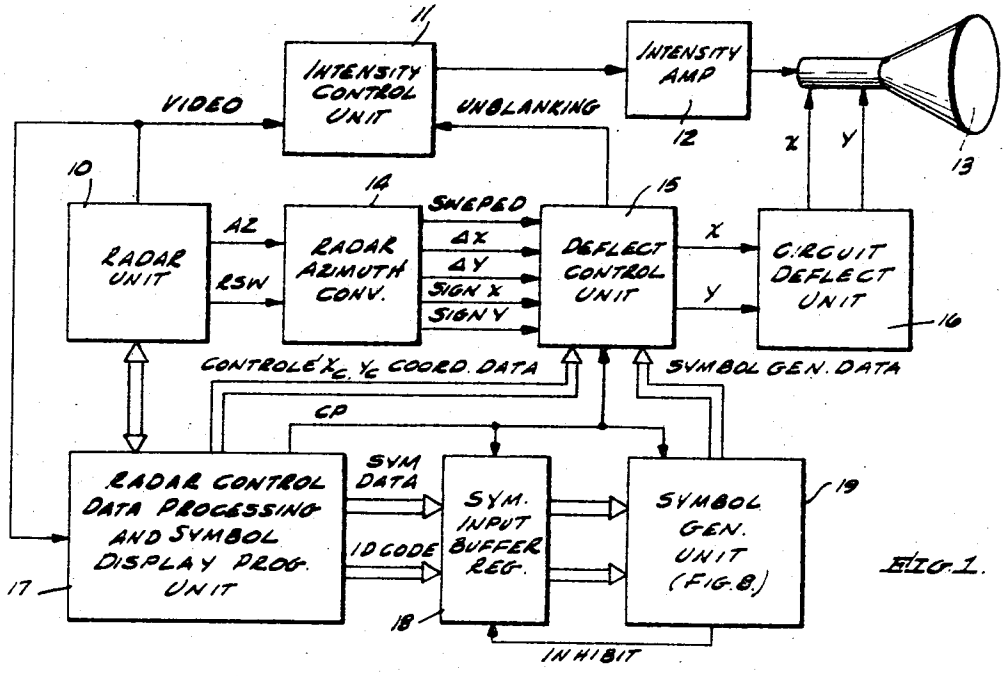


FIG. 1.

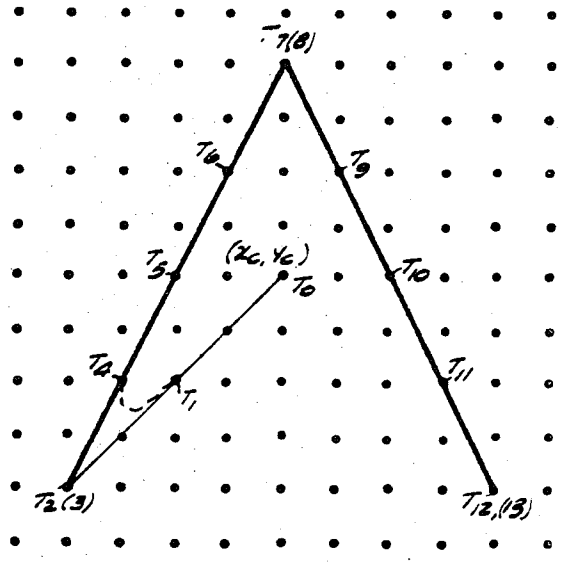


FIG. 2.

	+X		−X		+Y		−Y			
TIME	1	2	1	2	1	2	1	2	Z	S
1				X				X		
2				X				X		
3										
4	X					X			X	
5	X					X				
6	X					X				
7	X					X				
8										
9	X							X		
10	X							X		
11	X							X		
12	X							X		
13										
14									X	X

FIG 3

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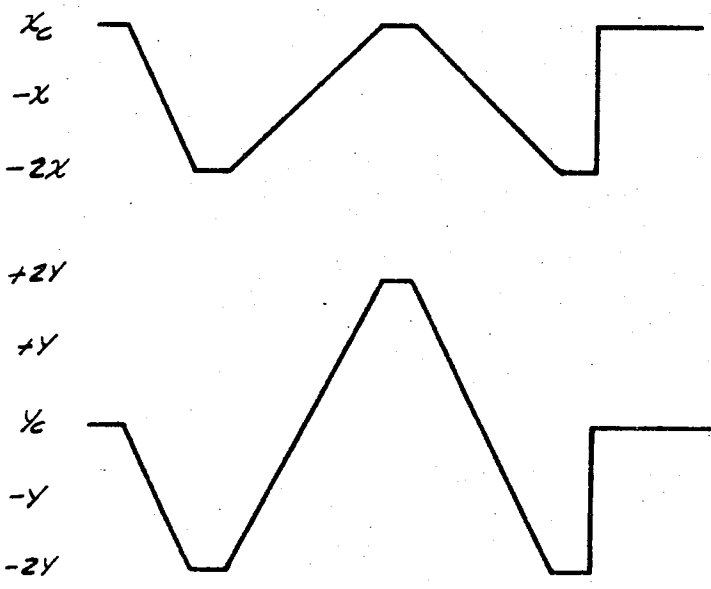


FIG. 4.

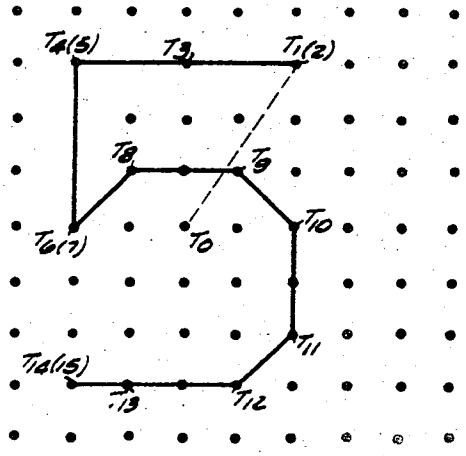


FIG. 6.

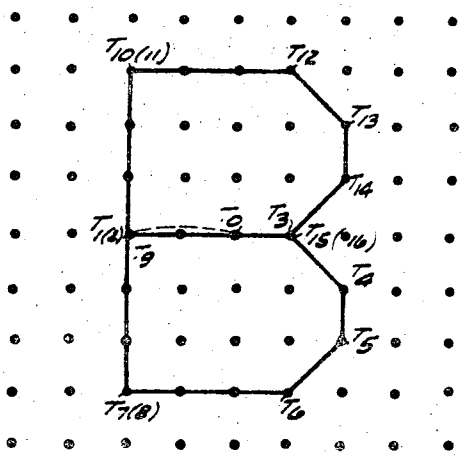


FIG. 5.

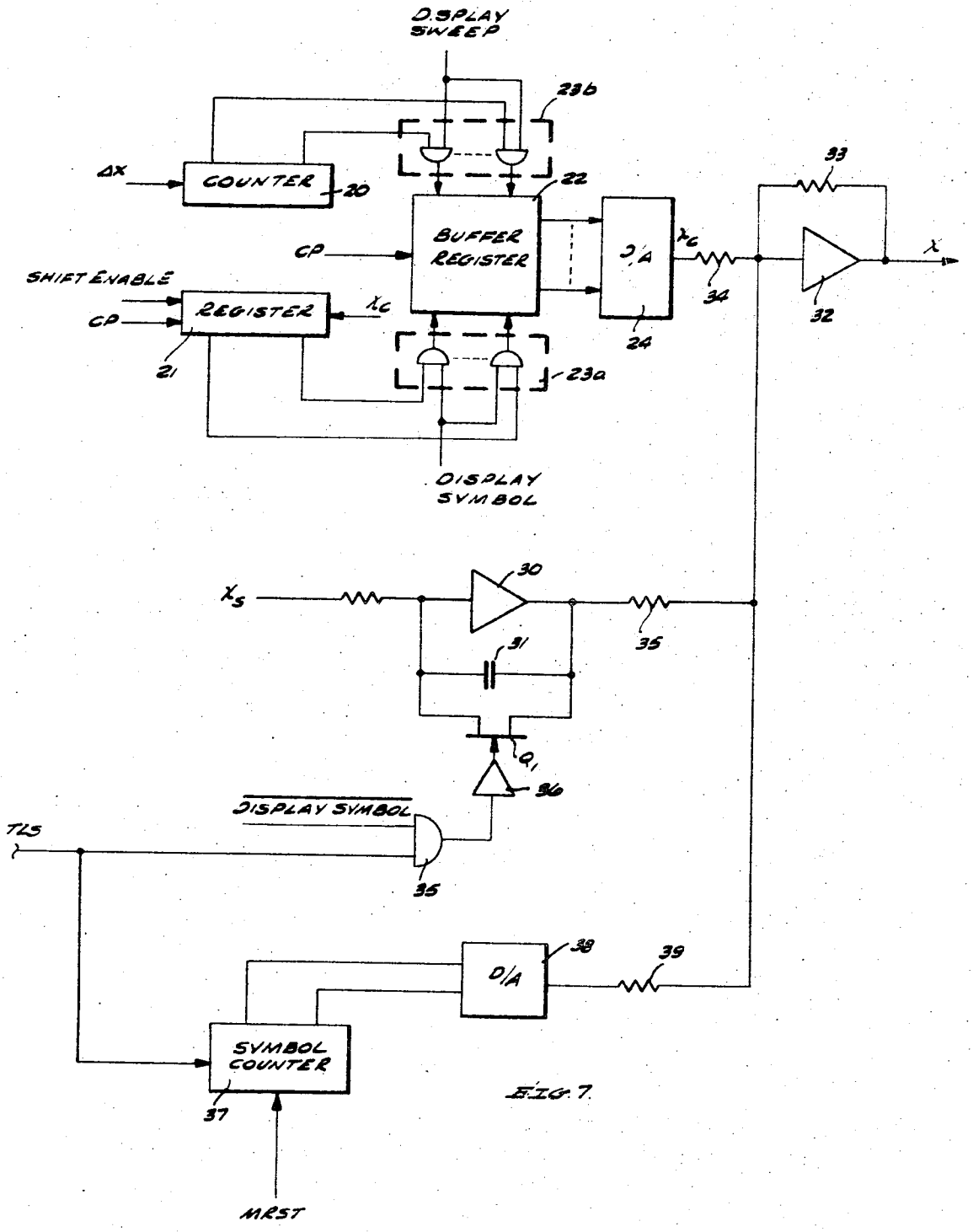

DISPLAY SWEEP
23b
ΔX
COUNTER
20
22
BUFFER REGISTER
D/A
33
CP
SHIFT ENABLE
REGISTER
21
23a
24
34
32
DISPLAY SYMBOL
30
31
35
Q1
36
DISPLAY SYMBOL
TLS
35
38
39
D/A
SYMBOL COUNTER
37
MRST

FIG. 7.

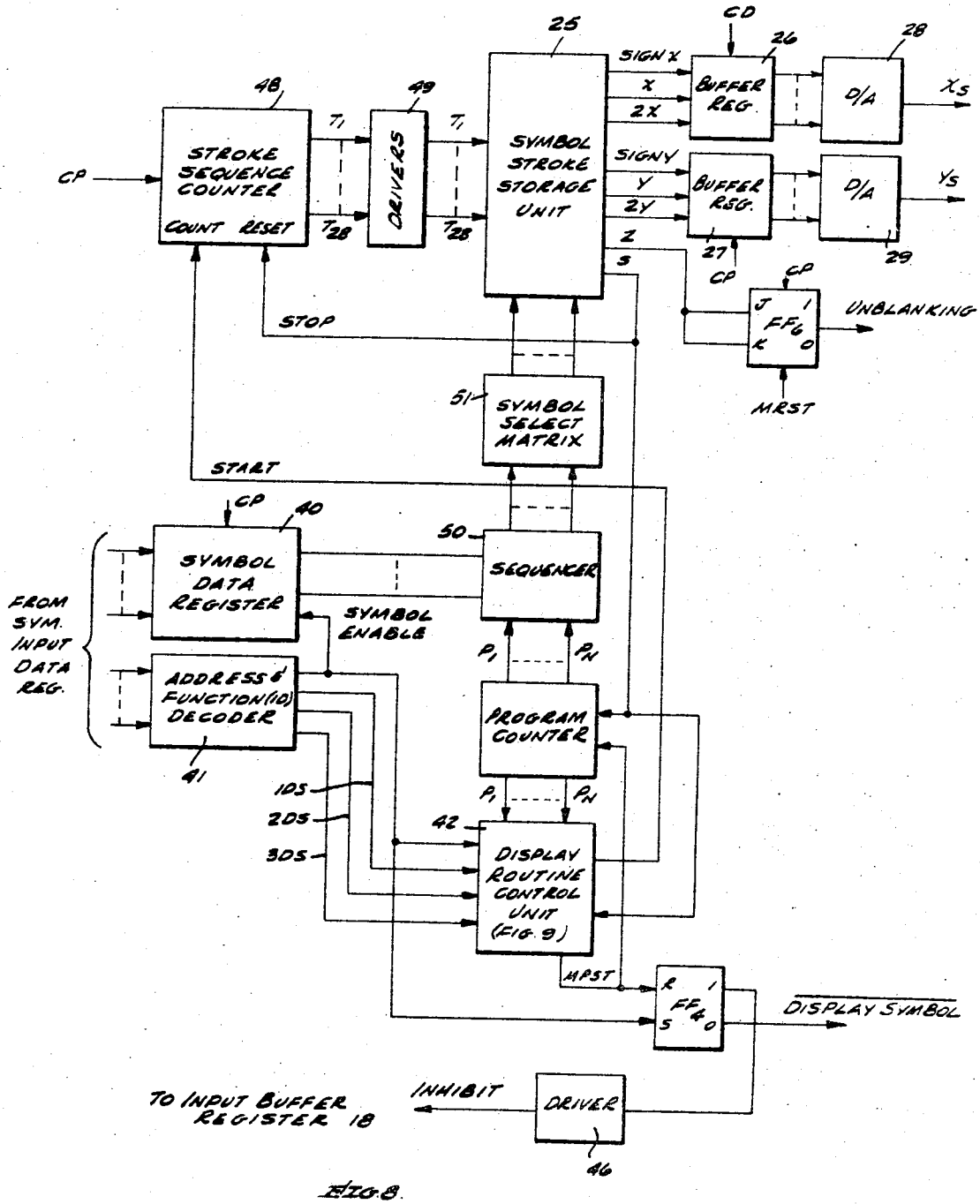

CP
STROKE SEQUENCE COUNTER
COUNT RESET
48
T_1
T_{28}
DRIVERS
49
SYMBOL STROKE STORAGE UNIT
25
SIGN X
X
2X
SIGN Y
Y
2Y
Z
S
CD
BUFFER REG.
26
BUFFER REG.
27
D/A
28
D/A
29
X_S
Y_S
CP
J 1 FF6 K 0
UNBLANKING
MRST
STOP
51
SYMBOL SELECT MATRIX
START
CP
40
SYMBOL DATA REGISTER
50
SEQUENCER
FROM SYM. INPUT DATA REG.
SYMBOL ENABLE
ADDRESS & FUNCTION(10) DECODER
41
P_1
P_N
PROGRAM COUNTER
10S
20S
30S
42
DISPLAY ROUTINE CONTROL UNIT (FIG. 9)
MRST
R 1 FF4 S 0
DISPLAY SYMBOL
TO INPUT BUFFER REGISTER 18
INHIBIT
DRIVER
46

FIG. 8

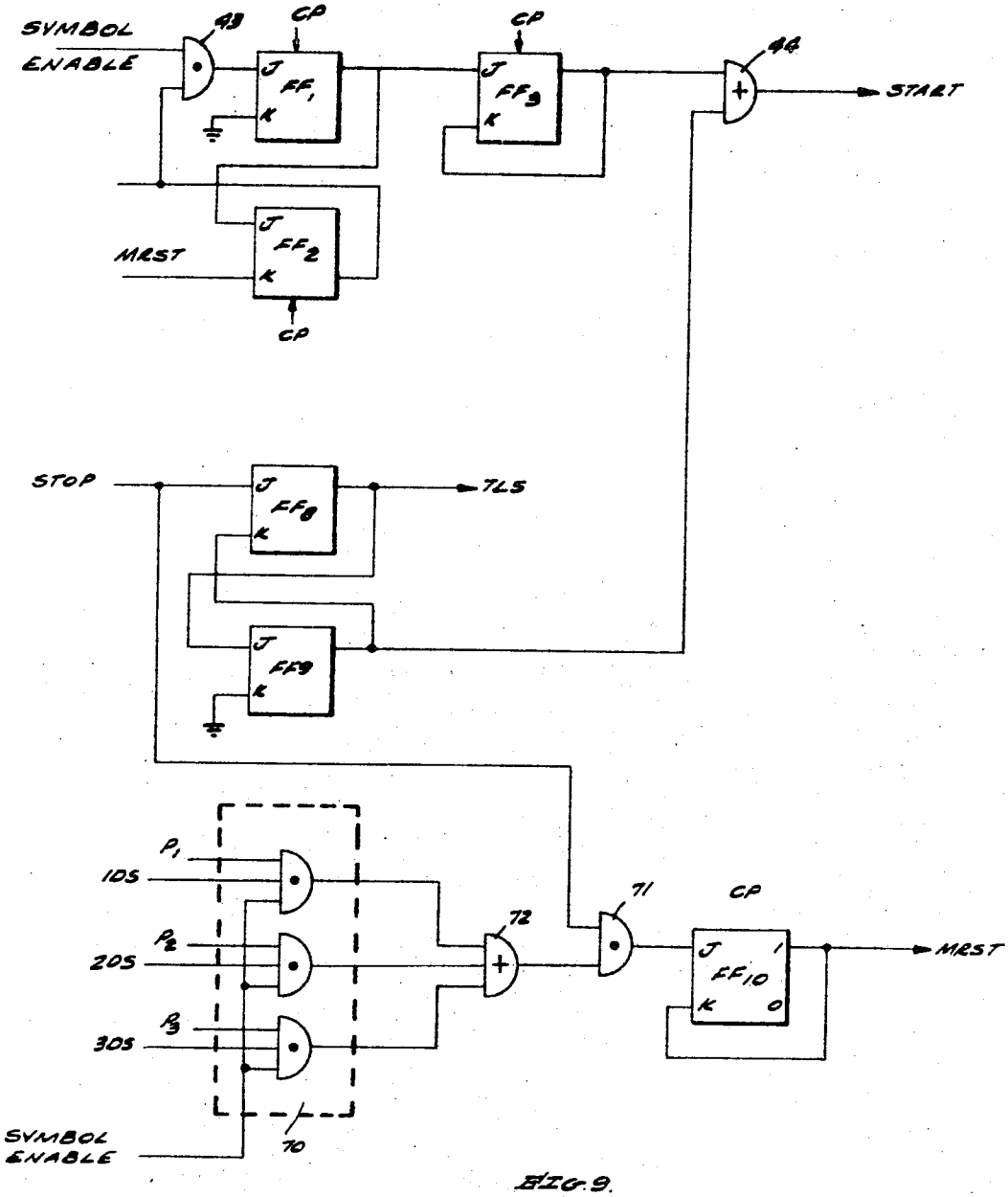

SYMBOL ENABLE
43
CP
FF1
CP
FF3
46
START
MRST
FF2
CP
STOP
FF8
75
FF9
P1
10S
P2
20S
P3
30S
72
71
CP
FF10
MRST
SYMBOL ENABLE
70

FIG. 9.

HIGH FIDELITY SYMBOL DISPLAY THROUGH LIMITED BANDWIDTH SYSTEM

The invention herein described was made in the course of or under a Contract or Subcontract thereunder with the Air Force.

BACKGROUND OF THE INVENTION

This invention relates to apparatus for displaying symbols on a cathode ray tube, and more particularly to apparatus for minimizing the time required to display a symbol on a cathode ray tube without distortion.

In many data processing systems it is desirable to display symbols on a cathode ray tube (CRT) using short strokes. Digital techniques are employed to drive the X and Y deflection channels of the CRT for each of the successive strokes of a given symbol being displayed, which may be a letter, numeral or arbitrary symbol.

A typical radar data processing system is one for displaying video signals from a radar unit, such as in a PPI display, with symbols periodically displayed at designated coordinates. Since the display channel for the video signals must be interrupted while a symbol is being displayed, it is important to minimize the time required to display the symbol. Otherwise, a significant section of a video range sweep display will be blanked. Also, minimizing the time required to generate a given symbol allows a greater number of symbols to be displayed within the display refresh period.

In most CRT display systems, electromagnetic deflection is used because it is not practical to obtain suitable electrostatic deflecting voltages. In electromagnetic deflection, the deflecting force is due to a magnetic field set up within the tube by a set of X and Y coordinate coils arranged around the neck of the tube. A suitable deflecting force is obtained from the set of coils by proper selection of the number of turns in the coils and the amplitude of driving current. Another advantage of electromagnetic deflection is that tube construction is simpler in that there are no deflection plates required within the tube.

A significant disadvantage of an electromagnetic deflection system is that the large inductances of the deflection coils give rise to delays in the deflection of the electron beam in response to X and Y deflection signals. Consequently, the electron beam tracing a symbol on the face of the cathode ray tube will lag behind the X and Y deflection signals. In turning a corner of about 45° or more, the electron beam will then tend to either overshoot or cut the corner, depending upon the rate at which the X and Y deflection signals are changing just before turning the corner. The cumulative effect of this phenomena is that, as symbol stroke time is shortened, the height and width of the symbol decreases. These problems are less in a CRT having an electrostatic deflection system, but still can be significant.

OBJECTS AND SUMMARY OF THE INVENTION

An object of this invention is to provide a system for developing a waveform to be applied to a cathode ray tube deflection system for display of symbols at a maximum rate with minimum distortion for a deflection system of given bandwidth.

Still another object is to provide for display on a cathode ray tube symbols using waveforms made up of cumulative short stroke values read from a digital storage unit, with the symbols having a minimum of distortion.

These and other objects of the invention are realized, in a exemplary embodiment of the present invention, by effectively storing in digital form X and Y deflection values for successive short strokes that make up the symbols. At a point where a given symbol requires the direction of the next stroke to change by more than about 45°, one full no-deflection stroke period is allowed to lapse before deflection values for the next stroke are read. The stroke periods are numbered in sequence, including the no-deflection strokes, and the values for the strokes are stored separately for retrieval in sequence.

The stroke values sequentially read in digital form for a given symbol are converted to analog form and integrated to provide symbol waveform signals X_s and Y_s which are superimposed on signals X_c and Y_c that designate the X and Y coordinates of a point on the face of the CRT at which the symbol is to be displayed.

A stroke sequence counter is driven by system clock pulses to address the stored stroke values of all symbols in sequence, but only one group of stroke values is read out for a given symbol addressed by coded binary signals received from a data processing unit. After all of the stroke values for the given symbol have been read from the storage unit, a stop code stored with the last stroke value resets and turns the stroke sequence counter off.

In accordance with one feature of the invention, a given symbol display is oriented with respect to a point designated by the X_c and Y_c coordinated signals. Stroke values for deflecting the beam from that point to a point where actual display of the given symbol is to begin are then read from the symbol stroke unit as one or more symbol strokes, but the beam is blanked until the first stroke to be displayed of the given symbol is read from the storage unit. That first stroke is identified by a blanking code bit stored with the X and Y deflection values and is used to initiate beam unblanking which is then terminated after the deflection values for the last stroke of the given symbol has been read and completed. To allow time for the last stroke to be completed, an additional no-deflection stroke is taken. The beam is then blanked during the next stroke period.

The novel features that are considered characteristic of this invention are set forth with particularity in the appended claims. The invention will best be understood from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a radar display system with symbol display capability provided in accordance with the present invention.

FIG. 2 is a diagram illustrating the manner in which a given symbol is divided into sequential strokes for display.

FIG. 3 is a table illustrating schematically the manner in which X and Y deflection values are stored for the successive strokes required to generate the symbol of FIG. 2.

FIG. 4 illustrates the symbol waveforms developed for the X and Y deflection channels from the stored deflection values of FIG. 3.

FIG. 5 illustrates the manner in which a letter is divided into successive strokes for display.

FIG. 6 illustrates the manner in which a numeral is divided into successive strokes for display.

FIG. 7 is a schematic diagram illustrating the manner in which the deflection control unit of FIG. 1 incorporates the symbol generating data from the symbol generating unit.

FIG. 8 is a schematic diagram for the symbol generating unit of FIG. 1.

FIG. 9 is a schematic diagram of the display routine control unit of FIG. 8.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring first to FIG. 1, a radar display system embodying the present invention includes a radar unit **10** which transmits a video signal to an intensity control unit **11** for controlling an intensity amplifier **12** to display on the face of the cathode ray tube **13** video information in synchronism with operation of the radar unit **10** as it sweeps in azimuth and range.

A radar azimuth converter **14** receives azimuth (AZ) and range sweep (RSW) data from the radar unit **10** and converts the azimuth data into trains of pulses representing Δx and Δy increments to control the cathode ray tube (CRT) **13**, such as for a PPI display in which the Polar coordinates of range and azimuth are converted to rectangular Cartesian coordinates. The conversion is through a radar azimuth converter **14**. A deflection control unit **15** accepts the trains of pulses Δx and Δy and converts them to analog voltages X and Y which produce a radar sweep on the CRT through a conventional CRT deflection unit **16**.

As will be noted more fully hereinafter with reference to FIG. 7, offset coordinates X_c and Y_c may be entered into the deflection control unit **15** to originate a radar sweep or display a symbol at any point within the display area as though it were the origin. The X and Y coordinate data is entered from a unit **17** which provides radar control, data processing and symbol display programming. The nature of the unit **17** is then that of a special purpose digital computer with a stored program and a console from which an operator viewing the CRT may, for example, enter X and Y coordinate data for display of a given symbol or a group of symbols at any point called for by the situation being scanned by the radar unit **10**.

When the stored program, or the operator, calls for the display of a symbol, the radar video display is interrupted by setting a sweep enable signal false. At the same time, the unit **17** transfers symbol code data and an identification (ID) code to a symbol input buffer register **18**. The symbol code data consists of coded words identifying one or more symbols to be displayed while the ID code consists of a group of binary digits which indicate the number of symbols to be displayed and, where more than one radar display system is being controlled by the same unit **17**, and identification of the CRT on which the symbols are to be displayed. For simplicity, it is assumed that only one CRT is being controlled by the unit **17** so that the ID code will then serve only to indicate the number of symbols to be displayed on one line starting with the first symbol centered at the point designated by the X_c and Y_c coordinate data entered.

The system thus far described in general terms is common to many radar display systems presently in use and is therefore presented here only as a typical environment for the present invention embodied in a symbol generating unit **19** and in other units, as will be described more fully with reference to FIGS. 7 to 9.

The symbol generating unit **19** is operated in synchronism with the symbol input buffer register **18** and the deflection control unit **15** by clock pulses (CP) from the unit **17**. After time has been allowed for the cathode ray beam to be positioned at a point designated by the coordinate data (h_c, Y_c) through the CRT deflection unit **16**, a symbol waveform is transmitted to the deflection control unit **15** where they are added to the X_c and Y_c coordinate signals.

While the symbol generating unit **19** is displaying one or more symbols, the symbol input buffer register **18** is prevented from receiving any further data from the unit **17** by an inhibit signal. In practice, the unit **17** would first determine whether such an inhibit signal is present before attempting to transfer data to the system input buffer register **18** in order to avoid wasting data processing time if the symbol generating unit **19** is busy processing a previous message.

The CRT deflection unit **16** may be electrostatic or electromagnetic but the latter is to be assumed not only because it is of the type most commonly used but also because it is the type which will benefit most from the present invention since the large deflection coils normally employed for rapid deflection of the electron beam with relatively small signals have large inductances, thereby giving rise to time constants for the X and Y deflection which are significant when display of a symbol having sharp corners is attempted. In an electrostatic deflection system, the deflection plates must be charged to the instantaneous value of the deflection signal presenting significant capacitance to the deflection circuits. There may be a sufficiently large time constant involved in charging the deflection plates to render display of symbols with sharp corners difficult. When that is the case, the present invention can be employed to equal advantage. Accordingly, the term "CRT deflection system" or "CRT deflection unit" is used herein to refer to either electromagnetic or electrostatic deflection.

FIG. 2 illustrates a simple symbol (inverted V or open triangle) and the 13 strokes required to produce it on the face of the CRT starting at the coordinate position X_c, Y_c at the center of the symbol. For simplicity, the end points of strokes are identified by the time periods T_1 to T_{13} required to display the symbol. The dashed line to point T_2 indicates the beam is blanked.

Two stroke periods are allowed to deflect the beam to point T_2. Thereafter, the beam is turned on and the symbol display proceeds by deflecting the beam toward point T_4 and then points T_5, T_6 and T_7. Since that requires changing the direction of the beam deflection by more than 45°, a full stroke period is allowed at point T_2. That is indicated by the subscript **3** in parenthesis at point t_2. Then during the fourth stroke period, as the beam is deflected to point T_4, the beam is unblanked. If the beam had been unblanked and deflected toward point T_4 during the third stroke period, the symbol display would have started with a trace along a dotted line shown. The result would obvi-

ously have been some distortion and a variation in the height of the symbol.

Allowing a full stroke period of rest at the point T_2 enables the CRT deflection system to position the electron beam at the point T_2 so that during the fourth stroke period, when the beam is unblanked, a trace is displayed from the point T_2 to the point T_4. This results in the loss of one full stroke period in "turning the corner," but allows the CRT deflection system to accurately draw the symbol at its full intended height, but this is outweighed by the advantage of this system which is: For a given deflection channel bandwidth and symbol fidelity standard, the time required to generate a given symbol is less, using the properly selected stroke time and resting one stroke period at corners, than it would be using another longer stroke time based on no rest periods at the corners. It should be understood that a grid of dots is shown in FIG. **2** (and FIGS. **5** and **6**) only to facilitate illustrating the X and Y stroke values from one point to the next. Those dots do not actually appear in the display of a symbol.

The straight portion from the point T_2 to the point T_7 is divided into four strokes with no waiting between strokes, but it should be understood that selection of the number of strokes forms no part of the present invention since that is largely determined by the characteristics of the CRT and its deflection system, and the size of the symbol. For a given CRT and symbol size, each stroke would normally be selected to be as long as possible consistent with a minimum level of brightness that can be achieved through the intensity control unit **11** and amplifier **12** which are normally programmed to provide greater intensity signals for faster beam deflection rates.

A full no-deflection stroke is programmed for the point T_7 as indicted by the subscript **8** in parenthesis. Thereafter, four strokes T_9 to T_{12} direct the beam to the end point T_{12}. There another full no-deflection stroke is programmed to allow the beam to reach point T_{12} before blanking is initiated. Otherwise, blanking would occur while the beam is still between points T_{11} and T_{12} to reduce the height of the symbol.

FIG. **3** is a chart of the program required to display the symbol of FIG. **2**. The left column indicates the stroke periods 1 to 13 indicated in FIG. **2** by the end points T_1 and T_{13} of the stroke periods. An additional stroke (Time **14**) is programmed to blank the beam and stop the symbol generating sequence in response to respective code bits in columns Z and S.

A code bit is indicated in the table by an X that is to be interpreted as a binary **1**. The absence of an X in any column at any stroke time is then to be interpreted as a binary **0**.

The first four columns of the table following the time column designate the number of positive or negative unit increments required along the X axis of the CRT. The next four columns provide the corresponding symbol program data for the Y axis. Since the symbol of FIG. **2** is generated by X and Y deflection values of only one or two units, four columns for each axis (with a code bit in only one column) is sufficient for a maximum stroke length of $2\sqrt{2}$ units. For other symbols, a maximum of **3** units of deflection in each axis is provided during a stroke period.

By storing the table of FIG. **3** as the program data for the symbol of FIG. **2**, and providing for retrieval of the data on a stroke by stroke basis, deflection waveforms X and Y shown in FIG. **4** are produced when the stroke deflection values are added as analog stroke signals X_s and Y_s to the coordinate signals X_c and Y_c of the starting point. The stroke deflection values are not added as step functions, but rather as substantially linear ramps obtained through an integrator using an operational amplifier. During a no-deflection stroke at each of times 3, 8, 13 and 14 the output of the integrator is held constant at the levels reached during the preceding stroke period.

Each symbol requires a different number of strokes. Accordingly, the stop code bit is important to terminate the symbol sequence. The letter B illustrated in FIG. **5** requires 16 stroke periods plus one for the blanking and stop code bits in columns Z and S. The X and Y deflection values for the symbol stroke can be determined directly from FIG. **5**. Some horizontal and vertical stroke values are 3 units. For example, the stroke values for the X and Y channels during the third stroke period are +3 and 0, respectively. Accordingly, at time 3 of the table for the symbol B, no bits would be stored in the four columns for the Y channel, and code bits would be stored in the +X and +2X columns for the Y channel. The numeral **5** in FIG. **6** requires 15 stroke periods plus one stroke for the blanking and stop code.

All of the letters of the alphabet, Arabic numerals and special symbols can be programmed, with maximum deflection strokes along a given axis of three units, in a predetermined maximum number of stroke periods, such as 28. Accordingly, as will be pointed out more full hereinafter, a time counter for a maximum number of stroke periods is provided, but is reset by the stop code bit whenever the sequence for a given symbol has been completed. However, any maximum number can be provided for a given system, such as to accommodate larger or more complex symbols. In addition, the maximum deflection values along each axis may be increased to 4 or more units, if desired.

A preferred embodiment of the symbol generating unit **19** of FIG. **1** will now be described with reference to FIGS. **7** to **9**. The routine for displaying one or more symbols is started by the radar control, data processing and symbol display programming unit **17** (FIG. **1**) which interrupts the video display of radar information, and enters coordinate data for the first symbol. That is accomplished by the unit **17** (FIG. **1**) setting a display sweep signal false, and a display symbol signal true, to disable transfer of the content of the content of a counter **20** and enable transfer of the content of a register **21** buffer register via AND gates **23***a*. Before the display symbol signal is made true, a coordinating value X_c is shifted into the register **21** in response to system clock pulses. That is accomplished by a shift enable signal applied to the register **21** by the display programming unit **17**. Once the display symbol signal is thereafter made true, the next clock pulse CP will load the coordinate value into the buffer register **22** where it is held until the symbol display routine has been completed, at which time the display sweep signal is made true to enable transfer of the content of the counter **20** to be loaded into the buffer register **22** in

response to each successive clock pulse CP via AND gate **23***b*.

The coordinate value stored in the buffer register **22** is converted to an analog signal by a digital-to-analog (D/A) converter **24** to drive the CRT beam in the X axis to a point designated for the first symbol to be displayed. An analog signal is similarly provided for the Y-axis channel.

To display a symbol, the present invention employs a symbol stroke storage unit **24** (FIG. **8**) to provide voltage signals X_s and Y_s proportional to successive X and Y stroke values via buffer registers **26** and **27**, and respective digital-to-analog converters **28** and **29**. The step voltage signals X_s and Y_s of the stroke values are integrated to provide ramp signals from one stroke value to another, and added to the coordinate signals to provide symbol waveforms starting at the designated point, such as the waveforms of FIG. **4** for the symbol of FIG. **2**.

An operational amplifier **30** (FIG. **7**) with a feedback capacitor **31** integrates the step voltage signal X_s, and an operational amplifier **32** having a feedback resistor **33** equal to coupling resistors **34** and **35** sums resulting ramp signals with the static deflection signal X_c for the X axis. A similar arrangement is provided for the step voltage signal Y_s in the Y channel (not shown).

A field effect transistor Q_1 of the junction-type or insulated-gate type is biased on during video display of radar data to maintain the capacitor **31** discharged. When a symbol is to be displayed, the compliment of a display symbol signal ($\overline{\text{DISPLAY SYMBOL}}$) transmitted through an OR gate **35** drives the gate of the field-effect transistor Q_1 below the pinchoff voltage level via an inverting amplifier **36**. That then enables the step voltages to be integrated until the symbol display routine is completed, at which time the complement of the display symbol signal is again set true to turn the transistor Q_1 on.

If more than one symbol is to be displayed, a track label position (TLS) signal is generated for two system clock periods following the display of each symbol to reset the integrator (i.e., to discharge the capacitor). At the same time, a symbol counter **37** is incremented by the TLS pulse. The output of that counter is converted to an analog signal by a digital-to-analog converter **38**, and the analog signal is coupled to the operational amplifier **32** by a resistor **39** for summing with the output signal from the digital-to-analog converter **23**, thereby shifting the starting point for the next symbol a predetermined distance along the X axis only. When the last of the symbols to be displayed on one line has been displayed, a master reset (MRST) signal resets the counter **37** to zero and terminates the display symbol signal, as will be more fully described with reference to FIGS. **8** and **9**.

Referring now to FIG. **8**, when a symbol is to be displayed, the radar control, data processing and display programming unit **17** (FIG. **1**) transfers symbol data to a register **40** and an ID code to a decoder **41**. The symbol data may consist of one or more 18-bit words, each word specifying three symbols. For simplicity, only one word is employed in the present exemplary embodiment. If up to six symbols were to be displayed on one line during a single display routine, the symbol data register **40** could be expanded to receive one word of symbol data before the second word is received with an ID code.

The ID code is a 6-bit code received from the symbol input buffer register where it is transferred by the unit **17** as an "instruction" in a manner typical of systems employing a digital computer to control external operations. The ID code is essentially an operation code, having for example, the four most significant digits coded to provide a symbol enable signal for a given one of a plurality of CRT display systems and the two least significant digits to provide a signal on one of three lines **1DS**, **2DS** and **3DS**, according to how many symbols are to be displayed. The symbol enable signal enables the symbol data register **40** to store the symbol data word. Accordingly, the symbol data register may be comprised of clocked J-K flip-flops with control of the J and K input terminals according to the following logic equations for a given flip-flop:

$$J = D_n \cdot \text{SYMBOL ENABLE}$$

$$K = \bar{D}_n \cdot \text{SYMBOL ENABLE}$$

where D_n is the data bit to be stored.

The symbol enable signal is also transmitted to a display routine control unit **42** (FIG. **8**) which generates an initial start signal. That is accomplished by a J–K flip-flop FF_2 (FIG. **9**) which is set by the next clock pulse once the symbol enable signal is true. The following clock pulse then sets a J–K flip-flop FF_2. The false output terminal of the flip-flop FF_2 disables a gate **43**. A following clock pulse then resets the flip-flop FF_1. A third J–K flip-flop FF_3 is set when the flip-flop FF_2 is set, but whereas the flip-flop FF_2 does not reset until the master reset (MRST) signal is generated, the flip-flop FF_3 will reset on the following clock pulse, thereby generating an initial start signal via an OR gate **44** that is one clock period long. Because the flip-flop FF_2 remains set, no further start signals may be generated by toggling the flip-flop FF_3 until a symbol display program has been completed and the MRST signal has been generated.

The symbol enable signal also sets a flip-flop FF_4 (FIG. **8**) to provide the complement of the display symbol signal to the integrator (FIG. **7**). The true output terminal of the flip-flop FF_4 transmits an inhibit signal to the input buffer register **18** (FIG. **1**) via a driver **46** to prevent any further symbol data words from being transmitted for display until all the symbols already programmed have been displayed and the signal MRST transmitted by the display routine control unit **42** resets the flip-flop FF_4.

The initial start signal from the control unit **42** sets the first stage of a sequence counter **48** to start a symbol display sequence timed by a system clock pulses (CP). The counter **48** is preferably implemented as a ring counter so that once the first stage is on, clock pulses will transfer the on state to successive stages until a stop signal is applied to all stages to turn off the one stage that is on and hold off all other stages.

The sequence counter **48** is employed to cause stroke values of a symbol to be read out in succession by transmitting to the storage unit **25** timing signals T_1 to T_{28} on separate lines via drivers **49**. It is for that reason the counter **48** is preferably mechanized as a ring counter. Once started, the stroke values are read

out of the storage unit in sequence by energizing successive lines in response to clock pulses until the stop code bit is read to reset the counter **48**. Once every stage of the counter is turned off, further application of clock pulses will have no effect on it, and all output lines T_1 to T_{28} are de-energized.

The symbol stroke storage unit **25** is mechanized with standard logic gates. The logic gates for each of the successive symbols to be displayed is selected by the 6-bit codes in the symbol data register **40** through a sequencer **50**. The logic gates for any one symbol is then selected by a symbol select matrix **51** which decodes a 6-bit symbol data code to energize one of 64 lines into the storage unit. The selection matrix may be mechanized as essentially 64 diode AND gates, each AND gate having six input terminals energized by a unique combination of the selected 6-bit symbol data code signals. For example, if the first symbol to be displayed is identified by the binary number 000110, the second and third least significant bit positions of that gate are connected to receive input signals from the true sides of flip-flops of corresponding orders in the data register **40** via the sequencer **50**, while all other input terminals are connected to receive input signals from the false sides of flip-flops of all other orders. The term "matrix" then pertains to only a rectangular arrangement of 64 output lines orthogonal to 12 input lines. Once each output line is connected to a suitable source of bias voltage by a separate resistor, the AND gates can be readily implemented by connecting diodes at proper intersections between input and output lines in a manner well known to those skilled in the art.

The sequencer **50** is also preferably mechanized with diode AND gates in a matrix of N input lines P_1 to P_N for display of from 1 to N symbols, where N is equal to three in this exemplary embodiment, and 36 orthogonal lines connected at one end to the true and false output terminals of 18 flip-flops in the data register. Each of the 36 lines is connected at the other end to a biasing resistor. Diodes are then connected at appropriate intersections to form three sets of twelve AND gates. The corresponding output terminals of the three sets are then connected to the respective ones of the 12 input lines to the symbol select matrix **51** by OR gates. In that manner, the true and false terminals of flip-flops in the data register **40** are effectively connected to the symbol select matrix **51** in three groups of six true and six false output terminals, i.e., in groups of true and false output terminals from three groups of 6 flip-flops each.

The mechanization for the storage unit **25** is illustrated by the following logic equations for the symbol of FIG. **2**:

$$+X = T_4(SC)_n + T_5(SC)_n + T_6(SC)_n + T_7(SC)_n + T_9(SC)_n + T_{10}(SC)_n + T_{11}(SC)_n + T_{12}(SC)_n$$

$$-2X = T_1(SC)_n + T_2(SC)_n$$

$$+2Y = T_4(SC)_n + T_5(SC)_n + T_6(SC)_n + T_7(SC)_n$$

$$-2Y = T_1(SC)_n + T_2(SC)_n + T_9(SC)_n + T_{10}(SC)_n + T_{11}(SC)_n + T_{12}(SC)_n$$

$$Z = T_4(SC)_n + T_{14}(SC)_n$$

$$S = T_{14}(SC)_n$$

where $(SC)_n$ represents a given one of 64 output lines from the symbol select matrix **51**. The corresponding output signal for all symbols are combined through 10 OR gates, one OR gate for the Z (blanking control) code bit, and one OR gate for the S (stop) code bit, and one OR gate for each of the respective X and Y values. The signals for the X and Y values are then encoded into 3-bit (sign and magnitude) codes, thus reducing the input to each of the buffer registers **26** and **27** from four to three. The conversion logic equations are as follows:

$$\text{Sign } X = (-X) + (-2X)$$
$$2X = (+2X) + (-2X)$$
$$X = (+X) + (-X)$$
$$\text{Sign } Y = (-Y) + (-2Y)$$
$$2Y = (+2Y) + (-2Y)$$
$$Y = (+Y) + (-Y)$$

This code conversion also facilitates implementing the digital-to-analog converters.

The flip-flops of the buffer registers **26** and **27** may be of the D type. The input at the single input of a given stage at the time a clock pulse occurs completely determines the state of the flip-flop. When a no-deflection stroke value is read from the storage unit, such as at times T_3, T_8 and T_{13} for the symbol of FIG. **2**, the last deflection stroke value is to be retained until the following times T_4, T_9 and T_{14}, respectively. At those times all output terminals of the symbol stroke storage unit are zero, so the registers **26** and **27** are reset, but the integrators, such as the integrator for the X channel (FIG. **7**), are not reset. Instead, they retain the last deflection stroke value because with all stages of the registers reset, no currents are being summed at the output terminals of the digitals-to-analog converters (i.e., at the summing junctions of the integrators).

As noted hereinbefore, the Z bit code controls the beam unblanking circuit of the CRT for symbol display. That may be accomplished by setting a JK flip-flop FF_6 in response to the first Z bit read and resetting it in response to the second Z bit read. To further assure resetting at the end of a symbol display program, the signal MRST may be applied to the flip-flop FF_6 as a direct reset, as shown. The true output of the flip-flop is transmitted to the intensity control unit **11** via the deflection control unit **15** in place of the unblanking control normally provided for range sweep display of radar video information.

A program counter **56** counts each stop code bit read and successively energizes the lines P_1 to P_N until the display routine control unit **42** detects that the designated number of symbols have been displayed and the program counter has been incremented once again. Detection of that condition initiates the signal MRST which resets the flip-flop FF_4, as noted hereinbefore, and resets the program counter to zero, thereby concluding a symbol display routine.

It should be noted that, when the program counter is reset to zero, not one of the lines P_1 to P_N is energized. Accordingly, not one of the 6-bit symbol codes in the register **40** is selected. That effectively provides a 64th code for the symbol selection matrix **51** to select from the storage unit s symbol sequence having only a stop code at a predetermined time, such as T_{18}. The first symbol of a display routine is thus caused to be simply a time delay count following the start signal to allow time for the beam deflection system to settle with the electron beam at the designated starting point (X_c, Y_c) for the first symbol.

Each of the stop code bit signals read from the storage unit **25** are also applied to the display routine control unit **42** to initiate another start signal. That is accomplished by J–K flip-flops FF_8 and FF_9. The flip-flop FF_8 is set by a clock pulse each time a stop code signal is received by it. The flip-flop FF_9 is then set by the next clock pulse. A following clock pulse then resets both flip-flops. The flip-flop FF_9 is thus set for one clock period to transmit a start signal through the OR gate **44**. The true output of the flip-flop FF_8 which is two clock pulse periods wide, is then the track label step signal (TLS) employed to reset the integrator capacitor **31** and increment the symbol counter **37**, as described hereinbefore with reference to FIG. 7.

When the program counter has been incremented by the stop code bit of the next to last symbol to be displayed, one of a plurality of AND gates **70** enables an AND gate **71** via an OR gate **72**, to set a flip-flop FF_{10} in response to the stop code of the next symbol to be displayed. For example, if the ID code specified that two symbols be displayed, the line **2DS** is energized. When a stop code bit of the first symbol displayed advances the program counter to the count of 2, the line P_2 is energized to enable the AND gate **71** via the OR gate **72** and AND gate **73**. Thus, the stop code bit of the second symbol sets the flip-flop FF_{10} to produce a master reset signal (MRST). The next clock pulse then resets the flip-flop FF_{10}. Once the signal MRST resets the flip-flop FF_4 (FIG. 8), the false output ($\overline{\text{DISPLAY SYMBOL}}$) resets the integrators to terminate the generation of symbol "waveforms," as described for the *X* channel with reference to FIG. 7.

The program counter **56** may be a conventional binary counter with output decoding gates to selectively energize the line P_1 to P_N in response to counts 1 to N. When reset, all lines are de-energized to provide an initial (dummy) sequencing of the symbol stroke storage unit as described hereinbefore.

Although the present invention has been described with reference to an exemplary embodiment, it is to be understood that additional embodiments and modifications will be obvious to those skilled in the art, particularly those required to meet operating requirements in different environments. For example, the rest period need not be equal to a stroke period; it may instead be equal to half of a stroke period, particularly if a higher clock rate is used and effectively divided by two in driving the sequence counter. Accordingly, it is not intended that the scope of the invention be determined by the disclosed exemplary embodiments, but rather should be determined by the breadth of the appended claims.

What is claimed is:

1. A system for displaying on the face of a cathode ray tube a symbol formed with substantially straight line strokes of an electron beam controlled by an *X-Y* rectangular Cartesian coordinate beam deflection system, comprising;

means for storing *X* and *Y* deflection values required for each of a sequence of strokes, each set of deflection values being specified relative to the end point of a preceding stroke, except values of the first set which are relative to a starting point, and for effectively storing zeros as no-deflection values between deflection values which will change direction of said beam by more than a predetermined amount;

means for reading out of said storage means said *X* and *Y* deflection values in sequence, including said no-deflection values;

means responsive to said reading means for generating signals corresponding in amplitude and polarity to the magnitude and sign of said *X* and *Y* deflection values;

means for integrating said signals to provide waveforms comprising sequences of ramp voltages for deflection of said beam in said straight line strokes forming said symbol.

2. The combination of claim 5 including:

means for generating static signals defining a point on the face of said tube at which said symbol is to be displayed; and

means for adding said waveforms to said static signals.

3. The combination of claim 5 wherein said cathode ray tube has a beam unblanking means, said point defined by said static signals differs from said starting point, said storage means includes deflection values required to move said beam from said defined point to said starting point in at least one initial stroke, and said storage means further includes a beam unblanking code with the next non-zero deflection value to be read out for the next stroke from said starting point, said combination including means responsive to said unblanking code for producing an unblanking signal to cause said beam unblanking means to unblank said beams.

4. The combination of claim 7 including means for terminating said beam unblanking signal a predetermined period after the last non-zero deflection value has been read from said storage means.

5. The combination of claim 8 wherein said means for terminating said beam unblanking signal comprises an unblanking code read from said storage means as the second non-deflection value following said last non-zero deflection value.

6. A symbol display system employing short straight line strokes to form symbols on the face of a cathode ray tube having a beam deflection system, said strokes proceeding from point to point, the starting point of a stroke being the end point of the last stroke immediately preceding it, and the initial starting point being defined by static deflection signals in a rectangular Cartesian coordinate system comprising;

means for storing in digital form stroke values of symbols to be displayed with zeros as non-deflection strokes between successive strokes having directions of beam deflection that differ by more than about 45°;

means for addressing a group of stored stroke values pertaining to a selected one of said symbols;

means for reading said stored stroke values pertaining to any selected one of said symbols in sequence;

means for converting successive stroke values read into analog step voltage signals;

means for integrating successive step voltage signals to produce a symbol waveform; and

means for adding said symbol waveform to said static deflection signals.

7. A symbol display system as defined in claim 10 wherein said cathode ray tube has a beam unblanking means, and said stroke values stored in digital code include beam unblanking control signals for unblanking from a first stroke forming a given symbol to a second no-deflection stroke value following a first no-deflection stroke value after a final stroke forming said given symbol, and means responsive to said beam unblanking signal to said beam unblanking means.

8. A symbol display system as defined in claim 11 wherein said addressing means include means for addressing more than one group of stroke values pertaining to more than one of said symbols for display in sequence, each displaced from the other a predetermined amount, and said second no-deflection stroke value following a first no-deflection stroke value includes a stop code digit, said display system including;

means for programming the addressing of more than one group of stroke values;

means for advancing said programming means from the address of one programmed group of stroke value to another in response to said stop code digit;

means responsive to said stop code digit for changing said static deflection signals to move the initial starting point for each symbol displayed a predetermined distance in a predetermined direction; and

means responsive to said stop code digit for resetting said integrating means to zero.

9. In a radar system employing a cathode ray tube having an X-Y rectangular Cartesian coordinate beam deflection system for display of video data, and means for interrupting display of video data for displaying at least one of a plurality of selectable symbols at a desired position on the face of the cathode ray tube, the combination comprising;

first means for receiving and storing in digital form coordinate values of said position,

second means for converting said digital coordinate value into static analog deflection control signals,

third means for storing for each of said selectable symbols a sequence of sets of X and Y deflection values required for each of a sequence of strokes, each set of deflection values being specified relative to the end point of a preceding stroke, except values of the first set which are relative to a starting point, and for effectively storing zeroes as no-deflection values between deflection values which will change direction of said beam by more than a predetermined amount;

fourth means for receiving and storing in digital code form identification of a given symbol to be displayed;

fifth means responsive to said fourth means for addressing in said third means a sequence of sets of X and Y deflection values required for display of said given symbol;

sixth means for reading in sequence said sets of X and Y deflection values of said given symbol, with constant time intervals between reading sets;

seventh means responsive to said sixth means for converting respective X and Y deflection values of each set into analog step voltage signals of amplitudes proportional to corresponding deflection values;

eight means responsive to said seventh means for converting each sequence of said stop voltage signals into a sequence of ramp voltage signals to provide symbol waveforms having substantially static voltage levels from the beginning of a time interval upon reading no-deflection values until the next time interval, and

ninth means responsive to said second means and said eighth means for superimposing each of said symbol waveforms on analog deflection control signals along corresponding reference axis.

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PO-1050
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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,717,872 Dated February 20, 1973

Inventor(s) MELVIN E. SNOOK ET AL

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 12, line 15, the claim reference numeral "5" should read --1--.

Column 12, line 21, the claim reference numeral "5" should read --1--.

Column 12, line 34, the claim reference numeral "7" should read --3--.

Column 12, line 38, the claim reference numeral "8" should read --4--.

Column 13, line 1, the claim reference numeral "10" should read --6--.

Column 13, line 10, the claim reference numeral "11" should read --7--.

Signed and sealed this 17th day of September 1974.

(SEAL)
Attest:

McCOY M. GIBSON JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

PO-1050
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