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Weng et al.

(54) **CHIP PACKAGE STRUCTURE AND MANUFACTURING METHODS THEREOF**

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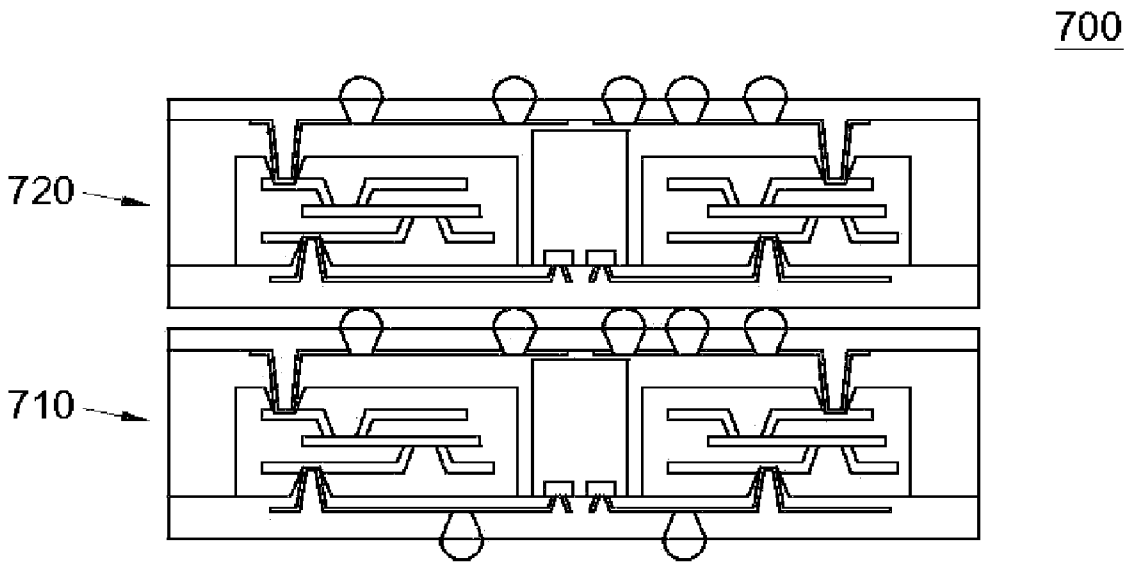
(57) **ABSTRACT**

A chip package structure includes a chip module, a plurality of pre-patterned structures, a filling material layer, and a redistribution layer. The chip module includes a chip including an upper surface, a side surface, and an active surface. The pre-patterned structures are disposed around the chip. Each of the pre-patterned structures includes a circuit, a first surface, an upper surface opposite the first surface, and a side surface. The filling material layer encapsulates the chip and the pre-patterned structures. The filling material layer includes a second surface, and encapsulates the upper and side surfaces of the chip, and the upper and side surfaces of each of the pre-patterned structures. The active surface, each first surface, and the second surface are substantially co-planar. The redistribution layer is disposed on the active surface, each first surface, and the second surface. The redistribution layer electrically connects the chip and each circuit.



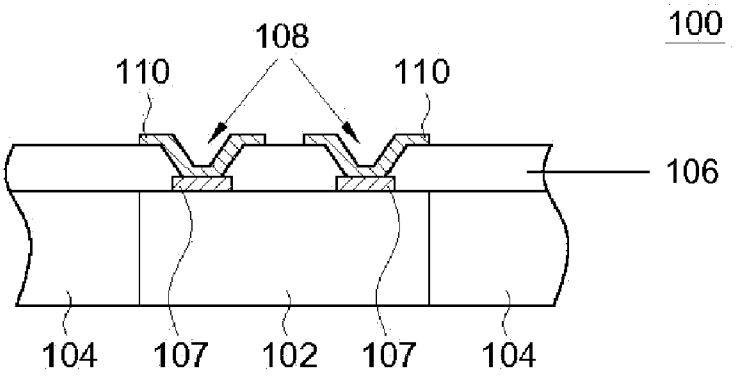


FIG. 1(PRIOR ART)

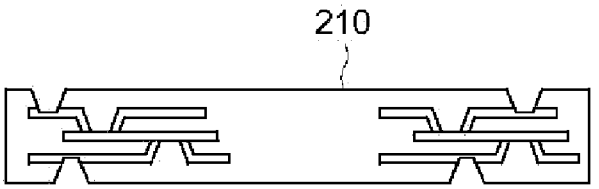


FIG. 2A

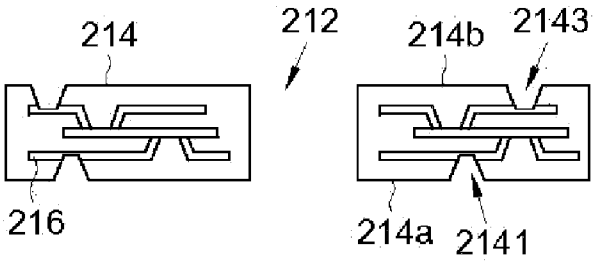


FIG. 2B

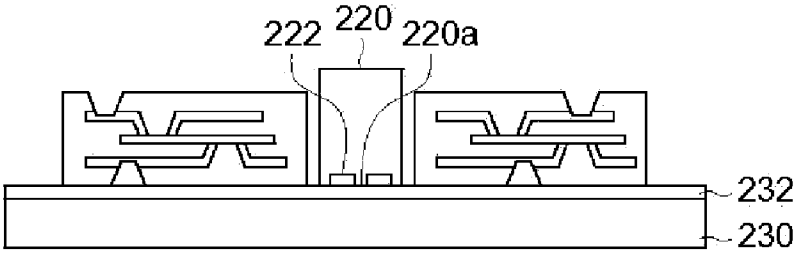


FIG. 2C

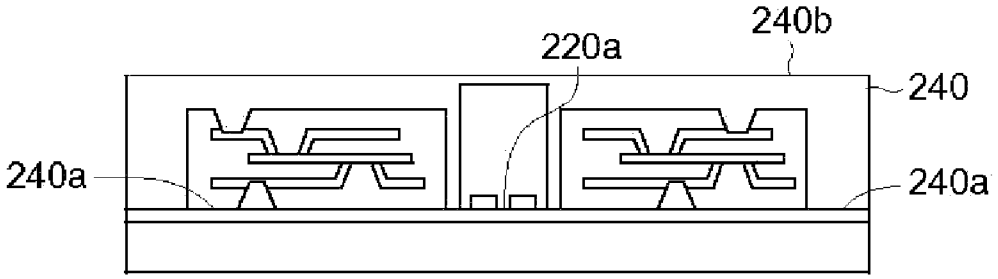


FIG. 2D

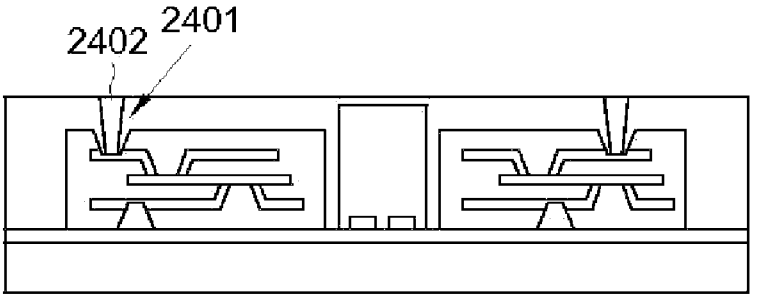


FIG. 2E

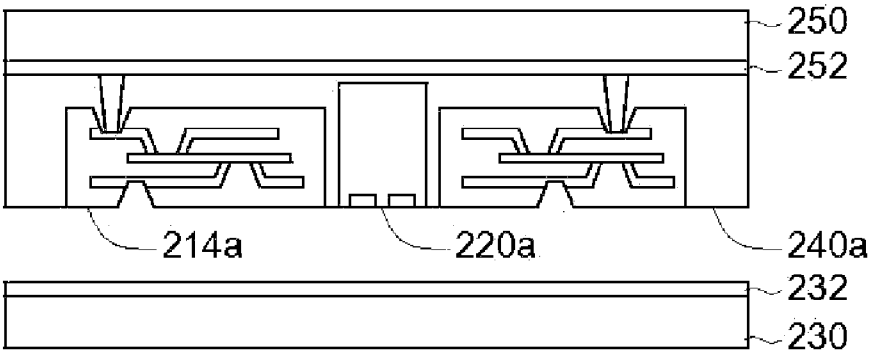


FIG. 2F

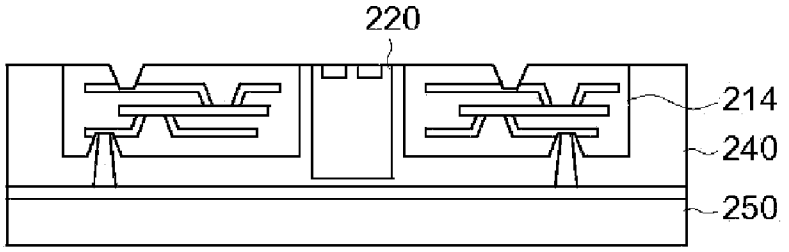


FIG. 2G

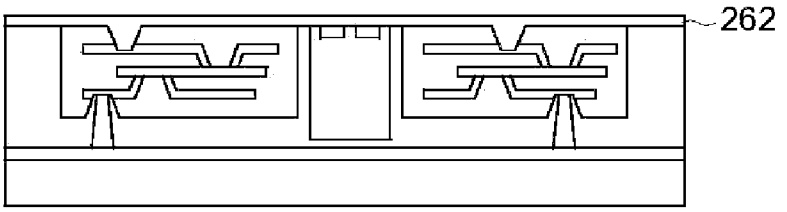


FIG. 2H

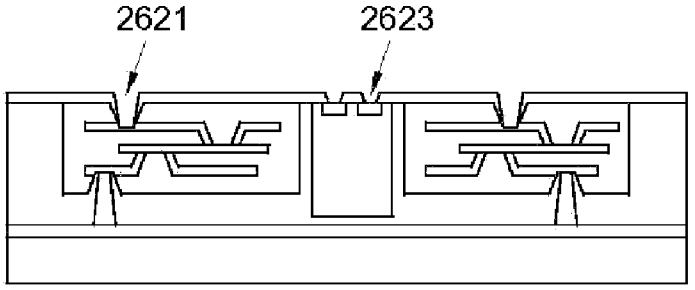


FIG. 2I

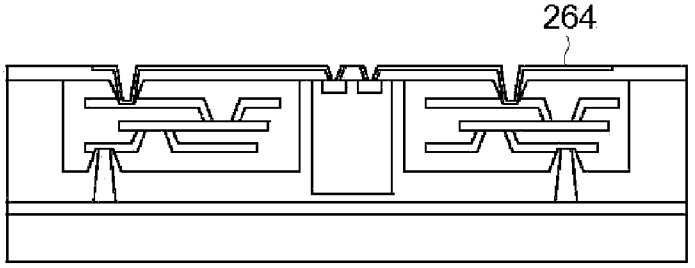


FIG. 2J

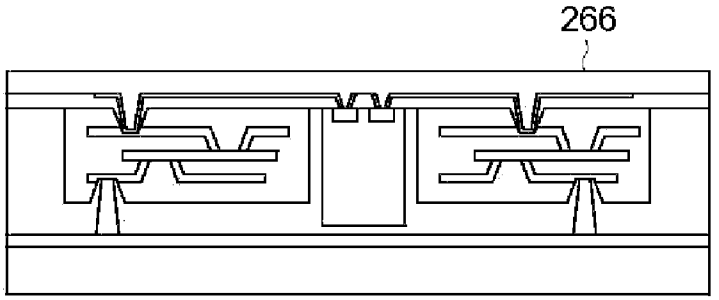


FIG. 2K

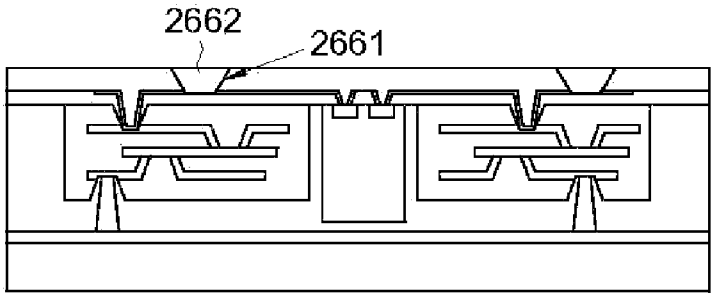


FIG. 2L

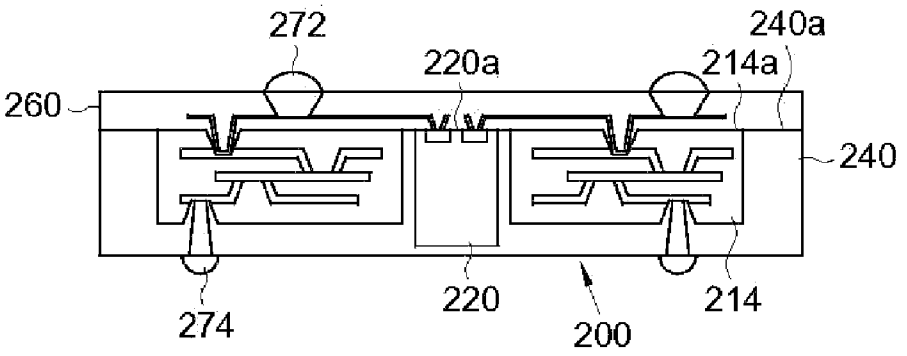


FIG. 2M

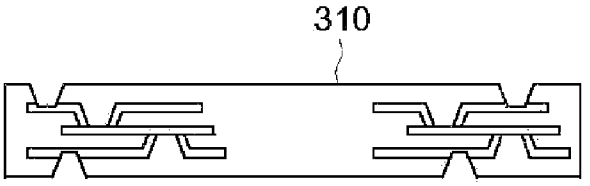


FIG. 3A

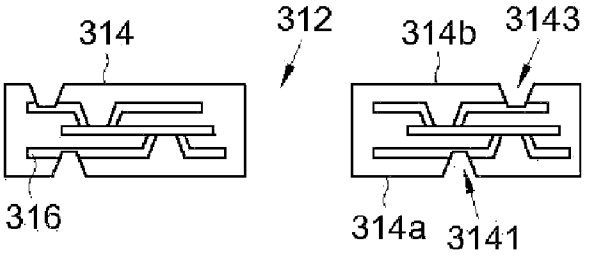


FIG. 3B

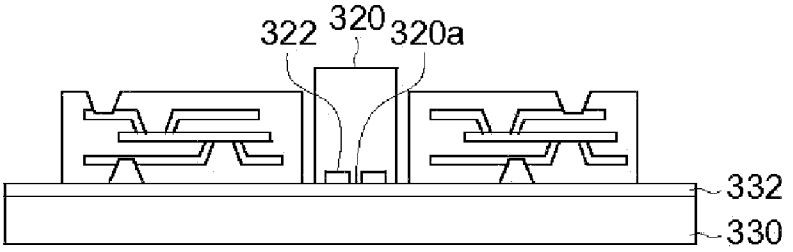


FIG. 3C

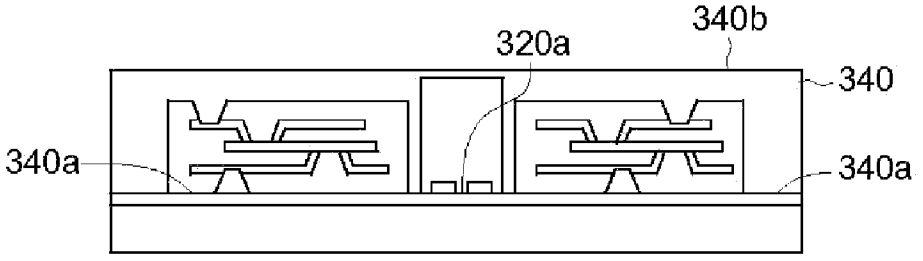


FIG. 3D

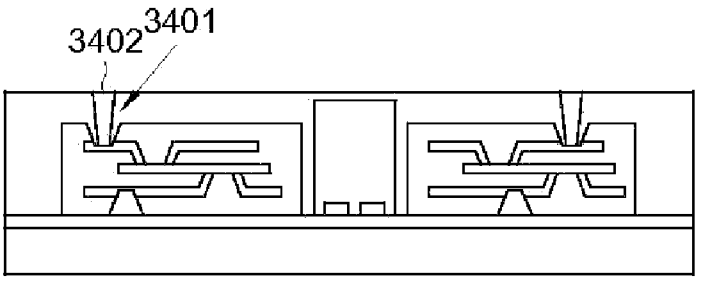


FIG. 3E

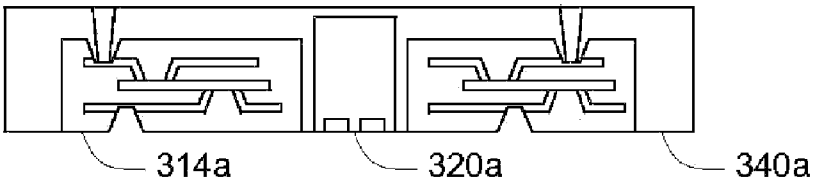


FIG. 3F

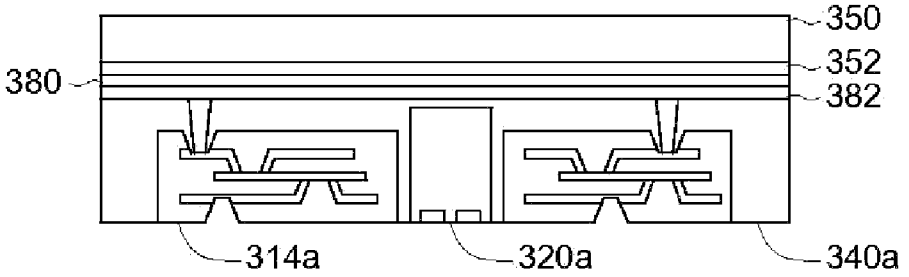


FIG. 3G

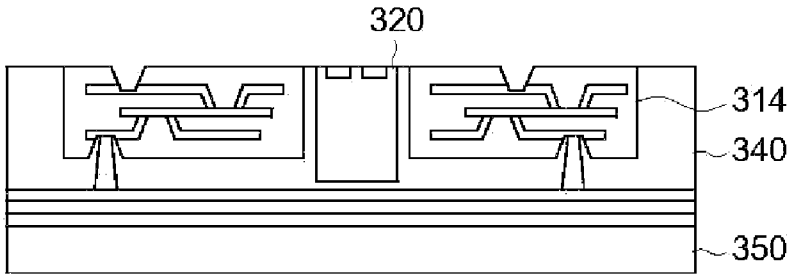


FIG. 3H

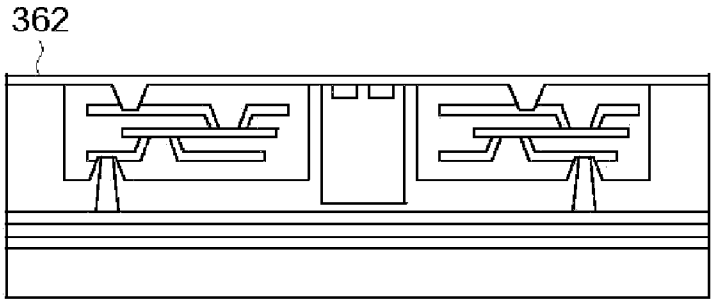


FIG. 3I

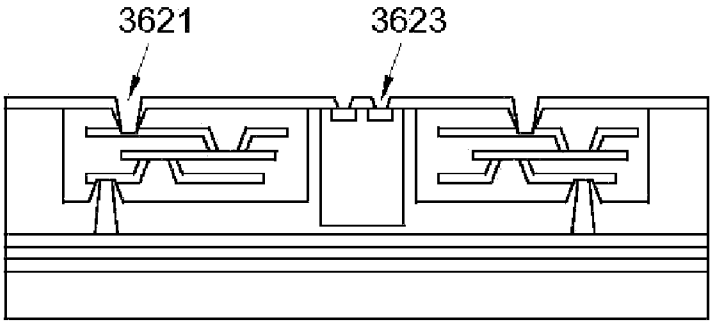


FIG. 3J

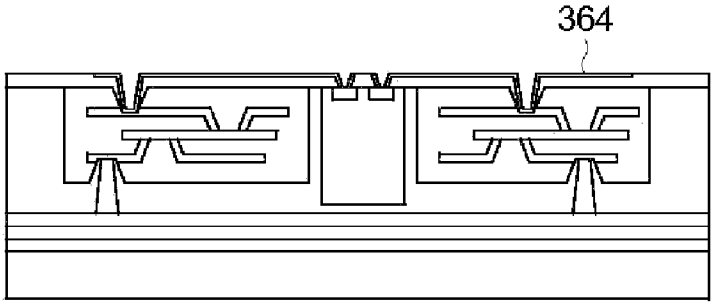


FIG. 3K

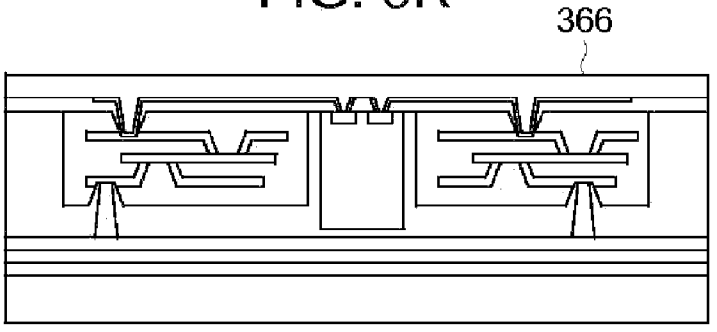


FIG. 3L

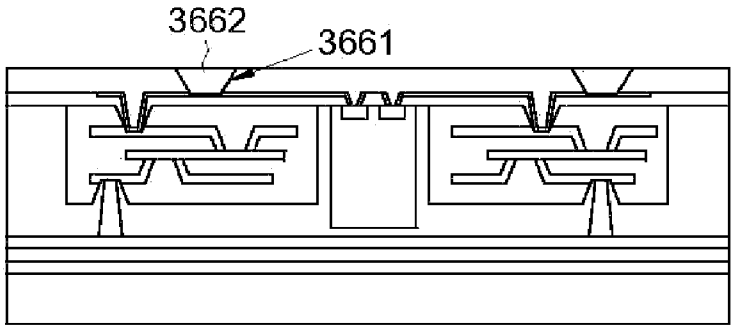


FIG. 3M

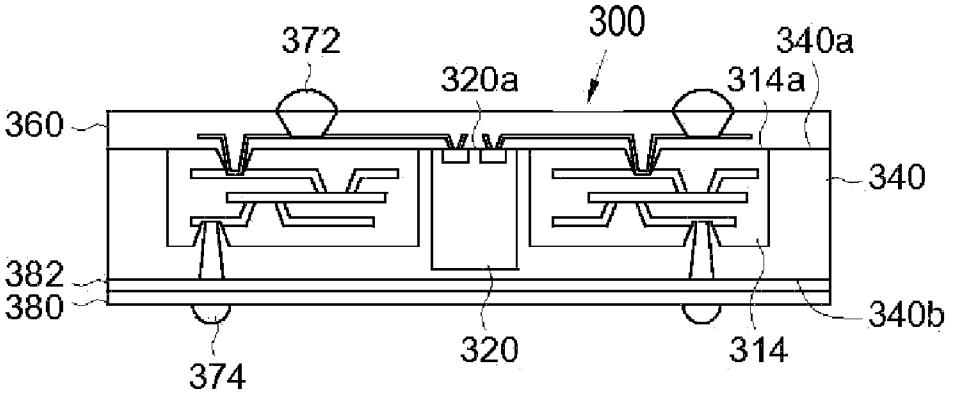


FIG. 3N

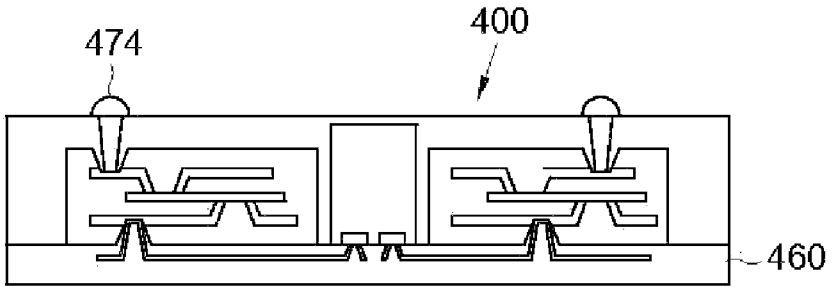


FIG. 4

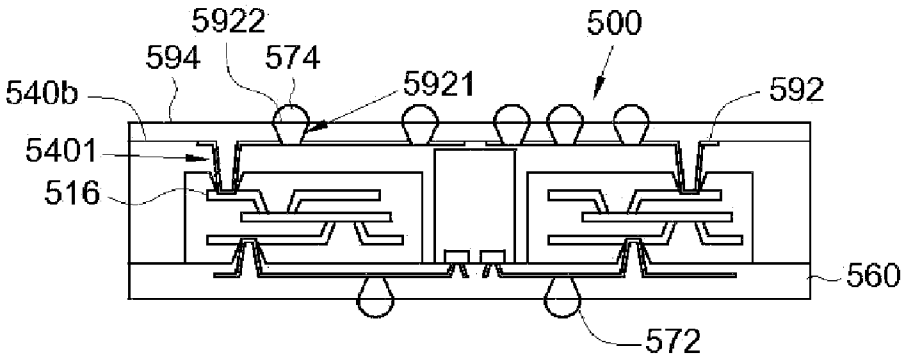


FIG. 5

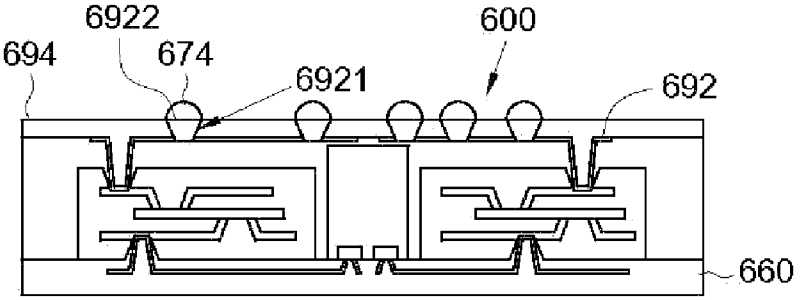


FIG. 6

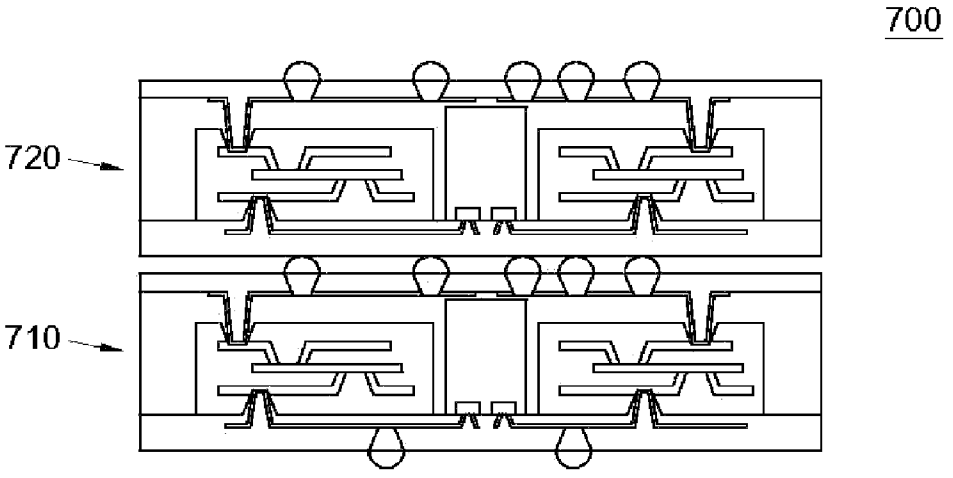


FIG. 7

CHIP PACKAGE STRUCTURE AND MANUFACTURING METHODS THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation of U.S. patent application Ser. No. 12/648,270, filed Dec. 28, 2009, which claims the benefit of Taiwan application Serial No. 98120583, filed Jun. 19, 2009, the subject matter of which is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention generally relates to electronic device packaging. More particularly, the present invention relates to a chip package structure and manufacturing methods thereof.

BACKGROUND OF THE INVENTION

[0003] FIG. **1** is a schematic view showing a conventional chip package structure in accordance with prior art. A conventional single-chip or multi-chip package structure is shown. The single-chip or multi-chip package structure **100** includes at least one chip **102**, a plurality of structural material layers **104**, a dielectric layer **106**, a plurality of solder pads **107**, and a metal layer **110**. A plurality of solder pads **107** are disposed on the chip **102**. A plurality of structural material layers **104** are connected to a lateral side of the chip **102**, wherein the surface of the structural material layer **104** is aligned with the surface of the chip **102**. The dielectric layer **106** is disposed on the structural material layer **104** and the chip **102**, wherein the top surface of the surface of the chip **102** is aligned with the surface of the structural material layer **104**. The dielectric layer **106** has a plurality of openings **108**. The metal layer **110** is disposed on the dielectric layer **106** and the side-wall of the openings **108**.

[0004] In order to increase the density of electrical connections of the package structure, a through molding compound technology is typically applied to the structural material layer **104** first, such as mechanical drilling through the structural material layer **104** to enable electrical connectivity to the metal layer **110**. However, at present, the through molding compound technology is costly.

SUMMARY OF THE INVENTION

[0005] Accordingly, one aspect of the present invention is directed to a chip package structure and manufacturing methods thereof The chip package structure may be a single-chip or multi-chip package structure.

[0006] In one innovative aspect, the invention relates to a chip package structure. In one embodiment, the chip package structure includes a chip module, a plurality of pre-patterned structures, a filling material layer, and a redistribution layer. The chip module includes a chip including an upper surface, a side surface, and an active surface. The plurality of pre-patterned structures are disposed around the chip. Each of the plurality of pre-patterned structures includes a circuit, a first surface, an upper surface opposite the first surface, and a side surface. The filling material layer encapsulates the chip and the plurality of pre-patterned structures. The filling material layer includes a second surface, and encapsulates the upper surface of the chip, the side surface of the chip, the upper surface of each of the plurality of pre-patterned structures, and the side surface of each of the plurality of pre-patterned structures. The active surface, the first surface of each of the plurality of pre-patterned structures, and the second surface are substantially co-planar. The redistribution layer is disposed on the active surface, the first surface of each of the plurality of pre-patterned structures, and the second surface. The redistribution layer electrically connects the chip and the circuit in each of the plurality of pre-patterned structures.

[0007] In another innovative aspect, the invention relates to a method of forming a chip package structure. In one embodiment, the method includes providing a plurality of separate pre-patterned structures, where each of the plurality of separate pre-patterned structures includes a circuit, a first surface, an upper surface opposite the first surface, and a side surface. The method further includes providing a chip module including a chip, where the chip includes an upper surface, a side surface, and an active surface opposite the upper surface of the chip. The method further includes providing a carrier. The method further includes disposing the plurality of separate pre-patterned structures and the chip adjacent to the carrier such that the plurality of separate pre-patterned structures are positioned around the chip. The method further includes forming a filling material layer around the chip and the plurality of separate pre-patterned structures so that: (a) the filling material layer substantially covers the upper surface of the chip, the side surface of the chip, the upper surface of each of the plurality of separate pre-patterned structures, and the side surface of each of the plurality of separate pre-patterned structures; and (b) a second surface of the filling material layer is substantially co-planar with the active surface and the first surface of each of the plurality of separate pre-patterned structures. The method further includes disposing a redistribution layer on the active surface, the first surface of each of the plurality of separate pre-patterned structures, and the second surface, wherein the redistribution layer electrically connects the chip and the circuit in each of the plurality of separate pre-patterned structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings are included to provide a further understanding of some embodiments of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of some embodiments of the invention.

[0009] FIG. **1** is a schematic view showing a conventional chip package structure in accordance with prior art;

[0010] FIGS. **2**A through **2**M are schematic views showing a method for manufacturing a chip package structure according to a first embodiment of the invention;

[0011] FIGS. **3**A through **3**N are schematic views showing a method for manufacturing a chip package structure according to a fifth embodiment of the invention;

[0012] FIG. **4** shows a schematic view of a chip package structure according to a second embodiment of the invention;

[0013] FIG. **5** shows a schematic view of a chip package structure according to a third embodiment of the invention;

[0014] FIG. **6** shows a schematic view of a chip package structure according to a fourth embodiment of the invention; and

[0015] FIG. **7** shows a schematic view of a multi-chip package structure according to a sixth embodiment of the invention.

DETAILED DESCRIPTION

[0016] Reference will now be made in detail to some embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the descriptions to refer to the same or like parts.

Definitions

[0017] The following definitions apply to some of the aspects described with respect to some embodiments of the invention. These definitions may likewise be expanded upon herein.

[0018] As used herein, the singular terms "a", "an" and "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to a protruding metal block can include multiple protruding metal blocks unless the context clearly dictates otherwise.

[0019] As used herein, the term "set" refers to a collection of one or more components. Thus, for example, a set of layers can include a single layer or multiple layers. Components of a set also can be referred to as members of the set. Components of a set can be the same or different. In some instances, components of a set can share one or more common characteristics.

[0020] As used herein, the term "adjacent" refers to being near or adjoining. Adjacent components can be spaced apart from one another or can be in actual or direct contact with one another. In some instances, adjacent components can be connected to one another or can be formed integrally with one another.

[0021] As used herein, terms such as "inner," "top," "upper," "bottom," "above," "below," "upwardly," "downwardly," "side," and "lateral" refer to a relative orientation of a set of components, such as in accordance with the drawings, but do not require a particular orientation of those components during manufacturing or use.

[0022] As used herein, the terms "connect", "connected" and "connection" refer to an operational coupling or linking. Connected components can be directly coupled to one another or can be indirectly coupled to one another, such as via another set of components.

[0023] As used herein, the terms "substantially" and "substantial" refer to a considerable degree or extent. When used in conjunction with an event or circumstance, the terms can refer to instances in which the event or circumstance occurs precisely as well as instances in which the event or circumstance occurs to a close approximation, such as accounting for typical tolerance levels of the manufacturing operations described herein.

[0024] As used herein, the terms "conductive" refers to an ability to transport an electric current. Electrically conductive materials typically correspond to those materials that exhibit little or no opposition to flow of an electric current. One measure of electrical conductivity is in terms of Siemens per meter ("$S \cdot m^{-1}$"). Typically, an electrically conductive material is one having a conductivity greater than about 10^4 $S \cdot m^{-1}$, such as at least about 10^5 $S \cdot m^{-1}$ or at least about 10^6 $S \cdot m^{-1}$. Electrical conductivity of a material can sometimes vary with temperature. Unless otherwise specified, electrical conductivity of a material is defined at room temperature.

[0025] Aspects of the present invention can be used for fabricating various package structures, such as stacked type packages, multiple-chip packages, or high frequency device packages.

[0026] According to embodiments of the chip package structure of the invention, the pre-patterned structure is placed in the structural material around the embedded chip, and at least one surface of the chip, the pre-patterned structure and the filling material layer are substantially co-planar. Embodiments of the invention are applicable to single-chip and multi-chip package structures, as well as to fan-out and fan-in package structures. Embodiments of the package structures of the invention can be conveniently stacked to form a package-on-package (POP) package.

First Embodiment

[0027] Referring to FIG. **2**M, a schematic view of a method for manufacturing a chip package structure according to a first embodiment of the invention is shown. The chip package structure **200** includes a chip module, a plurality of pre-patterned structures **214**, a filling material layer **240**, and a redistribution layer **260**. The chip module includes a chip **220** including an active surface **220***a*, an upper surface opposite the active surface **220***a*, and a side surface extending between the active surface **220***a* and the upper surface of the chip **220**. The pre-patterned structures **214** are disposed around the chip **220**. Also, referring to FIG. **2**B, each of the pre-patterned structures **214** includes a circuit **216**, a first surface **214***a*, an upper surface **214***b* opposite the first surface **214***a*, and a side surface extending between the first surface **214***a* and the upper surface **214***b*. In FIG. **2**M, the filling material layer **240** encapsulates the chip **220** and the pre-patterned structures **214**. The filling material layer **240** encapsulates the upper surface of the chip **220**, the side surface of the chip **220**, the upper surface **214***b* of each of the pre-patterned structures **214**, and the side surface of each of the pre-patterned structures **214**. The filling material layer **240** has a second surface **240***a*. The active surface **220***a*, each first surface **214***a* and the second surface **240***a* are substantially co-planar. The filling material layer **240** may be made from a photo-imageable or a non-photo-imageable material. This material is preferably but not limited to a molding compound, and other structural materials which can be used as fillers are also applicable to embodiments of the invention. The redistribution layer **260** is disposed on the active surface **220***a*, each first surface **214***a*, and the second surface **240***a*, and electrically connects the chip **220** and each circuit **214**. Furthermore, the chip package structure **200** may further include a plurality of external connectors **272** and **274** respectively disposed on the redistribution layer **260** and the filling material layer **240**.

[0028] The pre-patterned structure **214** of this embodiment of the invention is placed in the structural material around the embedded chip **200** of the chip package structure **200**, and serves as a supporting structure of the package, not only increasing the density of electrical connections in small-sized packages, but also incurring lower cost than conventional through molding compound technology. Furthermore, in this embodiment of the invention, the active surface **220***a*, each first surface **214***a* and the second surface **240***a* are substantially co-planar, not only effectively increasing the process conformity rate of the redistribution layer **260**, but also incurring lower manufacturing cost. For example, the co-planar

design may enable coatings such as a dielectric layer **262** (shown in FIG. **2**H) to have a substantially uniform thickness, which may simplify a coating process, and may enable the exposing energy to be consistent in an exposing process that may be used, for example, to create openings **2621** (shown in FIG. **2**I). In this embodiment, the method for manufacturing the chip package structure **200** includes the following steps.

[0029] Referring to FIG. **2**A, a substrate **210** is provided, wherein the substrate preferably is an organic substrate or a silicon substrate. Next, as indicated in FIG. **2**B, a through hole **212** is formed on the substrate **210** to form a plurality of pre-patterned structures **214**, wherein each of the pre-patterned structures **214** includes a circuit **216**, a first surface **214***a*, an upper surface **214***b* opposite to the first surface **214***a*, and a side surface extending between the first surface **214***a* and the upper surface **214***b*. At least one of the pre-patterned structures **214** may include a slot **2141** on the first surface **214***a*, where the slot **2141** exposes a part of the circuit **216**. At least one of the pre-patterned structures **214** may include another slot **2143** on the upper surface **214***b*, where the another slot **2143** exposes another part of the circuit **216**. The at least one of the pre-patterned structures **214** may include multiple interconnected trace layers embedded between the first surface **214***a* and the upper surface **214***b*. The multiple interconnected trace layers may be interconnected, such as by vias.

[0030] As indicated in FIG. **2**C, a chip module is provided, wherein the chip module includes a chip **220** having an active surface **220***a* and at least one pad **222** disposed on the active surface **220***a*. Moreover, the chip **220** and the pre-patterned structures **214** are placed on a counterpart carrier **230** that may have an adhesive layer **232**, so that the chip **220** is accommodated in the through hole **212**, and the pre-patterned structures **214** are disposed around the chip **220**. As the through hole **212** is slightly larger than the chip **220**, a gap is formed between the chip **220** and the pre-patterned structures **214**.

[0031] Referring to FIG. **2**D, a filling material layer **240** is formed for encapsulating the chip **220** and the pre-patterned structures **214**. Meanwhile, the filling material layer **240** is further disposed in the gap between the chip **220** and each of the pre-patterned structures **214**. The filling material layer **240** encapsulates the upper surface of the chip **220**, the side surface of the chip **220**, the upper surface **214***b* of each of the pre-patterned structures **214**, and the side surface of each of the pre-patterned structures **214**. As indicated in FIG. **2**D, the filling material layer **240** includes a second surface **240***a* and an upper surface **240***b* opposite the second surface **240***a*. The active surface **220***a*, each first surface **214***a*, and the second surface **240***a* are substantially co-planar.

[0032] In FIG. **2**E, a hole **2401** may be formed in the filling material layer **240**, where the hole **2401** penetrates to the another slot **2143** (illustrated in FIG. **2**B) from the upper surface **240***b*. A conductive material **2402** may be placed in the hole **2401**.

[0033] Referring to FIG. **2**F, a process carrier **250** including an adhesive layer **252** may be disposed on the upper surface **240***b* (illustrated in FIG. **2**D), and the counterpart carrier **230** including the adhesive layer **232** may be removed to expose the active surface **220***a*, each first surface **214***a*, and the second surface **240***a*.

[0034] Then, the process carrier **250**, the filling material layer **240**, the chip **220**, and the pre-patterned structures **214** encapsulated by the filling material layer **240** are inverted as indicated in FIG. **2**G.

[0035] Next, a redistribution layer **260** (illustrated in FIG. **2**M) is disposed on the active surface **220***a*, each first surface **214***a*, and the second surface **240***a* to electrically connect the chip **220** and each circuit **216**. The redistribution layer **260** passes through the slot **2141** (illustrated in FIG. **2**B) to electrically connect to a part of the circuit **216**, and is electrically connected to the chip **220** through the pad **222** (illustrated in FIG. **2**C). In this embodiment, the formation of the redistribution layer **260** includes the following steps. As indicated in FIG. **2**H, a first dielectric layer **262** is formed, where the first dielectric layer **262** and the filling material layer **240** may be made from the same or different materials. In FIG. **2**I, first openings **2621** and **2623** of the first dielectric layer **262** are formed, where the first opening **2621** corresponds to the slot **2141** that exposes a part of the circuit **216**, and the first opening **2623** exposes the pad **222**. The first openings **2621** and **2623** are preferably formed by way of exposing and developing, but may also be formed by other methods such as laser drilling, mechanical drilling, or punching. Next, as indicated in FIG. **2**J, a patterned conductive layer **264** is disposed on a top surface of the first dielectric layer **262**, side-walls of the first openings **2621** and **2623**, the exposed pad **222**, and the exposed part of the circuit **216**. Then, as indicated in FIG. **2**K, a second dielectric layer **266** is disposed on the patterned conductive layer **264** and the first dielectric layer **262**. In FIG. **2**L, a plurality of second openings **2661** are formed on the second dielectric layer **262** for exposing the patterned conductive layer **264** (illustrated in FIG. **2**J). A conductive material **2662** may be placed in second openings **2661**. The second dielectric layer **266** and the filling material layer **240** may be made from the same or different materials.

[0036] Referring to FIG. **2**M, a plurality of external connectors **272** may be disposed on the conductive material **2662**, and a plurality of external connectors **274** may be disposed on the conductive material **2402** to form a package having the chip package structure **200**. The external connectors **272** and **274** are preferably solder bumps or solder balls.

Second Embodiment

[0037] Compared with the first embodiment, this second embodiment of the invention omits the forming a plurality of second openings **2661** on the second dielectric layer **262** and accommodating the conductive material **2662** in a plurality of second openings **2661** (shown in FIG. **2**L), and omits disposing a plurality of external connectors **272** on the conductive material **2662** (shown in FIG. **2**M) to form a package having the chip package structure **400** of FIG. **4**. That is, the manufacturing method of the chip package structure **400** of this second embodiment of the invention includes the processing in FIGS. **2**A through **2**K and a part of the processing in FIG. **2**M. The redistribution layer **460** of the chip package structure **400** of FIG. **4** does not have an opening, no external connector is disposed on the corresponding side of the chip package structure **400**, and the external connector **474** disposed on another side of the chip package structure **400** may provide electrical connectivity to circuitry outside the chip package structure **400**.

Third Embodiment

[0038] Compared with the first embodiment, this third embodiment of the invention omits the forming the hole **2401**

on the filling material layer **240** and accommodating the conductive material **2402** (shown in FIG. **2**E). In this embodiment, the processing shown in FIG. **2**E is replaced by the following processing. Referring to FIG. **5**, a conductive layer **592** is disposed on an upper surface **540***b* of the filling material layer **540**, a side-wall of the hole **5401** on the filling material layer **540**, and a part of the circuit **516** exposed from the hole **5401**. In addition, a dielectric layer **594** is disposed on the conductive layer **592**, where the dielectric layer **594** and the filling material layer **540** may be made from the same or different materials. The dielectric layer **594** has a plurality of openings **5921**, which expose the conductive layer **592**. The openings **5921** are preferably formed by way of exposing and developing, but may also be formed by other methods such as laser drilling, mechanical drilling, or punching in the present process. Furthermore, the conductive material **5922** is filled in the openings **5921**. That is, the manufacturing method of the chip package structure **500** of this third embodiment of the invention not only includes the processing shown in FIGS. **2**A through **2**D, a part of the processing shown in FIG. **2**E, and the processing shown in FIGS. **2**F through **2**M, but also includes the steps of forming the conductive layer **592**, forming the dielectric layer **594** having a plurality of openings **5921**, and interposing the conductive material **5922** into the openings **5921**. Compared with the first embodiment, one side of the chip package structure **500** of this third embodiment of the invention may have more external connectors **574**.

Fourth Embodiment

[0039] Compared with the third embodiment, this fourth embodiment of the invention omits forming a plurality of second openings **2661** on the second dielectric layer **262** and accommodating the conductive material **2662** in a plurality of second openings **2661** (shown in FIG. **2**L), and omits disposing a plurality of external connectors **272** on the conductive material **2662** (shown in FIG. **2**M) to form a package having the chip package structure **600** of FIG. **6**. That is, the manufacturing method of the chip package structure **600** of the present embodiment of the invention not only includes the processing shown in FIGS. **2**A through **2**D, a part of the processing shown in FIG. **2**E, the processing shown in FIGS. **2**F through **2**K, and a part of the processing shown in FIG. **2**M, but also includes forming the conductive layer **692**, forming the dielectric layer **694** having a plurality of openings **6921**, and interposing the conductive material **6922** into the openings **6921**. Compared with the third embodiment, the redistribution layer **660** of this fourth embodiment of the invention does not have an opening, so the corresponding side of the chip package structure **600** does not have an external connector. The external connector **674** disposed on another side of the chip package structure **600** may provide electrical connectivity to circuitry outside the chip package structure **600**. Compared with the first embodiment, another side of the chip package structure **600** of FIG. **6** may also have more external connectors **674**.

Fifth Embodiment

[0040] Referring to FIG. **3**N, a schematic view of a method for manufacturing a chip package structure according to a fifth embodiment of the invention is shown. The chip package structure **300** includes a chip module, a plurality of pre-patterned structures **314**, a filling material layer **340**, a redistribution layer **360**, and a protection layer **380**. The protection layer **380** may be disposed on an adhesive layer **382**, and the adhesive layer **382** may be disposed on an upper surface **340***b* of the filling material layer **340** so that the adhesive layer **382** connects the protection layer **380** and the filling material layer **340**. The chip module includes a chip **320** including an active surface **320***a*, an upper surface opposite the active surface **320***a*, and a side surface extending between the active surface **320***a* and the upper surface of the chip **320**. The pre-patterned structures **314** are disposed around the chip **320**. Also, referring to FIG. **3**B, each of the pre-patterned structure **314** includes a circuit **316**, a first surface **314***a*, an upper surface **314***b* opposite the first surface **314***a*, and a side surface extending between the first surface **314***a* and the upper surface **314***b*. In FIG. **3**N, the filling material layer **340** encapsulates the chip **320** and the pre-patterned structures **314**. The filling material layer **340** encapsulates the upper surface of the chip **320**, the side surface of the chip **320**, the upper surface **314***b* of each of the pre-patterned structures **314**, and the side surface of each of the pre-patterned structures **314**. The filling material layer **340** has a second surface **340***a* and an upper surface **340***b*, and the active surface **320***a*, each first surface **314***a*, and the second surface **240***a* are substantially co-planar. The filling material layer **340** may be made from a photo-imageable or a non-photo-imageable material. This material is preferably but not limited to a molding compound, and other structural materials which can be used as fillers are also applicable to embodiments of the invention. The redistribution layer **360** is disposed on the active surface **320***a*, each first surface **314***a*, and the second surface **340***a*, and electrically connects the chip **320** and each circuit **314**. The adhesive layer **382** is disposed on another second surface **340***b*, and the protection layer **380** is disposed on the adhesive layer, wherein the adhesive layer **382** is used for connecting the protection layer **380** and the filling material layer **340**. Preferably, the protection layer **380** is a thermal fin. Furthermore, the chip package structure **300** further includes a plurality of external connectors **372** and **374** respectively disposed on the redistribution layer **360** and the filling material layer **340**.

[0041] The pre-patterned structure **314** of this fifth embodiment of the invention is placed in the structural material around the embedded chip **300** of the chip package structure **300**, and serves as a supporting structure of the package, not only increasing the density of electrical connections in small-sized packages, but also incurring lower cost than the conventional through molding compound technology. Furthermore, in this fifth embodiment of the invention, the active surface **220***a*, each first surface **214***a*, and the second surface **240***a* are substantially co-planar, not only effectively increasing the process conformity rate of the redistribution layer **360**, but also incurring lower manufacturing cost. For example, the co-planar design may enable coatings such as a dielectric layer **362** (shown in FIG. **3**I) to have a substantially uniform thickness, which may simplify a coating process, and may enable the exposing energy to be consistent in an exposing process that may be used, for example, to create openings **3621** (shown in FIG. **3**J). In this embodiment, the method for manufacturing the chip package structure **300** includes the following steps.

[0042] Referring to FIG. **3**A, a substrate **310** is provided, wherein the substrate preferably is an organic substrate or a silicon substrate. Next, as indicated in FIG. **3**B, a through hole **312** is formed on the substrate **310** to form a plurality of pre-patterned structures **314**, wherein each of the pre-pat-

terned structure **314** includes a circuit **316**, a first surface **314***a*, an upper surface **314***b* opposite to the first surface **314***a*, and a side surface extending between the first surface **314***a* and the upper surface **314***b*. At least one of the pre-patterned structures **314** may include a slot **3141** on the first surface **314***a*, wherein the slot **3141** exposes a part of the circuit **316**. At least one of the pre-patterned structures **314** may include another slot **3143** on the upper surface **314***b*, where the another slot **3143** exposes another part of the circuit **316**. The at least one of the pre-patterned structures **314** may include multiple interconnected trace layers embedded between the first surface **314***a* and the upper surface **314***b*. The multiple interconnected trace layers may be interconnected, such as by vias.

[0043] As indicated in FIG. **3**C, a chip module is provided, wherein the chip module includes a chip **320** having an active surface **320***a* and at least one pad **322** disposed on the active surface **320***a*. Moreover, the chip **320** and the pre-patterned structures **314** are placed on a counterpart carrier **330** that may have an adhesive layer **332**, so that the chip **320** is accommodated in the through hole **312**, and the pre-patterned structures **314** are disposed around the chip **320**. As the through hole **312** is slightly larger than the chip **320**, a gap is formed between the chip **320** and the pre-patterned structures **314**.

[0044] Referring to FIG. **3**D, a filling material layer **340** is formed for encapsulating the chip **320** and the pre-patterned structures **314**. Meanwhile, the filling material layer **340** is further disposed in the gap between the chip **320** and each of the pre-patterned structures **314**. The filling material layer **340** encapsulates the upper surface of the chip **320**, the side surface of the chip **320**, the upper surface **314***b* of each of the pre-patterned structures **314**, and the side surface of each of the pre-patterned structures **314**. The filling material layer is made from a photo-imageable or a non-photo-imageable material. This material is preferably but not limited to a molding compound, and other structural materials which can be used as fillers are also applicable to embodiments of the invention. As indicated in FIG. **3**D, the filling material layer **340** includes a second surface **340***a* and an upper surface **340***b* opposite to the second surface **340***a*. The active surface **320***a*, each first surface **314***a*, and the second surface **340***a* are substantially co-planar.

[0045] In FIG. **3**E, a hole **3401** may be formed in the filling material layer **340**, where the hole **3401** penetrates to the another slot **3143** (illustrated in FIG. **3**B) from the upper surface **340***b*. A conductive material **3402** may be placed in the hole **3401**.

[0046] Referring to FIG. **3**F, the counterpart carrier **330** including the adhesive layer **332** may be removed to expose the active surface **320***a*, each first surface **314***a*, and the second surface **340***a*.

[0047] Next, in FIG. **3**G, a protection layer **380**, an adhesive layer **382**, and a process carrier **350** including an adhesive layer **352** may be sequentially stacked on the upper surface **340***b* (illustrated in FIG. **3**D). The adhesive layer **382** connects the protection layer **380** and the filling material layer **340**, and the adhesive layer **352** is connects the protection layer **380** and the process carrier **350**.

[0048] Then, the process carrier **350** including an adhesive layer **352**, the protection layer **380**, the adhesive layer **382**, the filling material layer **340**, the chip **320**, and the pre-patterned structures **314** encapsulated by the filling material **340** are inverted as indicated in FIG. **3**H.

[0049] Next, a redistribution layer **360** (illustrated in FIG. **3**N) is disposed on the active surface **320***a*, each first surface **314***a*, and the second surface **340***a* to electrically connect the chip **320** and each circuit **316** (illustrated in FIG. **3**B). The redistribution layer **360** passes through the slot **3141** (illustrated in FIG. **3**B) to electrically connect to part of the circuit **316**, and is electrically connected to the chip **320** through the pad **322** (illustrated in FIG. **3**C). In this embodiment, the formation of the redistribution layer **360** includes the following steps. As indicated in FIG. **3**I, a first dielectric layer **362** is formed, where the first dielectric layer **362** and the filling material layer **340** may be made from the same or different materials. In FIG. **3**J, first openings **3621** and **3623** are formed on the first dielectric layer **362**, where the first opening **3621** corresponds to the slot **3141** (illustrated in FIG. **3**B) that exposes a part of the circuit **316**, and the first opening **3623** exposes the pad **322** (illustrated in FIG. **3**C). The first openings **3621** and **3623** are preferably formed by way of exposing and developing, but may also be formed by other methods such as laser drilling, mechanical drilling, or punching. Next, as indicated in FIG. **3**K, a patterned conductive layer **364** is disposed on a top surface of the first dielectric layer **362**, side-walls of the first openings **3621** and **3623**, the exposed pad **322** (illustrated in FIG. **3**C), and the exposed part of the circuit **316**. Then, as indicated in FIG. **3**L, a second dielectric layer **366** is disposed on the patterned conductive layer **364** (illustrated in FIG. **3**K) and the first dielectric layer **362** (illustrated in FIG. **3**J), where the second dielectric layer **366** and the filling material layer **340** may be made from the same or different materials. In FIG. **3**M, a plurality of second openings **3661** are formed on the second dielectric layer **362** to expose the patterned conductive layer **364** (illustrated in FIG. **3**J) and to accommodate a conductive material **3662**. The second opening **3661** is preferably formed by way of exposing and developing, but may also be formed by other methods such as laser drilling, mechanical drilling, or punching.

[0050] Referring to FIG. **3**N, a plurality of external connectors **372** may be disposed on the conductive material **3662**, and a plurality of external connectors **374** may be disposed on the conductive material **3402** to form a package having the chip package structure **300**. The external connector **372** and **374** are preferably solder bumps or solder balls.

[0051] Compared with the fifth embodiment, another embodiment of the invention omits forming a plurality of second openings **3661** on the second dielectric layer **362** and accommodating the conductive material **3662** in a plurality of second openings **3661** (shown in FIG. **3**M), and omits disposing a plurality of external connectors **372** on the conductive material **3662** (shown in FIG. **3**N). That is, the method for manufacturing a chip package structure according to another embodiment of the invention includes the processing shown in FIGS. **3**A through **3**L and a part of the processing shown in FIG. **3**M.

[0052] Compared with the fifth embodiment, yet another embodiment of the invention includes the processing shown in FIGS. **3**A through **3**D, a part of the processing shown in FIG. **3**E, and the processing shown in FIGS. **3**F through **3**N, and further includes processing similar to that described for the third embodiment such as forming the conductive layer, forming the dielectric layer having a plurality of holes, and interposing the conductive material into the gaps to replace the above processing shown in FIG. **3**E of forming the hole **3401** on the filling material layer **340** and accommodating the conductive material **3402**. Compared with the fifth embodi-

ment, one side of the chip package structure of the yet another embodiment may also have more external connectors.

[0053] Compared with the fifth embodiment, a further embodiment omits forming a plurality of second openings **3661** on the second dielectric layer **362** and accommodating the conductive material **3662** in a plurality of second openings **3661** (shown in FIG. **3**M), and omits disposing a plurality of external connectors **372** on the conductive material **3662** (shown in FIG. **3**N). That is, the method for manufacturing a chip package structure of the further embodiment not only includes the processing shown in FIGS. **3**A through **3**D, a part of the processing shown in FIG. **3**E, the processing shown in FIGS. **3**F through **3**L and a part of the processing shown in FIG. **3**N, and but also includes processing similar to that described for the fourth embodiment such as forming the conductive layer, forming the dielectric layer having a plurality of holes, and interposing the conductive material in the openings. Compared with the yet another embodiment, the redistribution layer of the further embodiment does not have an opening, so the corresponding side of the chip package structure does not have an external connector. The external connector disposed on another side of the chip package structure may provide electrical connectivity to circuitry outside the chip package structure. Compared with the fifth embodiment, another side of the further chip package structure may also have more external connectors.

[0054] The chip package structure disclosed in the above embodiments is a single-chip package structure, but can be a multi-chip package structure if the chip module includes a plurality of chips. There are a plurality of pre-patterned structures disposed around each chip. Furthermore, the active surface of the chips, the second surface of the filling material layer, and the first surfaces of the pre-patterned structures are substantially co-planar.

[0055] Furthermore, the single-chip or the multi-chip package structure disclosed in the above embodiments can be stacked to form a package-on-package (POP) package, which includes a plurality of identical or different packages sequentially stacked. Referring to FIG. **7**, a multi-chip package structure according to a sixth embodiment of the invention is shown. In this embodiment, the package-on-package structure **700** includes a first package **710** and a second package **720**. The second package **720** is attached above the first package **710**, and at least one of the first package **710** and the second package **720** can be a single-chip or a multi-chip package structure disclosed in the above described embodiments.

[0056] The chip package structure disclosed in the above described embodiments of the invention has many advantages as exemplified below.

[0057] 1. The pre-patterned structure placed in the structural material around the embedded chip serves as a supporting structure of the package, not only increasing the density of electrical connection in small-sized packages, but also incurring lower cost than conventional through molding compound technology.

[0058] 2. The design that the active surface of the chip, each first surface of each pre-patterned structure, and the second surface of the filling material layer are substantially co-planar effectively increases the process conformity rate of the redistribution layer and reduces the manufacturing cost. For example, the co-planar design may enable coatings such as a dielectric layer **262** (shown in FIG. **2**H) to have a substantially uniform thickness, which may simplify a coating process, and may enable the exposing energy to be consistent in an exposing process that may be used, for example, to create openings **2621** (shown in FIG. **2**I).

[0059] 3. Embodiments of the invention are very flexible, and are applicable to single-chip and multi-chip package structures as well as fan-out and fan-in package structures. Package structures of embodiments of the invention can be conveniently stacked to form a package-on-package (POP) package.

[0060] While the invention has been described by way of example and in terms of several embodiments, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. A semiconductor package, comprising:
- a chip having an active surface;
- a pre-patterned structure disposed adjacent to lateral surfaces of the chip, the pre-patterned structure having a contact on a surface oriented in the same direction as the active surface;
- a redistribution layer that electrically connects the active surface of the chip with the contact; and
- a filling material that covers portions of the chip, exposing the active surface and the pre-patterned structure.

2. The semiconductor package of claim **1**, wherein the active surface of the chip is substantially co-planar with a surface of the pre-patterned structure.

3. The semiconductor package of claim **2**, wherein the redistribution layer is disposed adjacent to the active surface of the chip and the substantially co-planar surface of the pre-patterned structure.

4. The semiconductor package of claim **1**, wherein the pre-patterned structure includes interconnected trace layers.

5. The semiconductor package of claim **1**, wherein the filling material covers the lateral surfaces of the chip.

6. The semiconductor package of claim **1**, wherein the filling material substantially covers a surface of the pre-patterned structure and has an opening to expose a contact on the surface of the pre-patterned structure.

7. The semiconductor package of claim **1**, further including a second redistribution layer disposed adjacent to an inactive surface of the chip and electrically connected to the pre-patterned structure.

8. A semiconductor package, comprising:
- a chip having an active surface;
- an interposer disposed adjacent to a lateral surface of the chip, the interposer having a contact on a surface oriented in the same direction as the active surface;
- a redistribution layer that electrically connects the active surface of the chip with the contact; and
- a filling material that covers portions of the chip, exposing the active surface and the pre-patterned structure.

9. The semiconductor package of claim **8**, wherein the active surface of the chip is substantially co-planar with a surface of the interposer.

10. The semiconductor package of claim **9**, wherein the redistribution layer is disposed adjacent to the active surface of the chip and the substantially co-planar surface of the interposer.

11. The semiconductor package of claim **8**, wherein the interposer includes interconnected trace layers.

12. The semiconductor package of claim **8**, wherein the filling material covers the lateral surfaces of the chip.

13. The semiconductor package of claim **8**, wherein the filling material substantially covers a surface of the interposer and has an opening to expose a contact on the surface of the interposer.

14. The semiconductor package of claim **8**, further including a second redistribution layer disposed adjacent to an inactive surface of the chip and electrically connected to the interposer.

15. The semiconductor package of claim **14**, wherein the filling material has an opening wherein the second redistribution layer is electrically connected to the interposer through the opening.

16. The semiconductor package of claim **8**, further comprising an adhesive layer disposed on a surface of the filling material.

17. The semiconductor package of claim **16**, further comprising a protection layer disposed on the adhesive layer, wherein the adhesive layer connects the protection layer to the surface of the filling material.

18. A method of forming a semiconductor package, comprising:

providing a chip;

providing a plurality of separate pre-patterned structures, wherein each of the plurality of separate pre-patterned structures includes a circuit;

providing a carrier;

disposing the plurality of separate pre-patterned structures and the chip on the carrier such that the plurality of separate pre-patterned structures are positioned adjacent to lateral sides of the chip; and

disposing a filling material around the chip and the plurality of separate pre-patterned structures, exposing an active surface of the chip.

19. The method of claim **18**, wherein each of the plurality of separate pre-patterned structures includes multiple interconnected trace layers.

20. The method of claim **18**, further comprising:

creating a slot on a surface of each of the separate pre-patterned structures to expose the circuit of the pre-patterned structure; and

forming a redistribution layer disposed adjacent to the active surface of the chip and substantially co-planar surfaces of the plurality of the separate pre-patterned structures, wherein the redistribution layer electrically connects the chip and the circuit in each of the plurality of separate pre-patterned structures through the slots.

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