# United States Patent [19]

**Takahashi**

[11] **3,783,192**

[45] **Jan. 1, 1974**


[54] **DECODER FOR USE IN MATRIX FOUR-CHANNEL SYSTEM**


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[73] Assignee: **Sansui Electric Co., Ltd.**, Tokyo, Japan



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Nov. 30, 1972 Japan ..... 47/120033

[52] **U.S. Cl.** ..... **179/1 GQ, 179/100.4 ST, 179/100.1 TD**

[51] **Int. Cl.** ..... **H04r 5/04**

[58] **Field of Search** ..... 179/1 GQ, 1 G, 1 GP, 179/15 BT, 100.4 ST, 100.1 TD



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*Primary Examiner*—William C. Cooper
*Assistant Examiner*—Thomas D'Amico
*Attorney*—Ford W. Harris, Jr. et al.



[57] **ABSTRACT**

A decoder for use in an SQ matrix four-channel system comprises first and second matrix circuits for forming a difference signal and a sum signal of the first and second channel signals respectively. The output signals from the first and second matrix circuits are supplied to third and fourth matrix circuits to produce reproduced rear signals which are supplied to two rear loudspeakers disposed to the rear of a listener. Between the first and second matrix circuits and third and fourth matrix circuits is connected at least one phase shifter which gives a phase difference of about 90° between the output signals from the first and second matrix circuits. The first and second channel signals are supplied to respective ones of two front loudspeakers disposed in the front of the listener.


**14 Claims, 19 Drawing Figures**

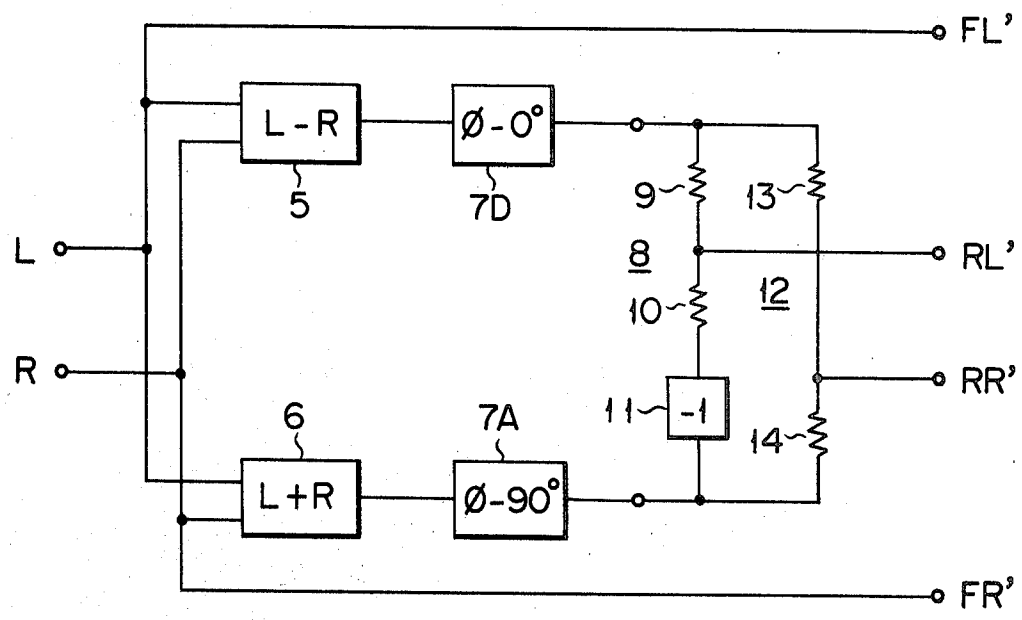


FIG. 1

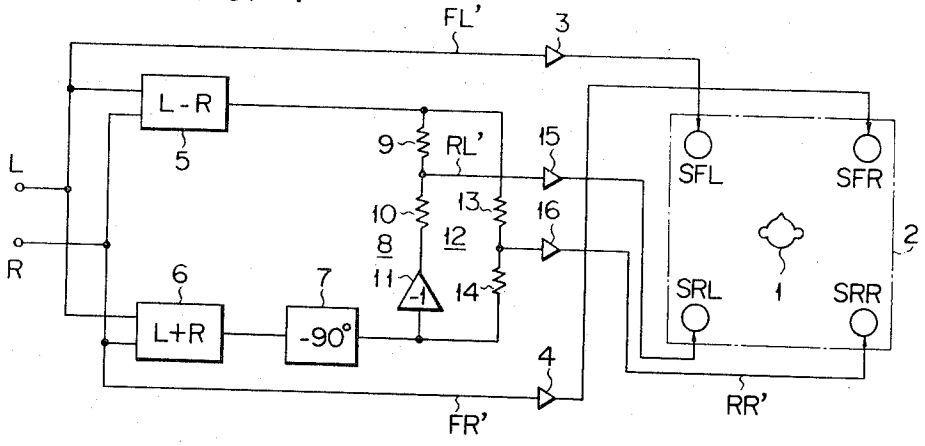



FIG. 2A

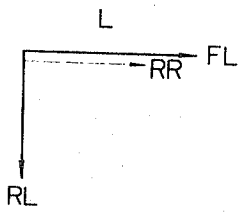



FIG. 2B

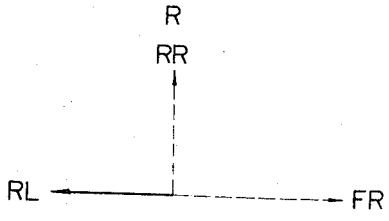



FIG. 3A

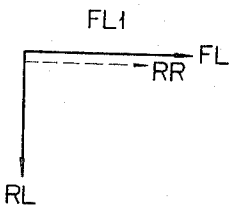



FIG. 3B

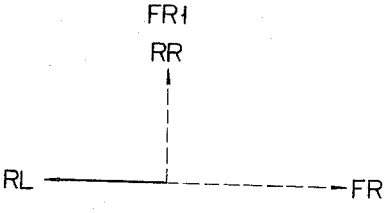



FIG. 3C

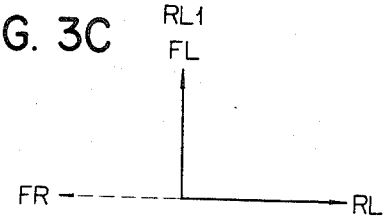



FIG. 3D

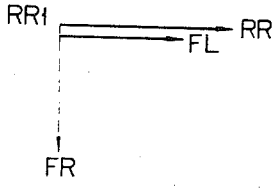


FIG. 4A

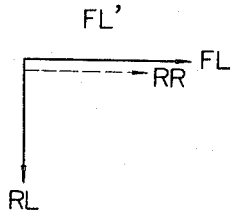



FIG. 4B

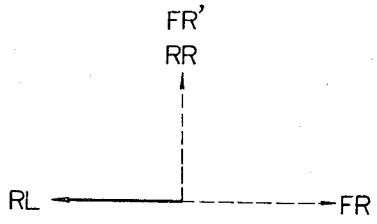



FIG. 4C

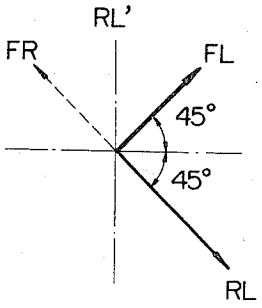



FIG. 4D

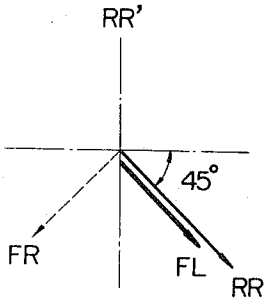



FIG. 5

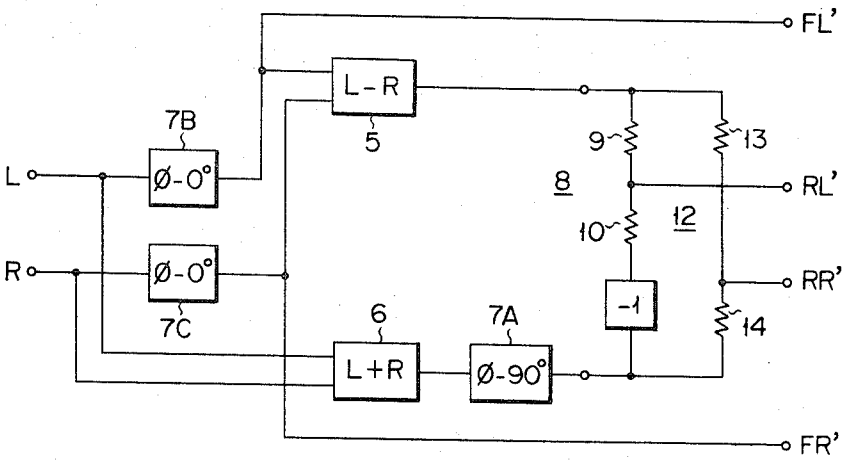


FIG. 6

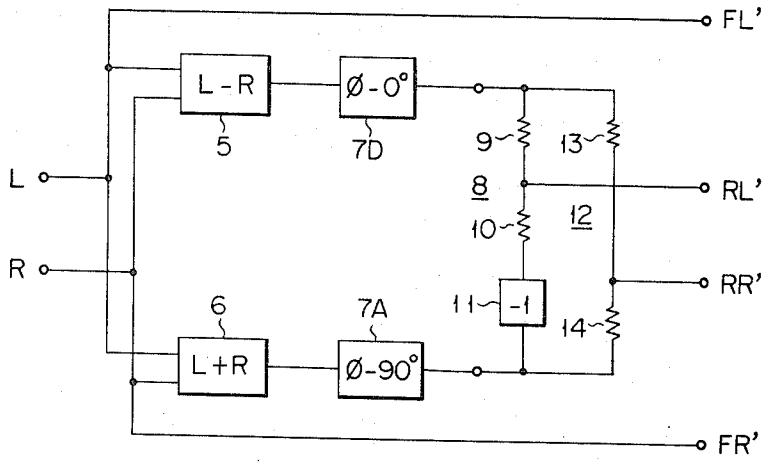



FIG. 7

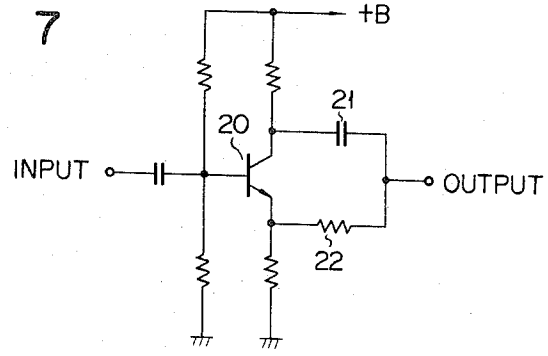



FIG. 8

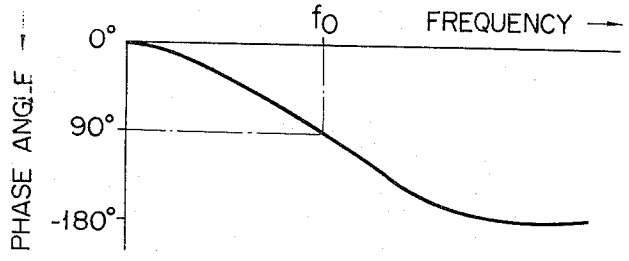


FIG. 9

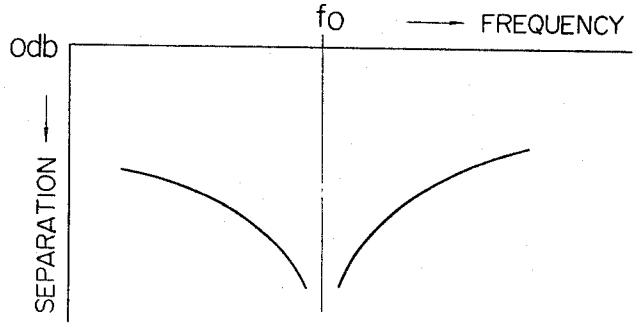

fo
FREQUENCY
odb
SEPARATION

FIG. 10

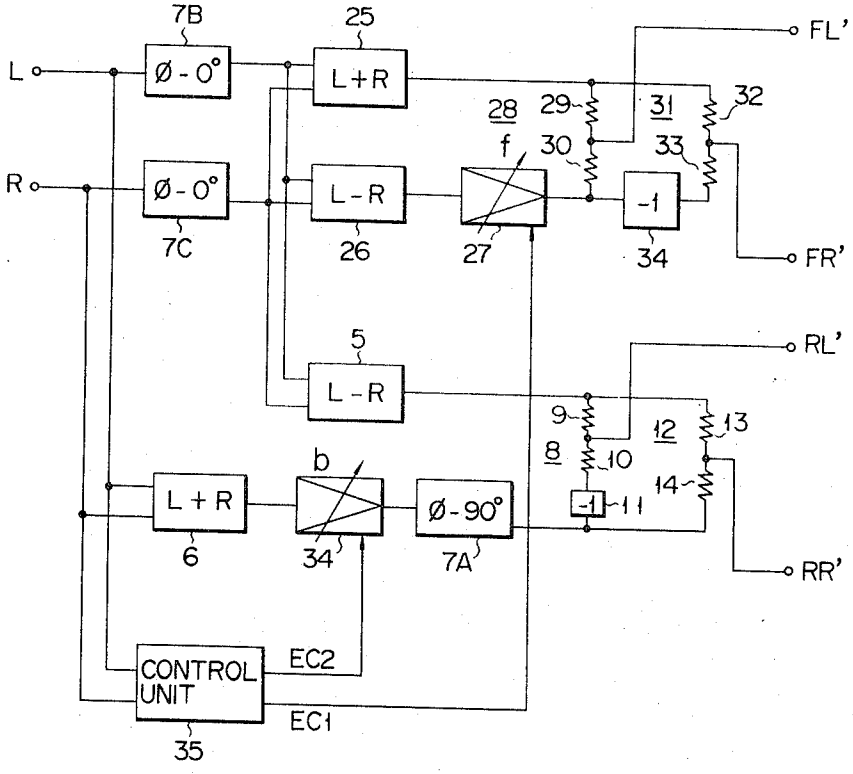

7B
25
L
Ø - 0°
L+R
FL'
28
29
31
32
f
30
33
R
Ø - 0°
L - R
-1
7C
26
27
34
FR'
5
RL'
L - R
9
12
13
8
10
b
14
L + R
Ø - 90°
-1
11
6
34
7A
RR'
CONTROL UNIT
EC2
EC1
35

FIG. 11

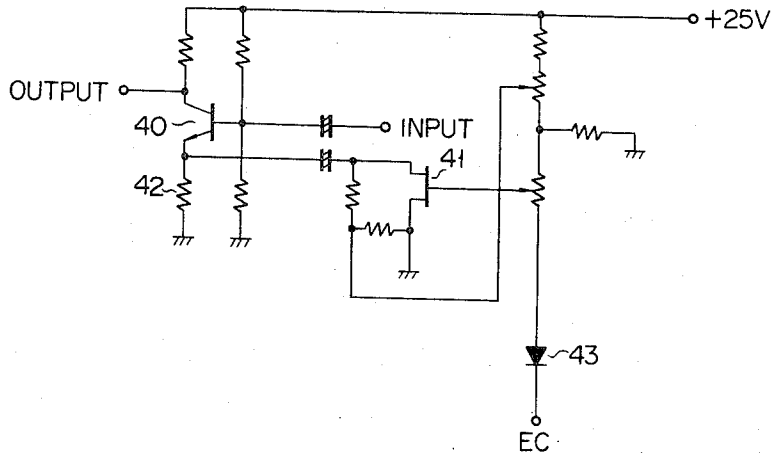
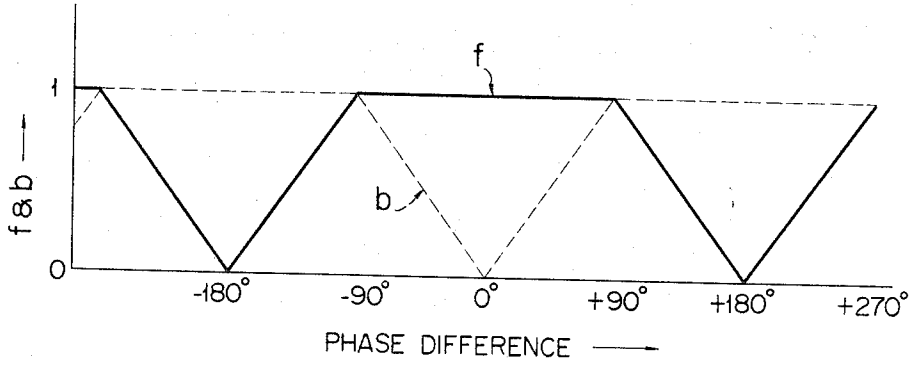

+25V
OUTPUT
40
INPUT
41
42
43
EC

FIG. 12


f
1
f & b
b
0
-180°
-90°
0°
+90°
+180°
+270°
PHASE DIFFERENCE

# DECODER FOR USE IN MATRIX FOUR-CHANNEL SYSTEM

This invention relates to a decoder suitable for use in a matrix four-channel system wherein four-channel original signals are encoded into two-channel signals and the two-channel signals are decoded into four-channel signals closely resembling the original signals.

In recent years, various types of matrix four-channel reproducing systems have been developed wherein four-channel original signals are convertd into two-channel signals, the two-channel signals are sent to a decoder through a transmission medium such as a stereo disc, a magnetic tape or an FM stereo broadcasting system to be converted into four-channel signals which are closely resembling the original signals and the decoded four-channel signals are supplied to four loudspeakers arranged about a listener. A typical example is known as the "CBS SQ system."

However, as the decoder used in the conventional SQ system requires four expensive phase shifters the construction of the decoder is complicated and expensive.

In the SQ system, while the separations between the front channels and between the rear channels are complete, the separation between the front and rear channels is poor. Especially, the poor separation between rear and front channels for the signals to be located at the front center or rear center presents a serious problem.

It is an object of this invention to provide an improved decoder of a simple and inexpensive construction which requires to use at most three phase shifters.

Another object of this invention is to provide a decoder especially suitable for use in the SQ system which can improve the separation between the front and rear channels by adding additional means to the above described type of a decoder for use in the SQ system.

According to one aspect of the invention there is provided a decoder for decoding a first channel signal normally containing one front signal and two rear signals having a phase difference of 90°, and a second channel signal normally containing another front signal and said two rear signals having a phase difference of 90° to produce reproduced four-channel signals which are to be supplied to two front loudspeakers and two rear loudspeakers which are disposed about a listener, said decoder comprising: a first matrix circuit connected to receive said first and second channel signals for forming a difference signal between said first and second channel signals; a second matrix circuit connected to receive said first and second channel signals for forming a sum signal of said first and second channel signals; a third matrix circuit connected to receive the output signals of said first and second matrix circuits for forming an output signal to be supplied to one of said rear loudspeakers; a fourth matrix circuit connected to receive the output signals from said first and second matrix circuits for forming an output signal to be supplied to the other of said rear loudspeakers; at least one phase shifter connected between said first and second matrix circuits and said third and fourth matrix circuits for providing a phase difference of about 90° between the outputs from said first and second matrix circuits; first and second coupling means for coupling said first and second channel signals to respective ones of said two front loudspeakers; and third and fourth coupling means for coupling the outputs from said third and fourth matrix circuits to respective ones of said two rear loudspeakers.



The present invention can be more fully understood from the following detailed description when taken in connection with reference to the accompanying drawings, in which:

FIG. 1 is a connection diagram showing a basic construction of a decoder embodying the invention;

FIGS. 2A and 2B show vector diagrams of two-channel signals utilized in a matrix four-channel system to which the invention is suitable;

FIGS. 3A to 3D show vector diagrams of the four-channel reproduced signals produced by a conventional decoder;

FIGS. 4A to 4D show vector diagrams of the reproduced four-channel signals produced by a decoder;

FIG. 5 is a connection diagram of the most ideal decoder embodying the invention;

FIG. 6 shows a modification of the circuit shown in FIG. 5;

FIG. 7 shows a connection diagram of a phase shifter;

FIG. 8 is a graph showing the phase shift characteristic of the phase shifter shown in FIG. 7;

FIG. 9 is a graph showing the separation characteristic between the rear signals obtained by using the phase shifter shown in FIG. 7 in the decoder shown in FIG. 1;

FIG. 10 shows a block diagram of a modified decoder capable of improving the separation between the front and rear channels;

FIG. 11 shows one example of the variable gain amplifiers shown in FIG. 10; and

FIG. 12 shows the relationship between the amplification factors of the variable gain amplifiers shown in FIG. 10 and the phase difference between two-channel signals.

Referring now to FIG. 1 of the accompanying drawings which shows the basic construction of an SQ decoder embodying the invention, two front loudspeakers SFL and SFR and two rear loudspeakers SRL and SRR are disposed to surround a listener 1 in a listening room 2, in a manner well known in the conventional four-channel reproducing systems. A first channel signal or left signal L and a second channel signal or right signal R which are in a stereophonic relationship are produced from an SQ matrix four-channel medium such as a stereo phonograph record, a magnetic tape of an FM stereo receiver. The left signal L is applied to the loudspeaker SFL through a power amplifier 3 as a front-left signal FL′ while the right signal R is applied to the loudspeaker SFR through a power amplifier 4 as a front-right signal FR′. Further, the left and right signals L and R are applied to a first matrix circuit 5 which produces a difference signal (L − R) and to a second matrix circuit 6 which produces a sum signal (L + R). The sum signal (L + R) is passed through a − 90° phase shifter 7 to produce a signal whose phase is lagged 90° with reference to the difference signal (L − R). The difference signal (L − R) and the phase shifted sum signal (L + R) are applied across a third matrix circuit or subtracter circuit 8 comprising resistors 9 and 10 having equal value and an inverter 11 which are connected in series and a fourth matrix circuit or adder circuit 12 comprising serially connected resistors 13 and 14 of equal value. A rear-left signal RL′ is derived out from the junction between resistors 9 and 10 of the third matrix circuit 8 and this signal is applied to the loud-

speaker SRL via a power amplifier **15**, whereas a rear-right signal RR′ derived out from the junction between resistors **13** and **14** of the fourth matrix circuit **12** is applied to the loudspeaker SRR via a power amplifier **16**.

The purpose of phase shifter **7** is to establish a 90° difference between the difference signal (L − R) and sum signal (L + R). Instead of inserting the −90° phase shifter **7** in the circuit of the sum signal (L + R), it is also possible to insert a +90° phase shifter in the circuit of the difference signal (L − R). The phase shifter **7** may be a +90° phase shifter, in which case the inverter **11** is to be connected in the fourth matrix circuit **12**. Alternatively, a −90° phase shifter may be connected in the circuit of the difference signal (L − R) in which case too, the inverter **11** is included in the fourth matrix circuit **12**. It should be understood that phase shifter **7** is designed to give a definite phase difference between input and output signals thereof over the entire audio frequency range.

The SQ decoder shown in FIG. **1** operates as follows. The left and right signals L and R produced from an SQ matrix four-channel medium are expressed, respectively, by the following equations:

$$L=FL + 0.7RR + 0.7RL \angle -90°$$

$$R = FR + 0.7RR \angle +90° - 0.7RL$$

where FL, FR, RL and RR represent the four-channel original signals. The vector diagrams of the signals L and R are shown in FIGS. **2A** and **2B**, respectively.

Four-channel signals reproduced from a conventional SQ decoder are expressed by the following equations:

$$FL1 = LF + 0.7RR + 0.7RL \angle -90°$$

$$FR1 = FR + 0.7RR \angle +90° - 0.7RL$$

$$RL1 = RL + 0.7FL \angle +90° - 0.7FR$$

$$RR1 + RR + 0.7FL + 0.7FR \angle -90°$$

The vector diagrams of these reproduced four-channel signals are shown in FIGS. **3A** to **3D** repsectively.

The reproduced four-channel signals FL′, FR′, RL′ and RR′ produced by the SQ decoder shown in FIG. **1** are expressed by the following equations:

$$FL' = FL + 0.7RR - j0.7RL$$

$$FR' = FR + j0.7RR - 0.7RL$$

$$RL' = 1/2[L - R + j(L + R)] = 1/2[L + jR - (R - jL)] = 1/2[-j1.4RL + FL + jFR - (-1.4RL - jFL + FR)] = 1/2(2RL \angle -45° + 1.4FL \angle +45° + 1.4RR\angle +135°) = RL \angle -45° + 0.7FL \angle +45° + 0.7FR \angle +135°$$

$$RR' = 1/2[L - R - j(L + R)] = 1/2[(L - jR - (R + jL)] = 1/2[1.4RR + FL - jFR - (j1.4RR + jFL + FR)] = 1/2(2RR\angle -45° + 1.4FL \angle -45° + 1.4FR\angle -135°) = RR\angle -45° + 0.7FL\angle -45° + 0.7FR\angle -135°$$

The vector diagrams of these reproduced four channel signals are shown in FIGS. **4A** to **4D**, respectively. It can be noted that the vector diagrams of the reproduced front signals FL′ and FR′ are the same as those of signals FL1 and FR1 shown in FIGS. **3A** and **3B**. As will be seen from the vector diagrams of the reproduced rear signals RL′ and RR′ shown in FIGS. **4C** and **4D**, the original signals RL and RR contained therein are in phase with each other, although being lagged by −45° in phase with respect to the original signals FL and FR contained in the reproduced front signals FL′ and FR′ shown in FIGS. **4A** and **4B**. Yet the separation between the reproduced front signals FL′ and FR′ with respect to the original front signals FL and FR and the separation between reproduced rear signals RL′ and RR′ with respect to the original rear signals RL and RR are perfect as in the conventional decoder.

Although above description is based on the assumption that the phase shifter **7** shown in FIG. **1** gives phase shifts of a definite amount to the input signals over the entire audio frequency range, in practice, this is not possible with a single phase shifter.

For this reason, in order to preserve the desirable phase characteristics of the SQ system over the entire audio frequency range it is advantageous to use an SQ decoder as shown in FIG. **5** in which circuit elements corresponding to those shown in FIG. **1** are designated by the same reference characters. In the decoder shown in FIG. **5**, the output signals from phase shifters **7B** and **7C** which are connected to receive the left and right signals L and R respectively are utilized as the front signals FL′ and FR′ respectively and supplied to first matrix circuit **5**. The second matrix circuit **6** is arranged to receive directly the left and right signals L and R.

$\phi - 0°$ phase shifters **7B** and **7C** have the same frequency-phase shift characteristic, the amount of phase shift $\phi$ varying with frequency. A $\phi - 90°$ phase shifter **7A** having a −90° lagging phase characteristic with respect to the phase shifters **7B** and **7C** over the entire audio frequency range is connected with the output side of the second matrix circuit **6**. Thus, it will be clear that there is a 90° phase difference between the output $(L - R)\angle\phi$ of the first matrix circuit **5** and the output $(L + R)\angle\phi - 90°$ of the phase shifter **7A** over the entire audio frequency range. Accordingly, in the decoder shown in FIG. **5**, it is possible to perform the same function as the conventional decoder by utilizing three phase shifters **7A**, **7B** and **7C**. In this case, since it is necessary for one phase shifter to have several stages of phase shifters, each as shown in FIG. **7**, possibility of elimination of one phase shifter provides a very economical advantage.

FIG. **6** shows a modification of the decoder shown in FIG. **5** wherein instead of using phase shifters **7B** and **7C** in FIG. **5**, a single $\phi - 0°$ phase shifter **7D** having the same phase shift characteristic is connected to the output side of the first matrix circuit **5**, whereby a 90° phase shift is provided between the difference signal (L − R) and sum signal (L + R) over the entire audio frequency range, thus obtaining a perfect separation between the rear signals RL′ and RR′. Although, with the decoder shown in FIG. **6** there occur phase differences which vary dependent upon frequencies between the reproduced front signals FL′ and FR′ and the reproduced rear signals RL′ and RR′, such phase differences do not cause any practical trouble.

The phase shifter **7** utilized in the decoder shown in FIG. **1** may be substituted by a phase shifter shown in FIG. **7** and having a phase shift characteristic as shown in FIG. **8**. The phase shifter shown in FIG. **7** comprises a transistor **20** with its collector-emitter path connected across a source of supply indicated by B+ and the ground. Across the collector-emitter path there is connected a series circuit including a capacitor **21** and resistor **22**. The base electrode of transistor **20** is connected to receive an input signal, i.e., the sum signal (L + R) in this case, and the phase shifted sum signal is taken out from the junction between the capacitor **21** and resistor **22**. Various circuit elements of the phase shifter shown in FIG. **7** are selected such that the phase

angle of the output signal is shifted by −90° with respect to the input signal at a predetermined frequency $f_0$, for example at 1 KHz, in the audio frequency band. Consequently, at the frequency $f_0$, a 90° phase difference is given between the sum signal (L + R) and the difference signal (L − R), and thus the separation between the rear signals RL′ and RR′ will be infinitively large at the frequency $f_0$ as shown in FIG. 9. With an SQ decoder comprising only one phase shifter shown in FIG. 7, the separation between the reproduced rear signals RL′ and RR′ in a frequency band separated from the predetermined frequency $f_0$ is poor as shown in FIG. 9. Such poor separation, however, does not cause any substantial trouble.

In the SQ system, both the separations between front signals FL′ and FR′ and between rear signals RL′ and RR′ are infinity as shown by the above described equations regarding reproduced four-channel signals, but the separation between the front and rear channels is poor. Especially, the cross talk between the front and rear channels with reference to the front-center signal (in the case of FL=FR) or to the rear-center signal (in the case of RL=RR) presents a problem.

A decoder is shown in FIG. 10 which can improve the separation between front and rear channels of the SQ decoder shown in FIG. 5 which is the most ideal one to this invention. The circuit elements corresponding to those shown in FIG. 5 are designated by the same reference characters. In the circuit shown in FIG. 10, there are added a fifth matrix circuit 25 and a sixth matrix circuit 26 which produce the sum signal (L + R) and the difference signal (L − R), respectively in response to the left and right signals L and R which are supplied to the matrix circuits 25 and 26 through phase shifters 7B and 7C respectively. Further, a first variable gain amplifier 27 is connected to the output of the sixth matrix circuit 26. The outputs from the fifth matrix circuit 25 and amplifier 21 are applied across a seventh matrix circuit or adder 28 including serially connected resistors 29 and 30 of the equal value and across an eighth matrix circuit or subtracter 31 including resistors 32 and 33 of equal value and an inverter 34 which are connected in series. Output signals FL′ and FR′ are derived out respectively from the junction between resistors 29 and 30 of the seventh matrix circuit 28 and the junction between resistors 32 and 33 of the eighth matrix circuit 31. Further, a second variable gain amplifier 34 is connected between the second matrix circuit 6 and the phase shifter 7A. There is also provided a control unit 35 for detecting the phase relationship between the left and right signals L and R to form first and second control output sgnals EC1 and EC2. The first control signal EC1 is applied to the first variable gain amplifier 27 to control the amplification factor $f$ thereof, whereas the second control signal EC2 is applied to the second variable gain amplfier 34 to control the amplification factor $b$ thereof. It will be clear that where the first and second variable gain amplifiers 27 and 34 and the control unit 35 are eliminated, the decoder shown in FIG. 10 operates identically with that shown in FIG. 5.

As above described, the purpose of the control unit 35 is to detect the phase relationship between the left and right signals L and R and may comprise a phase discriminator which detects the phase difference between the left and right signals L and R or a level comparator which detects the phase relationship between the left and right signals in accordance with the difference in the levels of the sum and difference signals of the two signals. As such a phase discriminator or level comparator may be used the ones disclosed in the copending U.S. Pat. application Ser. No. 298,933, filed Oct. 19, 1972, entitled "Decoder for use in 4-2-4 playback system."

As shown in FIG. 12, the amplification factor $f$ of the first variable gain amplifier 27 is set to be unity when the phase difference between the left and right signals L and R is in a range of from −90° to +90°, whereas the amplification factor $b$ of the second variable gain amplifier is set to be in a range of from 0 to unity. Thus, for example, the case wherein the phase difference is zero corresponds to a condition where the left and right signals L and R contain only the front-center signals (FL=FR). In such a case, the amplification factor $b$ of the second variable gain amplifier 34 is set to be nearly equal to zero so as to substantially block the output signals from the second matrix circuit 6. The relationship between the levels of the sum and difference signals under this condition is expressed by $|L+R| > |L-R|$.

When the phase difference between the left and right signals L and R is in a range of from +90° to +270° the amplification factor $b$ of the second variable gain amplifier 34 is set to be unity whereas that $f$ of the first variable amplifier 27 is set to be in the range of from zero to unity. Thus, a case where the phase difference is +180° corresponds to a case wherein the left and right signals L and R contain only the rear-center signals (RL=RR). Under these conditions, the amplification factor $f$ of the first variable gain amplifier 27 is set to be substantially zero so as to block output signals from the sixth matrix circuit 26. The relationship between the levels of the sum and difference signals under this condition is expressed by an equation $|L+R| < |L-R|$.

The construction of the first and second variable gain amplifiers 27 and 34 will be described briefly with reference to the connection diagram shown in FIG. 11. Since both amplifiers have the same construction only one of them is described. The illustrated amplifier comprises a transistor 40, and a field effect transistor 41 acting as a variable resistor connected across an emitter resistor 42. Upon the gate electrode of the field effect transistor 41 is impressed a predetermined bias voltage (for example +13 volts) from a bias circuit so as to set the amplification factor of transistor 40 to be unity. A diode 43, poled as shown, is connected between the gate electrode of the field effect transistor 41 and the output terminal of the control unit which produces the control output EC. The control unit 35 is constructed such that it produces the control signals EC1 and EC2 of the same voltage (+13 volts for example) when the phase difference between the input signals L and R equals 90°. For this reason, under these conditions, the control signal EC from the control unit balances with the gate voltage of the field effect transistor 41 to maintain the amplification factor of the transistor 40 at unity. When the phase difference between the input signals L and R is in a range of from −90° to +90° the control signal EC1 varies greatly in the positive direction from +13 volts, but such a voltage variation is blocked by the diode 43 from being transmitted to the gate electrode of the field effect transistor 41. Accordingly, the amplification factor of transistor 40

will not be varied. On the other hand, the control signal EC2 from the control unit **35** varies greatly in the negative direction from +13 volts and this voltage variation in the negative direction is transmitted to the gate electrode of the field effect transistor **41** through the diode **43**. This decreases the bias voltage to the gate electrode below +13 volts, thus decreasing the amplification factor of transistor **40** below unity. Thus, it will be understood that the amplification factors *f* and *b* of the first and second variable gain amplifiers **27** and **34** vary as shown in FIG. **12**.

The decoder shown in FIG. **10** operates as follows: Where the phase difference between the left and right signals L and R is zero degree, that is, where only the front-center signals, for example, are present, the amplification factors *f* and *b* of the first and second variable gain amplifiers **27** and **34** are set to be unity and zero, respectively. As a result, signals L and R are utilized as the reproduced front signals FL′ and FR′. On the other hand, as the output (L − R) from the first matrix circuit **5** is substantailly zero and the output (L + R) from the second matrix circuit **6** is essentially blocked by the second variable gain amplifier **34** (in this case b=**0**), the reproduced rear signals RL′ and RR′ are substantially zero. In other words, the separation between the front and rear channels is essentially infinity for the front-center signal.

Where the phase difference between the left and right signals L and R is equal to 180°, that is, where only the rear-center signals are present, the amplification factors *f* and *b* of the first and second variable gain amplifiers **27** and **34** are equal to **0** and unity respectively. For this reason, the output (L + R) from the fifth matrix circuit is essentially zero and the output (L − R) from the sixth matrix circuit **26** is blocked by the amplifier **27** whose amplification factor *f* has been set to zero so that the reproduced front signals FL′ and FR′ are substantially zero. On the other hand, signals RL<−45° and RR<−45° are derived out as the reproduced rear signals RL′ and RR′. Thus, the separation between the front and rear channels for the rear-center signal is substantially infinite.

It will be clear that control means similar to that shown in FIG. **10** can be provided for the decoders shown in FIGS. **1** and **6**.

What is claimed is:

**1.** A decoder for decoding a first channel signal normally containing one front signal and two rear signals having a phase difference of 90°, and a second channel signal normally containing another front signal and said two rear signals having a phase difference of 90° to produce reproduced four-channel signals which are to be supplied to two front loudspeakers and two rear loudspeakers which are disposed about a listener, said decoder comprising:

a first matrix circuit connected to receive said first and second channel signals for forming a difference signal between said first and second channel signals;

a second matrix circuit connected to receive said first and second channel signals for forming a sum signal of said first and second channel signals;

a third matrix circuit connected to receive the output signals of said first and second matrix circuits for additively combining said output signal to form an output signal to be supplied to one of said rear loudspeakers;

a fourth matrix circuit connected to receive the output signals from said first and second matrix circuits for subtractively combining said output signals to form an output signal to be supplied to the other of said rear loud-speakers;

at least one phase shifter connected between said first and second matrix circuits and said third and fourth matrix circuits for providing a phase difference of about 90° between the outputs from said first and second matrix circuits;

first and second coupling means for coupling said first and second channel signals to respective ones of said two front loudspeakers; and

third and fourth coupling means for coupling the outputs from said third and fourth matrix circuits to respective ones of said two rear loudspeakers.

**2.** The decoder according to claim **1** which further comprises a second phase shifter for coupling said first channel signal to said first matrix circuit and said first coupling means; and a third phase shifter for coupling said second channel signal to said first matrix circuit and to said second coupling means, said second and third phase shifters having the same phase shift characteristic over the entire audio frequency range and said first phase shifter having a phase shift characteristic which is different by about 90° from those of said second and third phase shifters over the entire audio frequency range.

**3.** The decoder according to claim **1** wherein first and second phase shifters are connected between said first and second matrix circuits and said third and fourth matrix circuits, said first phase shifter is connected to receive the output from said first matrix circuit, said second phase shifter is connected to receive the output from said second matrix circuit and said first and second phase shifters have phase shift characteristics of about 90° difference over the entire audio frequency range.

**4.** The decoder according to claim **1** wherein said phase shifter has a phase shift characteristic such that it provides a 90° phase difference between the input and output signals at a given frequency in the entire audio frequency range.

**5.** The decoder according to claim **4** wherein said phase shifter comprises a transistor including a base electrode, a collector electrode and an emitter electrode, and a series circuit connected across the collector and emitter electrodes of said transistor, said series circuit incluidng a capacitor and resistor, and wherein the base electrode of said transistor is connected to receive said input signal and said output signal is taken out from the junction between said capacitor and said resistor of said series circuit.

**6.** The decoder according to claim **1** which further comprises a fifth matrix circuit connected to receive said first and second channel signals for forming a sum signal of said first and second channel signals; a sixth matrix circuit connected to receive said first and second channel signals for forming a difference signal of said first and second channel signals; a seventh matrix circuit connected to receive the output signals from said fifth and sixth matrix circuits for forming a signal to be supplied to said first coupling means; an eighth matrix circuit connected to receive the output signals from said fifth and sixth matrix circuits for forming a signal to be supplied to said second coupling means; a control unit for detecting the phase relationship be-

tween said first and second channel signals to form first and second control signals; a first variable gain amplifier connected to the output side of said sixth matrix circuit to vary the amplification factor thereof in response to said first control signal from said control unit; and a second variable gain amplifier connected to the output side of said second matrix circuit to vary the amplification factor thereof in response to said second control signal from said control unit.

**7.** The decoder according to claim **6** wherein said first variable gain amplifier includes means responsive to said first control signal from said control unit for setting the amplification factor of said first variable gain amplifier to be substantially unity when said first and second channel signals are in phase, and to be substantially zero when said first and second signals have opposite phases, and said second variable gain amplifier includes means responsive to said second control signal from said control unit for setting the amplification factor of said second variable gain amplifier to be substantially zero when said first and second channel signals are in phase, and to be substantially unity when said first and second channel signals have opposite phases.

**8.** The decoder according to claim **1** wherein one of said third and fourth matrix circuits is an adder and the other is a subtracter.

**9.** The decoder according to claim **8** wherein said adder includes two equally valued resistors and said subtracter includes a series connection of an inverter and two equally valued resistors.

**10.** The decoder according to claim **6** wherein said seventh matrix circuit is an adder, and said eighth matrix circuit is a subtracter.

**11.** The decoder according to claim **10** wherein said adder includes a series connection of two equally valued resistors, and said subtracter includes a series connection of an inverter and two equally valued resistors.

**12.** A signal converting apparatus for converting two channel signals into four channel output signals which are coupled to four loudspeakers disposed around a listener, said apparatus comprising:

first means for producing a sum signal of said two channel signals;

second means for producing a difference signal of said two channel signals;

third means for additively combining only said sum and difference signals to produce a first output signal;

fourth means for subtractively combining only said sum and difference signals to produce a second output signal;

fifth means for additively combining only said sum and difference signals to produce a third output signal;

sixth means for subtractively combining only said sum and difference signals to produce a fourth output signal; and

seventh means for introducing a predetermined phase difference between said sum and difference signals which are supplied to said fifth and sixth means.

**13.** The signal converting apparatus according to claim **12** wherein said predetermined phase difference is about 90°.

**14.** The signal converting apparatus according to claim **12** further comprising:

eighth means for detecting phase relationship between said two channel signals to produce first and second control signals;

ninth means responsive to said first control signal from said eighth means for varying the level of said difference signal which is supplied to said third and fourth means; and

tenth means responsive to said second control signal from said eighth means for varying the level of said sum signal which is supplied to said fifth and sixth means.

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