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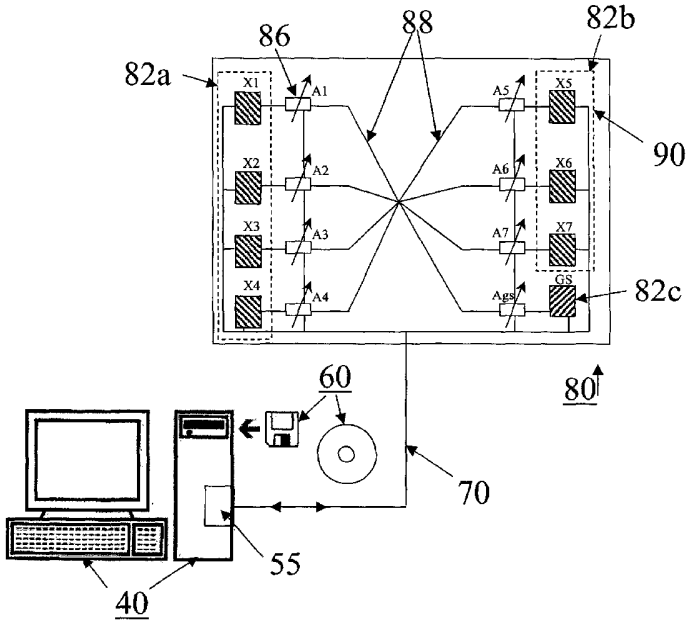
(54) Title: RF CHIP TESTING METHOD AND SYSTEM



(57) Abstract: A method and system for testing RF chips for radio specification compliance is described. The system comprises a test board (80) having a plurality of interconnected sockets (82a,b,c) for receiving chips to be tested. In testing, signals generated by transmitter circuitry (20) within a group of test chips are used to test the receiver (30) functionality of the other chips loaded in the system. Hence, for tests requiring several analogue radio signals, a plurality of chips are tested at the same time using signals generated from other chips. Additionally, the system does not require expensive dedicated RF analogue signal generating equipment.

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DESCRIPTION

RF CHIP TESTING METHOD AND SYSTEM

The present invention relates to radio frequency (RF) testing methods and further relates to a testing system suitable for practising such methods. The present invention has particular, but not exclusive, application in the testing of the RF functionality of integrated circuit chips and the compliance of such functionality with an intended radio standard or specification.

Radio frequency integrated circuit (IC or 'chip') manufacturing requires testing to determine whether the manufactured ICs are compliant with a radio standard (e.g. Bluetooth™, GSM™, IEEE802.15.4) and operational in other respects. Typically, a pick and place machine will place the chip device to be tested in a suitably constructed test board or 'test head' of specialised automated test equipment (ATE). The ATE applies the appropriate test signals to the device under test (DUT) and passes or rejects the device. Such individual chip testing exhibits a problem in that it is time consuming and hence adds to the overall manufacturing cost.

Another particular problem in testing the functionality of an RF chip for compliance with a radio standard exists in that the specification may require the ATE to generate several specific analogue RF signals at the same time in order to test, for example, the interference performance of the receiver of the DUT. Special signal generating hardware is therefore required, adding cost to the ATE, and therefore expense to the manufacturer. Furthermore, the application of such signals is often via long probes brought down into contact with the pin-out of the chips, requiring a specially constructed and controlled test suite. The use of such probes results in unspecified and difficult to quantify losses reducing the accuracy of any such test.

It is therefore an object of the present invention to provide an improved method and system for RF chip testing.

According to a first aspect of the present invention there is provided a method for testing a plurality of integrated circuit chips for compliance with a radio standard, each chip having transmission means and receiving means for sending and receiving RF signals, the method comprising:

- placing the chips in close proximity to one another,
- testing the transmission means of each chip with respect to a known good reference chip,
- selecting a number of the chips to form a generating group, the remaining chips forming a receiving group, and
- testing the receiving group using signals generated by the generating group.

According to a further aspect of the present invention there is provided a testing system for testing a plurality of integrated circuit chips, each chip having transmission means and receiving means for sending and receiving RF signals, the system comprising:

a computer having communication, control and data acquisition means for communicating with, controlling and acquiring data from testing means to which it is connected,

the testing means comprising a plurality of chip sockets adapted to physically accept and electronically interface with a chip placed therein, and wherein each socket is provided with signal propagation and attenuation means for sending and receiving signals to each of the other sockets under the control of the computer,

and where in operation the computer selects a group of chips to generate test signals which are propagated via the propagation means to a reception test group of chips.

The method and system of the present invention implement applicant's appreciation that many compliance tests in the RF field require a number of signals to be generated, and that the RF chips being tested may be utilised in the system to generate such signals. Hence, a system is provided in which a group of chips, having passed transmission generation tests for example, are

utilised to generate the signals required to test the reception hardware of the other chips.

Preferably, the number of chips selected corresponds to the number of signals required for the particular test. For example, in an interference test a "wanted" signal with two other "interfering signals" must be generated on certain specified channels to determine the quality of the receiver. In such an example test, three chips are therefore required to be selected for the test. If one considers the situation where there are eight chips mounted in the system, then such an interference test requires that three chips are selected (the generating group) to provide the three signals to the remaining five chips (the receiving test group). Following the test, three of the five chips just tested may be selected for the generation group and these then provide the signals to the previous generating group. Hence, such an interference test only requires two "passes" to test all eight chips, and no extra signal generating hardware. This compared with eight individual tests required in a conventional system which in addition requires signal generating hardware to generate the three signals for the above example test, and individual probing (which has the disadvantage of including unknown losses due to such probing).

Advantageously, each chip's signal may be attenuated via programmable attenuators before being provided to the test group of chips. This allows for imbalance in transmission and reception power required for a test. For example the Bluetooth specification requires a transmission power of 0dBm whilst the chips receiving hardware requires a signal of the order of -70dBm, therefore the signals generated by the group of chips require 70dB attenuation.

In a preferred embodiment, the computer is a standard PC with a digital data acquisition card to interface it to the test board. The control and test routines and analysis of data captured by the card are provided in software. Hence this digital test equipment is relatively inexpensive and flexible enabling different tests for different radio specifications to be installed or downloaded as required by the customer.

The present invention will now be described, by way of example only, and with reference to the accompanying drawings wherein:

Figure 1 is a block diagram of the circuitry of an RF chip being a device under test (DUT);

Figure 2 is a schematic diagram of a system for testing a chip as shown in Fig. 1;

Figure 3 is flow diagram representing example steps of a method embodying the invention;

Figure 4 is another flow diagram representing example steps of a method embodying the invention in which intermodulation and other receiver tests are performed.

It should be noted that the Figures are diagrammatic and not drawn to scale. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to corresponding or similar features in modified and different embodiments.

Figure 1 shows a typical transceiver architecture for an RF chip. This architecture comprises a baseband section 10 connected with a transmission chain 20 comprising a digital to analog converter (DAC) for converting the intended digital signal to an analogue signal, a mixing stage where the signal is mixed with the output of a frequency synthesiser block 22 and a power amplifier for amplifying the resulting signal. A receiving chain 30 comprises an antenna filter, a low noise amplifier, a mixing stage, channel filtering and demodulating stage. Such a general transceiver having transmission and reception means for generating and transmitting/receiving signals is well known to those skilled in the art. In an application, for example a mobile phone or personal digital assistant (PDA), the transceiver is connected to an antenna for radiating or receiving radiated signals. In a testing environment, prior to incorporation in a final product such as a mobile phone, the transceiver (Tx) 20 and receiver (Rx) 30 blocks are connected to relevant pins of the chip

(if packaged) or a pad/probe applied to the appropriate test location on the silicon die containing the transceiver circuitry (if testing is prior to packaging).

An integrated circuit for producing for example, Bluetooth signals may do so via such an architecture as shown in Fig. 1, together with a layered protocol. The Bluetooth protocol or specification as laid out in the Bluetooth specification v1.1 requires the radio performance of such a chip to meet certain test requirements. Pages 20-32 of the aforementioned specification, which are incorporated herein for reference and to which the reader is now directed, specify among others the following tests: output power and power control of the transmitter, sensitivity, interference performance, intermodulation characteristic and receiver signal strength indicator.

It is to be noted that several of these tests require a number of signals to be generated at the same time. In particular, characterisation of the receiver for interference performance involves co-channel and adjacent channel tests which each require two transmission signals to be generated. The characterisation and testing of the intermodulation characteristics of the receiver require three signals to be generated - a wanted signal at a first frequency f_0 with a power level 6dB over the reference sensitivity level, a static sine wave signal at another frequency f_1 with a power level of -39 dBm and a bluetooth modulated signal at a further frequency f_2 with a power level of -39dBm, such that $f_0 - 2f_1 - f_2$ and $\text{mod}(f_2-f_1) = n*1$ MHz where n can be 3, 4, or 5. In general the Bit Error Rate (BER) is measured and evaluated against a predetermined level (e.g. 0.1%) to provide a pass/fail for these tests.

Figure 2 is a diagram of a digital testing system embodying the present invention. The system comprises a computer in the form of a PC 40 having a display and a digital acquisition card (DAQ) 55, a suitable example being National Instruments™ PCI 7030/6030E. Testing routines, control and analysis software are provided with the computer on suitable media 60, or may be downloaded over a suitable internet link (not shown). The computer and DAQ are connected to a test board or "test head" 80 via a SCSI link 70 although other suitable interface links 70 may be used (IEEE1394 'Firewire', and USB being common examples).

The board 80 comprises in this embodiment eight chip sockets 82a,b,c (labelled X1,X2 to X7, and GS in the diagram) for accepting radio chips for testing. Each socket interfaces electronically (via techniques well known in the art such as tensioned pins or solderbump pads) with the chip mounted therein. Suitably designed tracks 88 with programmable attenuators 86 (A1 to A7, Ags) for interconnecting and propagating signals from one chip socket to another are provided. Control and input/output (I/O) data is passed between the computer 40 and sockets via the test head link 70. In this embodiment the socket 82c is provided for a "golden sample" chip. This chip has been previously tested and characterised and is used as a reference with which to compare the characteristics of other chips just manufactured.

Figure 3 illustrates a flow chart example of a testing method performed by the system of Figure 2, and as implemented by software 60. In the method chips are loaded into sockets 82a,b. The golden sample socket 82c is loaded with a golden sample. In the basic method according to the invention the transmission circuitry 20 of each chip is tested (step 100) with respect to the golden sample. For example the power output of each transceiver may be measured and compared with the known golden sample power output which is within the specified Bluetooth requirements. After testing all of the loaded chips X1-X7, the computer determines (step 102) whether the result was a pass or fail for each chip and stores the result in memory. The testing then moves onto testing the receiver chain 30 of each chip for specification compliance.

In step 104 the computer selects a first group of chips (for example the chips mounted in sockets X5, X6 and X7 as denoted by the dashed box labelled 82b in Figure 2) which will form a signal generating group for generating the signals which must be received by the remaining test chips 82a in order to test the receiver circuitry 30 of those remaining chips. Under the control of the computer the receiving group of chips are each subjected to the signals generated by the first group, thereby testing the receiver circuitry 30 of those chips in parallel (step 106). In this embodiment, the transmitted signals from X5, X6 and X7 are attenuated by the programmable attenuators A5, A6,

A7 and then passed down signal propagation tracks 88 to the receiver test group 82a of X1, X2, X3 and X4. Following step 106, the generating group becomes a receiving group to enable testing of the receiver circuitry of those chips, and a new second generating group is selected ('SEL 2G' step 108) to generate the test signals. The receiving group (which acted as the first generating group previously) is subsequently tested in step 110 and the results from the tests analysed.

Hence, RF analogue signals which are required for testing the receiver functionality of a radio chip are generated "on-board" by a group of chips which themselves form part of the test. Additionally, the signals are routed to the test chips in parallel, hence saving time and effectively testing the receiver group of chips instantaneously.

Figure 4 illustrates a flowchart giving a particular example of testing requirements which are necessary for evaluating a Bluetooth™ radio chip and wherein a methodology embodying the invention is applied. In this particular example seven chips labelled X1 to X7 are to be tested with respect to a golden sample for transmission characteristics (power output and control) and receiver characteristics (intermodulation, co-channel, adjacent channel, sensitivity and Receiver Signal Strength Indicator (RSSI)), wherein:

- block 120 - IC's X_i (i=1 to 7) are loaded as is the golden sample chip, following which;
- block 122 - IC X_i transmits a signal s_i at a first frequency f1 to the golden sample chip, and attenuator A_i is programmed to reduce the power of signal s_i, after which;
- in block 124 the BER of the signal s_i as received by the golden sample is analysed and a decision is made as to whether the transmitter of X_i is either:
    - not within specification (block 126), X_i is characterised as a reject and is not included in any further tests,
    - or is within specification, the result is stored and
- in block 128, a determination is made (is i<7?) whether all chips have been tested. If there are still chips to be tested then i=i+1 and the

program flow follows path 130 back to block 122. Once all chips have been tested (i=7) then the program flow moves to the next required tests in block 132;

- Block 132 - Intermodulation tests are performed to determine receiver characteristics. X1, X3 and X3 selected to provide a wanted signal, an interfering signal and a co-channel signal respectively. A1, A2 and A3 are programmed to limit outputs;
- Block 134 - the signals are provided by X1, X2 and X3 to the remaining chips X4, X5, X6 and X7 and the results analysed for each IC as to whether it:
    - Fails - block 136 - IC is rejected as receiver not within specification
    - Or passes in which case flow moves to
- Block 138 wherein X4, X5 and X6 are selected to generate the intermodulation test signals and A4, A5 and A6 programmable attenuators are programmed to limit outputs, following which:
- Block 140, the signals are provided by X4, X5 and X6 to the remaining chips X1, X2, X3 and the results analysed for each IC as to whether it:
    - Fails - block 142 - IC is rejected as receiver not within specification
    - Or passes in which case flow moves to
- Block 144 wherein the remaining RF tests (co-channel, Adjacent channel, sensitivity and RSSI calibration are performed on those chips which have previously passed the transmitter tests (block 124) and the intermodulation receiver tests (blocks 134 and 140) after which
- those IC which have passed all tests are noted as being within test specification requirements.

In the above embodiments an example testing system and methods were described with reference to packaged Bluetooth™ radio chips.

In an alternative embodiment the sockets for accepting chips are replaced with suitably designed solder pads on which singulated die may be placed. Testing may then be executed as described previously. Hence, in this

embodiment a manufacturer is able to test integrated circuit chips in the form of singulated die before packaging, thereby enabling faster quality testing "upstream" of the packaging process.

Those skilled in the art of testing will recognise that implementing the example testing flow charts of Fig. 3 and Fig. 4 is a matter of software design for the digital testing equipment designer. The overall software control, interfacing and analysis aspects of the testing system may be routinely implemented by those skilled in the art of designing and building test heads and testing systems. Other well known features of automatic testing equipment, such as a "pick and place" machine for handling and loading/unloading chips from the test head, and the marking of chips with ink in the event of a test failure, although not mentioned in the above embodiments, will be recognised as being compatible with the above.

Furthermore, in the foregoing embodiments, the method and system aspects of the present invention were described as applied to packaged chips or singulated die IC, the IC being a Bluetooth™ compatible design. Those skilled in the art will recognise that the testing method and systems aspects of the present invention can readily be applied to other different radio chips requiring confirmation of conformity with a particular specification for which those chips are designed. Many radio chips require testing for so-called "front end linearity," with the radio specification specifying the linearity and absolute standards required. For example, radio standards such as IEEE802.15.4 ('ZigBee'), 'GSM', and the so called '3G' telephony standards require radio chips which can benefit from specification testing equipment and methods embodying the present invention.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the design, manufacture and use of RF testing systems, test heads and component parts thereof and which may be used instead of or in addition to features already described herein without departing from the spirit and scope of the present invention.

CLAIMS

1. A method for testing a plurality of integrated circuit chips for compliance with a radio standard, each chip having transmission means and receiving means for sending and receiving RF signals, the method comprising:

- placing the chips in close proximity to one another,
- testing (100) the transmission means of each chip with respect to a known good reference chip,
- selecting (104) a number of the chips to form a generating group, the remaining chips forming a receiving group, and
- testing the receiving group (106) using signals generated by the generating group.

2. A method according to claim 1, wherein the chips are mounted on a test board prior to testing.

3. A method according to claim 1 or claim 2, wherein the selection of generating and receiving groups (104, 106) is repeated (108, 110) until all chips have been tested.

4. A method according to claim 3, wherein the number of chips selected to form a generating group is determined at least in part by the testing requirements.

5. A method according to claim 4, wherein the testing requirements specify a test requiring at least two generated signals.

6. A method according to claim 4 or claim 5, wherein the testing requirements specify an intermodulation test requiring three generated signals.

7. A testing system for testing a plurality of integrated circuit chips, each chip having transmission means (10, 20) and receiving means (10, 30) for sending and receiving RF signals, the system comprising:

a computer (40) having communication, control and data acquisition means (55) for communicating with, controlling and acquiring data from testing means to which it is connected,

the testing means (80) comprising a plurality of chip sockets (82a, b, c) adapted to physically accept and electronically interface with a chip placed therein, and wherein each socket is provided with signal propagation (88) and attenuation means (86) for sending and receiving signals to each of the other sockets under the control of the computer (40),

and where in operation the computer selects a group of chips (82b) to generate test signals which are propagated via the propagation means to a reception test group of chips (82a).

8. A system according to claim 7, wherein the sockets are located on a test board 80.

9. A system according to claim 7 or claim 8, wherein the signals generated by the selected group are radio frequency signals.

10. A test board (80) comprising a plurality of chip sockets (82a, b, c) adapted to physically accept and electronically interface with a chip placed therein, and wherein each socket is provided with signal propagation (88) and attenuation means (86) for sending and receiving test signals generated by at least one chip to each of the other sockets.

11. A computer program comprising instructions for performing a method according to any of claims 1 to 4 when run on a testing computer (40).

12. A computer readable storage medium (60) having recorded thereon data representing instructions for performing a method according to any of claims 1 to 6 when said data is loaded on a testing computer (40).

5

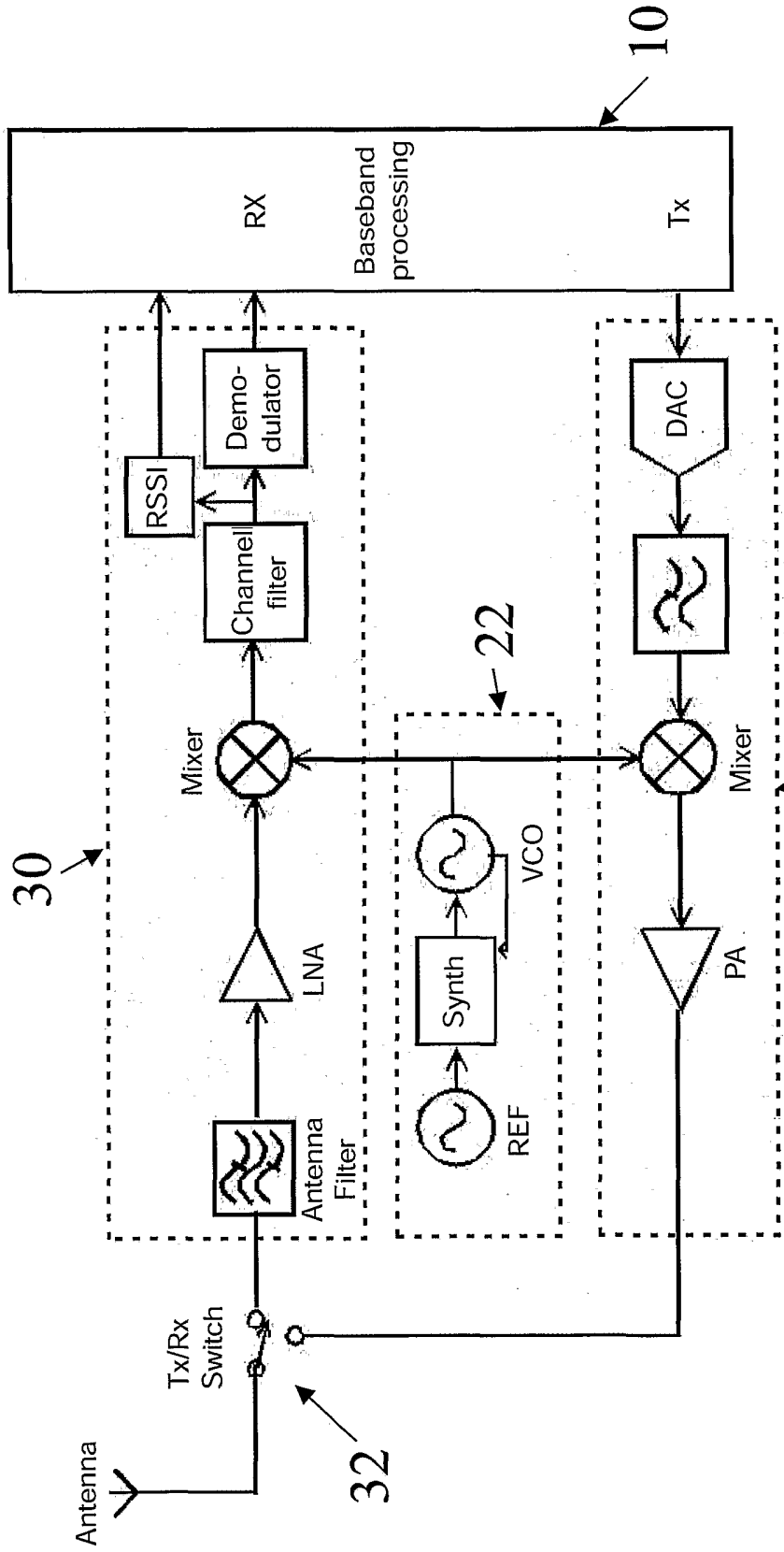
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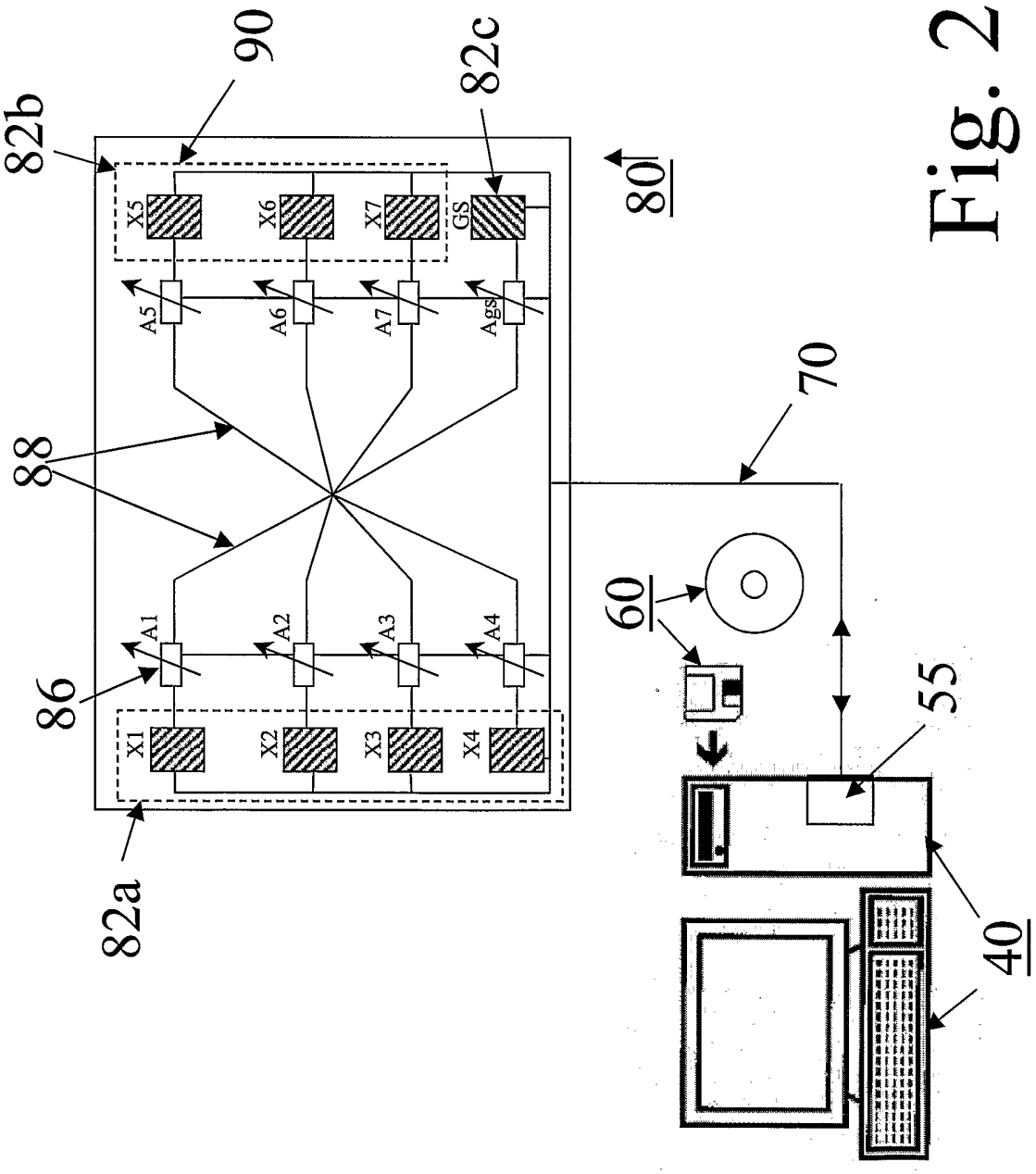
Fig. 1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82a
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Fig. 2

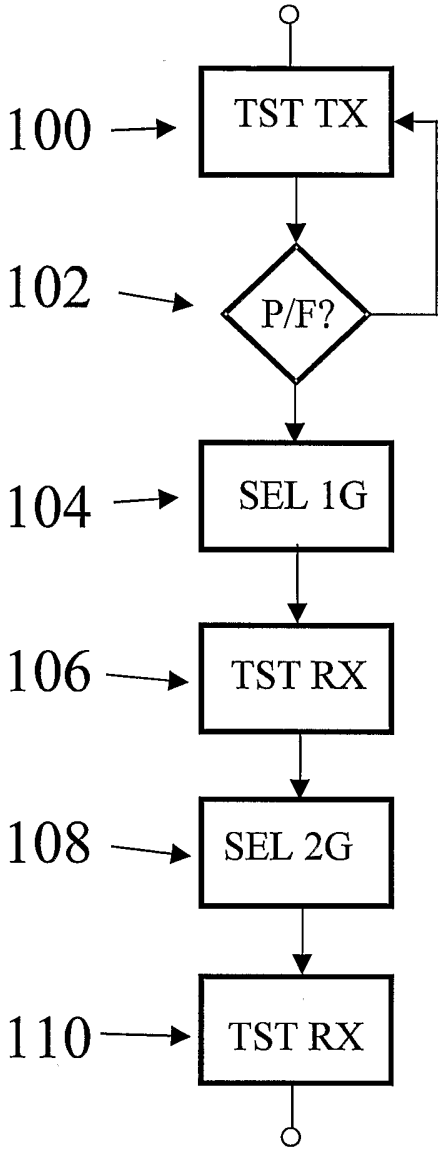
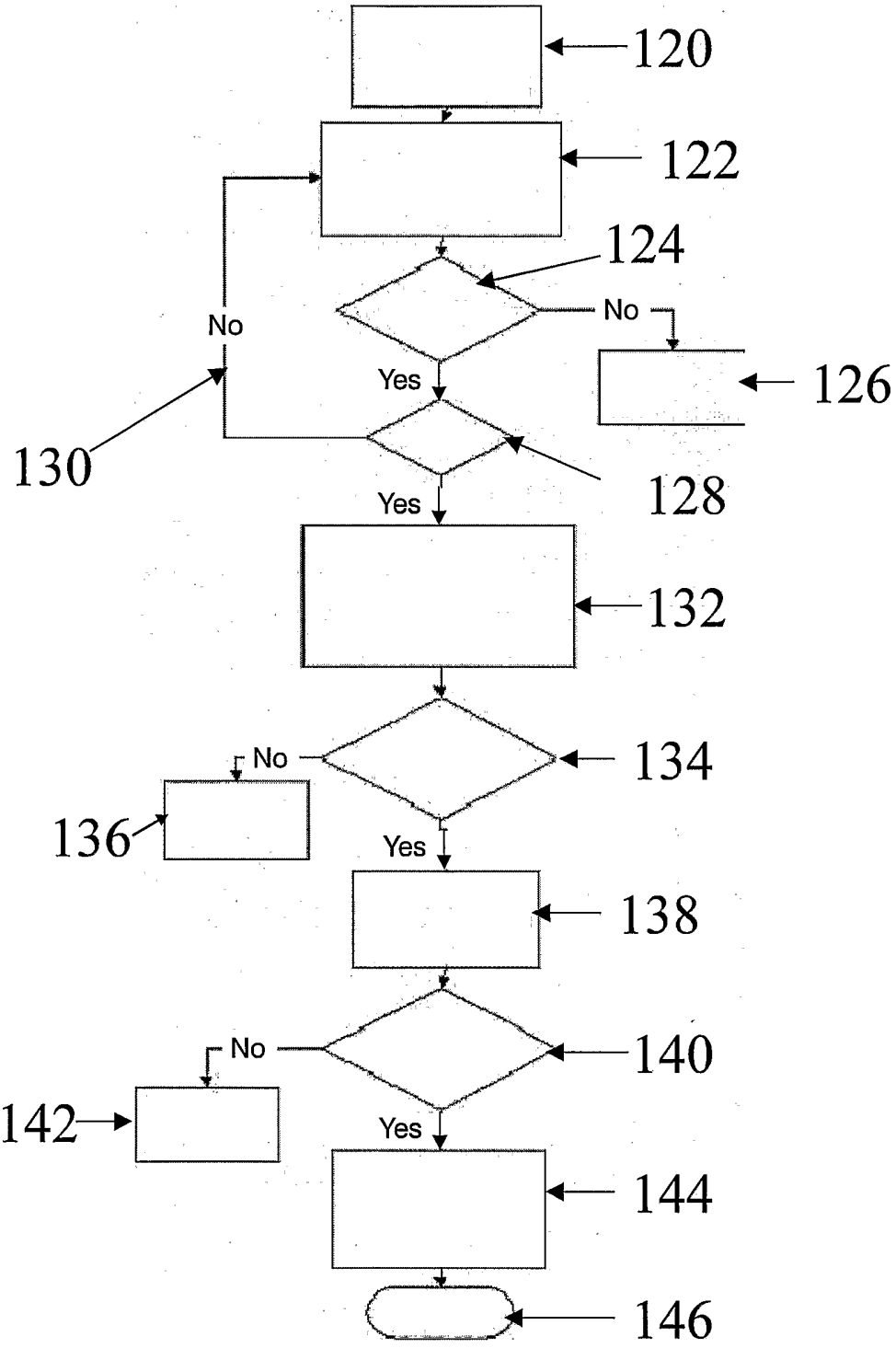


Fig. 3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No
Yes
126
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132
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134
136
Yes
138
No
140
142
Yes
144
146

Fig. 4

INTERNATIONAL SEARCH REPORT

PCT/IB 03/03987

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01R1/04 G01R31/00 H04B17/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01R H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 337 316 A (WEISS ET AL.) 9 August 1994 (1994-08-09) column 1, line 42 - column 2, line 37; figures 1-5	1,7,9
A	US 5 481 186 A (HEUTMAKER ET AL.) 2 January 1996 (1996-01-02) column 1, line 54 - column 2, line 26; figures 1,2	1,7,9
A	PATENT ABSTRACTS OF JAPAN vol. 2002, no. 11, & JP 2002 214292 A (ADVANTEST CORP), 31 July 2002 (2002-07-31) abstract	7,10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
29 January 2004	10/02/2004

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INTERNATIONAL SEARCH REPORT

PCT/IB 03/03987

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	DE 32 29 749 A (SIEMENS) 16 February 1984 (1984-02-16) abstract; figures 1-3	1,2,7-10
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