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(71) Applicant: **MOTOROLA, INC., A CORPORATION OF THE STATE OF DELAWARE** [US/US]; 1303 East Algonquin Road, Schaumburg, , IL 60196 (US).

(72) Inventors: **ARUNACHALAM, Valli,**; 9303 Rolling Oak Trail, Austin, TX 78750 (US). **VENTZEK, Peter, L. G.**; 10843 Redmond Road, Austin, TX 78739 (US). **RAUF, Shahid,**; 712 Yale Drive, Pfluggerville, TX 78660 (US). **DENNING, Dean, J.**; 12007 Pearce Lane, Del Valle, TX 78617 (US). **ZHANG, Jiming,**; 11236 South Bay, Austin, TX 78739 (US).

(74) Agents: **CHASTAIN, Lee, E.** et al.; MOTOROLA, INC., Corporate Law Department, 7700 West Parmer Lane, MD: TX32/PL02, Austin, TX 78729 (US).

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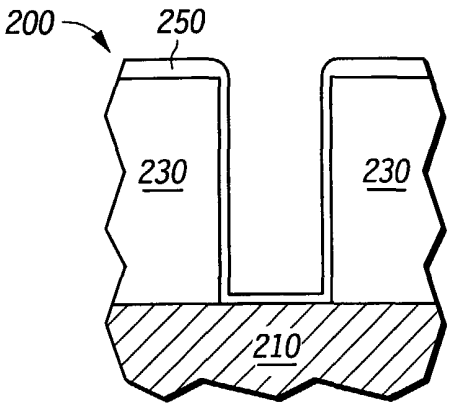
(54) Title: POST DEPOSITION SPUTTERING



(57) Abstract: A method for improving the conformality and optimizing step coverage in semiconductor features (200) such as vias (200) and trenches is described herein. By performing an additional sputtering step after at least part of the metal (250) has been deposited on a wafer feature, undesirably thick metal. deposits near the top and at the bottom of a feature (200) can be reduced. By reducing the overhang at the top of a feature (200) such as a via (200), it is easier for metal species to reach and be deposited on the sidewalls. By reducing the thickness of deposited metal at the bottom of a via (200), via (200) resistance can be decreased. The extra sputtering step may be performed a single time after all metal has been deposited. Alternatively, a small amount of metal may be deposited, a sputtering step may be performed, more metal may be deposited, and additional sputtering steps can be performed.

POST DEPOSITION SPUTTERING

Field of the Invention

The present invention relates generally to semiconductor processes, and more particularly to physical vapor deposition of metals.

Related Art

With the decreasing dimensions and increasing aspect ratios of many semiconductor features, it is becoming increasingly difficult to preserve conformality of metal films deposited inside of vias, trenches and similar features. Metal films are commonly deposited using a conventional physical vapor deposition (PVD) or ionized physical vapor deposition (IPVD) process. When depositing metals using one of these two techniques, excess metal is often deposited in certain areas of the feature, while not enough metal is deposited in other areas of the feature.

Particular problems are encountered when an excessively thick layer of metal is deposited at the bottom of features such as vias and trenches, and when too much metal is deposited at the opening of these features. For example, an excessively thick barrier layer of tantalum at the bottom of a via can result in a high via resistance, while too much metal deposited at the opening of a via can reduce the amount of metal being deposited on the walls of the via. This uneven deposition of metals is often referred to

as non-conformality, and much effort has been devoted to minimizing its effects.

For example, in order to minimize breadloafing, i.e. the accumulation of material at the opening of a via, which can prevent uniform material deposition, a technique called corner clipping is sometimes employed prior to metal deposition. Corner clipping removes material (e.g. dielectric material) from the top corners of features thereby limiting metal build up in that region that can consequently over-shadow or block access to the inside walls of the feature.

In order to reduce the thickness of the metal deposited at the bottom of features such as vias and trenches using ionized physical vapor deposition, process parameters such as wafer voltage, target voltage, coil voltage, etc. can be adjusted to increase the sputtering effect of plasma ions.

Unfortunately these measures are not completely effective, particularly in cases where a feature has a high aspect ratio and/or small dimensions. As a result, the conformality of the metal deposited on the feature is less than perfect. Therefore, what is needed is a way to improve the conformality of metal deposited on semiconductor features, and particularly, metal deposited on features having high aspect ratios and relatively small dimensions.

Brief Description of the Drawings

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIG. 1 is a basic schematic of an IPVD chamber according to one embodiment of the present invention;

FIG. 2 is a cut away view of a via demonstrating breadloafing and excess accumulation of material at the bottom of the via;

FIG. 3 is a cut away view of the same via illustrated in FIG. 2 after post deposition sputtering according to a preferred embodiment of the present invention;

FIGS. 4-7 are cut away views illustrating a via at different times during a sputtering process according to a preferred embodiment of the present invention;

FIG. 8 is a cut away view illustrating a via filled with metal according to a preferred embodiment of the present invention; and

FIG. 9 is a series of graphs illustrating the relationship between tantalum ion density, magnitude of wafer bias, and target voltage according to a preferred embodiment of the present invention.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other

elements to help improve the understanding of the embodiments of the present invention.

Detailed Description

In order to overcome at least some of the limitations of the prior art, at least one embodiment of the present invention provides a method for forming a conductive layer in a via. The method comprises the steps of providing a substrate having a conductor, forming an insulating layer over the conductor, and forming the via through the insulating layer to the conductor. The method further comprises the steps of sputter depositing a metal layer in the via selected from at least one of tantalum, titanium, tantalum nitride, titanium nitride, tungsten, and tungsten nitride, terminating the step of sputter depositing, and then partially sputter etching the metal layer at the bottom through the application of wafer bias to reduce the thickness. The purpose of optimizing the thickness of the metal layer is, according to at least one embodiment, to obtain a low via resistance and to meet reliability requirements. According to another embodiment, the sequence of metal deposition and sputtering can be repeated multiple times to achieve process objectives.

One advantage of a preferred embodiment of the present invention is that via resistance can be lowered. Other advantages of at least one embodiment of the present invention are that electromigration performance can be improved, and the occurrence of voiding during electroplating can be decreased.

Referring now to FIG.1, an IPVD (ionized physical vapor deposition) chamber according to the present invention will be discussed. IPVD chamber 100, comprises inlet 166,rotating magnet assembly 110, target 120, wafer pedestal 150, and rf coil 130. Inlet 166 is provided for introducing a sputtering agent, such as argon, helium, etc., into IPVD chamber 100. Target voltage 164 is applied to rotating magnet assembly 110, and provides a direct current (DC) bias to sputtering target 120. In one embodiment, sputtering target 120 is a tantalum target, and is used in depositing a barrier metal layer. Other target types can be used for depositing metals other than tantalum, consistent with the objects of the present invention. Exemplary other conductive materials to form such a conductive layer include titanium, tantalum nitride, titanium nitride, tungsten, and tungsten nitride.

An rf voltage 160 is applied to wafer pedestal 150 in order to bias wafer 140, which is held by wafer pedestal 150. Wafer 140 is biased in order to accelerate plasma components, such as argon 170 and tantalum 78 ions, towards wafer 140. RF voltage 162 is applied to rf coil 130 in order to generate a plasma comprising ions and neutrals released from sputtering target 120 as well as argon ions 170, excited argon atoms 171 and electrons 176. All the components of IPVD chamber 100 cooperate to deposit a metal onto the surface of the wafer 140, and into features formed therein.

In use, wafer 140 is placed on wafer pedestal 150 at the beginning of the deposition process. The wafer has features which are desired to be covered by a conductive layer. This conductive layer is preferably a metal such as tantalum, titanium, tantalum nitride, titanium nitride, tungsten, tungsten nitride, copper, copper alloys, other metal alloys, or the like. The wafer pedestal 150 is then energized with rf energy 160(thereby biasing wafer 140),and a sputtering agent, such as argon, helium, a mixture of argon and helium, or the like, is introduced into IPVD chamber 100 through inlet 166. The rf coil 130 is energized with rf energy, and sputtering target 120 is energized with DC voltage.

At this point, metal is being deposited onto wafer 140, and some sputtering is occurring simultaneously on the wafer. The net effect is there is sputtering depositing occurring. When the target voltage 164 to sputtering target 120 is switched off, this step of sputter depositing is terminated. The sputtering agent, however, sputters metal from areas of accumulation (such as at the top corners of a via and the via bottom) to other areas (such as the walls of a via). The net effect is that there is sputter depositing followed by sputter etching. In at least one embodiment, target voltage 164 is turned on again, and the metal deposition begins again.

In at least one embodiment, the target voltage 164 is switched from a predetermined negative voltage (on) to zero volts (off) at a frequency greater than 0.02 Hertz. Other embodiments

switch the target voltage 164 off only after all desired metal deposition has been completed. Note also that in at least one embodiment, the step of energizing the sputtering target 120 occurs before wafer 140 is energized.

Referring next to FIG. 2 the basic structure of a via 200 according to one embodiment of the present invention will be discussed. Via 200 is a semiconductor feature constructed to connect a conductive layer or line, such as metal line 210, to another conductive layer or line above the via (not illustrated). In order to construct via 200, dielectric 230 is deposited on top of metal line 210 using a chemical vapor deposition step. Dielectric 230 effectively isolates metal line 210 from other semiconductor features. Note that dielectric 230 may be deposited in a single step, or in a series of steps, and that dielectric 230 may comprise a single layer of a material or otherwise.

Next, the physical boundaries of via 200 are defined by photolithography and etch processes commonly employed by those skilled in the art. Frequently a sputter clean step is also performed to clean out the bottom of the via to ensure better contact with metal line 210, while at the same time knocking back the top corners of the via to limit breadloafing. Once the bottom of via 200 has been cleaned out, a barrier metal layer 250 is deposited. Barrier metal layer 250 may be formed of any suitable conductive material or combination of conductive materials, and

serves to prevent migration of a future metal layer (often copper) into the dielectric material.

FIG. 2 illustrates barrier metal layer 250 having non-optimized pre-sputtering thicknesses a and b. Pre-sputtering bottom thickness a, at the bottom of via 200, is thicker than desired. Excessive thickness at the bottom of via 200 is undesirable because it can cause unacceptably high via resistance. Pre-sputtering overhang thickness b, at the top of via 200, is sometimes referred to as breadloafing. Breadloafing is undesirable because it can overshadow the inside of via 200 and prevent proper deposition of metals on the walls of via 200.

Referring now to FIG. 3, the same via 200 illustrated in FIG. 2 is shown after post deposition sputtering has been performed according to a preferred embodiment of the present invention. Note that post deposition sputtering bottom thickness A is less than pre-sputtering bottom thickness a, and that post deposition sputtering top thickness B is less than pre-sputtering overhang thickness b. This difference in thickness occurs because during the post deposition sputtering phase, relatively little new deposition is occurring. Instead, excess material from thicker areas of metal barrier layer 250 is being sputtered away, and is redeposited in thinner areas of metal barrier layer 250. The resulting metal barrier layer 250 is more conformal than metal barrier layer 250 before a post deposition sputtering step. In at least one embodiment of the present invention, an optimal post

deposition sputtering bottom thickness A is less than about 1.25 times thicker than the average sidewall thickness.

In at least one embodiment of the present invention, a single post deposition sputtering step is employed to redistribute excess metal from the top and bottom of via 200, to the walls of via 200. In another embodiment, however, multiple cycles of deposition and post deposition sputtering are performed, rather than performing a single post deposition sputtering step after an entire layer of the metal has been deposited.

Referring now to FIGS. 4-7, a multiple-cycle post physical vapor deposition sputtering process will be discussed according to the present invention. Reference numerals and letters in FIGS. 4-7 which are similar or identical to reference numerals and letters in FIGS. 1-3 indicate similar or identical features and/or elements. FIG. 4 illustrates a first step in a multiple-cycle deposition-sputtering process. In FIG. 4 metal barrier layer 250 is deposited in via 200. Note that breadloafing has begun, but is not yet significant, and that metal barrier layer 250 is beginning to thicken at the bottom of via 200.

FIG.5 illustrates the results of the first post deposition sputtering step. This sputtering step is preferably performed by turning the target voltage 164 (FIG. 1) off, while leaving the wafer bias voltage 160 (FIG. 1) on. The first post deposition sputtering step is performed at this point in the metal deposition process in order to keep breadloafing from becoming too severe, and to keep

metal barrier layer 250 from becoming excessively thick at the bottom of via 200. This sputtering step redistributes material in barrier metal layer 250, resulting in barrier layer 250 being substantially conformal to via 200. Note that breadloafing has been reduced, and the thickness of barrier metal layer 250 at the bottom of via 200 has also been reduced.

As shown in FIG. 6, after the first post deposition sputtering step, another metal deposition step is performed in which additional metal is deposited in via 200. The metal deposition is reinitiated by turning target voltage 164 (FIG.1) back on. Note that barrier metal layer 250 again begins to develop overhangs at the top of via 200, and that metal builds up again on the bottom of via 200. In order to keep the undesired deposition of metal to a minimum, another post deposition sputtering step is performed.

FIG. 7 illustrates the net results of the additional deposition-post deposition sputtering steps. Note that barrier metal layer 250 now substantially conforms to the underlying structure of via 200. The deposition-sputtering cycle just discussed can be performed as many times as desired to achieve process objectives. It will also be appreciated that although the preceding discussion is based on the formation of a via, other similar structures may be formed using the principles set forth herein.

Referring next to FIG. 8, a via filled with metal according to a preferred embodiment of the present invention is discussed. Via 800 is preferably formed on top of metal line 210 and comprises

barrier metal layer 250, seed layer 810, and electroplated copper 820. The construction of barrier metal layer 250 has been discussed in reference to previous figures. Seed layer 810 is preferably an ionized PVD copper layer that is formed in substantially the same manner as barrier metal layer 250, except that a copper target and rf coil are used in the deposition process instead of a tantalum target and rf coil. After barrier metal layer 250 and seed layer 810 have been formed using the deposition/post deposition sputtering techniques described herein, via 800 is completed by filling it with electroplated copper 820 such that it provides a conductive connection between metal line 210 and a similar line above the via 800 (not shown in FIG.8).

By employing the principles set forth in this disclosure, barrier metal layer 250 can be made substantially more conformal than otherwise possible. Given that a subsequent layer deposited on a conformal layer can be made more conformal than a subsequent layer deposited on a non-conformal layer, seed layer 810 begins from a conformal state, and can be formed to maintain conformality when via 800 is constructed according to the principles of the present invention.

Referring next to FIG. 9, a method according to at least one embodiment of the present invention in which metal deposition and sputtering are alternated is discussed. Refer also to FIGS. 4-7, which illustrate various stages in the filling of a via. A method according to the present invention begins by depositing metal

inside a feature on the wafer such as a via or trench by applying wafer bias 920 to the wafer, and turning target voltage 164 on. As shown in FIG. 9, tantalum ion density 910 is highest when target voltage 164 is on. Note also that, given a constant power situation, an inverse relationship holds between the magnitude of the wafer bias 920 and target voltage 164. That is to say, when target voltage 164 is turned on, the magnitude of wafer bias 920 decreases, and when target voltage 164 is turned off, the magnitude of wafer bias 920 increases.

After a desired amount of metal has been deposited, target voltage 164 is turned off. As the result of turning target voltage 164 off, tantalum ion density 910 and neutral density are reduced. As just noted, given constant power to wafer 140 (FIG. 1), the magnitude of the wafer bias necessarily increases as the ion density decreases. When the wafer bias increases, the argon atoms are subjected to a higher potential, and are accelerated to a greater velocity. The greater velocity of the argon atoms results in more sputtering when the argon atoms strike the wafer. However, since the density of the tantalum ions is reduced, very little metal deposition takes place.

This cycle of energizing and de-energizing a sputtering target by turning target voltage 164 on and off can be referred to as target pulsing. The target may be pulsed at any suitable predetermined frequency, and for any suitable number of cycles, until the desired layer thickness and conformality are achieved.

The pulsing frequency is preferably, but not necessarily, on the order of 2 KHz, based on ion residence time calculations. The pulsing frequency may be as low as .02 Hz.

In summary, a preferred embodiment of the present invention provides a method for improving conformality of metal deposition layers by introducing a separate sputter step. This sputtering step may be performed using argon ions, helium ions, a combination of argon and helium ions or otherwise. Using argon for example, argon ions are generated in a plasma by an inductive rf coil, and are accelerated towards a wafer by a negative bias applied to the wafer. Energetic ions sputter material from regions where film thickness is high to those where it is low. This means that material is sputtered from the upper corners of the feature to the sidewalls of the feature, and also from the bottom of the feature to the sidewalls, thereby effecting conformality. The sputtering step may be implemented either after deposition of the layer is finished, or as an intermediate step during the deposition of the layer.

The additional sputtering step serves to help optimize and control the evolution of the film profile such that step coverage is optimized. In one embodiment, the optimum step coverage occurs when the thickness of a layer, measured at the bottom of a via is less than 1.25 times the average sidewall thickness of the same layer. In addition to optimizing the step coverage, the present invention may be utilized to minimize barrier layer thickness at the

bottom of a via, trench, or other feature. By minimizing the barrier layer coverage at the bottom of a feature such as a via, the via resistance can be decreased, which is beneficial in most applications.

Although the invention has been described with respect to specific conductivity types or polarity of potentials, skilled artisans appreciated that conductivity types and polarities of potentials may be reversed. Note that by reversal, we mean pulsing in the case of a dielectric target or negative ion sputtering.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or

any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

CLAIMS

1. A method for forming a conductive layer in a via comprising the steps of:

providing a substrate having a conductor;

forming an insulating layer over the conductor;

forming the via through the insulating layer to the conductor; and

sputter depositing a conductive layer in the via selected from of tantalum, titanium, tantalum nitride, titanium nitride, tungsten, and tungsten nitride;

terminating the step of sputter depositing; and

after terminating the step of sputter depositing, sputter etching the metal layer to form the conductive layer.

2. The method of claim 1, wherein the steps of sputter etching and sputter depositing use a sputter agent comprising argon.

3. The method of claim 1, wherein the conductive layer comprises tantalum.

4.The method of claim 3, wherein the conductive layer further comprises tantalum nitride.

5. The method of claim 1, wherein the conductive layer comprises tantalum nitride.

6. The method of claim 1, further comprising depositing a copper seed layer over the conductive barrier layer.

7. The method of claim 1, further comprising filling the via with copper.

8. A method of forming a first conductive layer in a via, comprising the steps of:

providing a substrate having a second conductive layer;

forming an insulating layer over the second conductive layer;

forming the via through the insulating layer to the second conductive layer;

sputter depositing a first layer in the via selected from a group consisting of tantalum, titanium, tantalum nitride, titanium nitride, tungsten, and tungsten nitride;

sputter etching the first layer;

after sputter etching the first layer, sputter depositing a second layer in the via selected from copper, copper alloys, nickel-

iron alloy, tantalum, titanium, tantalum nitride, titanium nitride, tungsten, and tungsten nitride; and

sputter etching the second layer to form the first conductive layer.

9. The method of claim 8, wherein the steps of sputter etching and sputter depositing use a sputter agent comprising argon.

10. The method of claim 8, wherein the first layer is tantalum.

11. The method of claim 8, further comprising depositing a copper seed layer over the first layer.

12. The method of claim 8, further comprising filling the via with copper.

13. A method of forming a conductive barrier layer in a via in a semiconductor wafer using a sputtering chamber having a sputtering target, a wafer pedestal, an rf coil, and a inlet for introducing a sputtering agent into the chamber;

placing the semiconductor wafer on the wafer pedestal;

introducing the sputtering agent into the chamber;

energizing the wafer pedestal;

energizing the rf coil; and

energizing the sputtering target at a predetermined frequency to form the conductive layer.

14. The method of claim 13, wherein the step of energizing the sputtering target occurs after the steps of placing the semiconductor wafer, energizing the wafer pedestal, introducing the sputtering agent, and energizing the rf coil.

15. The method of claim 13, wherein the step of energizing the sputtering target occurs before energizing the wafer.

16. The method of claim 13, wherein the predetermined frequency is greater than 0.02 hertz.

17. The method of claim 13, wherein the step of energizing the sputtering target switches between a predetermined negative voltage and zero voltage.

18. A semiconductor device structure, comprising:

a semiconductor substrate having a conductor over the substrate, an insulating layer over the conductor, and a via through the insulating layer ;

a substantially conformal conductive layer in the via; and

a fill comprising copper in the via.

19. The semiconductor device structure of claim 18, wherein the via has sidewall and a bottom, wherein the conductive layer has a minimum sidewall thickness on the sidewall of the via and a bottom thickness on the bottom, and wherein the bottom thickness is less than 1.25 times thicker than the average sidewall thickness.

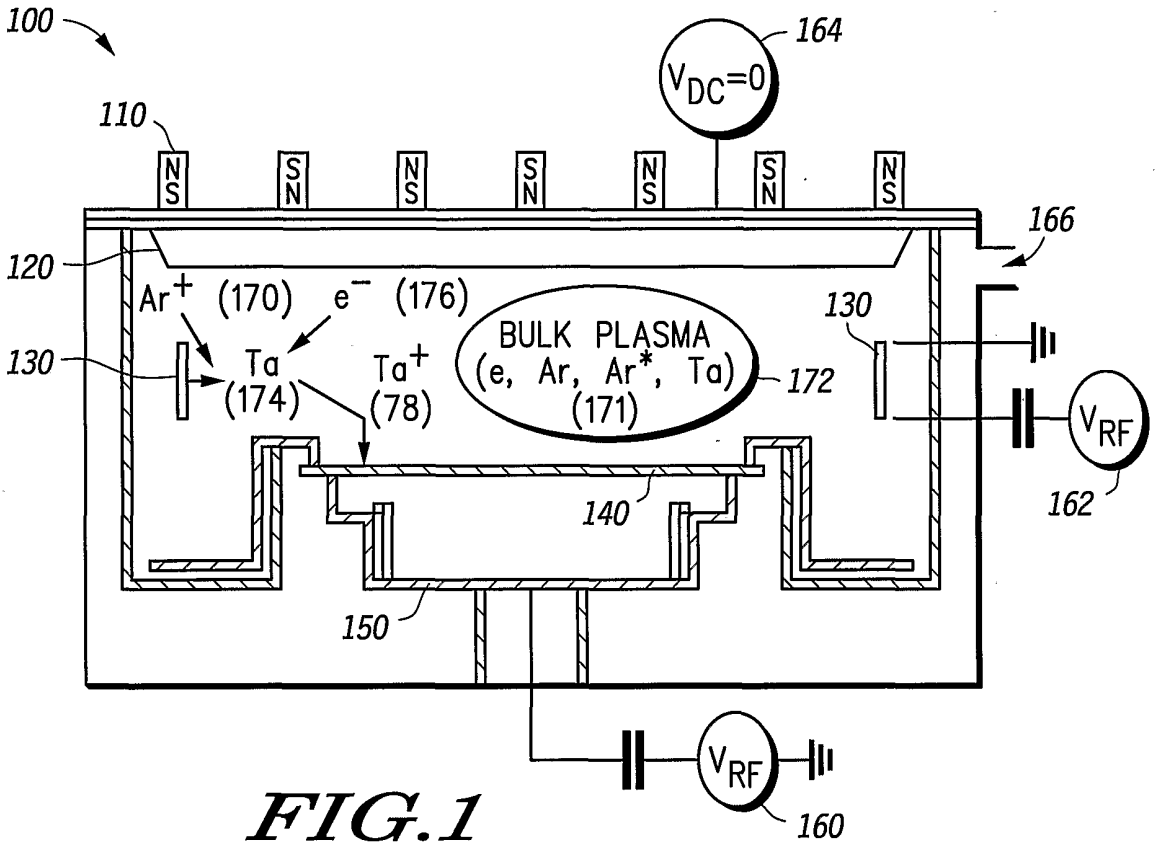


FIG.1

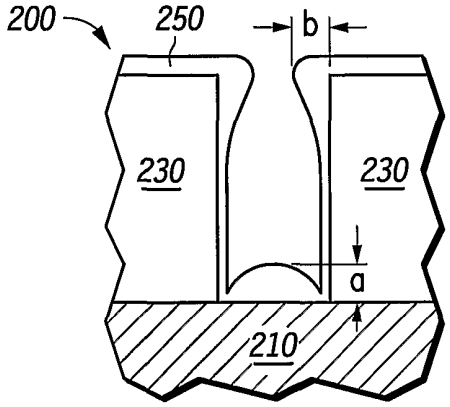


FIG.2

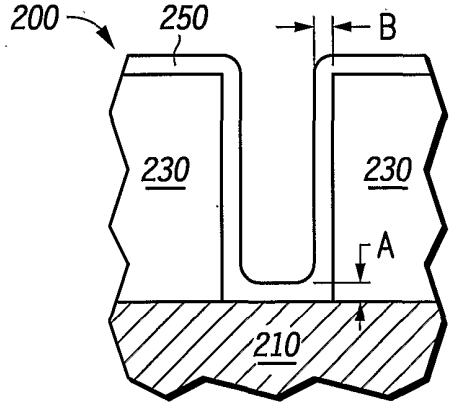


FIG.3

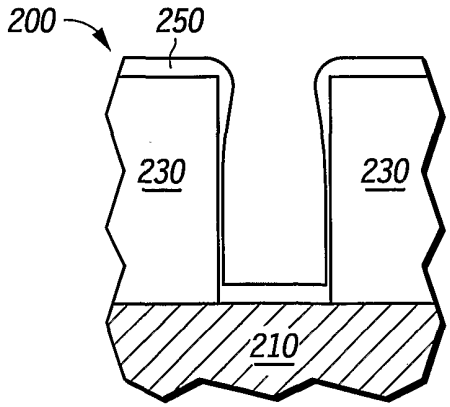


FIG.4

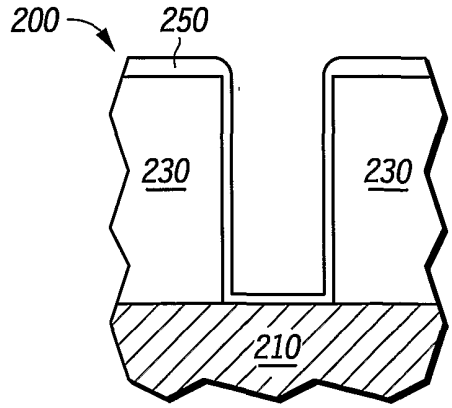


FIG.5

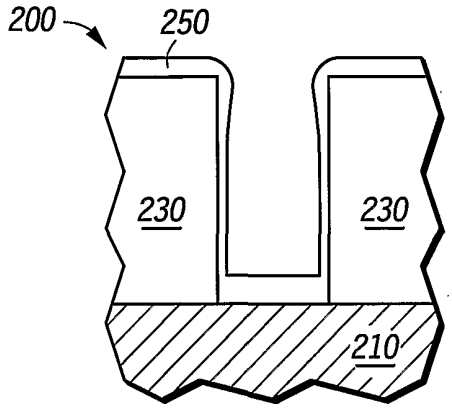


FIG.6

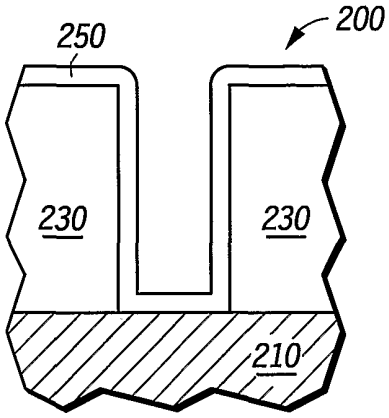


FIG.7

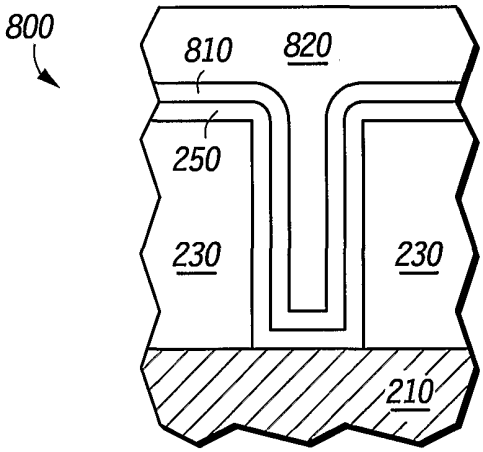


FIG.8

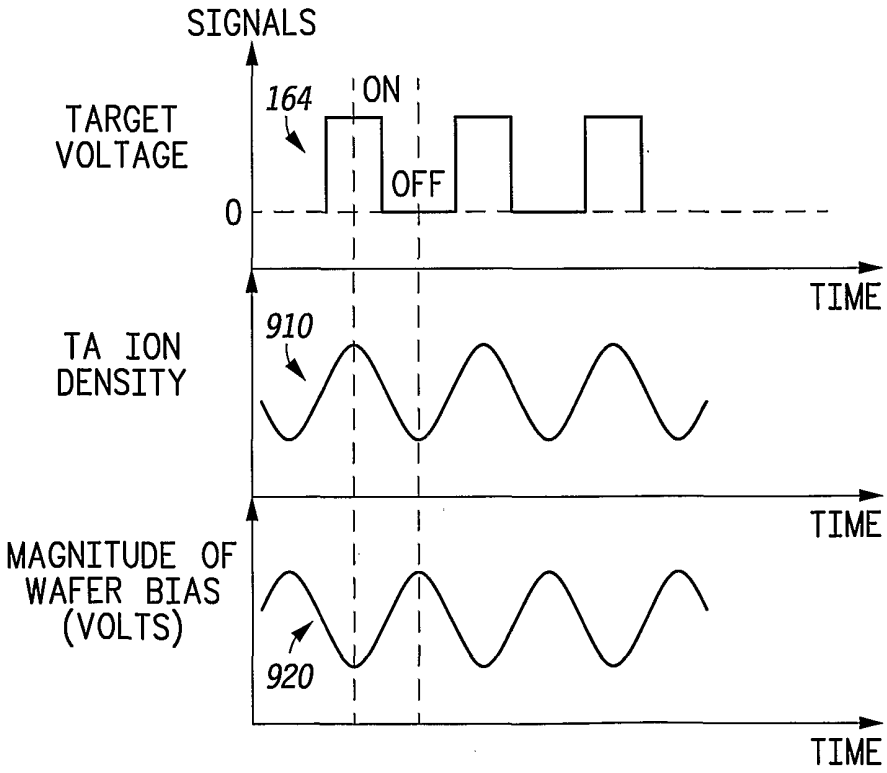


FIG.9