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[Continued on next page]

(54) Title: PIPELINED ADC INTER-STAGE ERROR CALIBRATION

(57) Abstract: An analog-to-digital converter (ADC) (200) includes a plurality of pipelined ADCs (202-1, 202- 2) and an adjustment circuit (204). Each pipelined ADC is adapted to receive an analog input signal (AIN) and to generate an output signal (Da, Db) for an output circuit (206), has an adjustable transfer function, and includes a compensator. The adjustment circuit (204) is coupled to each pipelined ADC to be able to adjust the transfer function for each pipelined ADC so as to generally eliminate an estimation ambiguity. Additionally, the adjustment circuit estimates an inter-stage error that includes at least one of an inter-stage gain error and a DAC gain error and adjusts the compensator for each pipelined ADC to compensate for the inter-stage error.

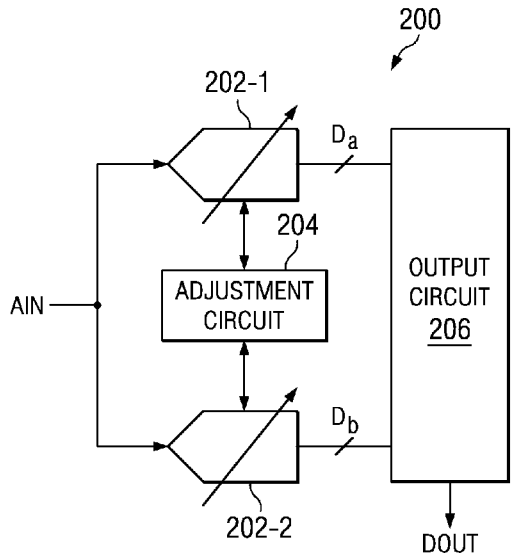

FIG. 2

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PIPELINED ADC INTER-STAGE ERROR CALIBRATION

[0001] This relates generally to pipelined analog-to-digital converter (ADC) and, more particularly, to a pipelined ADC that employs a split ADC architecture to compensate for inter-stage gain error or digital-to-analog converter (DAC) gain error in each stage.

BACKGROUND

[0002] Pipelined ADCs have been used extensively (for example) in high performance digital communication systems, waveform acquisitions, and instrumentations. While the speed of state-of-the-art pipelined ADC has exceeded 100 MSPS, the resolution is generally limited by the inter-stage gain error and/or DAC gain error resulting from circuit non-idealities (i.e., capacitor mismatch and finite operational amplifier (opamp) gain, and so forth). Thus, most pipelined ADCs with more than 12-bit resolution usually require some linearity enhancement techniques.

[0003] There also exists an architecture, known as a split ADC architecture, that can be used to perform background calibrations, and, turning to FIG. 1, an example of a convention ADC 100 using a split ADC architecture can be seen. This ADC 100 generally comprises channels or ADCs 102-1 and 102-2, adders 104-1 and 104-2, and a divider 106. Typically, ADCs 102-1 and 102-2 have the same general structure, and, in operation, receive the same analog input signal AIN so as to perform a data conversion at approximately the same time (generating digital output signals DA and DB, respectively). The difference ΔD between these output signals DA and DB, which is generated by adder 104-2 (which operates as a subtractor), can be used for calibrating ADCs 102-1 and 102-2, while an average of the output signals DA and DB (generated by adder 104-1 and divider 106) would correspond to a digital output for ADC 100. However, there are difficulties in compensating for inter-stage gain errors and/or DAC gain errors when ADCs 102-1 and 102-2 are pipelined ADCs.

[0004] Therefore, there is a need for a method and/or apparatus that compensates for inter-stage gain error and/or DAC gain error in a pipelined ADC.

[0005] Some examples of conventional circuits are described in: Park et al., "A 10-b 100MS/s CMOS pipelined ADC with 1.8V power supply," Proc. ISSCC Digest Technical Papers, pp. 130–131, Feb. 2001; McNeill et al., "Split ADC Architecture for Deterministic Digital Background Calibration of a 16-bit 1-MS/s ADC," IEEE Journal of Solid State Circuits, vol. 40, pp. 2437-2445, Dec. 2005; Li et al., "Background calibration techniques for multistage pipelined ADCs with digital redundancy," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 50, no. 9, pp. 531–538, Sep. 2003; U.S. Patent No. 6,081,215; U.S. Patent No. 6,445,317 U.S. Patent No. 6,452,518; U.S. Patent No. 7,312,734; and U.S. Patent Publication No. 2006/0176197.

SUMMARY

[0006] An example embodiment, accordingly, provides an apparatus. The apparatus comprises a plurality of pipelined analog-to-digital converters (ADCs), wherein each pipelined ADC is adapted to receive an analog input signal, and wherein each pipelined ADC has a transfer function that is adjustable, and wherein each pipelined ADC includes a compensator; and an adjustment circuit that is coupled to each pipelined ADC, wherein the adjustment circuit adjusts the transfer function for each pipelined ADC so as to generally eliminate an estimation ambiguity, and wherein the adjustment circuit estimates an inter-stage error that includes at least one of an inter-stage gain error and a digital-to-analog converter (DAC) gain error and adjusts the compensator for each pipelined ADC to compensate for the inter-stage error.

[0007] In an example embodiment, each pipelined ADC further comprises: a plurality of stages that are coupled to one another in a sequence; and a backend sub-ADC that is coupled to a last stage of the sequence.

[0008] In an example embodiment, each compensator further comprises: a digital adder that is coupled to each stage of the sequence of its pipelined ADC; and a digital multiplier that is coupled between to the backend sub-ADC and the digital adder and that is coupled to the adjustment circuit, wherein the adjustment circuit adjusts the gain for the digital multiplier to compensate for the inter-stage error.

[0009] In an example embodiment, each stage for each pipelined ADC further comprises: an input terminal; a sub-ADC that is coupled to the input terminal; a DAC that is coupled to the sub-ADC; an subtractor that is coupled to input terminal and the DAC; and a residue amplifier that is coupled to the subtractor.

[0010] In an example embodiment, each sub-ADC further comprises a plurality of comparators that are adapted to be shifted so as to adjust the transfer function of its pipelined ADC.

[0011] In an example embodiment, the adjustment circuit shifts the sub-ADC of the first stage of at least one of the pipelined ADCs by ¼ of a least significant bit (LSB).

[0012] In an example embodiment, each stage for the pipelined ADC further comprises an analog multiplier that is coupled between the input terminal and the sub-ADC, wherein gain of the analog multiplier is adjusted by the adjustment circuit.

[0013] In an example embodiment, a method for calibrating a ADC having a first pipelined ADC and a second pipelined ADC is provided. The method comprising shifting a first set of comparators of a first sub-ADC of a first stage of the first pipelined ADC by a first amount to adjust a first transfer function of the first pipelined ADC; shifting a second set of comparators of a first sub-ADC of a first stage of the second pipelined ADC by a second amount to adjust a second transfer function of the second pipelined ADC; estimating an inter-stage error for the ADC once first set of comparators and the second set of comparators have been shifted, wherein the inter-stage error includes at least one of an inter-stage gain error and a DAC gain error; and adjusting a first compensator of the first pipelined ADC and a second compensator of the second pipelined ADC to compensate for the inter-stage error.

[0014] In an example embodiment, the step of adjusting further comprises: adjusting a first gain of a first digital multiplier of the first pipelined ADC; multiplying a digital output from a first back-end sub-ADC of the first pipelined ADC by the first gain; adding a digital output for each stage of the second pipelined ADC and for the first digital multiplier together; adjusting a second gain of a second digital multiplier of the second pipelined ADC; multiplying a digital output from a second back-end sub-ADC of the second pipelined ADC by the second gain; and adding a digital output for each stage of the second pipelined ADC and for the second digital multiplier together.

[0015] In an example embodiment, the method further comprises: estimating a gain mismatch between the first and second pipelined ADCs; estimating an offset mismatch between the first and second pipelined ADCs; and compensating for the gain and offset mismatches.

[0016] In an example embodiment, the first and second amounts are ¼ of an LSB.

[0017] In an example embodiment, an apparatus is provided. The apparatus comprises a first pipelined ADC having a first transfer function and having: a first track-and-hold (T/H) circuit that is adapted to receive an analog input signal; a first set of stages that are coupled to one another in a first sequence, wherein a first stage of the first sequence is coupled to the first T/H circuit, and wherein at least one of the stages from the first set of stages is adjustable so as to adjust a first transfer function; a first backend sub-ADC that is coupled to a last stage of the first sequence; and a first compensator that is coupled to each stage from the first set of stages and the first backend sub-ADC; a second pipelined ADC having a second transfer function and having: a second T/H circuit that is adapted to receive the analog input signal; a second set of stages that are coupled to one another in a second sequence, wherein a first stage of the second sequence is coupled to the second T/H circuit, and wherein at least one of the stages from second set of stages is adjustable so as to adjust a second transfer function; a second backend sub-ADC that is coupled to a last stage of the second sequence; and a second compensator that is coupled to each stage from the second set of stages and the second backend sub-ADC; and an adjustment circuit that is coupled to the first and second pipelined ADCs so as to adjust the first and second transfer functions and that is coupled to the first and second compensators, wherein the adjustment circuit estimates inter-stage error that includes at least one of an inter-stage gain error and a DAC gain error and adjusts the first and second compensators to compensate for the inter-stage error.

[0018] In an example embodiment, the first compensator further comprises a first digital adder that is coupled to each stage from the first set of stages; and a first digital multiplier that is coupled between to the first backend sub-ADC and the first digital adder and that is coupled to the adjustment circuit.

[0019] In an example embodiment, the first compensator further comprises: a second digital adder that is coupled to each stage from the second set of stages; and a first digital multiplier that is coupled between to the second backend sub-ADC and the second digital adder and that is coupled to the adjustment circuit.

[0020] In an example embodiment, each stage from the first and second sets of stages further comprises: an input terminal; a sub-ADC that is coupled to the input terminal; a DAC that is coupled to the sub-ADC; an subtractor that is coupled to input terminal and the DAC; and a residue amplifier that is coupled to the subtractor.

[0021] In aan example embodiment, each sub-ADC further comprises a flash ADC having a plurality of comparators, wherein each of the comparators are adapted to be shifted.

[0022] In an example embodiment, the adjustment circuit shifts the sub-ADC of the first stage of at least one of the pipelined ADCs by ¼ of an LSB.

[0023] In accordance with an example embodiment, the apparatus further comprises an output circuit that is coupled to the first and second digital adders.

[0024] In an example embodiment, the first pipelined ADC further comprises a first mismatch compensator that is coupled between the first T/H circuit and the first stage of the first set of stages, and wherein second pipelined ADC further comprises a second mismatch compensator that is coupled between the second T/H circuit and the first stage of the second set of stages, and wherein the adjustment circuit estimate gain and offset mismatches between the first and second pipelined ADC and adjusts the first and second mismatch circuit.

[0025] In an example embodiment, the adjustment circuit estimates the inter-stage error, the gain mismatch, and the offset mismatch using a least mean square (LMS) algorithm.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] FIG. 1 shows an example of a conventional ADC;

[0027] FIG. 2 shows an example of an ADC in accordance with an example embodiment;

[0028] FIG. 3 shows an example of a pipelined ADC of FIG. 2;

[0029] FIGS. 4 and 5 show examples of a stage of FIG. 3;

[0030] FIG. 6 shows an example of the sub-ADC of FIGS. 4 and 5;

[0031] FIG. 7A and 7B depict adjustments for the transfer functions of the pipelined ADCs of FIG. 2;

[0032] FIGS. 8A and 8B depict the spurious-free dynamic range (SFDR) of the ADC of FIG. 2 with and without calibration; and

[0033] FIG. 9 depicts the convergence of a calibration method used by the ADC of FIG. 2.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0034] FIG. 2 illustrates an example ADC 200 that generally comprises pipelined ADCs 202-1 and 202-2, adjustment circuit 204, and output circuit 206. Here, two pipelined ADCs are shown for the sake of simplicity but additional pipelined ADCs or an ADC tree may be employed. In operation, each of ADCs 202-1 and 202-2 have generally the same structure and receive the analog input signal AIN so as to generate output signals D_a and D_b for the output circuit 206 (which can average these signals and can perform digital correction). The adjustment circuit 204 provides adjustments to the ADCs 202-1 and 202-2 to compensate for inter-stage gain errors and/or DAC gain errors (within ADCs 202-1 and 202-2) and gain/offset mismatches (between ADCs 202-1 and 202-2).

[0035] In FIG. 3, each pipeline ADC 202-1 and 202-2 (hereinafter 202 for FIG. 3) can be seen in greater detail. As shown, pipeline ADC 202 generally comprises a compensator 314 (which generally includes a digital multiplier or digital gain block 312 and an adder or combiner 310) and a pipeline 301 (which includes a track-and-hold (T/H) circuit 302, a mismatch compensator 308, a set of stages 304-1 to 304-N coupled together in a sequence, and a backend sub-ADC 306). In operation, the adjustment circuit 206 receives an output from the adder 310 (which combines the digital outputs from stages 304-1 to 304-N and backend sub-ADC 306) and should be able to compensate for inter-stage gain error and/or DAC gain error by perform adjustments (namely, adjusting the gain) to the digital multiplier 312 (which is coupled between the adder 310 and backend sub-ADC 306). However, under these circumstances, an estimation ambiguity exists that generally prevents an accurate estimation.

[0036] For simplicity, it can be assumed that there is one stage (i.e., 304-1) and a backend sub-ADC (i.e., 306). The output signals D_a and D_b would then be:

(1) $$D_a = D_{1,a} + g_a D_{2,a}$$, and

(2) $$D_b = D_{1,b} + g_b D_{2,b}$$,

where $D_{1,a}$ and $D_{1,b}$ are the output from the stages (i.e., 304-1), $D_{2,a}$ and $D_{2,b}$ are the output from the backend sub-ADCs (i.e., 306), and g_a and g_b are gains of the digital multipliers (i.e., 312). Because the output from the stages (i.e., 304-1) $D_{1,a}$ and $D_{1,b}$ should be the same, the difference ΔD would then be:

(3) $$\Delta D = D_a - D_b = g_a D_{2,a} - g_b D_{2,b}.$$

The optimal solution for the digital multipliers (i.e., 306) is:

$$g_a^{opt} = \frac{1}{G_{1a}}, \text{ and} \quad (4)$$

$$g_b^{opt} = \frac{1}{G_{1b}}, \quad (5)$$

where $G_{1,a}$ and $G_{1,b}$ denote the inter-stage gains and/or DAC gain errors, so, when the difference is minimized using a least mean square (LMS) algorithm, there is an estimation ambiguity because the number of variables exceeds the number of equations in the system. Namely, the estimation ambiguity is:

$$\hat{g}_a = \alpha g_a^{opt}, \text{ and} \quad (6)$$

$$\hat{g}_b = \alpha g_b^{opt}. \quad (7)$$

To address, this estimation ambiguity, adjustment circuit 204 can adjust the transfer function of each of the pipeline ADCs (i.e., 204-1 and 204-2 of FIG. 2), and there are several ways to adjust these transfer functions.

[0037] FIGS. 4 and 5 illustrate examples of one of the stages 304-1 to 304-N (hereinafter 304-A and 304-B for FIGS. 4 and 5, respectively) which can be adjusted by the adjustment circuit 204 can be seen. Stage 304-A generally comprises a sub-ADC 402-1, a DAC 404, an adder 408 (which operates as a subtractor), and a residue amplifier 406, while stage 304-B includes sub-ADC 402-1 and analog multiplier 502. Typically, the an analog signal (either from the T/H circuit 302 or a previous stage) is converted by sub-ADC 402-1 (or 402-1) to a digital signal. This digital signal is provided to adder 310 and DAC 404. The DAC 404 converts the signal back to an analog signal, and the analog signal from the DAC 404 (which can introduce a DAC gain) is subtracted from the analog signal from the T/H circuit 302 or a previous stage by adder 408 to generate a residue signal. This residue signal is amplified by residue amplifier 406 (which can introduce an inter-stage gain).

[0038] As shown in FIG. 6, sub-ADC 402-1 or 402-2 (hereinafter 402) can be one of a variety of types of ADCs but is typically a flash ADC (as shown). This flash ADC 402 generally comprises a voltage divider 604 (which generally includes resistors R1 to R(M+1) coupled in series with one another) and comparators 602-1 to 602-M. Generally, each comparator 602-1 to

602-M is coupled to voltage divider 604 and receives an analog input signal to generate a digital output signal.

[0039] Turning back to FIG. 4, adjustments to the transfer function can be accomplished by making direct adjustments to the sub-ADC 402-1. Preferably, adjustments to the transfer function can be performed by shifting the comparators 602-1 to 602-M (i.e., shifting the reference voltage REF) within sub-ADC 402-1 with an adjustment signal ADJ. Usually, the transfer functions for each of pipeline ADCs 202-1 and 202-2 are supposed to match (as shown in FIG. 7A) match, but to resolve the estimation ambiguity described above, the comparators 602-1 to 602-M for one or more of the stages each of pipeline ADCs can be shifted by predetermined amounts. For example and as shown in FIG. 7B, the comparators 602-1 to 602-M for a the first stage (i.e., 304-1) for pipeline ADC 202-1 can be shifted by +¼ of a least significant bit (LSB), while the comparators 602-1 to 602-M for a the first stage (i.e., 304-1) for pipeline ADC 202-2 can be shifted by -¼ of an LSB. By doing this, however, some resolution in digital redundancy is lost.

[0040] Alternatively, as shown in FIG. 5, the analog signal from the T/H circuit 302 or from the previous stage can be modified before being converted. As shown, a multiplier 502 can be included in the signal path. The adjustment circuit 206 can provide a gain MUL (or alternatively a signal) to achieve substantially the same goal as directly adjusting ADC 402-1 described above.

[0041] It should also be noted that with multi-pipeline ADCs (i.e., ADC 200), there are gain and offset mismatches between the channels. These mismatches are not generally zeroed when the multipliers (i.e., 312) are adjusted to be substantially optimal. Thus, the estimation should take gain and offset mismatches into account. Assuming, again, (for the sake of simplicity of description) that there are two pipelined ADCs (as shown in FIG. 2) that each have two stages, where K_a and K_b denote the global gain for pipeline ADCs 202-1 and 202-2 (respectively), OS_a and OS_b denote the offset of for pipeline ADCs 202-1 and 202-2 (respectively), and D_0 is the ideal output. Ignoring inter-state gain and DAC gain error, the output signals D_a and D_b would be:

$$D_a = K_a D_0 + OS_a, \text{ and} \quad (8)$$

$$D_b = K_b D_0 + OS_b. \quad (9)$$

A weighted difference δD can be defined as follows using equations (8) and (9) above:

$$\delta D \equiv KD_a - D_b + OS = (KK_a - K_b)D_o + (OS + OS_a - OS_b), \quad (10)$$

where K and OS are the gain and offset adjustments for mismatch compensator 308. The resulting cost function J would be:

$$J = \delta D^2. \quad (11)$$

When the gain adjustment K and the offset adjustment OS for mismatch compensator converge to:

$$K = \frac{K_b}{K_a}, \text{ and} \quad (12)$$

$$OS = OS_b - OS_a, \quad (13)$$

minimization of the cost function J would be zero, indicating gain and offset mismatches can be compensated for. Expanding this cost function to an adaptive estimation (which includes estimation for inter-stage gain error and/or DAC gain error), the output signals D_a and D_b become:

$$D_a = K_a(D_{1,a} + g_a D_{2,a}) + OS_a, \text{ and} \quad (14)$$

$$D_b = K_b(D_{1,b} + g_a D_{2,b}) + OS_b. \quad (15)$$

An LMS algorithm can then be applied to the cost function J (of equation (11) above which uses the output signals D_a and D_b of equations (14) and (15)), leading to the following equations:

$$\hat{g}_a(k+1) = \hat{g}_a(k) - \mu_a \nabla J_{g_a}, \quad (16)$$

$$\hat{g}_b(k+1) = \hat{g}_b(k) - \mu_b \nabla J_{g_b}, \quad (17)$$

$$\hat{K}(k+1) = \hat{K}(k) - \mu_K \nabla J_K, \text{ and} \quad (18)$$

$$\hat{OS}(k+1) = \hat{OS}(k) - \mu_{OS} \nabla J_{OS}. \quad (19)$$

Thus, using equations (16)-(19) above, the adjustment circuit 204 can estimate (and compensate for) inter-stage gain error, DAC gain error and gain/offset mismatches at about the same time.

[0042] FIGS. 8A through 9 show the results of some example simulations. For this example, each of pipelined ADCs 202-1 and 202-2 is a 16-bit pipelined ADC having four stages.

Each of the four stages in the pipeline for this example has 4, 5, 5, and 5 bits for each stage, respectively. Correspondingly, the optimal inter-stage gains are 8 and 16 for the first and second stages. For this example, it is assumed that both pipelines have gain errors in the first two stages, and the gain implemented for pipelined ADCs 202-1 and 202-2 are shown in Table 1 below.

Table 1

	Pipelined ADC 202-1	Pipelined ADC 202-2
Stage 1	8.0092	7.9077
Stage 2	16.1278	16.0653

To model the channel mismatches, a 0.05% gain mismatch and 10 LSB offset mismatch were introduced. In FIGS. 8A and 8B, the SFDRs before and after the calibration are shown, and it can be observed that the SFDR is improved from 74dB to 113dB. Additionally, the convergence curve of the digital multipliers (i.e., 312) for each of pipelined ADCs 202-1 and 202-2 can be seen in FIG. 9, showing a convergence at about 40,000 samples when using a 1/10 LSB shift instead of ¼ LSB shift (that would result in a longer convergence time), which is about 100 times faster than any other known approach and which is not restrictive (unlike some energy-free approaches).

[0043] Those skilled in the art to which the invention relates will appreciate that modifications may be made to the described examples, and that many other embodiments are possible, without departing from the scope of the claimed invention.

CLAIMS

1. An apparatus comprising:

a plurality of pipelined analog-to-digital converters (ADCs), wherein each pipelined ADC is adapted to receive an analog input signal, and wherein each pipelined ADC has a transfer function that is adjustable, and wherein each pipelined ADC includes a compensator; and

an adjustment circuit that is coupled to each pipelined ADC, wherein the adjustment circuit adjusts the transfer function for each pipelined ADC so as to generally eliminate an estimation ambiguity, and wherein the adjustment circuit estimates a inter-stage error that includes at least one inter-stage gain error and a digital-to-analog converter (DAC) gain error, and adjusts the compensator for each pipelined ADC to compensate for the inter-stage error.

2. The apparatus of Claim 1, wherein each pipelined ADC further comprises:
a plurality of stages that are coupled to one another in a sequence; and a backend sub-ADC that is coupled to a last stage of the sequence.

3. The apparatus of Claim 2, wherein each compensator further comprises:

a digital adder that is coupled to each stage of the sequence of its pipelined ADC; and

a digital multiplier that is coupled between to the backend sub-ADC and the digital adder and that is coupled to the adjustment circuit, wherein the adjustment circuit adjusts the gain for the digital multiplier to compensate for the inter-stage error.

4. The apparatus of Claim 3, wherein each stage for each pipelined ADC further comprises:

an input terminal;

a sub-ADC that is coupled to the input terminal;

a DAC that is coupled to the sub-ADC;

an subtractor that is coupled to input terminal and the DAC; and

a residue amplifier that is coupled to the subtractor.

5. The apparatus of Claim 4, wherein each sub-ADC further comprises a plurality of comparators that are adapted to be shifted so as to adjust the transfer function of its pipelined ADC.

6. The apparatus of Claim 5, wherein the adjustment circuit shifts the sub-ADC of the first stage of at least one of the pipelined ADCs by ¼ of a least significant bit (LSB).

7. The apparatus of Claim 4, wherein each stage for the pipelined ADC further comprises an analog multiplier that is coupled between the input terminal and the sub-ADC, wherein gain of the analog multiplier is adjusted by the adjustment circuit.

8. A method for calibrating a ADC having a first pipelined ADC and a second pipelined ADC, the method comprising:

shifting a first set of comparators of a first sub-ADC of a first stage of the first pipelined ADC by a first amount to adjust a first transfer function of the first pipelined ADC;

shifting a second set of comparators of a first sub-ADC of a first stage of the second pipelined ADC by a second amount to adjust a second transfer function of the second pipelined ADC;

estimating an inter-stage error for the ADC once first set of comparators and the second set of comparators have been shifted, wherein the inter-stage error includes at least one of an inter-stage error and a DAC gain error; and

adjusting a first compensator of the first pipelined ADC and a second compensator of the second pipelined ADC to compensate for the inter-stage error.

9. The method of Claim 8, wherein the step of adjusting further comprises:

adjusting a first gain of a first digital multiplier of the first pipelined ADC;

multiplying a digital output from a first back-end sub-ADC of the first pipelined ADC by the first gain;

adding a digital output for each stage of the second pipelined ADC and for the first digital multiplier together;

adjusting a second gain of a second digital multiplier of the second pipelined ADC;

multiplying a digital output from a second back-end sub-ADC of the second pipelined ADC by the second gain; and

adding a digital output for each stage of the second pipelined ADC and for the second digital multiplier together.

10. The method of Claim 9, wherein the method further comprises:

estimating a gain mismatch between the first and second pipelined ADCs;

estimating an offset mismatch between the first and second pipelined ADCs; and

compensating for the gain and offset mismatches.

11. The method of Claim 10, wherein the first and second amounts are ¼ of an LSB.

12. An apparatus comprising:

a first pipelined ADC having a first transfer function and having:

a first track-and-hold (T/H) circuit that is adapted to receive an analog input signal;

a first set of stages that are coupled to one another in a first sequence, wherein a first stage of the first sequence is coupled to the first T/H circuit, and wherein at least one of the stages from the first set of stages is adjustable so as to adjust a first transfer function;

a first backend sub-ADC that is coupled to a last stage of the first sequence; and

a first compensator that is coupled to each stage from the first set of stages and the first backend sub-ADC;

a second pipelined ADC having a second transfer function and having:

a second T/H circuit that is adapted to receive the analog input signal;

a second set of stages that are coupled to one another in a second sequence, wherein a first stage of the second sequence is coupled to the second T/H circuit, and wherein at least one of the stages from second set of stages is adjustable so as to adjust a second transfer function;

a second backend sub-ADC that is coupled to a last stage of the second sequence; and

a second compensator that is coupled to each stage from the second set of stages and the second backend sub-ADC; and

an adjustment circuit that is coupled to the first and second pipelined ADCs so as to adjust the first and second transfer functions and that is coupled to the first and second

compensators, wherein the adjustment circuit estimates inter-stage error that includes at least one of an inter-stage gain error and a DAC gain error and adjusts the first and second compensators to compensate for the inter-stage error.

13. The apparatus of Claim 12, wherein the first compensator further comprises:

a first digital adder that is coupled to each stage from the first set of stages; and

a first digital multiplier that is coupled between to the first backend sub-ADC and the first digital adder and that is coupled to the adjustment circuit.

14. The apparatus of Claim 13, wherein the first compensator further comprises:

a second digital adder that is coupled to each stage from the second set of stages; and

a first digital multiplier that is coupled between to the second backend sub-ADC and the second digital adder and that is coupled to the adjustment circuit.

15. The apparatus of Claim 14, wherein each stage from the first and second sets of stages further comprises:

an input terminal;

a sub-ADC that is coupled to the input terminal;

a DAC that is coupled to the sub-ADC;

an subtractor that is coupled to input terminal and the DAC; and

a residue amplifier that is coupled to the subtractor.

16. The apparatus of Claim 15, wherein each sub-ADC further comprises a flash ADC having a plurality of comparators, wherein each of the comparators are adapted to be shifted.

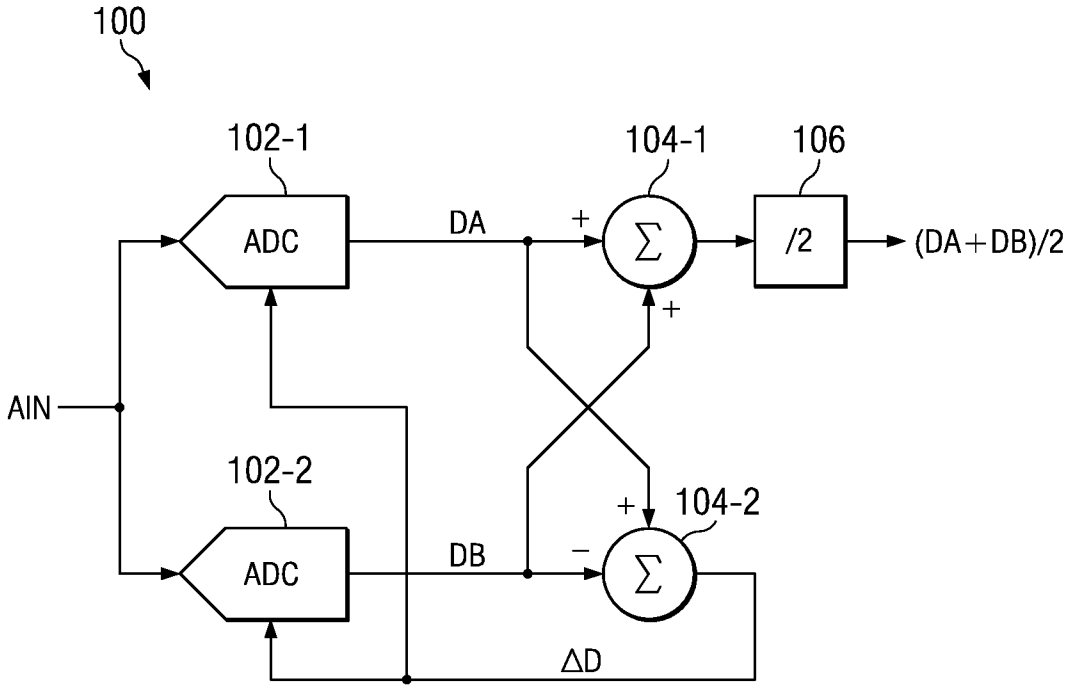

FIG. 1
(PRIOR ART)

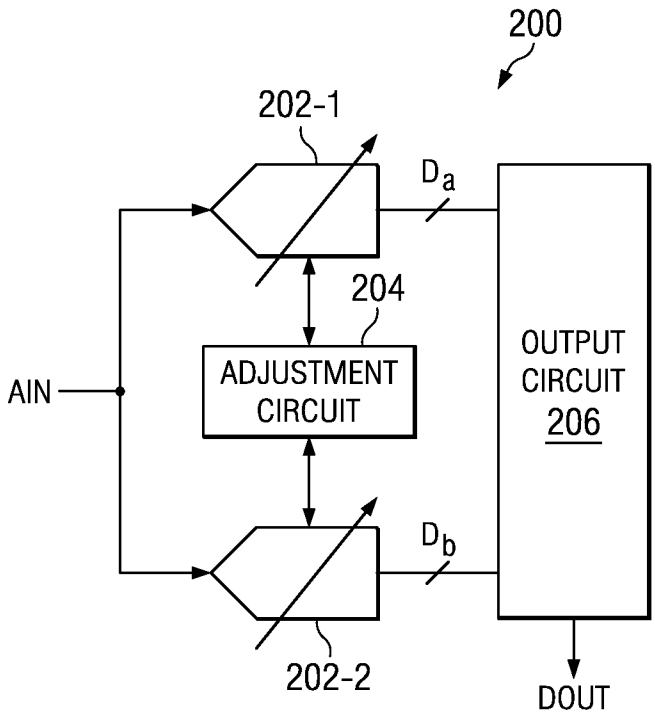

FIG. 2

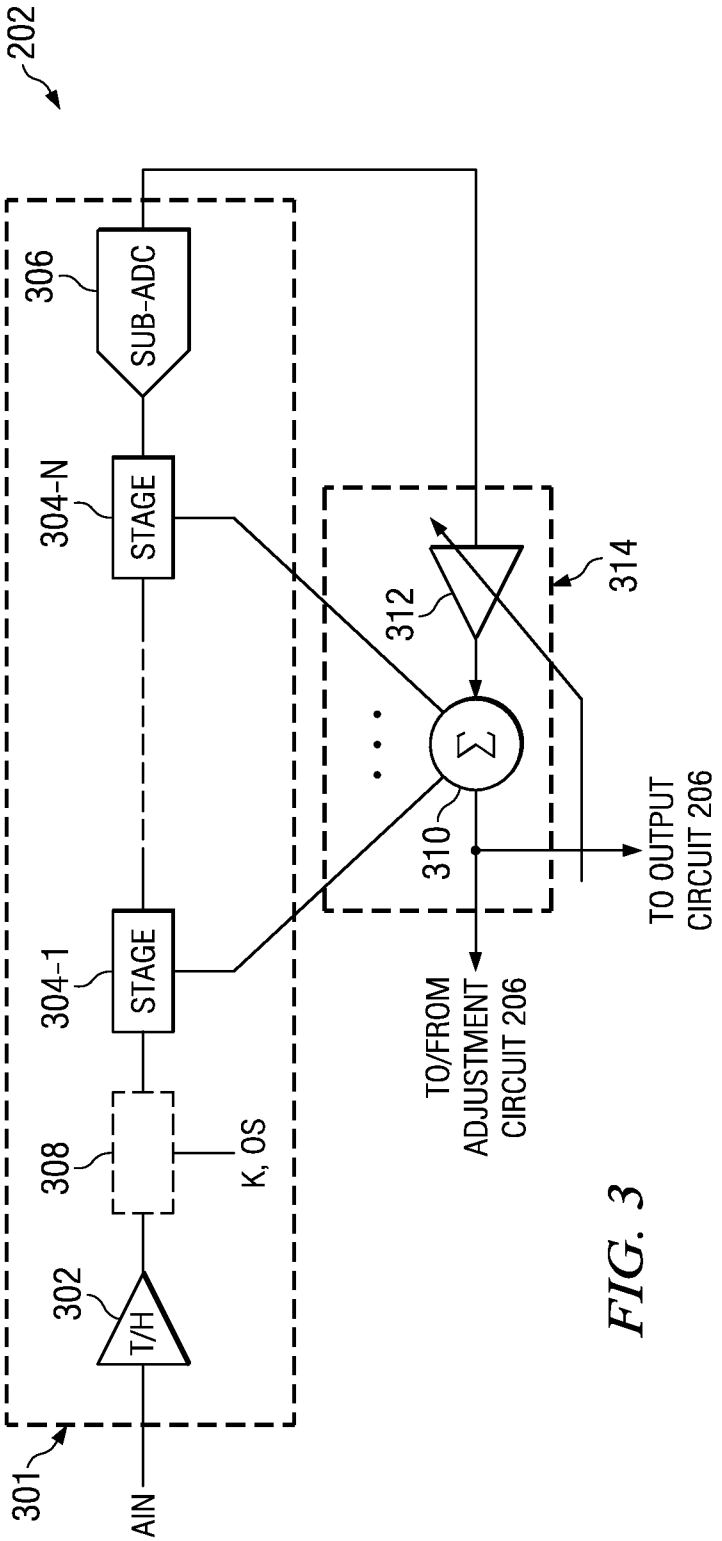
202
306
SUB-ADC
304-N
STAGE
304-1
STAGE
308
K, OS
302
T/H
301
AIN
312
314
310
TO/FROM ADJUSTMENT CIRCUIT 206
TO OUTPUT CIRCUIT 206

FIG. 3

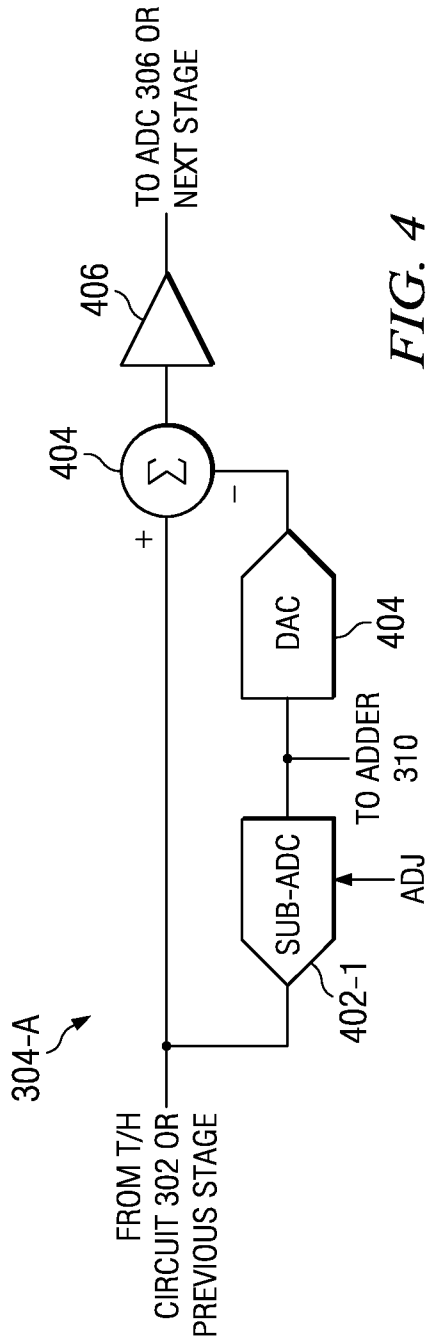
TO ADC 306 OR NEXT STAGE
406
404
+
−
DAC
404
TO ADDER 310
ADJ
SUB-ADC
402-1
304-A
FROM T/H CIRCUIT 302 OR PREVIOUS STAGE

FIG. 4

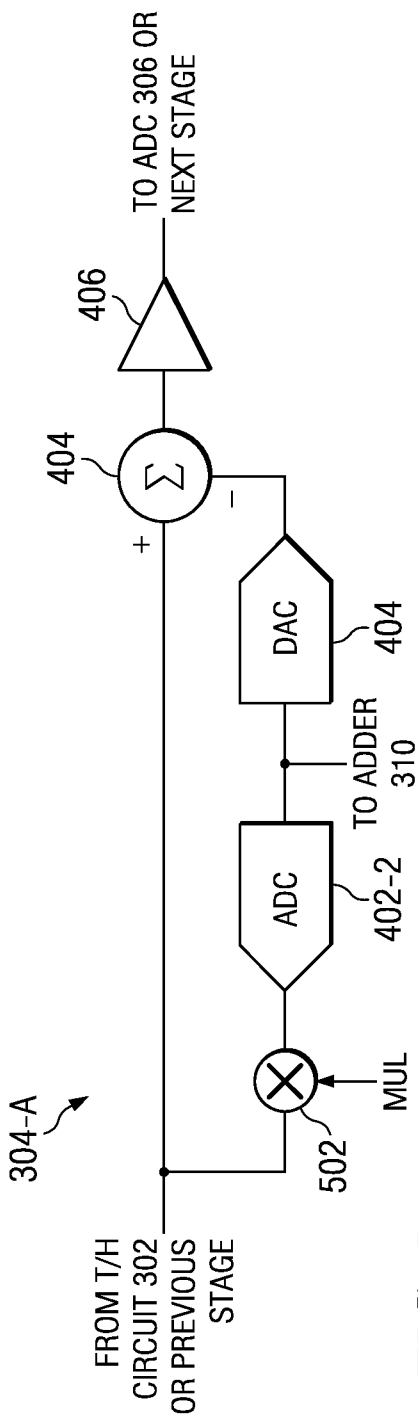
FROM T/H CIRCUIT 302 OR PREVIOUS STAGE
304-A
502
MUL
ADC
402-2
TO ADDER 310
DAC
404
404
406
TO ADC 306 OR NEXT STAGE

FIG. 5

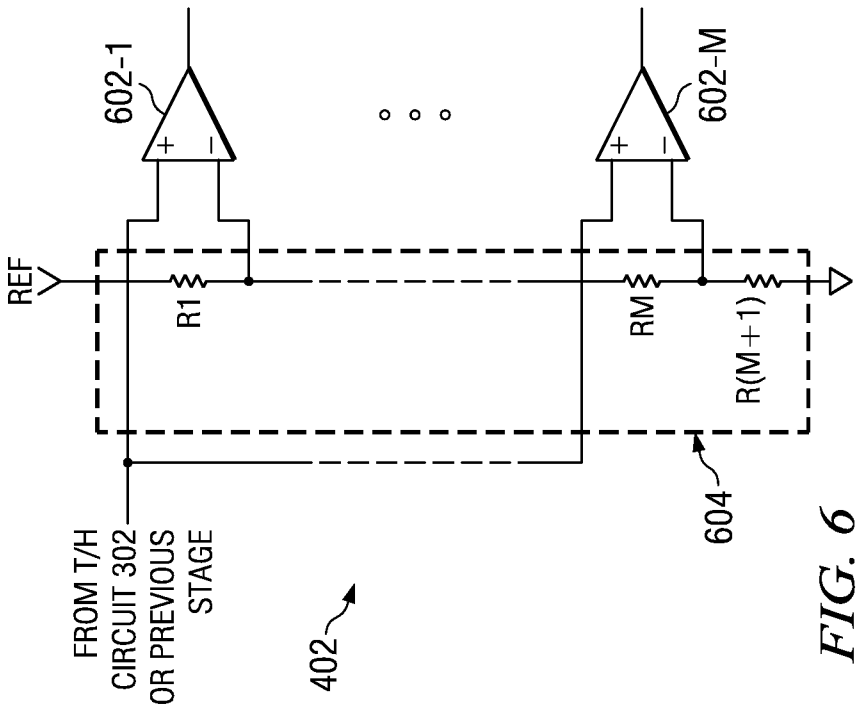
602-1
602-M
REF
R1
RM
R(M+1)
FROM T/H CIRCUIT 302 OR PREVIOUS STAGE
402
604

FIG. 6

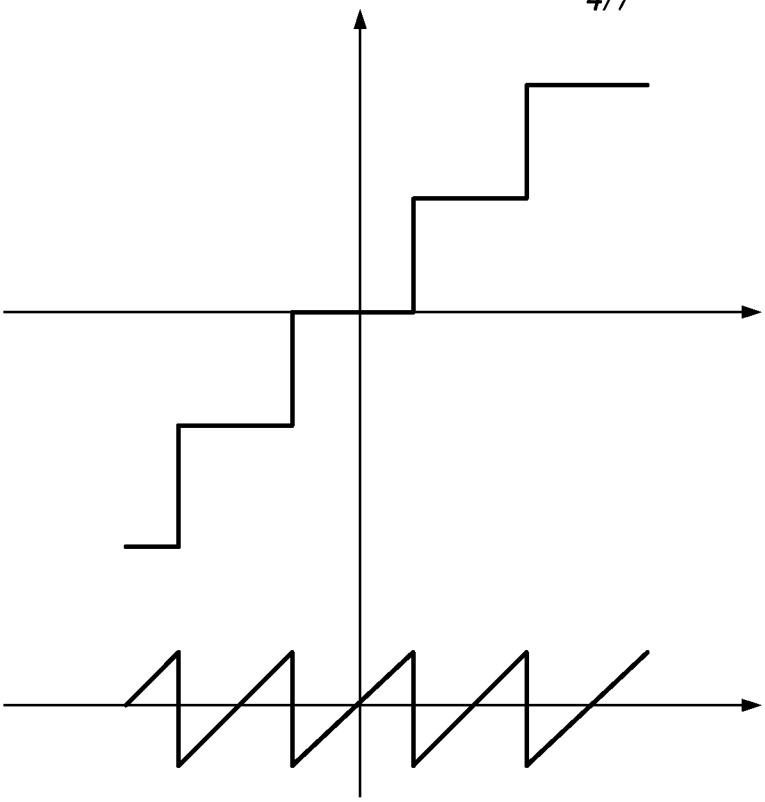

FIG. 7A

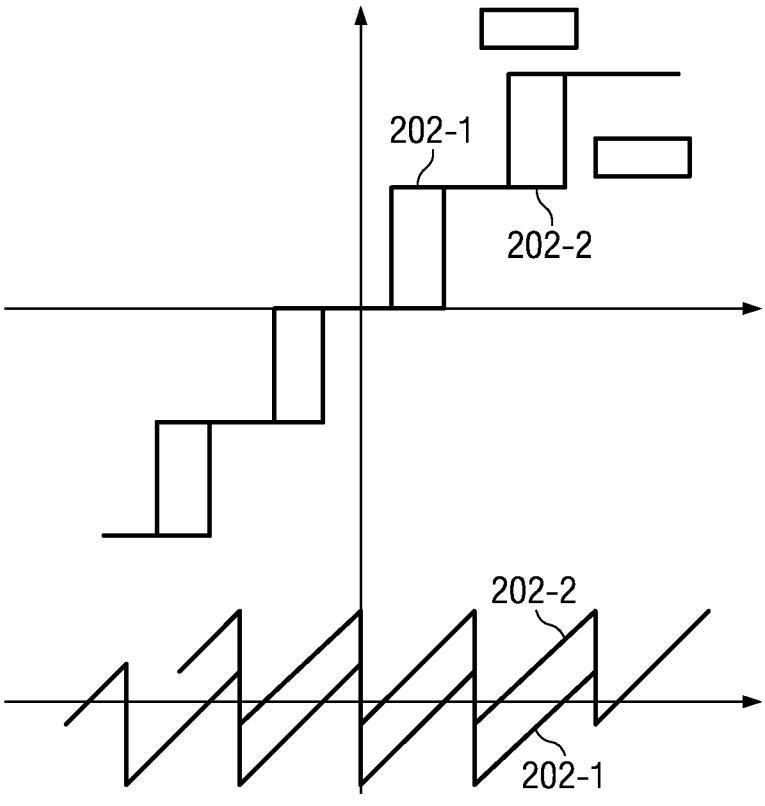

FIG. 7B

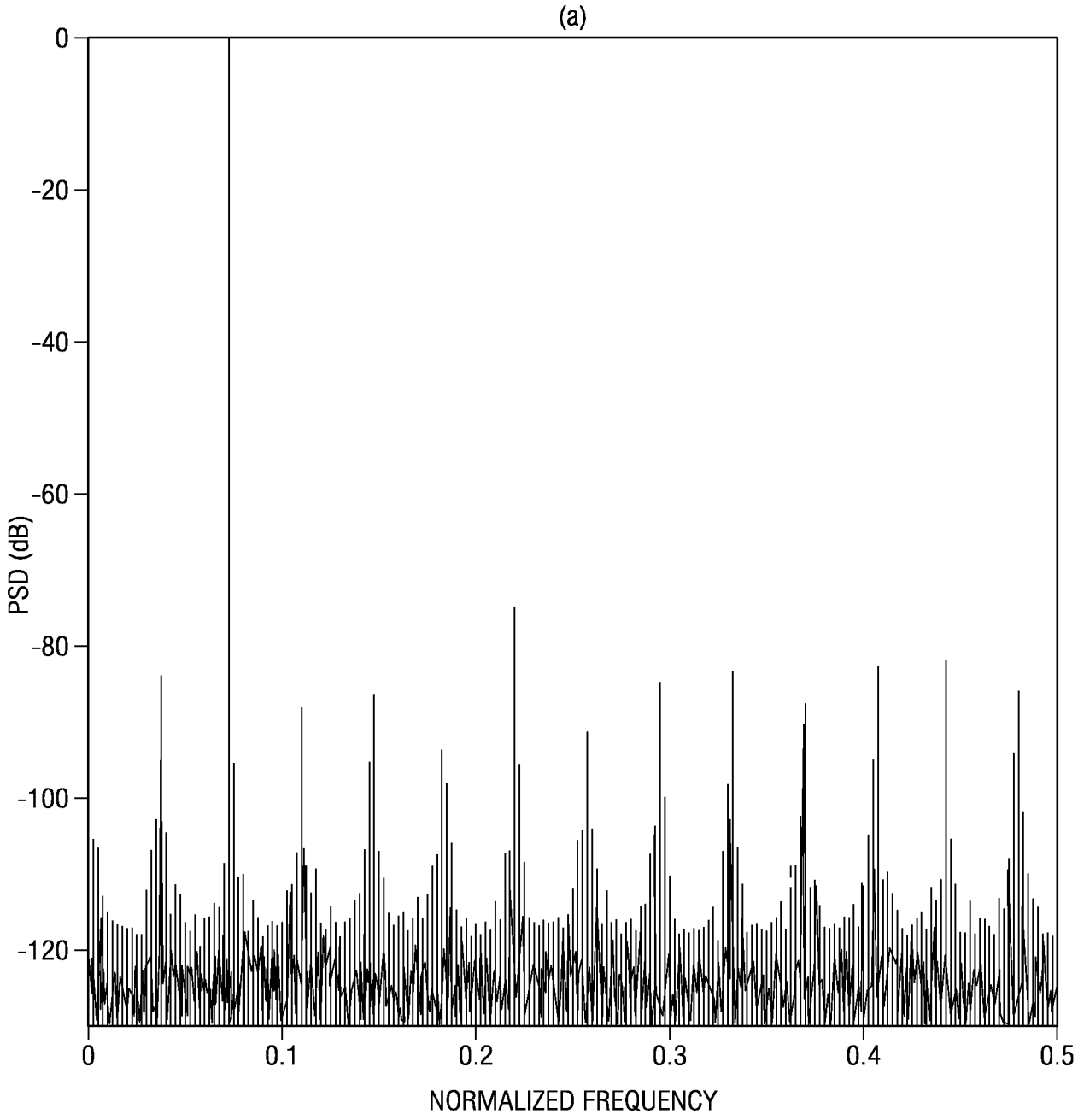
(a)
0
-20
-40
-60
-80
-100
-120
PSD (dB)
0
0.1
0.2
0.3
0.4
0.5
NORMALIZED FREQUENCY

FIG. 8A

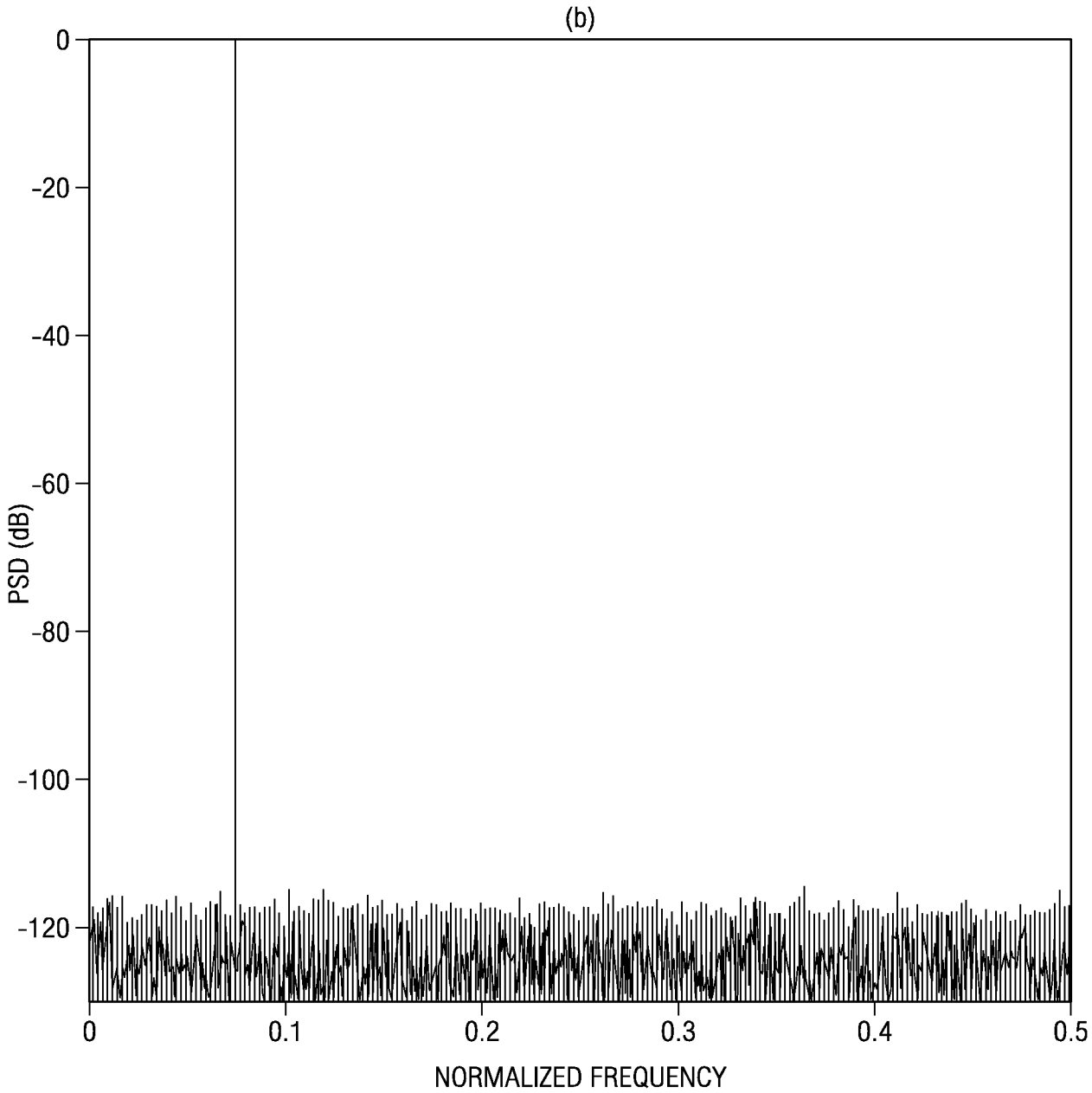
(b)
0
-20
-40
-60
-80
-100
-120
PSD (dB)
0
0.1
0.2
0.3
0.4
0.5
NORMALIZED FREQUENCY

FIG. 8B

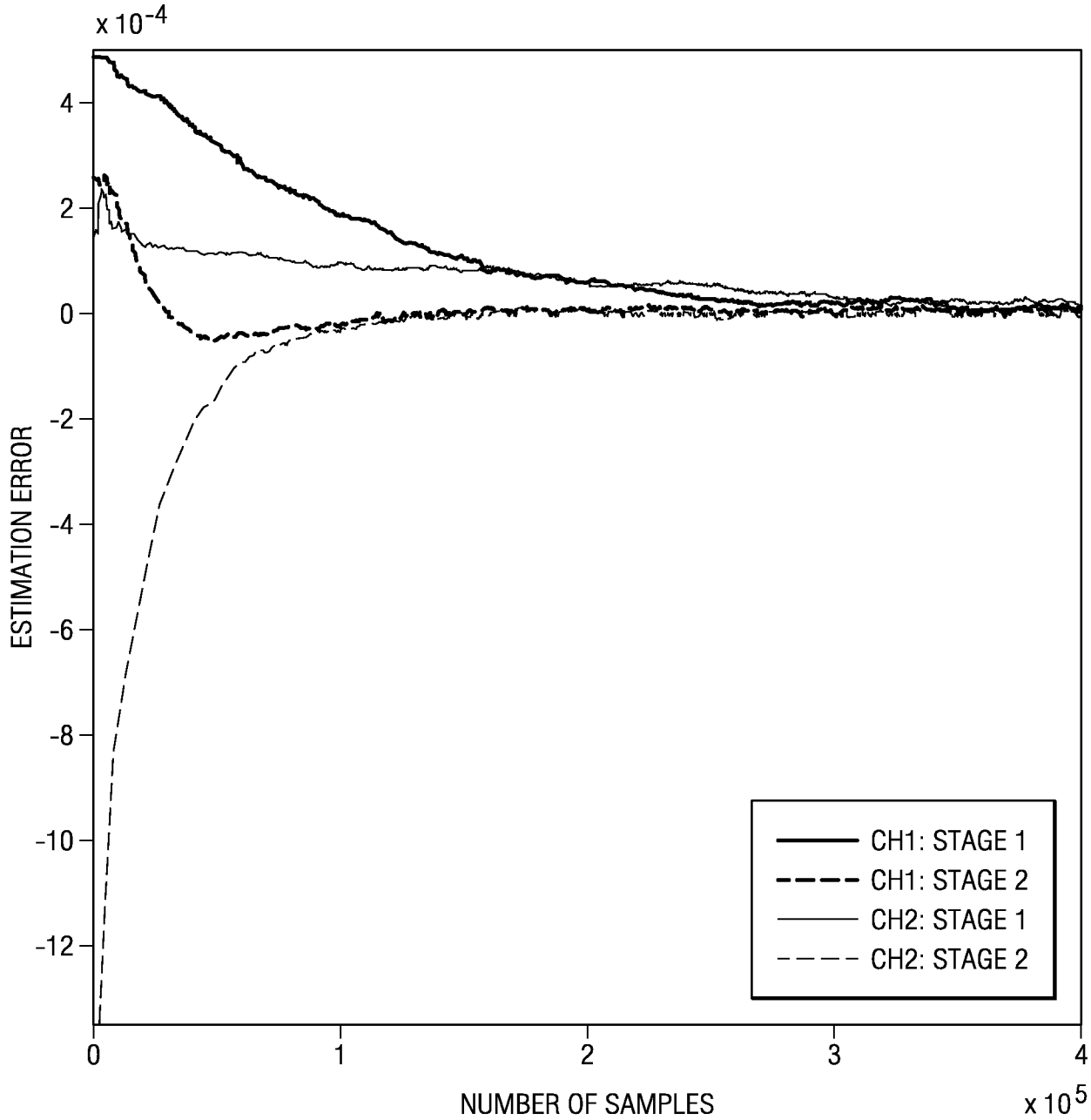
x 10-4
4
2
0
-2
-4
-6
-8
-10
-12
ESTIMATION ERROR
0
1
2
3
4
NUMBER OF SAMPLES
x 10 5
CH1: STAGE 1
CH1: STAGE 2
CH2: STAGE 1
CH2: STAGE 2

FIG. 9