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(54) **Title**: METHOD OF STACKING CHIPS

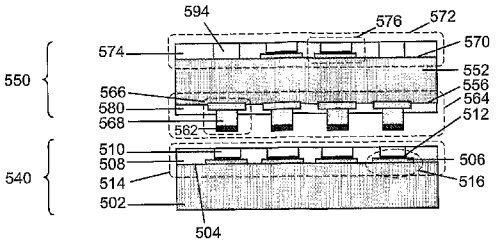


Figure 5A

(57) **Abstract**: According to an embodiment of the present invention, a method of stacking chips is provided. The method includes: providing a first substrate, wherein, on or within a surface of the first substrate, a first contact structure is arranged, wherein the first contact structure includes an intermediate layer and at least one contact for contacting the first substrate, the intermediate layer being provided on the surface of the first substrate and having at least one recess, the at least one recess accommodating or allowing access to the at least one contact; providing a second substrate, wherein on a surface of the second substrate, a second contact structure is arranged, the second contact structure having at least one contact; and inserting the second contact structure into the at least one recess of the intermediate layer.

METHOD OF STACKING CHIPS

Field

[001] The invention relates to a method of stacking chips.

Background

[002] Stacking chips is one way of making more compact chip packages.

[003] In producing packages having stacked chips, one or more chips are stacked one on top of the other, with a landing chip acting as a first base chip.

[004] One known chip stacking methodology uses a C4 (Controlled Collapse Chip Connection) bump process. Each chip is assembled in a sequential manner, thereby leading to low throughput. Moreover, a landing chip experiences multiple applications of high temperature producing solder joints with different inter-metallic composition between adjacent chips. Also, previously formed joints melt during each re-flow step, resulting in die shift and solder bridging.

[005] Another known stacking methodology stacks up_to 8 chips using a thermo-compression method. In this approach, each chip is bonded to a chip below by applying heat and pressure for a duration of around 1 minute using a low volume of solder. The solder is completely converted into intermetallic compound (IMC) by the thermo-compression bonding. The IMC does not melt during the subsequent bonding. However, this approach also uses a sequential process having a drawback of low throughput. Assuming a 3 chip stack on an 8" wafer at 200 locations, the time required is around 600 min.

[006] Another known method to create uniform joints in a stacked chip requires chips to be tacked or temporarily bonded with a landing chip. Then the chips are bonded using a wafer bonder. However, this approach requires special material such as an adhesive layer and a wafer bonder to press all the chips together and form permanent joints.

[007] There is thus a need to provide a chip stack methodology that produces uniform joints and has a high throughput.

Summary of the Invention

[008] According to an embodiment of the present invention, a method of stacking chips is provided. The method includes: providing a first substrate, wherein, on or within a surface of the first substrate, a first contact structure is arranged, wherein the

first contact structure includes an intermediate layer and at least one contact for contacting the first substrate, the intermediate layer being provided on the surface of the first substrate and having at least one recess, the at least one recess accommodating or allowing access to the at least one contact; providing a second substrate, wherein on a surface of the second substrate, a second contact structure is arranged, the second contact structure having at least one contact; and inserting the second contact structure into the at least one recess of the intermediate layer.

[009] One effect of this embodiment is that by inserting the second contact structure on the surface of the second substrate into the at least one recess in the intermediate layer on the surface of the first substrate, a mechanical interlocking arrangement is established between the first substrate and the second substrate. In stacking the second substrate onto the first substrate, the mechanical interlocking arrangement facilitates alignment of the second substrate to the first substrate, thereby minimising die shift between the first and the second substrates. When more substrates are stacked, in accordance with the method of the present invention, to produce a multiple chip stack arrangement, there is good alignment between any of the chips in the multiple chip stack arrangement due to the mechanical interlocking arrangement established between two adjacent chips. In implementing the stacking method of this embodiment of the invention, the modification required on existing chip stacking methodology does not require new materials or additional equipment. Signal / power / ground ports are routed through the chip by means of one or more through-silicon vias (TSV), edge contacts, etc.

[010] In the context of the present invention, the term "chip" may mean any type of semiconductor having electronics micro-fabricated or nano-fabricated thereon. Thus, the term "chip" may mean semiconductor substrates with integrated circuitry for purposes such as providing processing functions (such as AND, NAND, OR logic), a capacitor, an inductor or an entire system (such as being a Processor, a Memory, Radio Frequency Identification Tag). Alternatively, the term "chip" may also refer to semiconductor substrates having different layers deposited thereon from a fabrication process. The term "substrate" is meant to be understood in the context of semiconductor technology, i.e. "substrate" refers to bulk semiconductor material forming a base material for fabricating electronics thereon or therein. The term "contact structure" may refer to a structural arrangement formed on a surface of the substrate, the structural arrangement having one or more structures, wherein at least

one of the one or more structures may be a contact. The term "intermediate layer" may mean a layer that is separate to the substrate, even if the intermediate layer comprises the same material as the substrate. Preferably, the "intermediate layer" is an electrical insulating layer like a passivation layer covering the substrate, but it may also be a (partially) electrical conducting layer depending on the application of the substrate on which the intermediate layer is formed. Further, "intermediate layer" may mean a stack of different layers (intermediate sublayers). The term "contact" may mean a structure protruding from the surface of the substrate. The "contact" may be an electrical conductive structure, thereby providing electrical access to circuitry fabricated in the substrate when the contact structure is located at an input or output port of the fabricated circuitry. Alternatively, the "contact" may be an electrical insulating structure. The term "recess" may mean openings formed in the intermediate layer, the openings being of a depth that provides access to the surface of the substrate. Alternatively, the term "recess" may mean openings formed in the intermediate layer, the openings being of a depth less than the thickness of the substrate.

[011] In one embodiment, the intermediate layer on the surface of the first substrate has a plurality of recesses, while the surface of the second substrate has a plurality of second contact structures, wherein each of the plurality of recesses on the intermediate layer is adapted to receive a respective one of the plurality of second contact structures.

[012] In one embodiment of the present invention, processing of the first substrate occurs such that the contacts of the first contact structure are formed on the surface of the first substrate before the intermediate layer is formed.

[013] In another embodiment of the present invention, processing of the first substrate occurs such that the intermediate layer is formed on the surface of the first substrate, the at least one recess is formed in the intermediate layer and the at least one recess is partly filled with conductive material to form the at least one contact. Thus, the intermediate layer is first formed, followed by formation of the at least one recess in the intermediate layer and finally, formation of the at least one contact inside the at least one recess.

[014] In one embodiment of the present invention, after having inserted the second contact structure into the at least one recess of the intermediate layer, a portion of the at least one contact of the second contact structure is in contact with or proximate to

the inner walls of the at least one recess of the intermediate layer into which the at least one contact structure of the second substrate is inserted, to arrest movement between the second substrate and the first substrate.

[015] The term "proximate" may mean that there is little free play between the at least one contact of the second contact structure and its surrounding inner walls of the at least one recess of the intermediate layer. The little free play enhances the mechanical interlocking arrangement established between the first substrate and the second substrate by largely preventing die shift, i.e. movement of the second substrate relative to the first substrate, when the at least one contact of the second contact structure is inserted into the at least one recess of the intermediate layer. In one embodiment, the freeplay is in the range of from about 1um to about 10um. In another embodiment, the freeplay is in the range of from about 5um to about 10um. In another embodiment, the freeplay is in the range of from about 1um to about 20um.

[016] In one embodiment of the present invention, the at least one recess of the intermediate layer is formed such that it surrounds a portion of at least one contact of the second contact structure with a gap of from 5um to about 10um in-between.

[017] In another embodiment of the present invention, the at least one recess of the intermediate layer is formed such that it surrounds a portion of at least one contact of the second contact structure with a gap of from 1um to about 20um in-between.

[018] In embodiments of the invention, the portion of the at least one contact of the second contact structure in contact with or proximate to the inner walls of the at least one recess of the intermediate layer, or the portion of the at least one contact of the second contact structure surrounded by the at least one recess of the intermediate layer refers to the portion of the at least one contact of the second contact structure that is accommodated within the at least one recess. It will be appreciated that, in one embodiment, the at least one recess of the intermediate layer is of a depth that may only accommodate a portion of the at least one contact of the second contact structure. However, in another embodiment, the at least one recess of the intermediate layer is of a depth that may fully accommodate the at least one contact of the second contact structure.

[019] In one embodiment of the present invention, a width of the at least one recess may be around 40um, while a depth of the at least one recess may be around 10um. It will be appreciated that these dimensions are exemplary, so both the width and the

depth of the at least one recess may be any other suitable dimensions such as 80um and 15um respectively.

[020] According to one embodiment of the present invention, the intermediate layer comprises any one or more of a dielectric layer, a passivation layer or a re-distribution layer. The intermediate layer may comprise any one or more of the following electrical insulating materials: silicon dioxide, polymide, benzocyclobutene (BCB) or lead oxide (PbO). On the other hand, the intermediate layer may comprise any one or more of the following electrical conducting materials such as: aluminum, copper or nickel.

[021] The at least one contact of the second contact structure may include one or more structures. According to one embodiment of the present invention, the at least one contact of the second contact structure may include an interconnect post connected at one end to the surface of the second substrate, and a solder bump connected to an opposite end of the interconnect post. The term "interconnect post" may refer to a structure that allows one substrate to be elevated a certain height from an adjacent substrate, so that there is a gap between two adjacent chips in a stacked chip arrangement. The term "solder bump" may mean any material that melts by heating and connects the interconnect post on the second substrate and the electrical contact pad on the first substrate.

[022] In one embodiment, the cross-section of the interconnect post may be substantially uniform and have any one of the following shapes: circular, rectangular or triangular. In another embodiment, the cross-section of the interconnect post may be non-uniform. In such an embodiment, the cross-section may have a first portion and a second portion, both portions having any one of the following shapes: circular, rectangular or triangular, wherein the first portion has a different shape than the second portion. For instance, the first portion of the interconnect post may have a circular shape, while the second portion of the interconnect post may have a rectangular shape. Further, the width of the interconnect post, along with the width of its respective solder bump may be marginally smaller than the width of at least one recess of the intermediate layer of the first substrate, to form the mechanical interlocking arrangement mentioned above. In one embodiment of the invention, where a mechanical interlocking arrangement exists between the interconnect post and the at least one recess of the intermediate layer, the recess has a width that is larger than the width of the interconnect post by about 1um to 10um. In another

embodiment of the invention, where no mechanical interlocking arrangement exists between the interconnect post and the at least one recess of the intermediate layer, the recess has a width that is larger than the width of the interconnect post by about 10um to 20um.

[023] The interconnect post may have a height of around 20um. The thickness of the solder bump may be around 5um. It will be appreciated that these dimensions are exemplary, so the height of the interconnect post and the thickness of the solder bump may be any other suitable dimensions such as 30um and 10um respectively.

[024] The interconnect post may be composed of any one or more of the following materials: copper, an alloy of copper, nickel or silicon. The solder bump may be composed of any one or more of the following materials: tin, indium, bismuth or lead.

[025] The at least one contact of the first contact structure may include one or more structures. According to one embodiment of the present invention, the at least one contact of the first contact structure may include a contact pad connected, with one surface, to the surface of the first substrate; and a pad protection layer connected, to an opposite surface of the contact pad. The term "contact pad" may refer to an electrically conductive pad disposed on the surface of a substrate that serves as access to an input or output port of electronics fabricated inside a substrate. The term "contact pad" may also refer to an electrically conductive pad disposed on the surface of a substrate that serves as a dummy pad, i.e. it is not connected to an input or output port of electronics fabricated inside a substrate. Alternatively, the term "contact pad" may refer to an electrically insulating pad disposed on the surface of a substrate. The term "pad protection layer" may mean a volume of material such as tin, nickel, gold, aluminum or an organic protection layer. In embodiments of the invention, the organic protection layer is formed by dipping the substrate into an organic solution to coat the contact pad. For instance, if copper is used for the contact pad, the organic layer coat protects the contact pad from oxidising. In one embodiment, a pad protection layer may be of any suitable material and may be a solder material.

[026] It will be appreciated that a further contact pad may be placed on a surface (also known as the "backside" of the chip) opposite to the surface (also known as the "device side" of the chip) of the first substrate upon which the first contact structure is arranged. In another embodiment of the invention, the first contact structure of the first substrate may not have a contact pad, but only at least one recess in its respective intermediate layer.

[027] The contact pad may have a thickness of around 5um. The thickness of the pad protection layer may be around 4um. It will be appreciated that these dimensions are exemplary, so the thickness of the contact pad and the thickness of the pad protection layer may be any other suitable dimensions such as 10um and 2um respectively.

[028] The contact pad may include any one or more of the following materials: copper, aluminum, nickel or gold. The solder bump may include any one or more of the following materials: tin, indium, bismuth or lead.

[029] According to one embodiment of the present invention, on or within a further surface of the second substrate, a third contact structure is arranged, wherein the third contact structure includes an intermediate layer and at least one contact for contacting the second substrate. The intermediate layer is provided on the further surface of the second substrate and has at least one recess, the at least one recess accommodating or allowing access to the at least one contact. The further surface of the second substrate is opposite to the surface of the second substrate where the second contact structure is arranged. A third substrate is provided, wherein on a surface of the third substrate, a fourth contact structure is arranged, the fourth contact structure having at least one contact. The fourth contact structure is inserted into the at least one recess of the intermediate layer on the further surface of the second substrate. It will be appreciated that more substrates, such as eight to ten, may be stacked in this manner.

[030] For each chip stacked in the above manner, in one embodiment of the present invention, each contact structure on opposite surfaces of the chip substrate may have a contact pad on the respective surface (being either the "device side" or the "backside" of the chip). For each chip stacked in the above manner, in another embodiment of the invention, the respective contact structure of the chip substrate may not even have a contact pad, but only at least one recess in its respective intermediate layer.

[031] According to one embodiment of the present invention, the contacts (being in respect of either the second contact structure or the fourth contact structure) have shapes that match the shape of the recesses (formed in either the intermediate layer on the surface of the first substrate, the intermediate layer on the surface of the second substrate or an intermediate layer on a surface of a third substrate). These matching shapes enhance the mechanical interlocking arrangement established between adjacent substrates (such as the first and second substrates mentioned above).

[032] According to one embodiment of the present invention, the size of the stacked chips is around 12mm by around 12mm and a pitch between adjacent recesses of the intermediate layer is around 100um. It will be appreciated that these dimensions are exemplary, so the size of the stacked chips and the pitch between adjacent recesses of the intermediate layer may be any other suitable dimensions such as 5mm by 5mm and a pitch between adjacent recesses is 50um to 60um respectively. Other sets of suitable dimensions include chips having sizes ranging from 2mm by 2mm to 25mm by 25mm. The pitch between two adjacent recesses and another two adjacent recesses may also vary.

[033] According to one embodiment of the present invention, an initial heating process is applied to form joints between adjacent contacts. The term "joints" may refer to the adjacent contact structures or a portion of adjacent contact structures melting to form a single structure bonding adjacent chips together. The term "joints" may mean a bond formed between the interconnect post and the contact pad. In one embodiment, the joint formed from the initial heating process is a weak joint, where the shear load per joint is less than 5 grams.

[034] According to an embodiment of the present invention, the initial heating process may be conducted at a temperature of around 270°C. The initial heating process may be conducted for a duration of around 5 to 10 seconds. It will be appreciated that these parameters are exemplary, so the temperature and the duration may be any other suitable parameters such as 300°C and 2 seconds respectively.

[035] It will be appreciated that when adjacent substrates are pressed towards each other with sufficient force, the mechanical interlocking arrangement established between adjacent substrates (such as the first and second substrates mentioned above) is sufficient to prevent die shift, thereby rendering the initial heating process unnecessary.

[036] According to one embodiment of the present invention, a reflow process may be applied to form joints between adjacent contacts. It will be appreciated that the reflow process may supplement the initial heating process conducted at a temperature of around 270°C or conducted for a duration of around 5 to 10 seconds.

[037] According to another embodiment of the invention, the reflow process may be performed in a single step. The term "single step" may mean that only after a last chip is stacked, the reflow process would then be applied to form joints between adjacent contacts. In one embodiment of the invention, the joint that is formed from

the single step reflow process has a shear load per joint of more than 50grams. In a scenario where the initial heating process is not conducted, the reflow process may be the only heating process to form joints between adjacent contacts.

[038] The effect of performing the reflow process in a single step is that uniform joints are formed between adjacent contacts. In conventional chip stacking methodology, a reflow process is applied as each chip is stacked onto a previously mounted chip. Thus, a previously mounted chip (i.e. the landing wafer) undergoes repeated heating resulting in solder joints with different intermetallic compositions. Further, previously formed solder joints melt during each subsequent reflow process, leading to die shift and solder bridging. Thus, a single step reflow process avoids such repeated heating of previously mounted chips and also results in uniform joints formed between adjacent contacts. Thus, the single step reflow process facilitates batch processing, thereby improving through-put by avoiding repeated heating.

[039] In one embodiment of the present invention, the reflow process is conducted at a temperature of around 200°C. The reflow process may be conducted for a duration of around 5 minutes. It will be appreciated that these parameters are exemplary, so the temperature and the duration may be any other suitable parameters such as 260°C and 5 minutes respectively.

[040] According to one embodiment of the present invention, a stacked chip arrangement is provided. The stacked chip arrangement includes a first substrate; a first contact structure provided on a surface of the first substrate, the first contact structure having at least one contact; a second substrate; and a second contact structure provided on a surface of the second substrate, the second contact structure having at least one contact, wherein the first contact structure comprises an intermediate layer provided on the surface of the first substrate, the intermediate layer having at least one recess, the at least one recess accommodating and allowing access to the at least one contact of the first contact structure, wherein the at least one contact of the second contact structure is disposed within the at least one recess of the intermediate layer on the first substrate.

Brief Description of the Drawings

[041] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the

following description, various embodiments of the invention are described with reference to the following drawings, in which:

[042] Figure 1 shows a flow chart illustrating a method, according to one embodiment of the present invention, of stacking chips.

[043] Figures 2A to 2D show cross-sectional views illustrating steps of manufacturing a landing chip.

[044] Figures 3A to 3D show cross-sectional views illustrating steps of manufacturing a landing chip.

[045] Figures 4A to 4H show cross-sectional views illustrating steps of manufacturing a chip.

[046] Figures 5A to 5C show cross-sectional views illustrating steps of manufacturing a stacked chip using a method, in accordance to one embodiment of the invention.

[047] Figure 6A shows a cross-sectional view of a stacked chip arrangement built from a method, according to one embodiment of the present invention.

[048] Figure 6B shows a picture of a top view of a stacked chip arrangement built from a method, according to one embodiment of the present invention.

[049] Figure 7A shows a picture of a top view of a stacked chip arrangement built from a method, according to one embodiment of the present invention.

[050] Figure 7B shows a cross-sectional view of a stacked chip arrangement built from a method, according to one embodiment of the present invention.

[051] Figure 8 shows a picture of a cross-sectional view of an assembled sample.

[052] Figure 9 shows a picture of a cross-sectional view of a solder joint for a test chip.

[053] Figure 10A shows a picture of a cross-sectional view of a joint between a chip and a landing chip.

[054] Figure 10B shows a picture of a cross-sectional view of a joint between two chips.

[055] Figure 11A shows pictures of cross-sectional views of a joint between a chip and a landing chip.

[056] Figure 11B shows pictures of cross-sectional views of a joint between two chips.

Description

[057] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the invention. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

[058] Figure 1 shows a flow chart 100 illustrating a method, according to one embodiment of the present invention, of stacking chips.

[059] The method includes three steps 102, 104 and 106.

[060] In step 102, a first substrate is provided, wherein, on or within a surface of the first substrate, a first contact structure is arranged. The first contact structure includes an intermediate layer and at least one contact for contacting the first substrate, the intermediate layer being provided on the surface of the first substrate and having at least one recess. The at least one recess accommodates or allows access to the at least one contact.

[061] In step 104, a second substrate is provided, wherein on a surface of the second substrate, a second contact structure is arranged, the second contact structure having at least one contact.

[062] In step 106, the second contact structure is inserted into the at least one recess of the intermediate layer.

[063] Figures 2A to 2D show cross-sectional views illustrating steps of manufacturing a landing chip, the landing chip being subsequently used in a fabrication method in accordance to one embodiment of the invention. In the manufacturing steps shown in Figures 2A to 2D and with reference to step 102 of Figure 1, the contacts of the first contact structure are formed on the surface of the first substrate before the intermediate layer is formed. Further, it will be appreciated that, for the sake of simplicity, Figures 2A to 2D only show cross-sectional views depicting the formation of one contact and its surrounding intermediate layer.

[064] In Figure 2A, a first substrate 202 is provided. The first substrate 202 may comprise any one or more of the following materials such as silicon, gallium arsenide, bulk silicon or a silicon-germanium mixture.

[065] From Figure 2A, a layer (not shown) of material used for a contact pad is deposited onto a surface 204 of the first substrate 202. A patterned mask (not shown) is then placed onto the layer of material. The unmasked portion is subsequently etched away using a suitable reagent and the patterned mask washed away using a suitable reagent, thereby leaving behind a contact pad 206 formed on the surface 204 of the first substrate 202, as shown in Figure 2B.

[066] From Figure 2B, material (not shown) used for an intermediate layer may be deposited over the contact pad 206 and the surface 204 of the first substrate 202. A mask (not shown) patterned with a recess arrangement is located on the deposited material for the intermediate layer. The unmasked portion is subsequently etched away using a suitable reagent and the patterned mask washed away using a suitable reagent, thereby leaving behind the contact pad 206 and an intermediate layer 208 with a recess 210, as seen in Figure 2C. The recess 210 allows access to the contact pad 206. The mask is patterned such that a portion of the contact pad 206 formed is covered by a portion of the intermediate layer 208.

[067] From Figure 2C, tin, indium, aluminium, nickel (Ni), gold (Au) or any other suitable material (not shown) is deposited over the contact pad 206 by means of electoplating, electroless plating, physical vapour depostion, evaporation as seen in Figure 2D. The pad protection layer 212 and the contact pad 206 together have a height that is less than the height of the intermediate layer 208. From Figure 2D, a first contact structure 214 includes the intermediate layer 208 and a contact 216 for contacting the first substrate 202. The contact 216 includes the contact pad 206 and the pad protection layer 212. The intermediate layer 208 is provided on the surface 204 of the first substrate 202 and has the recess 210, the recess 210 accommodating or allowing access to the contact 216. The contact pad 206 is connected with one surface 206a, to the surface 204 of the first substrate 202; and the pad protection layer 212 is connected, to an opposite surface 206b of the contact pad 206. The resulting structure shown in Figure 2D is a landing chip 240 upon which a chip (not shown) may be mounted thereto.

[068] Figures 3A to 3D show cross-sectional views illustrating steps of manufacturing a landing chip, the landing chip being subsequently used in a fabrication method in accordance to one embodiment of the invention. In the manufacturing steps shown in Figures 3A to 3D and with reference to step 102 of Figure 1, processing of a first substrate occurs such that an intermediate layer is

formed on the surface of the first substrate (Figure 3B), a recess is formed in the intermediate layer (Figure 3C) and the recess is partly filled with conductive material to form the at least one contact (Figure 3D). In other words, the intermediate layer is first formed, followed by formation of a recess in the intermediate layer and finally, formation of at least one contact inside the at least one recess. It will be appreciated that, for the sake of simplicity, Figures 3A to 3D only show cross-sectional views depicting the formation of one contact and its surrounding intermediate layer.

[069] In Figure 3A, a first substrate 302 is provided. The first substrate 302 may comprise any one or more of the following materials such as silicon, gallium arsenide, bulk silicon or a silicon-germanium mixture.

[070] In Figure 3B, an intermediate layer 308 is formed on a surface 304 of the first substrate 302. The intermediate layer 308 may for example be deposited on the surface 304 through chemical vapour deposition, spin coating, and lamination.

[071] From Figure 3B, a mask (not shown) patterned with a recess arrangement is located on the intermediate layer 308. The unmasked portion is subsequently etched away using a suitable reagent and the patterned mask washed away using a suitable reagent, thereby leaving behind the intermediate layer 308 with a recess 310, as shown in Figure 3C.

[072] From Figure 3C, the recess 310 is partly filled, using a trench filling process, with material and an etching process performed to form a contact pad 306 (see Figure 3D).

[073] Comparing the contact pad 306 formed in Figure 3D with the contact pad 206 formed in Figure 2D, Figure 3D shows that the intermediate layer 308 does not cover the contact pad 306. The edges of the contact pad 306 are surrounded by an inner wall of the recess 310.

[074] Pad protection material (not shown) is deposited over the contact pad 306 and the intermediate layer 308. The pad protection layer 312 is disposed within the recess 310, as shown in Figure 3D. The pad protection layer 312 on the contact pad 306 together have a height that is less than the height of the intermediate layer 308.

[075] From Figure 3D, a first contact structure 314 includes the intermediate layer 308 and a contact 316 for contacting the first substrate 302. The contact 316 includes the contact pad 306 and the pad protection layer 312. The intermediate layer 308 is provided on the surface 304 of the first substrate 302 and has the recess 310, the recess 310 accommodating or allowing access to the contact 316. The contact pad

306 is connected with one surface 306a, to the surface 304 of the first substrate 302; and the pad protection layer 312 is connected, to an opposite surface 306b of the contact pad 306. The resulting structure shown in Figure 3D is a landing chip 340 upon which a chip (not shown) may be mounted thereto.

[076] Figures 4A to 4H show cross-sectional views illustrating steps of manufacturing a chip, the chip being subsequently used in a fabrication method in accordance to one embodiment of the invention (such as to mount on the landing chip 240 or 340 shown in Figures 2D and 3D respectively). It will be appreciated that, for the sake of simplicity, Figures 4A to 4H only show cross-sectional views depicting the formation of one contact and its encapsulation resin.

[077] In Figure 4A, a second substrate 452 is provided. The second substrate 452 may comprise any one or more of the following materials such as silicon, gallium arsenide, bulk silicon or a silicon-germanium mixture.

[078] A seed layer 454 is deposited on a surface 456 of a second substrate 452. The seed layer 454 is deposited by processes which include electroplating or electroless plating physical vapor deposition. Examples of the seed layer 454 include but are not limited to conductive materials or a combination of conductive materials like Titanium (Ti)/Gold (Au), Ti/Cu, Ti-alloy/Au, Ti-alloy/Cu, Ti/ Ni, Ti-alloy/Ni, Cr/Au, Cr/Cu or Cr/Ni.

[079] After depositing the seed layer 454 on the second substrate 452, a layer of photosensitive dry film 453 is applied to a surface of the seed layer 454 as shown in Figure 4B. The layer of dry film 453 is preformed or cut to the desired shape before being hot-roll laminated onto the surface of the seed layer 454. The layer of dry film 453 is photosensitive, meaning that it is a material that experiences a change in its physical properties when exposed to a radiation source. The dry film includes any commercially available dry film. Examples include Ashai Sunfort dry film and Dupont dry film. The average thickness of the dry film is typically between about 20um to about 50 μm or about 60 um to about 100 μm.

[080] Referring next to Figure 4C, the dry film 453 is processed so as to expose a portion 458 of the seed layer 454 via a through-hole 414 in the dry film 453. A mask (not shown) with a designated pattern is applied or aligned to the second substrate 452. Various designated areas of the photosensitive dry film 453 are exposed to radiation and the areas that are exposed to radiation are developed or removed to

expose the portion 458 of the seed layer 454 via the through-hole 414 in the dry film 453. The radiation includes ultra-violet radiation or optical radiation.

[081] The through-hole 414 is subsequently filled with conductive material 460 by electroplating as shown in Figure 4D.

[082] After deposition of the conductive material 460, a solder bump 462 is formed or deposited on the top surface of the conductive material 460 by a process which includes electroplating as shown in Figure 4E.

[083] The dry film 453 is removed or stripped from the seed layer 454 as shown in Figure 4F. Stripping involves immersing the structure containing the dry film in a heated solution of sodium hydroxide and agitating the sodium hydroxide until the dry film 453 lifts off from the seed layer 454.

[084] After removal of the dry film 453, a portion of the seed layer 454 is etched away as shown in Figure 4G. The etching may be a dry etch or a wet etch.

[085] In Figure 4H, an encapsulation resin 480 is formed, using a transfer molding method, on the surface 456 of the second substrate 452. In one embodiment, the encapsulation resin 480 is typically underfill material manufactured by Namics, Henkel. In another embodiment, another suitable material may be used for the encapsulation resin 480. The resulting structure shown in Figure 4H is a chip 450 which may be mounted onto a landing chip (not shown).

[086] From Figure 4H, the resulting seed layer 454 and the conductive material 460 form an interconnect post 468. The interconnect post 468 is connected at one end 468f to the surface 456 of the second substrate 452 and the solder bump 462 is connected to an opposite end 468 of the interconnect post 468. On the surface 456 of the second substrate 452, a second contact structure 464 is formed, the second contact structure 464 including the encapsulation resin 480 and a contact 466. The contact 466 of the second contact structure 464 includes the interconnect post 468 and the solder bump 462.

[087] It will be appreciated that the interconnect post 468 may be formed from using a photoresist process (not shown) instead of the photosensitive dry film process shown in Figures 4B to 4H. Referring to Figure 4A, a photoresist may be deposited by a spin coating process onto the seed layer 454.

[088] The manufacturing steps shown in Figures 2A to 2D, 3A to 3D and 4A to 4H are part of known fabrication procedures used in manufacturing stacked chips. For instance, conventional spin-on deposition and lamination techniques may be used.

Thus, it will be appreciated that in manufacturing chips that are to be subsequently used in a fabrication method in accordance to one embodiment of the invention, no new process steps, no customised masks, no customised equipment or no customised material are required. The above processes use standard wafer level re-distribution processes.

[089] Figures 5A to 5C show cross-sectional views illustrating steps of manufacturing a stacked chip using a method, in accordance to one embodiment of the invention. The manufacturing steps may be performed by conventional package assembly tools, such as the "Suss-Microtec FC150". It will be appreciated that the manufacturing steps can be used to produce 3D chip packages that are used in hand held portable products. Further, the manufacturing steps may also be used to produce chips used for memory module applications. Also, the manufacturing steps may be used to stack chips of different sizes.

[090] In Figure 5A, a first chip 540 and a second chip 550 are provided.

[091] The first chip 540 has a first substrate 502, wherein, on or within a surface 504 of the first substrate 502, a first contact structure 514 is arranged. The first contact structure 514 includes an intermediate layer 508 and at least one contact 516 for contacting the first substrate 502, the intermediate layer 508 being provided on the surface 504 of the first substrate 502 and having at least one recess 510. The at least one recess 510 accommodates or allows access to the at least one contact 516. The contact 516 includes a contact pad 506 and a pad protection layer 512.

[092] The second chip 550 has a second substrate 552, wherein on a surface 556 of the second substrate 552, a second contact structure 564 is arranged. The second contact structure 564 has at least one contact 566 and an encapsulation resin 580. The contact 566 includes an interconnect post 568 and a solder bump 562.

[093] On or within a further surface 570 of the second substrate 552, a third contact structure 572 is arranged. The third contact structure 572 includes an intermediate layer 574 and at least one contact 576 for contacting the second substrate 552. The intermediate layer 574 is provided on the further surface 570 of the second substrate 552 and has at least one recess 594, the at least one recess 594 accommodating or allowing access to the at least one contact 576. The further surface 570 of the second substrate 552 is opposite to the surface 556 of the second substrate 552 where the second contact structure 564 is arranged.

[094] During a pick and place operation, the second chip 550 is positioned over the first chip 540 so that each of the contacts 566 of the second contact structure 564 is aligned with a respective one of the at least one recess 510 of the intermediate layer 508 provided on the surface 504 of the first substrate 502. After alignment, the second chip 550 is pressed onto the first chip 540, whereby the second contact structure 564 is inserted into the at least one recess 510 of the intermediate layer 508, as shown in Figure 5B.

[095] After inserting the second contact structure 564 into the at least one recess 510 of the intermediate layer 508, a portion of the at least one contact 566 of the second contact structure 564 is in contact with or proximate to the inner walls of the at least one recess 510 of the intermediate layer 508 into which the at least one contact structure 564 of the second substrate 552 is inserted, to arrest movement between the second substrate 552 and the first substrate 502.

[096] The proximity or contact between the inner walls of the at least one recess 510 and the portion of the at least one contact 566 of the second contact structure 564 provides little free play between the contact 566 and the inner walls of the at least one recess 510, establishing a mechanical interlocking arrangement between the first chip 540 and the second chip 550. In stacking the second chip 550 onto the first chip 540, the mechanical interlocking arrangement facilitates alignment of the second chip 550 to the first chip 540, thereby minimising die shift between the first and the second chips 540 and 550. In this embodiment of the invention, the recess 510 of the intermediate layer 508 is formed such that it surrounds a portion of at least one contact 566 of the second contact structure 564 with a gap of from about 1um to about 10um in-between. These close dimensions help to avoid die shift, especially when more chips are stacked, in accordance with the method of the present invention, to produce a multiple chip stack arrangement. There will be good alignment between any of the chips in the multiple chip stack arrangement due to the mechanical interlocking arrangement established between two adjacent chips.

[097] According to one embodiment of the present invention, the insertion of the second contact structure 564 into the at least one recess 510 of the intermediate layer 508 may be followed by an initial heating process to form joints between adjacent contacts, i.e. the contact 566 of the second contact structure 564 and the contact 516 of the first contact structure 514. The initial heating process may be conducted at a temperature of around 270°C and for a duration of around 2 to 10 seconds. In this

initial heating process, the solder bump 562 melts and forms a joint with the contact pad 506 that enhances the mechanical interlocking arrangement that is already established between the first chip 540 and the second chip 550. In this manner, a joint is formed between the interconnect post 508 and the contact pad 506. The initial heating process may not be necessary, as the mechanical interlocking arrangement established between the first and the second chips 540 and 550 may be sufficient to prevent die shift.

[098] Figure 5B also shows that a third chip 582 is mounted onto the second chip 550. The third chip 582 includes a third substrate 584. On a surface 586 of the third substrate 584, a fourth contact structure 588 is arranged, the fourth contact structure 588 having at least one contact 590. The fourth contact structure 588 is inserted into the at least one recess 594 of the intermediate layer 574 on the further surface 570 of the second substrate 552.

[099] Similar to the insertion of the second contact structure 564 into the at least one recess 510 of the intermediate layer 508, the insertion of the fourth contact structure 588 into the at least one recess 594 of the intermediate layer 574 may be followed by another heating process to form joints between adjacent contacts. The heating process may be conducted at a temperature of around 270°C and for a duration of around 2 to 10 seconds.

[0100] If the third chip 582 is the last chip to be mounted, a reflow process shown in Figure 5C may be applied to form joints between all adjacent contacts (566 and 516; 590 and 576). Given that the reflow process is only performed once, the reflow process is a single step operation. In a scenario where a heating process is not conducted after each previous chip is mounted, the reflow process may be the only heating process to form joints between adjacent contacts (566 and 516; 590 and 576).

[0101] The effect of performing the reflow process in a single step is that uniform joints are formed between adjacent contacts (566 and 516; 590 and 576). In conventional chip stacking methodology, a reflow process is applied as each chip is stacked onto a previously mounted chip. Thus, a previously mounted chip (i.e. the landing wafer) undergoes repeated heating resulting in solder joints with different intermetallic compositions. Further, previously formed solder joints melt during each subsequent reflow process, leading to die shift and solder bridging. Thus, a single step reflow process avoids such repeated heating of previously mounted chips and also results in uniform joints formed between adjacent contacts.

[0102] The single step reflow process causes a joint to be formed between the interconnect post 508 and the contact pad 506. In one embodiment of the present invention, the reflow process is conducted at a temperature of around 260°C. The reflow process may be conducted for a duration of around 5 minutes.

[0103] It has been found that stacking three chips (540, 550 and 582) as shown in Figures 5A to 5C on an 8" wafer at 200 locations requires around 33 minutes. Such a throughput represents a significant improvement over a known stacking methodology which requires around 600 minutes.

[0104] The resulting structure shown in Figure 5C is a stacked chip arrangement 592. The stacked chip arrangement 592 includes a first substrate 502 and a second substrate 552. The first substrate 502 includes a first contact structure 514 provided on a surface 504 of the first substrate 502. The first contact structure 514 has at least one contact 516. The second substrate 552 includes a second contact structure 564 provided on a surface 556 of the second substrate 552. The second contact structure 564 has at least one contact 566. The first contact structure 514 includes an intermediate layer 508 provided on the surface 504 of the first substrate 502, the intermediate layer 508 having at least one recess 510, the at least one recess 510 accommodating and allowing access to the at least one contact 516 of the first contact structure 514. The at least one contact 566 of the second contact structure 564 is disposed within the at least one recess 510 of the intermediate layer 508 on the first substrate 502.

[0105] The stacked chip arrangement 592 further includes a third substrate 584. On a surface 586 of the third substrate 584, a fourth contact structure 588 is arranged, the fourth contact structure 588 having at least one contact 590. The fourth contact structure 588 is inserted into the at least one recess 594 of the intermediate layer 574 on the further surface 570 of the second substrate 552.

[0106] According to one embodiment of the present invention, the size of the stacked chips is around 12mm by around 12mm and a pitch between adjacent recesses of the intermediate layer is around 100um.

[0107] According to one embodiment of the present invention, the contacts 566 and 590 (being in respect of the second contact structure 564 and the fourth contact structure 588 respectively) have shapes that match the shape of the recesses 510 and 594 (formed in the intermediate layer 508 on the surface of the first substrate 502 and the intermediate layer 574 on the further surface of the second substrate 552). These

matching shapes enhance the mechanical interlocking arrangement established between adjacent chips (namely between the first chip 540 and the second chip 550; and between the second chip 550 and the third chip 582).

[0108] According to one embodiment of the present invention, each chip may have an area of around 12mm by around 12mm. A pitch between adjacent recesses of the intermediate layer (508, 574) may be around 100um.

[0109] Notwithstanding the materials, along with their respective parameters, presented thus far to fabricate a stacked chip arrangement using methods in accordance to embodiments of the invention, a stacked chip arrangement built in accordance to the invention may be composed of the following materials and have the following respective parameters.

[0110] A width of an at least one recess may be around 40um, while a depth of the at least one recess may be around 10um.

[0111] An intermediate layer may include any one or more of a dielectric layer, a passivation layer or a re-distribution layer, whereby the intermediate layer may comprise any one or more of the following electrical insulating materials: silicon dioxide, polymide, benzocyclobutene (BCB) or lead oxide (PbO). Alternatively, the intermediate layer may comprise any one or more of the following electrical conducting materials such as: copper, aluminum or nickel.

[0112] An interconnect post may have a height of around 20um.

[0113] A contact pad may have a thickness of around 5um. The contact pad may include any one or more of the following materials: copper, aluminum, nickel or gold.

[0114] The thickness of a solder bump may be around 5um.

[0115] The thickness of a pad protection layer may be around 4um.

[0116] The solder bump may include any one or more of the following materials: tin, indium, bismuth or lead. The pad protection layer may include any one or more of the following materials such as tin, nickel, gold, aluminum or an organic protection layer.

Experimental results

[0117] Figure 6A shows a cross-sectional view 602, taken along a location 606 (see Figure 6B) of a stacked chip arrangement 604 (see Figure 6B) built from a method, according to one embodiment of the present invention. Figure 6B shows a picture of a top view of the stacked chip arrangement 604.

[0118] Figure 7A shows a picture of a top view of a stacked chip arrangement 704 built from a method, according to one embodiment of the present invention. Figure 7B shows a cross-sectional view 702, taken along a location 706 (see Figure 7A) of the stacked chip arrangement 704 (see Figure 7A).

[0119] Figures 6A, 6B, 7A and 7B show that a 2 corner (i.e. [for Figure 6B] having locking structures placed at diagonal locations 606 and 612; [for Figure 7A] having locking structures placed at diagonal locations 706 and 712) and a 4 corner design (i.e. having locking structures at all four corners of the chip 604 [see Figure 6B] and 704 [see Figure 6B]) have good results. While at each location 606 and 706, a plurality of matching bump and recess pairs 608 are shown, it has been found that 25 of such pairs 608 is sufficient to produce good alignment when stacking chips. It was also found that a 10um oversize recesses (610, 710) show better results when compared to 5um and 15um oversize recesses (610, 710).

[0120] The assembly process steps, such as chip pick-up, alignment and stacking of multiple chips were studied using high-speed video imaging. Little die shift was observed during bonding and bond head release stages of the flip-chip bonding. Three chips were stacked one over the other and permanent joints were formed by subjecting the chips to a re-flow process in a five–zone convection re-flow oven. A picture of a cross-sectional view of the assembled sample is shown in Figure 8, where it can be observed that good joint formation exists in all the stack of three chips.

[0121] Electrical continuity of the solder joints was tested and found to be good (electrical resistance / joint is $< 10\ m\Omega$). Figure 9 shows a picture of a cross-sectional view of a solder joint for a test chip.

[0122] With reference to the assembled sample shown in Figure 8, the micro-joints of the first, second and third chip were analyzed to track the re-flow condition. It was found that most of the solder converted into inter-metallic compound. Pictures of the inter-metallic compound that was formed is shown in Figures 12A, 12B, 13A and 13B.

[0123] Figure 10A shows a picture of a cross-sectional view of a joint between chip 1 and landing chip, both from Figure 9; and a summary of the results of elemental composition analysis performed by EDX.

[0124] Figure 10B shows a picture of a cross-sectional view of a joint between chip 3 and chip 2, both from Figure 9; and a summary of the results of elemental composition analysis performed by EDX.

[0125] Figure 11A shows pictures of cross-sectional views of a joint between chip 1 and landing chip, both from Figure 9.

[0126] Figure 11B shows pictures of cross-sectional views of a joint between chip 3 and chip 2, both from Figure 8.

[0127] From Figures 10A, 10B, 11A and 11B, it can be observed that joints with good uniformity were achieved in the stacked chip assembly.

[0128] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

CLAIMS

1. A method of stacking chips, the method comprising:

providing a first substrate, wherein, on or within a surface of the first substrate, a first contact structure is arranged, wherein the first contact structure comprises an intermediate layer and at least one contact for contacting the first substrate, the intermediate layer being provided on the surface of the first substrate and having at least one recess, the at least one recess accommodating or allowing access to the at least one contact;

providing a second substrate, wherein on a surface of the second substrate, a second contact structure is arranged, the second contact structure having at least one contact; and

inserting the second contact structure into the at least one recess of the intermediate layer.

2. The method of claim 1, wherein the contacts of the first contact structure are formed on the surface of the first substrate before the intermediate layer is formed.

3. The method of claim 1, wherein the intermediate layer is formed on the surface of the first substrate, the at least one recess is formed in the intermediate layer and the at least one recess is partly filled with conductive material to form the at least one contact.

4. The method of claims 1 to 3, wherein, after having inserted the second contact structure into the at least one recess of the intermediate layer, a portion of the at least one contact of the second contact structure is in contact with or proximate to the inner walls of the at least one recess of the intermediate layer into which the at least one contact structure of the second substrate is inserted, to arrest movement between the second substrate and the first substrate.

5. The method of any one of the preceding claims, wherein the at least one recess of the intermediate layer is formed such that it surrounds a portion of the at least one contact of the second contact structure with a gap of from about to about 10um in-between.

6. The method of any one of the preceding claims, wherein a width of the at least one recess is around 40um.

7. The method of any one of the preceding claims, wherein a depth of the at least one recess is around 10um.

8. The method of any one of the preceding claims, wherein the intermediate layer comprises any one or more of a dielectric layer, a passivation layer or a re-distribution layer.

9. The method of any one of the preceding claims, wherein the intermediate layer comprises any one or more of the following materials: silicon dioxide, polymide, benzocyclobutene (BCB) or lead oxide (PbO).

10. The method of any one of the preceding claims, wherein the at least one contact of the second contact structure comprises an interconnect post connected at one end to the surface of the second substrate, and a solder bump connected to an opposite end of the interconnect post.

11. The method of claim 10, wherein the interconnect post has a height of around 20um.

12. The method of claims 10 or 11, wherein the thickness of the solder bump is around 5um.

13. The method of claims 10 to 12, wherein the interconnect post comprises any one or more of the following materials: copper, an alloy of copper, nickel or silicon.

14. The method of claims 10 to 13, wherein the solder bump comprises any one or more of the following materials: tin, indium, bismuth or lead.

15. The method of any one of the preceding claims, wherein the at least one contact of the first contact structure further comprises a contact pad connected, with

one surface, to the surface of the first substrate; and a pad protection layer connected, to an opposite surface of the contact pad.

16. The method of claim 15, wherein the intermediate layer covers a portion of the opposite surface of the contact pad and wherein the pad protection layer is disposed within the at least one recess of the intermediate layer.

17. The method of claim 16, wherein the contact pad has a thickness of around 5um.

18. The method of claims 15 to 17, wherein the thickness of the pad protection layer is around 4um

19. The method of claims 15 to 18, wherein the contact pad comprises any one or more of the following materials: copper, aluminum, nickel or gold.

20. The method of claims 15 to 19, wherein the solder bump comprises any one or more of the following materials: tin, indium, bismuth or lead.

21. The method of any one of the preceding claims, wherein

on or within a further surface of the second substrate, a third contact structure is arranged, wherein the third contact structure comprises an intermediate layer and at least one contact for contacting the second substrate, the intermediate layer being provided on the further surface of the second substrate and having at least one recess, the at least one recess accommodating or allowing access to the at least one contact, the further surface of the second substrate being opposite to the surface of the second substrate where the second contact structure is arranged;

providing a third substrate, wherein on a surface of the third substrate, a fourth contact structure is arranged, the fourth contact structure having at least one contact; and

inserting the fourth contact structure into the at least one recess of the intermediate layer on the further surface of the second substrate.

22. The method of any one of the preceding claims, wherein an area of the stacked chips is around 12mm by around 12mm and a pitch between adjacent recesses of the intermediate layer is around 100um.

23. The method of any one of the preceding claims, further comprising applying an initial heating process to form joints between adjacent contacts.

24. The method of claim 23, wherein the initial heating process is conducted at a temperature of around 270°C.

25. The method of claim 23, wherein the initial heating process is conducted for a duration of around 5 to 10 seconds.

26. The method of any one of the preceding claims, further comprising applying a reflow process to form joints between adjacent contacts.

27. The method of claim 26, wherein the reflow process is performed in a single step.

28. The method of claims 26 or 27, wherein the reflow process is conducted at a temperature of around 260°C.

29. The method of claims 26 or 27, wherein the reflow process is conducted for a duration of around 5 minutes.

30. A stacked chip arrangement comprising

a first substrate;

a first contact structure provided on a surface of the first substrate, the first contact structure having at least one contact;

a second substrate; and

a second contact structure provided on a surface of the second substrate, the second contact structure having at least one contact,

wherein the first contact structure comprises an intermediate layer provided on the surface of the first substrate, the intermediate layer having at least one recess, the

at least one recess accommodating and allowing access to the at least one contact of the first contact structure, wherein the at least one contact of the second contact structure is disposed within the at least one recess of the intermediate layer on the first substrate.

5

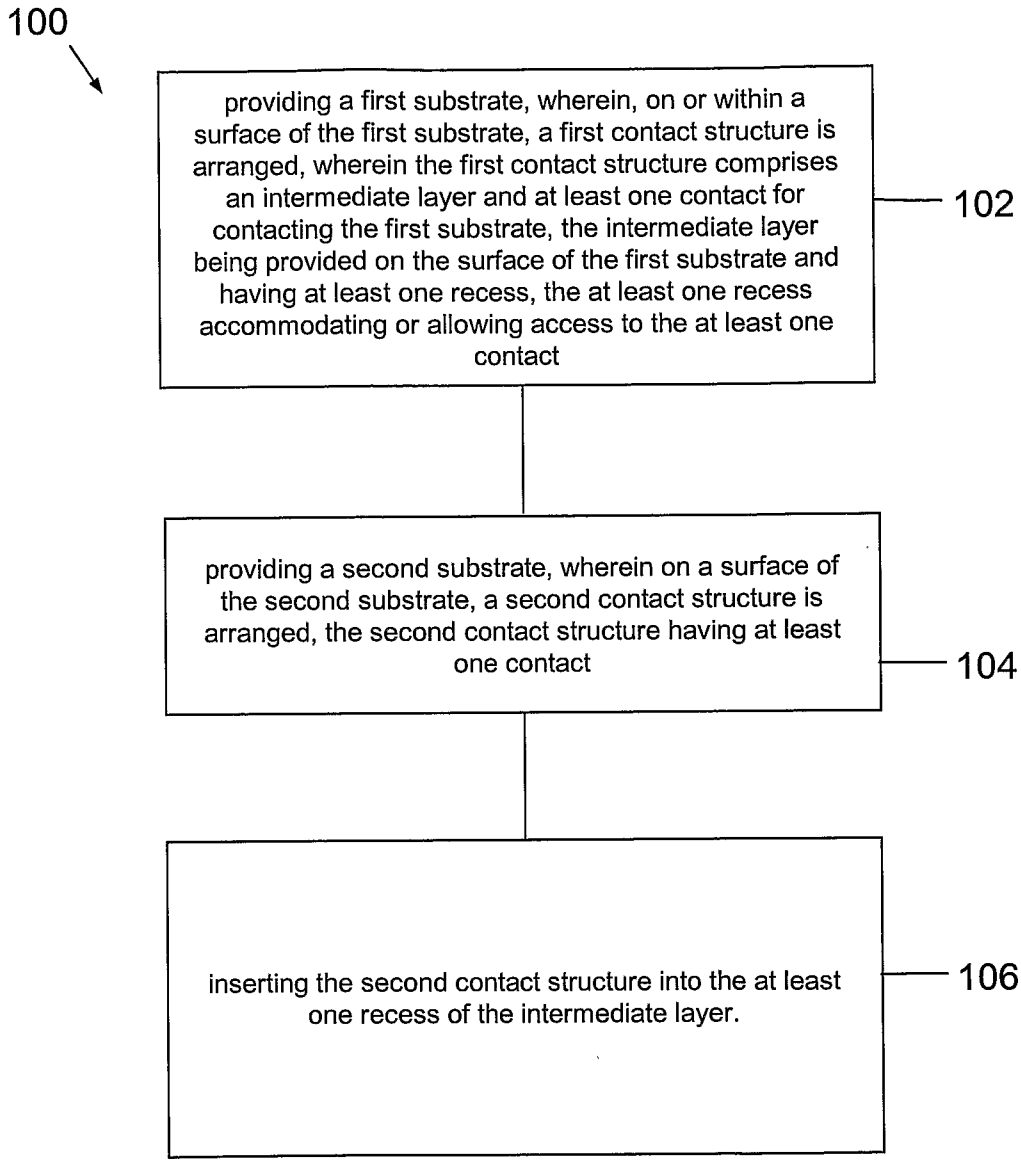

100
providing a first substrate, wherein, on or within a surface of the first substrate, a first contact structure is arranged, wherein the first contact structure comprises an intermediate layer and at least one contact for contacting the first substrate, the intermediate layer being provided on the surface of the first substrate and having at least one recess, the at least one recess accommodating or allowing access to the at least one contact
102
providing a second substrate, wherein on a surface of the second substrate, a second contact structure is arranged, the second contact structure having at least one contact
104
inserting the second contact structure into the at least one recess of the intermediate layer.
106

Figure 1

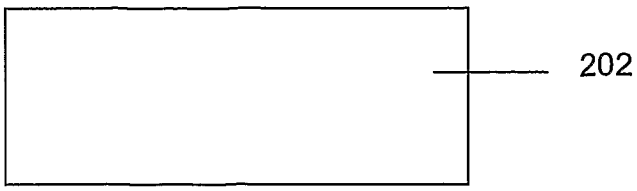


Figure 2A

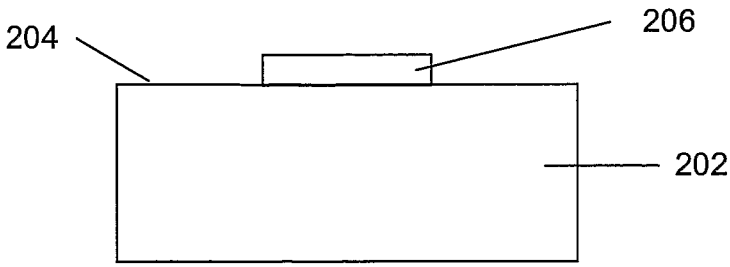


Figure 2B

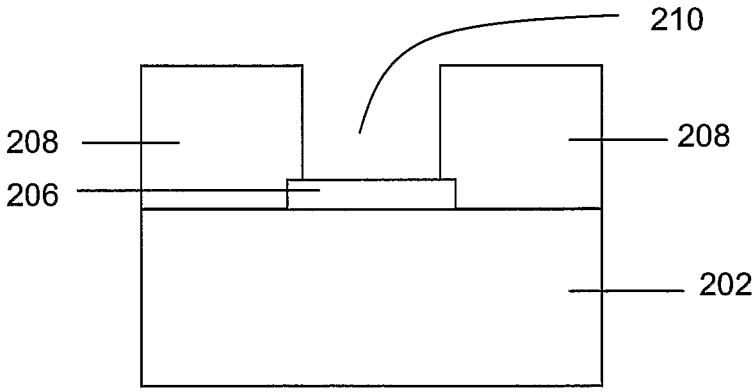


Figure 2C

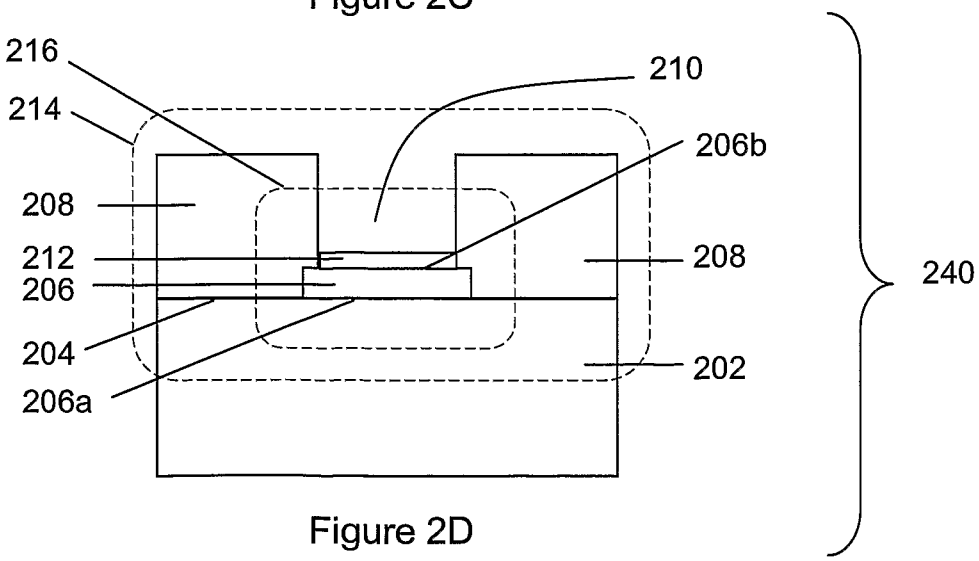


Figure 2D

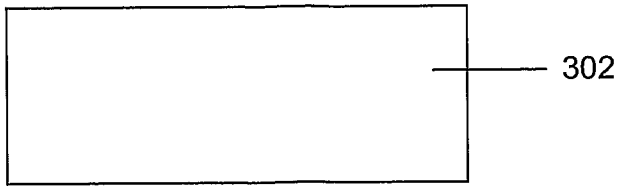


Figure 3A

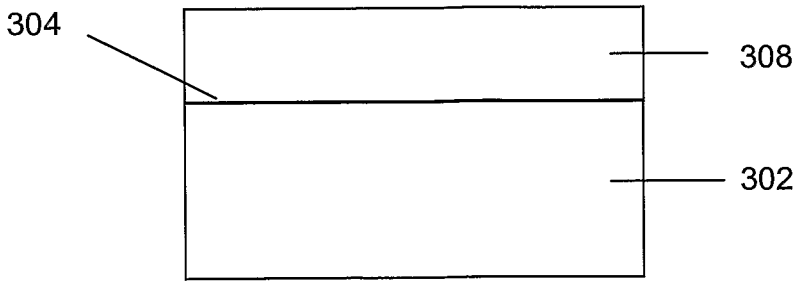


Figure 3B

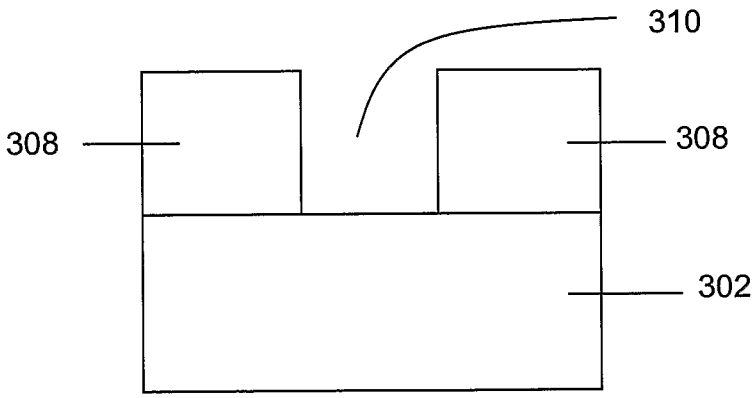


Figure 3C

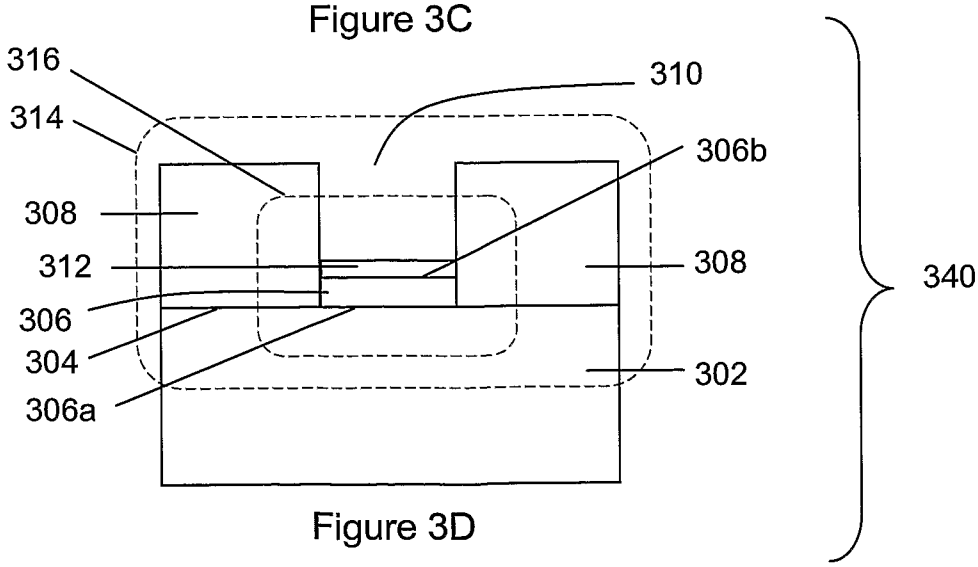


Figure 3D

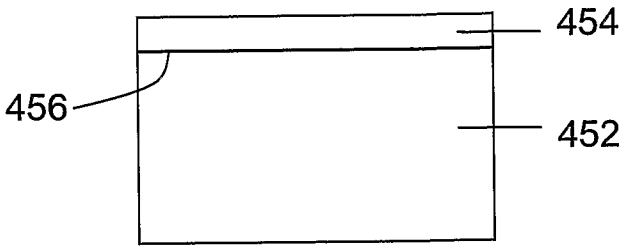


Figure 4A

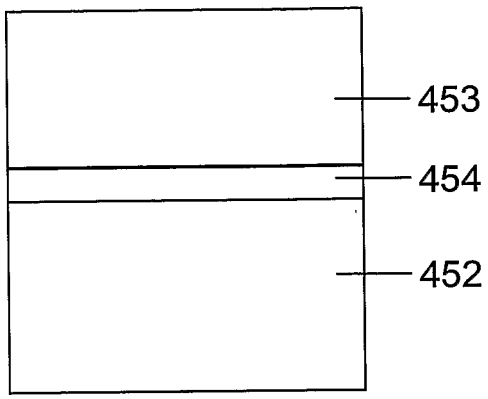


Figure 4B

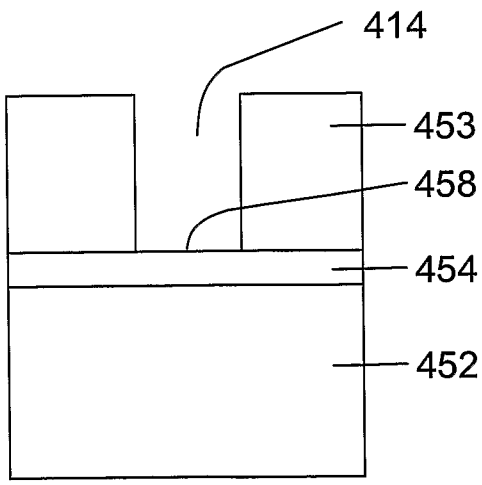


Figure 4C

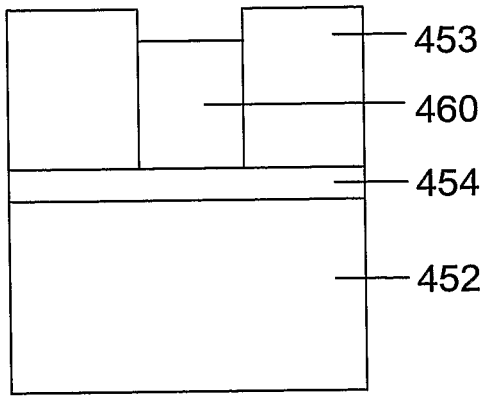


Figure 4D

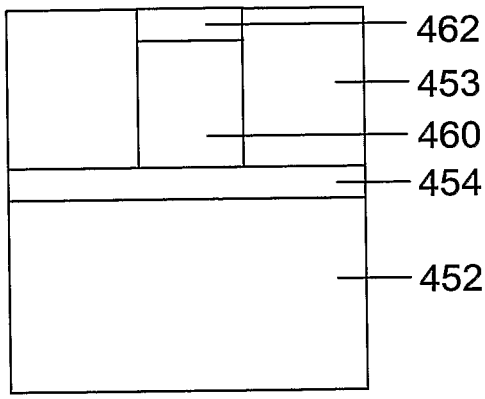


Figure 4E

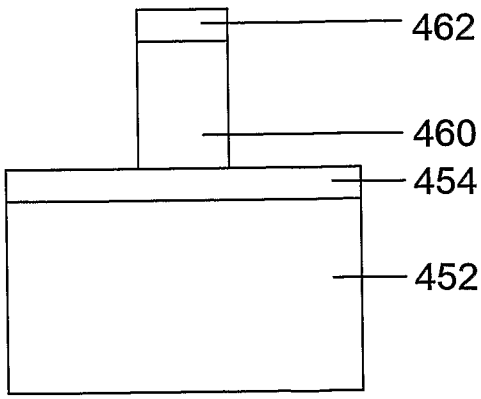


Figure 4F

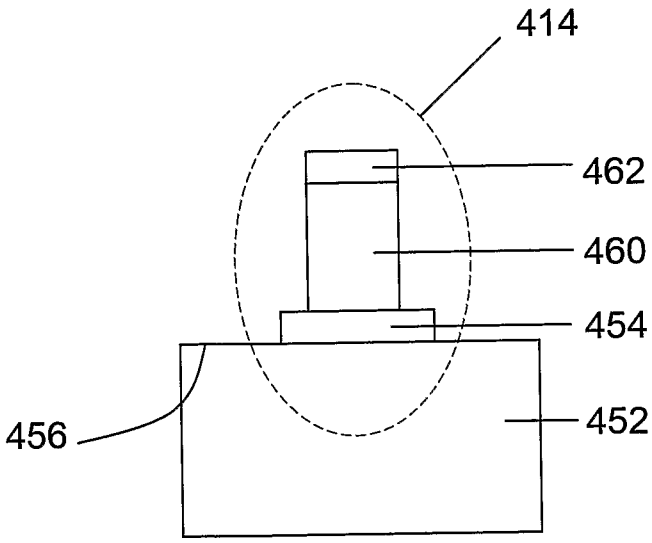


Figure 4G

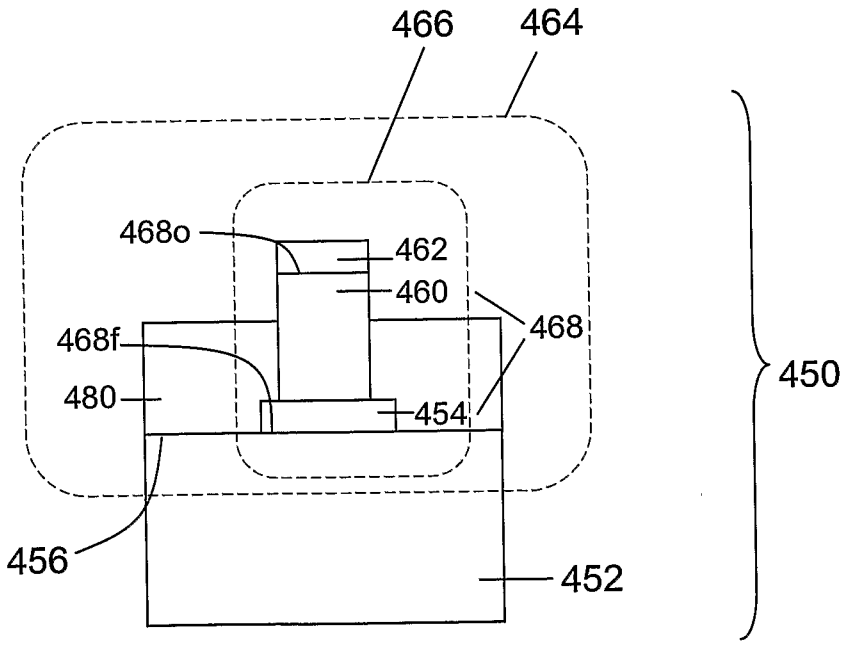


Figure 4H

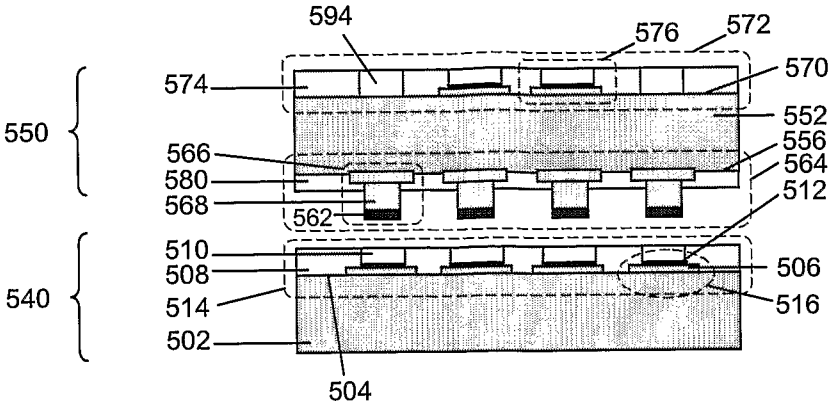


Figure 5A

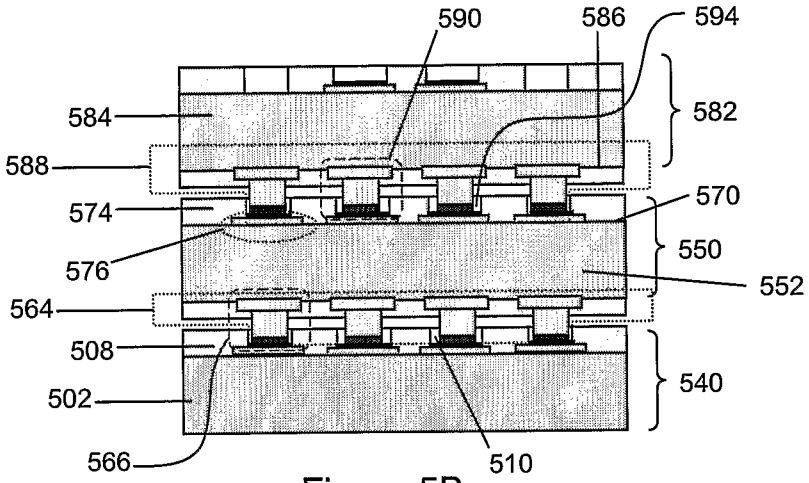


Figure 5B

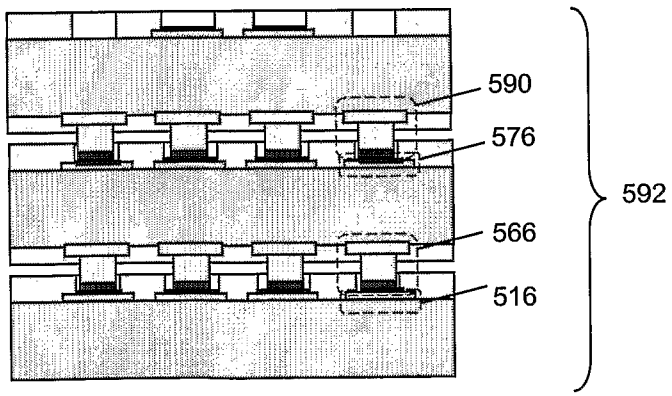


Figure 5C

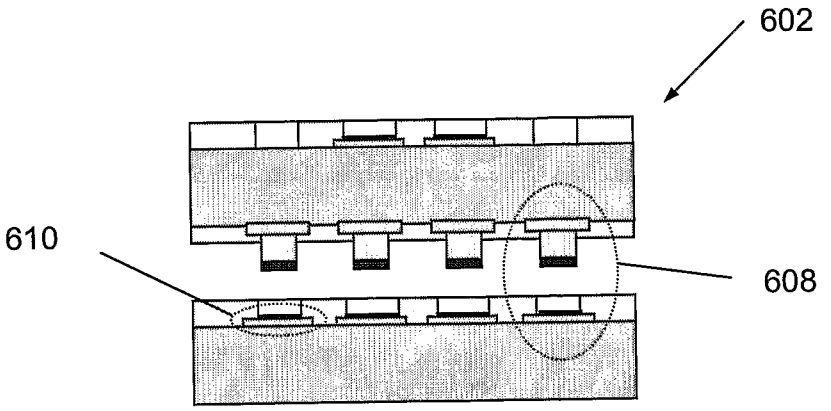


Figure 6A

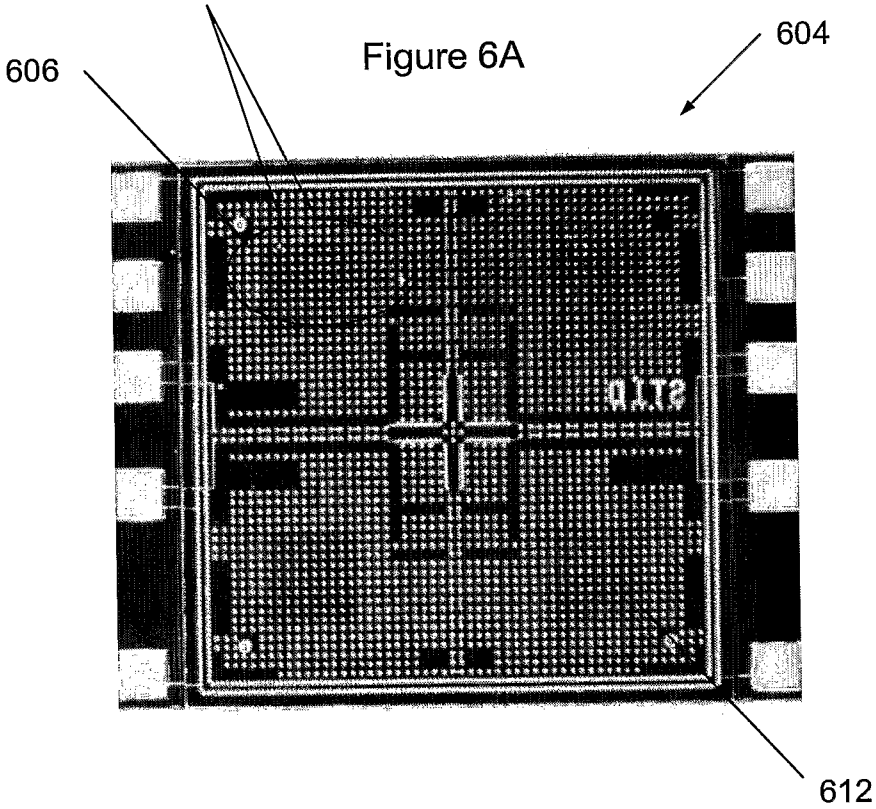


Figure 6B

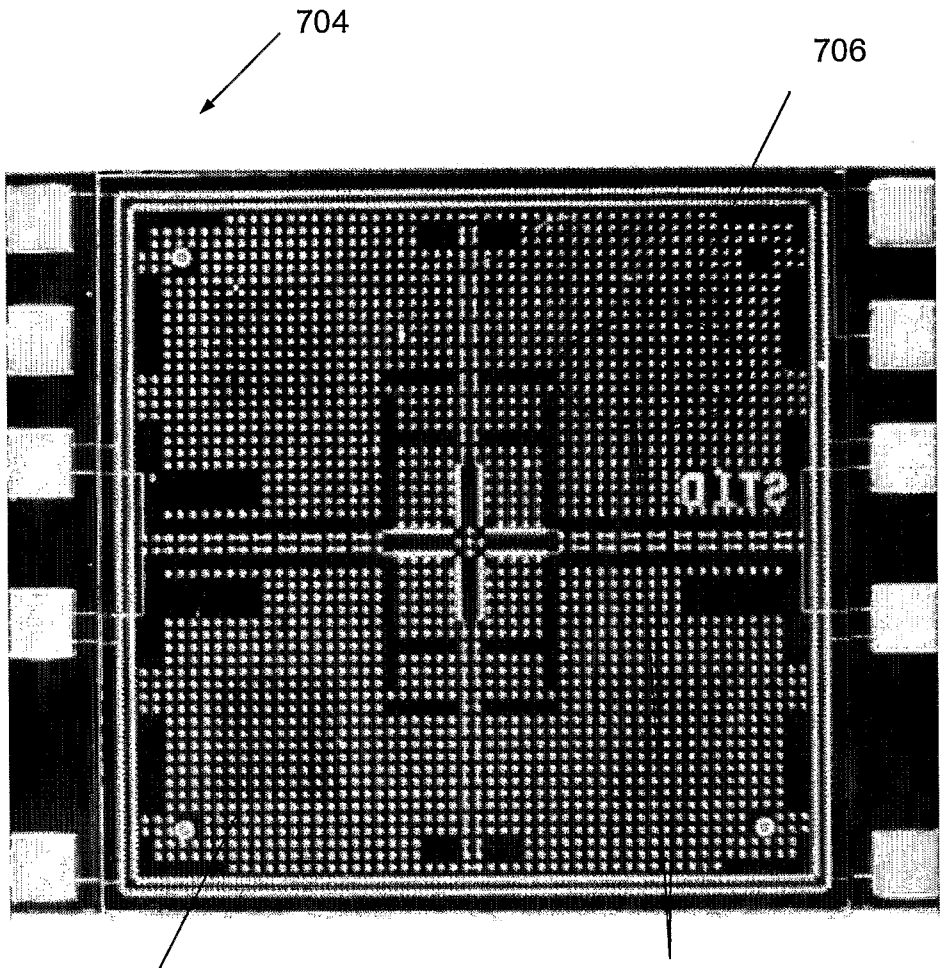


Figure 7A

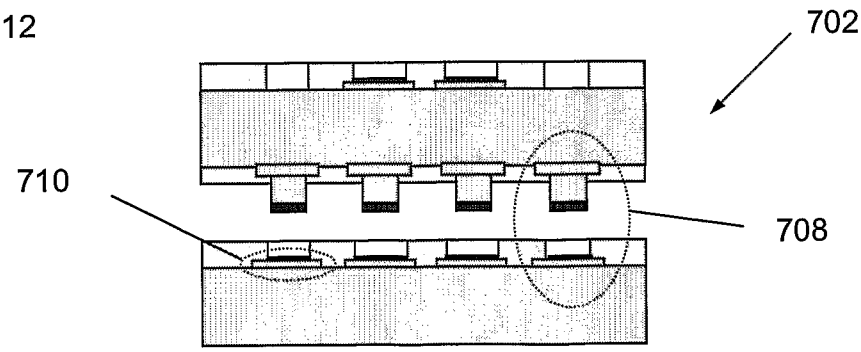


Figure 7B

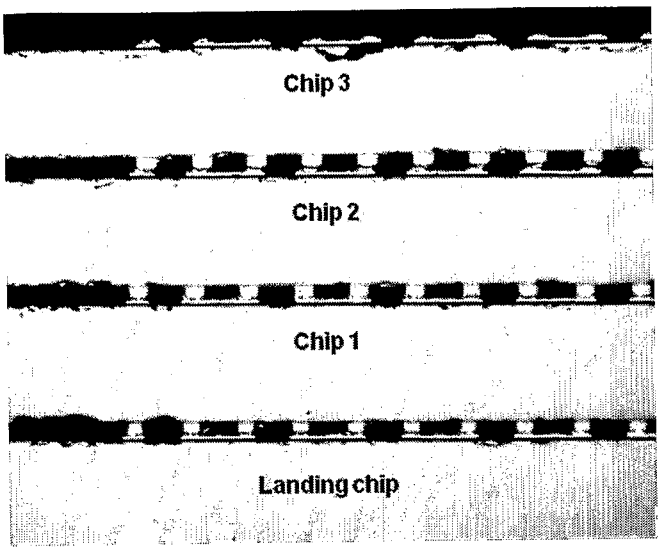


Figure 8

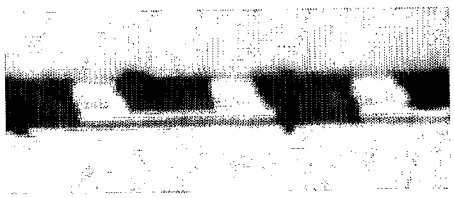
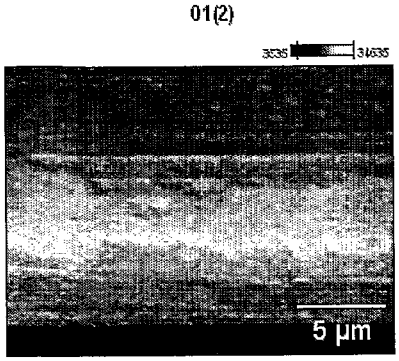
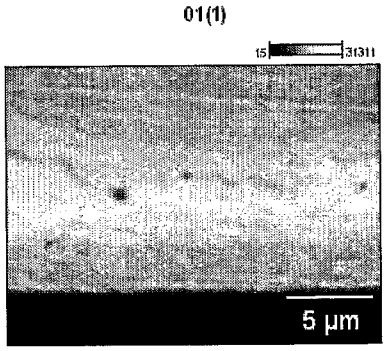


Figure 9



	Cu	Sn	Au
01(2)_pt1	41.43	58.57	0.00
01(2)_pt3	19.70	80.30	0.00

Figure 10A



	Cu	Sn	Au
01(1)_pt1	65.61	34.39	0.00
01(1)_pt3	6.88	92.26	0.86

Figure 10B

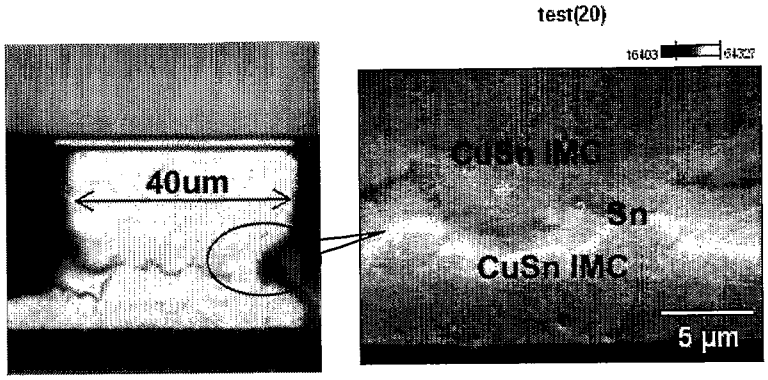


Figure 11A

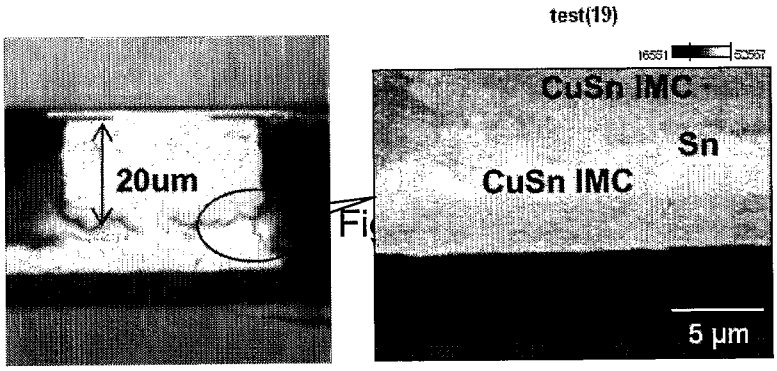


Figure 11B

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2010/000065

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H01L 23/538 (2006.01) ***H01L 21/60*** (2006.01) ***H01L 25/04*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

DWPI AND EPODOC: H01L21/IC OR H01L23/IC OR H01L25/IC, H05K1/14/IC, CHIP? OR ic OR PACKAGE OR DIE? , STACK+, RECESS+ OR HOLE? OR HOLLOW? OR CAVIT+ OR BORE? OR NOTCH+, INSERT+ OR ALIGN+ OR +FIT+ OR INTERLOCK+ OR MATCH+, (INTERMED+ OR MIDDLE OR SPAC+) 5D (LAYER+ OR FILM?)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2002/0085796 A1 (LIM et al) 4 July 2002 See para 14-16 and fig 3.	
A	Patent Abstracts of Japan, JP 11-017303 A (FUJITSU GENERAL LTD) 22 January 1999 See figure of the abstract.	
A	Patent Abstracts of Japan, JP 2008-294239 A (PANASONIC CORP) 4 December 2008 See figure of the abstract.	

☐ Further documents are listed in the continuation of Box C ☒ See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 March 2010	29 MAR 2010
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **S. T. PRING** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6283 2210

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG2010/000065

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member			
US	2002085796	CA	2366618	EP	1221428
JP	11017303	NONE			
JP	2008294239	NONE			

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX