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(54) Title: GROUP III-V MOSFET HAVING METAL DIFFUSION REGIONS

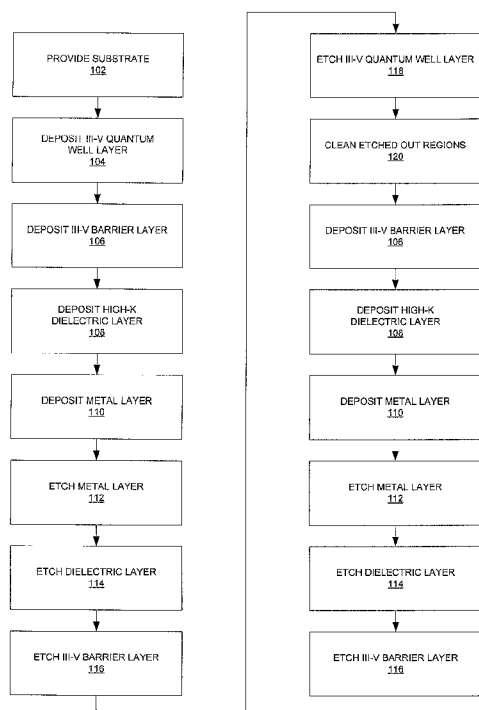


FIG._1

(57) Abstract: A group III-V MOSFET includes metal source and drain regions that are in direct contact with the quantum well region. Such an apparatus comprises a substrate, a III-V quantum well layer formed on the substrate, a III-V barrier layer formed on the quantum well layer, a gate dielectric layer formed on the barrier layer, a gate electrode formed on the gate dielectric layer, a first metal sidewall liner formed adjacent to both the quantum well layer and the barrier layer, a second metal sidewall liner formed adjacent to both the quantum well layer and the barrier layer, a metal source region adjacent to the first metal sidewall liner, and a metal drain region adjacent to the second metal sidewall liner.



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GROUP III-V MOSFET HAVING METAL DIFFUSION REGIONS

Background

As integrated circuit technology continues to scale down, energy efficiency becomes increasingly important. To that end, group III-V semiconductor materials have been proposed for use in future generation transistors because of their ability to enable high-speed switching at low supply voltages due to their excellent low and high-field electron transport properties. Group III-V materials are synthesized using elements from the 3rd and the 5th group of the periodic table, examples include gallium arsenide (GaAs), indium gallium arsenide (InGaAs), gallium phosphide (GaP), gallium nitride (GaN), gallium aluminum arsenide (GaAlAs), indium aluminum arsenide (InAlAs), indium phosphide (InP), indium arsenide (InAs), and indium antimonide (InSb).

Transistors developed using III-V materials are known as quantum-well field-effect transistors (QWFETs). In a QWFET, the III-V material is used to form a quantum-well channel region for the transistor while the source and drain (S/D) regions are formed using a metal-doped semiconducting material, such as doped silicon or doped germanium. Although the use of semiconducting materials for the S/D regions of conventional transistors is very well known, as III-V materials are incorporated into the channel region, there are numerous issues that need to be overcome. One such issue is the increased resistance of the S/D regions as their size is scaled down. Another issue is source-starvation. Fundamentally, group III-V materials have a lower carrier density than silicon. It is therefore important that the momentum relaxation time for electrons entering the source region be short, otherwise electrons in the source region are carried away so efficiently that the source region becomes starved of electrons. Source starvation then causes the injection velocity into the III-V channel region to decrease, which in turn causes the drain current to decrease as well.

Brief Description of the Drawings

Figure 1 is a method of forming a III-V transistor on a substrate in accordance with an implementation of the invention.

Figures 2A through 2H illustrate structures that are formed when the method of Figure 1 is carried out.

Figure 3A and 3B illustrate a method of forming a dual-metal sidewall liner in accordance with an implementation of the invention.

Figure 4A and 4B illustrate an alternative method of forming a dual-metal sidewall liner in accordance with an implementation of the invention.

Detailed Description

Described herein are systems and methods of forming III-V quantum well transistors with metal source and drain regions. In the following description, various aspects of the illustrative implementations will be described using terms commonly employed by those skilled in the art to convey the substance of their work to others skilled in the art. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some of the described aspects. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the illustrative implementations. However, it will be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order not to obscure the illustrative implementations.

Various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

In accordance with implementations of the invention, a III-V quantum well transistor is formed using a metal source region and a metal drain region. The use of metal in the source and drain regions provides lower resistance and more abrupt interfaces than doped semiconductor material. Accordingly, implementations of the invention provide a method to form source and drain regions having high-mobility and abrupt interfaces with the III-V channel region.

Figure 1 is a method 100 of forming a III-V transistor on a substrate in accordance with an implementation of the invention. Figures 2A through 2H illustrate structures that are formed when the method of Figure 1 is carried out.

The method 100 begins by providing a substrate upon which the III-V film will be grown (102 of Figure 1). The substrate is generally a semiconductor substrate and may be formed from known semiconductor materials, such as silicon or silicon-containing materials, germanium or germanium-containing materials, or other group IV containing materials.

In some implementations the substrate may be formed from a III-V material such as GaAs, GaP, GaN, GaAlAs, InAlAs, InP, and InAs. As will be explained below, a relatively wide bandgap III-V material may be used as the substrate to provide a barrier for the subsequently formed high-mobility quantum well layer. In some implementations, the semiconductor substrate may be doped in situ, for instance, the substrate may be p-doped in situ in order to form an n-type QWFET. In some implementations, the barrier layer may be counter-doped relative to the quantum well layer to mitigate short channel effects.

In further implementations, the substrate may be formed using one or more layers that include any combination of silicon, silicon-containing materials, germanium, germanium-containing materials, other group IV containing materials, and III-V materials such as GaAs, GaP, GaN, GaAlAs, InAlAs, InP, and InAs.

Figure 2A illustrates a substrate 200 that may serve as a foundation for the fabrication of a III-V transistor.

Next, a III-V film is deposited on the substrate for use as a high-mobility quantum well layer (104). The quantum well layer functions as the channel region in the III-V quantum well transistor. A relatively narrow bandgap III-V material is typically used as the quantum-well layer. In an implementation, a III-V material such as indium gallium arsenide (InGaAs) or indium antimonide (InSb) may be used to form the quantum well layer. The thickness of the quantum layer may range from one Angstrom ($\text{\AA}$) to 100 $\text{\AA}$. In alternate implementations, the quantum well layer may be formed using materials such as $\text{In}_x\text{Ga}_{1-x}\text{As}$ (where $x \geq 0.53$), InAsSb, or InAs.

Several different epitaxial processes may be employed to deposit the III-V quantum well layer on the substrate. In some implementations, the epitaxial film growth may be carried out using a molecular beam epitaxy (MBE) process, an electron beam (e-beam) deposition process, a metalorganic chemical vapor deposition (MOCVD) process, a metalorganic vapor phase epitaxy (MOVPE) process, or a pulsed laser deposition (PLD) process. Alternate deposition methods may also be employed, as will be appreciated by those of ordinary skill in the art.

Figure 2A illustrates a quantum well layer 202 formed on the substrate 200 that may serve as a channel region in the III-V quantum well transistor.

A second III-V layer is then deposited for use as a barrier layer (106). The second III-V layer is formed atop the III-V quantum well layer. The barrier layer serves as a transition between the quantum well layer and a gate dielectric layer. A relatively wide bandgap III-V material is used as the barrier layer. The wide
5 bandgap ensures that the carriers remain confined in the narrow bandgap quantum well layer. The use of a wide bandgap III-V material also reduces junction leakage and transistor off-state leakage. In implementations of the invention, III-V materials such as GaAs, GaP, GaN, GaAlAs, InAlAs, InP, InAlSb, GaAsSb, and AlGaP may be used as the barrier layer. In further implementations,
10 the barrier layer may be counter-doped relative to the quantum well layer to mitigate short channel effects. For instance, the barrier layer may be p-doped if the quantum well layer is n-type. The thickness of the III-V barrier layer may range from one Angstrom ($\text{\AA}$) to 100 $\text{\AA}$.

Again, several different epitaxial processes may be employed to grow the
15 III-V barrier layer on the quantum well layer. In some implementations, the epitaxial film growth may be carried out using an MBE process, an e-beam process, an MOCVD process, an MOVPE process, or a PLD process. Alternate deposition methods may also be employed, as will be appreciated by those of ordinary skill in the art.

20 In alternate implementations of the invention, one or more additional III-V layers may be included in conjunction with the III-V quantum well layer and the III-V barrier layer described herein. These additional III-V layers may be used for many purposes, including but not limited to providing transition layers, buffer layers, further barrier layers, and further channeling layers. These multiple III-V
25 layers may be referred to as a III-V stack.

Figure 2A illustrates a III-V barrier layer 204 formed atop the III-V quantum-well layer 202.

The substrate also has at least one high-k dielectric layer deposited on its surface, more specifically, deposited atop the III-V barrier layer (108). The high-k
30 dielectric layer may be formed using materials known for their applicability in gate stacks for integrated circuit structures, such as high-k gate dielectric materials. Some of the materials that may be used here for the dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, hafnium aluminum oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide,

zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. Particularly preferred are hafnium oxide, zirconium oxide, and aluminum oxide. In some implementations, the high-k gate dielectric layer may be formed using two or more dielectric layers, which may include a transition layer adjacent to the III-V barrier layer. In further implementations, the material used may have a dielectric constant (k) that is similar to or higher than a dielectric constant of the III-V barrier layer. Although a few examples of materials that may be used to form high-k gate dielectric layer are described here, that layer may be made from other materials.

The high-k dielectric layer may be formed on the III-V barrier layer using a conventional chemical vapor deposition (CVD) process, such as an atomic layer deposition (ALD) process. In such a process, a metal oxide precursor (e.g., a metal chloride) and steam may be fed at selected flow rates into a CVD reactor, which is then operated at a selected temperature and pressure to generate an atomically smooth interface between the III-V barrier layer and the high-k dielectric layer. The CVD reactor should be operated long enough to form a layer with the desired thickness. In most applications, the high-k dielectric layer should be less than about 60 Å thick, and more preferably between about 5 Å and about 50 Å thick. The electrical equivalent thickness of the dielectric layer may be less than 10 Å, and preferably less than 7 Å. In some implementations, the high-k dielectric layer may be annealed to improve its quality.

Figure 2A illustrates a high-k dielectric layer 206 formed atop the III-V barrier layer 204.

Finally, at least one metal layer is deposited atop the high-k dielectric layer (110). The metal layer may be formed using any suitable conductive material from which a metal gate electrode may be derived. In some implementations, the metal layer may be deposited using well known physical vapor deposition (PVD), ALD, or CVD processes. In other implementations, an electroplating or electroless plating process may be used to form the metal layer. Various combinations of deposition and plating processes may be used to form the metal layer.

When the metal layer will serve as an n-type workfunction metal, the metal used preferably has a workfunction that is between about 3.9 eV and about 4.2 eV. N-type materials that may be used to form the metal layer include hafnium, zirconium, titanium, tantalum, aluminum, and metal carbides that include these elements, i.e., titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide and aluminum carbide. The metal layer should be thick enough to ensure that any material formed on it will not significantly impact its workfunction. Preferably, the metal layer is between about 25 Å and about 300 Å thick, and more preferably is between about 25 Å and about 200 Å thick.

When the metal layer will serve as a p-type workfunction metal, the metal used preferably has a workfunction that is between about 4.9 eV and about 5.2 eV. P-type materials that may be used to form the metal layer include ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. Again, the metal layer should be thick enough to ensure that any material formed on it will not significantly impact its workfunction. Preferably, the metal layer is between about 25 Å and about 300 Å thick, and more preferably is between about 25 Å and about 200 Å thick.

In some implementations, a fill metal layer may also be deposited. The fill metal layer preferably consists of a material that may be easily polished and is preferably deposited over the entire device using a conventional metal deposition process. Such a fill metal may comprise titanium nitride, tungsten, titanium, aluminum, tantalum, tantalum nitride, cobalt, copper, nickel, or any other metal that may be polished and that may increase the thickness of the metal gate electrode being formed.

Figure 2A illustrates a metal layer 208 deposited atop the high-k dielectric layer 206. Although one metal layer is shown, in alternate implementations two or more metal layers may be used.

Next, a series of patterning processes may be carried out on the deposited layers to form at least a portion of the QWFET device. First, the metal layer is etched to form a metal gate electrode structure (112). Conventional etching processes that are well known in the art may be used to pattern the metal layer and form the metal gate electrode.

For instance, a photolithography process may be used to form a mask through which the metal layer may be patterned. A conventional

photolithography process may include depositing a photoresist material onto the metal layer, exposing the photoresist material to ultraviolet radiation or extreme ultraviolet radiation through a patterned optical mask, and developing the photoresist material. The photoresist material that remains after development functions as a mask allowing only selected portions of the metal layers to be exposed and etched, thereby defining structures such as the metal gate electrode. An etchant is then applied to remove those exposed portions of the metal layer and form the metal gate electrode. Finally, the photoresist mask is removed. The etching process used to remove the metal layer may include any known metal etching processes, including but not limited to a reactive ion etching (RIE) process, a wet etch process, or a dry etching process.

Figure 2B illustrates a metal gate electrode 210 that has been patterned atop the high-k dielectric layer 206.

After the metal gate electrode is formed, the remaining layers may be patterned to form openings in which the source and drain regions may be fabricated. This process generally begins by using a photolithography process to form a mask through which the underlying layers may be etched. Similar to above, the photolithography process may include depositing a photoresist material over the dielectric layer and metal gate electrode, exposing the photoresist material to ultraviolet radiation or extreme ultraviolet radiation through a patterned optical mask, and developing the photoresist material. The photoresist material that remains after development functions as a mask to allow only selected portions of the dielectric layer to be exposed, thereby defining openings for the source and drain regions.

Figure 2C illustrates a photoresist mask 212 that has been deposited and developed. The photoresist mask 212 includes openings 212A that define where the source and drain regions will be formed.

Once the photoresist mask layer is in place, the exposed underlying layers are etched. First, the dielectric layer is etched through the photoresist mask using an appropriate dielectric etching process (114). Such etching processes for dielectric materials are well known in the art and include wet and dry etching processes, such as buffered peroxide or hydrofluoric acid based wet etchants and chlorine or bromine based dry etchants. The etching of the dielectric layer

forms a gate dielectric layer under the metal gate electrode that is necessary for the gate stack of the QWFET being fabricated.

Figure 2D illustrates the etched dielectric layer that forms a gate dielectric layer 214. A portion of the underlying III-V barrier layer 204 is exposed when the dielectric layer is etched. In some implementations, the photoresist mask 212 may remain atop the etched gate dielectric layer 214 to function as a mask for the subsequent etching of the III-V layers. In further implementations, the photoresist mask 212 may be removed and the gate dielectric layer 214 may function as a mask.

In an alternate implementation of the invention, the high-k dielectric layer may be etched earlier in the process. For instance, the metal layer and the high-k dielectric layer may be etched in sequence to form the metal gate electrode and the high-k gate dielectric layer. Unlike what is shown in Figure 2D, an "in sequence" processing of the metal layer and dielectric layer provides a gate dielectric layer that is substantially the same width as the metal gate electrode.

As shown, the etching of the dielectric layer exposes the underlying III-V barrier layer. This III-V barrier layer is then etched using an etchant that is appropriate for the specific III-V material that is used in the barrier layer (116). Etchants appropriate for use in this instance are well known in the art. For instance, wet etchants that may be used here include, but are not limited to, etchants based on citric acid and peroxide, hydrochloric acid, or phosphoric. Dry etching processes that may be used here include, but are not limited to, argon based reactive ion etching and other physical sputtering processes.

Figure 2E illustrates the etched III-V barrier layer 216 atop the quantum well layer 202. A portion of the quantum well layer 202 is exposed when the etched III-V barrier layer 216 is formed.

Next, the exposed portion of the quantum well layer is etched using an appropriate etchant, such as an etchant that is appropriate for InGaAs or InSb (118). Etchants appropriate for use in this instance are well known in the art and some examples were provided above. In some implementations, the etching process may be modified or extended to perform a selective undercut etch of the quantum well layer as well. As will be recognized by those of skill in the art, undercutting the quantum well layer enables the later formed source and drain

regions to be in closer proximity to the channel region of the transistor. This reduces the overall resistance of the transistor.

Figure 2F illustrates the etched III-V quantum well layer 218. The quantum well layer 218 is etched down to the underlying substrate 200. Although not
5 shown, in some implementations the quantum well layer 218 may be undercut.

After etching of the III-V layers is complete, a cleaning process may be carried out on the etched out regions in the III-V layers in preparation for the metal deposition (120). Cleaning processes appropriate for III-V layers and substrates are well known in the art, for instance, hydrochloric acid may be used
10 to clean an InGaAs layer.

Finally, a metal deposition process is carried out to fill the etched out regions with a metal, a combination of metals, or a metal alloy to form the source and drain regions of the QWFET (122). The source and drain regions are therefore in direct contact with the III-V layers, such as the barrier layer and the quantum
15 well layer. Since an etching and metal deposition process is used to form the source and drain regions, the interfaces between the source/drain regions and the channel region tend to be very abrupt relative to conventional ion implantation, diffusion and activation processes. In implementations where the quantum well layer has been undercut, the abrupt source/drain regions extend
20 laterally towards the channel region. This causes the source and drain regions to be in close proximity to and possibly overlap with the gate electrode, thereby reducing the external resistance of the transistor.

Due to the nature of the materials used in the III-V layers, only specific metals are suitable for use in the source and drain regions. For instance, in an
25 NMOS QWFET, the metal, metal alloy, or combination of metals must have both an ohmic contact to the III-V quantum well layer (i.e., a relatively low barrier height to electrons on the quantum well layer) and a Schottky contact to the III-V barrier layer (i.e., a relatively high barrier height to electrons on the barrier layer). Two such metals include a titanium-tungsten alloy (TiW) and aluminum.

30 In some implementations of the invention, a metal sidewall liner may be deposited into the etched regions adjacent to, and in direct contact with, the III-V layers to form the appropriate ohmic and Schottky contacts to the III-V layers. In one such implementation, when the III-V quantum well layer is formed of InGaAs and the III-V barrier layer is formed of InAlAs, a TiW metal sidewall liner may be

deposited into the etched regions (124). A TiW sidewall liner provides an ohmic contact to the InGaAs quantum well layer and a Schottky contact to the InAlAs barrier layer. A metal deposition process such as chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering deposition, or atomic layer deposition (ALD) may be used to deposit the TiW sidewall liner. Alternate deposition processes known in the art to produce the TiW sidewall layer may be used as well. Once the sidewall liner is deposited, the remainder of the source and drain regions may be filled with a metal such as TiW, copper, tungsten, aluminum, a copper-aluminum alloy, or another suitable metal. In another implementation, alternate metals may be used for the metal sidewall liner, such as aluminum.

Figure 2F illustrates a TiW sidewall liner 220 that has been deposited into the etched out source and drain regions. To form the TiW sidewall structure as shown, a conformal layer of TiW is first deposited using a deposition process such as ALD. An anisotropic etching process is then carried out to etch away the TiW from the top down to form the TiW sidewall liner structure shown in Figure 2F. In some implementations, the TiW sidewall liner 220 may also be formed adjacent to the high-k gate dielectric layer, as shown in Figure 2F, while in some implementations the TiW sidewall liner 220 may be etched down such that it is only adjacent to the III-V layers (not shown). The photoresist mask 212 is still shown in Figure 2F, although in some implementations it may have been removed by this point in the process.

Figure 2G illustrates the QWFET transistor after the source and drain metal regions 222 have been deposited. Again, the metal used in the source region 222 and the drain region 222 may consist of the same material used in the liner 220, such as TiW, or it may be formed using another metal.

In another implementation, a dual-metal sidewall liner may be fabricated to form the appropriate ohmic and Schottky contacts to the III-V layers. For instance, a Ti-TiW sidewall liner may be formed, where the Ti metal forms a Schottky contact with the barrier layer and the TiW metal forms an ohmic contact with the quantum well layer. The Ti-TiW sidewall liner may be formed by first depositing a Ti sidewall liner. A Ti sidewall liner 300 is shown in Figure 3A. The Ti sidewall liner 300 may be formed using the same deposition and etching processes detailed above

for the TiW sidewall liner 220. The Ti sidewall liner provides a Schottky contact to the barrier layer, such as an InAlAs layer.

Next, a tungsten (W) liner may be formed within the etched regions adjacent to the Ti sidewall liner. A W liner 302 is also shown in Figure 3A. The height of the W liner 302 is shorter than the height of the Ti sidewall liner 300 because the W is intended to only contact the quantum well layer 218. Optimally, the height of the W liner 302 is substantially aligned with the height of the quantum well layer 218. The same deposition and etching processes detailed above for the TiW sidewall liner 220 may be used to form the W liner 302.

A diffusion process is then carried out to cause the W liner 302 to alloy with the bottom portion of the Ti sidewall liner 300 and form a dual-metal sidewall liner 304, shown in Figure 3B. An annealing process may be used to cause the diffusion to occur. The dual-metal sidewall liner 304 includes a Ti component 306 and a TiW component 308. The Ti component 306 is adjacent to the barrier layer 216 and forms a Schottky contact with the barrier layer 216. The TiW component 308 is adjacent to the quantum well layer 218 and forms an ohmic contact with the quantum well layer 218.

Although not shown, the remainder of the etched regions may then be filled with a metal to form the source and drain regions. Again, metals such as Ti, TiW, copper, tungsten, aluminum, a copper-aluminum alloy, and other compatible metals may be used to form the source and drain regions.

In alternate implementations, the above processes described in Figures 3A and 3B may be carried out with alternative metals. For instance, in one implementation, the above processes may be carried out using palladium (Pd) instead of Ti and silicon (Si) instead of W. The resulting structure is a dual-metal sidewall liner where Pd forms a Schottky contact with the barrier layer and PdSi forms an ohmic contact with the quantum well layer.

In yet another implementation of the invention, the initial metal sidewall liner, such as the Ti or Pd liner, may not be etched prior to deposition of the second liner, such as the W or the Si. This is shown in Figures 4A and 4B, where only the barrier layer 216 and the quantum well layer 218 are shown on the substrate 200. As demonstrated, the Ti (or Pd) sidewall liner 400 covers the bottom of the etched out region and the side of the III-V layers 216/218. The W (or Si) liner 402 is then formed atop the sidewall liner 400. After the diffusion process is carried out,

the final dual-metal sidewall liner 404, shown in Figure 4B, contains a Ti (or Pd) component 406 and a TiW (or PdSi) component 408. The dual-metal sidewall liner 404 may or may not be etched prior to metal deposition to form the source and drain regions. In some implementations, the metal for the source and drain regions may be deposited directly upon the Ti or Pd sidewall liner 400 covering the bottom of the etched out regions.

In various implementations of the invention, the metal or combination of metals used in the sidewall liners and the source or drain regions may include one or more of the following: platinum, palladium, chromium, titanium, gold, aluminum, iridium, tungsten, nobelium, and copper. Furthermore, placement of the metal sidewall liner in between the source/drain regions and the barrier layer reduces leakage.

Accordingly, various implementations of the invention have been shown in which a metal or metal combination is used in the source and drain regions of a QWFET transistor to make direct contact with the III-V barrier layer and III-V quantum well layer of the QWFET. The metal source and drain regions may include a metal sidewall liner or dual-metal sidewall liner adjacent to the III-V layers that forms a Schottky contact with the barrier layer and an ohmic contact with the quantum well layer. The use of the metal source and drain regions in conjunction with the III-V quantum well layer, including a dual-metal liner, provides several benefits including the enablement of scaling to sub 22 nm gate lengths, reducing source/drain resistance with the channel region, reducing leakage through the layers parallel to the channel layer, and allowing a low temperature thermal budget to be used since the formation of the metal source/drain regions and the single or dual-metal liners can occur at low temperatures.

The above description of illustrated implementations of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

These modifications may be made to the invention in light of the above detailed description. The terms used in the following claims should not be

construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather, the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

Claims

1. An apparatus comprising:
a gate electrode;
a gate dielectric layer subjacent to the gate electrode;
5 a III-V barrier layer subjacent to the gate dielectric layer;
a III-V quantum well layer subjacent to the barrier layer;
a metal source region adjacent to the quantum well layer; and
a metal drain region adjacent to the quantum well layer.
2. The apparatus of claim 1, wherein the gate electrode comprises a
10 metal and the gate dielectric comprises a high-k dielectric material.
3. The apparatus of claim 1, wherein the gate electrode is selected
from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum,
titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide and
aluminum carbide.
- 15 4. The apparatus of claim 1, wherein the gate electrode is selected
from the group consisting of ruthenium, palladium, platinum, cobalt, nickel,
ruthenium oxide, palladium oxide, platinum oxide, cobalt oxide, and nickel oxide.
5. The apparatus of claim 1, wherein the gate dielectric layer is
selected from the group consisting of hafnium oxide, hafnium silicon oxide,
20 lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon
oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium
titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead
scandium tantalum oxide, and lead zinc niobate.
6. The apparatus of claim 1, wherein the III-V barrier layer is selected
25 from the group consisting of GaAs, GaP, GaN, GaAlAs, InAlAs, InP, and InAs.
7. The apparatus of claim 1, wherein the III-V quantum well layer
comprises InGaAs or InSb.
8. An apparatus comprising:
a substrate;
30 a III-V quantum well layer formed on the substrate;
a III-V barrier layer formed on the quantum well layer;
a gate dielectric layer formed on the barrier layer;
a gate electrode formed on the gate dielectric layer;
a first metal sidewall liner formed adjacent to both the quantum well layer

and the barrier layer;

a second metal sidewall liner formed adjacent to both the quantum well layer and the barrier layer;

a metal source region adjacent to the first metal sidewall liner; and

5 a metal drain region adjacent to the second metal sidewall liner.

9. The apparatus of claim 8, wherein the gate electrode comprises a metal and the gate dielectric comprises a high-k dielectric material.

10. The apparatus of claim 8, wherein the III-V barrier layer is selected from the group consisting of GaAs, GaP, GaN, GaAlAs, InAlAs, InP, and InAs.

10 11. The apparatus of claim 1, wherein the III-V quantum well layer comprises InGaAs or InSb.

12. The apparatus of claim 8, wherein the first and second metal sidewall liners include at least one of platinum, palladium, chromium, titanium, gold, aluminum, iridium, tungsten, nobelium, and copper.

15 13. The apparatus of claim 8, wherein the first and second metal sidewall liners are dual-metal sidewall liners having a Ti component that is adjacent to the barrier layer and a TiW component that is adjacent to the quantum well layer.

20 14. The apparatus of claim 8, wherein the first and second metal sidewall liners are dual-metal sidewall liners having a Pd component that is adjacent to the barrier layer and a PdSi component that is adjacent to the quantum well layer.

15. An apparatus comprising:

a substrate;

25 a III-V stack formed on the substrate having a first sidewall and a second sidewall;

a gate dielectric layer formed on the III-V stack;

a gate electrode formed on the gate dielectric layer;

a first metal sidewall liner formed along the first sidewall of the III-V stack;

30 a second metal sidewall liner formed along the second sidewall of the III-V stack;

a metal source region adjacent to the first metal sidewall liner; and

a metal drain region adjacent to the second metal sidewall liner.

16. The apparatus of claim 15, wherein the III-V stack includes at least one barrier layer and at least one quantum well layer.

17. The apparatus of claim 16, wherein the first and second metal sidewall liners provide a Shottky contact with the barrier layer of the III-V stack and an ohmic contact with the quantum well layer of the III-V stack.

18. The apparatus of claim 16, wherein the first and second metal sidewall liners comprise dual-metal sidewall liners that provide a Shottky contact with the barrier layer of the III-V stack and an ohmic contact with the quantum well layer of the III-V stack.

19. An apparatus comprising:
a substrate;
a III-V quantum well layer formed on the substrate;
a III-V barrier layer formed over the quantum well layer;
a gate dielectric layer formed over the barrier layer;
a gate electrode formed on the gate dielectric layer;
a first metal sidewall liner in direct contact with both the quantum well layer and the barrier layer;
a second metal sidewall liner in direct contact with both the quantum well layer and the barrier layer;
a metal source region in direct contact with the first metal sidewall liner;
and
a metal drain region in direct contact with the second metal sidewall liner.

20. The apparatus of claim 19, wherein the first and second metal sidewall liners provide a Shottky contact with the barrier layer and an ohmic contact with the quantum well layer.

21. The apparatus of claim 19, wherein the III-V barrier layer is selected from the group consisting of GaAs, GaP, GaN, GaAlAs, InAlAs, InP, and InAs.

22. The apparatus of claim 19, wherein the III-V quantum well layer comprises InGaAs or InSb.

23. The apparatus of claim 19, wherein the first and second metal sidewall liners include at least one of platinum, palladium, chromium, titanium, gold, aluminum, iridium, tungsten, nobelium, and copper.

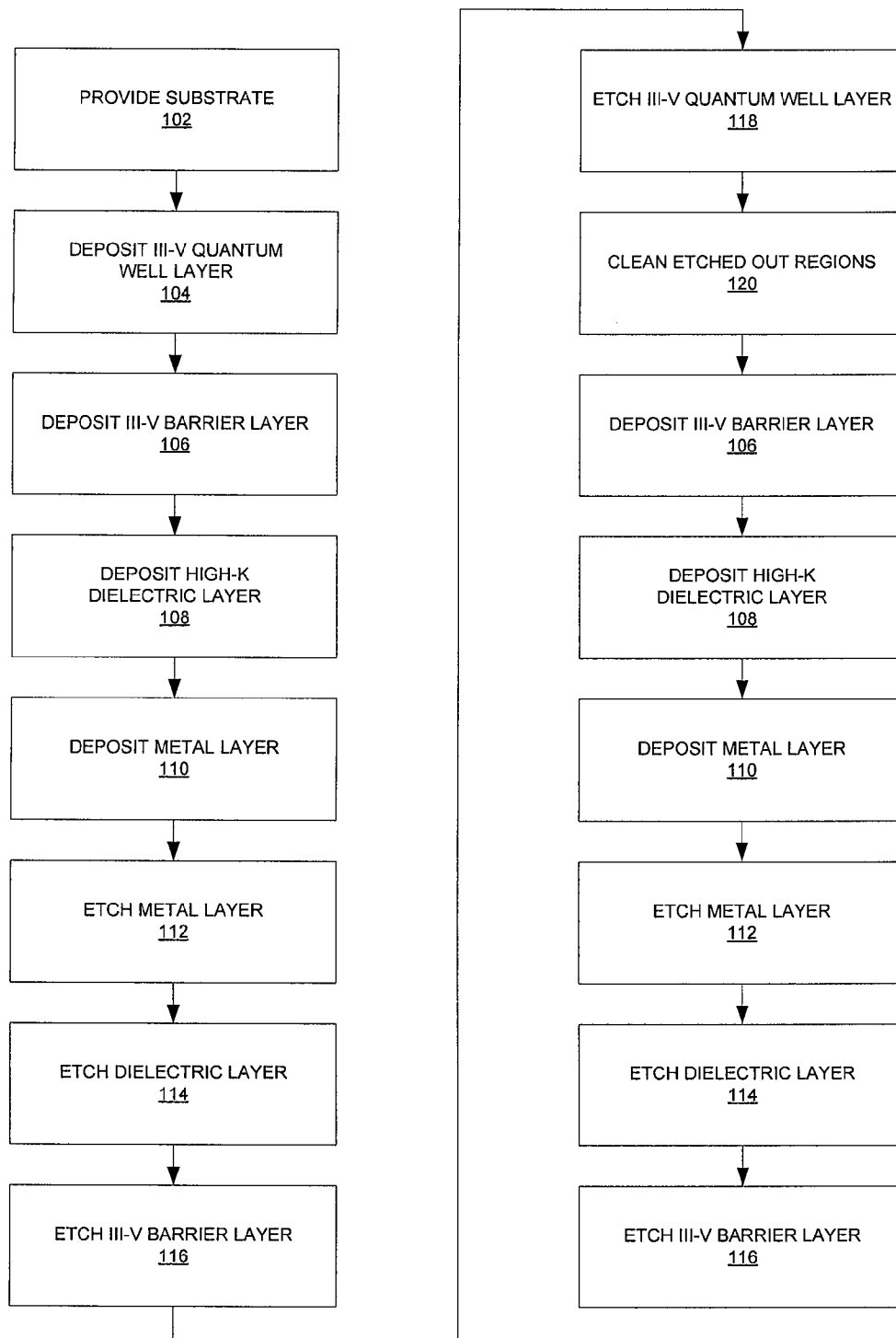


FIG._1

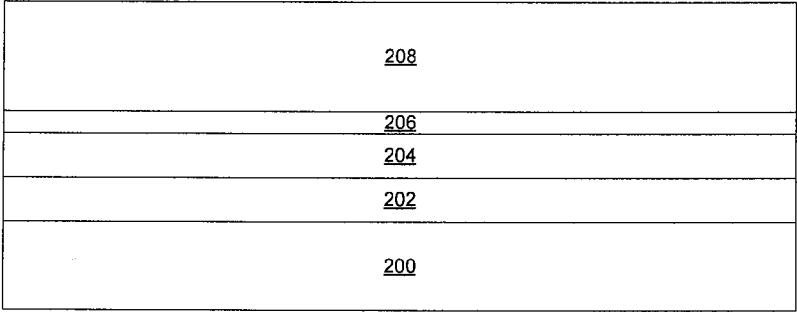


FIG. 2A

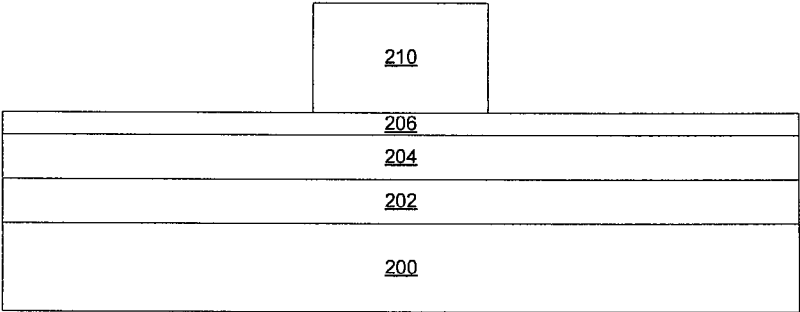


FIG. 2B

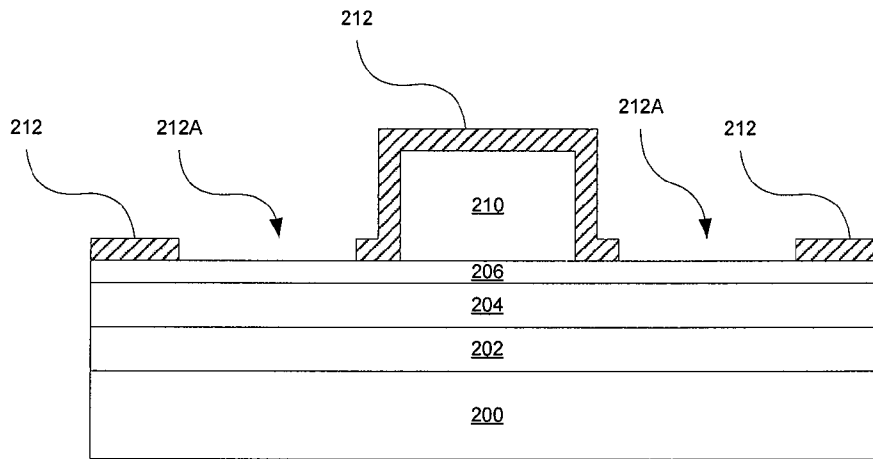


FIG. 2C

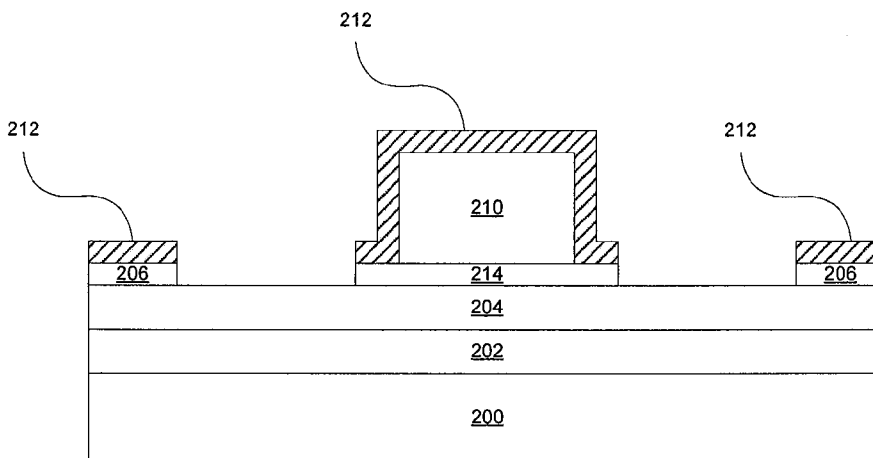


FIG. 2D

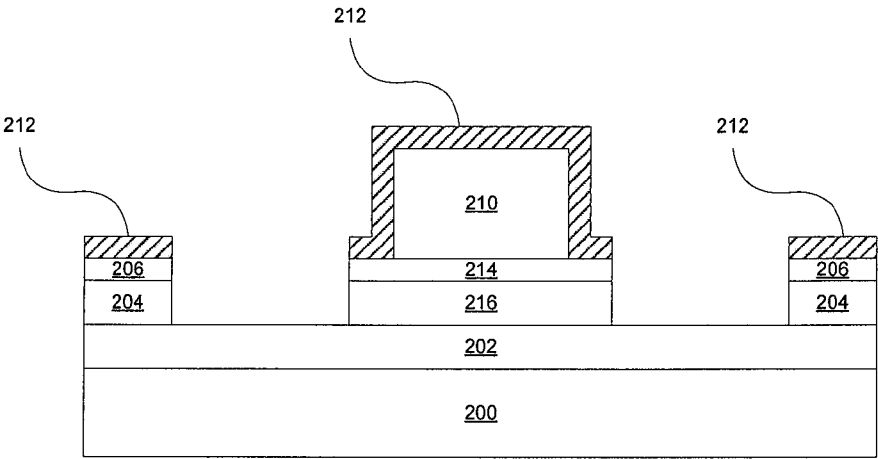


FIG._2E

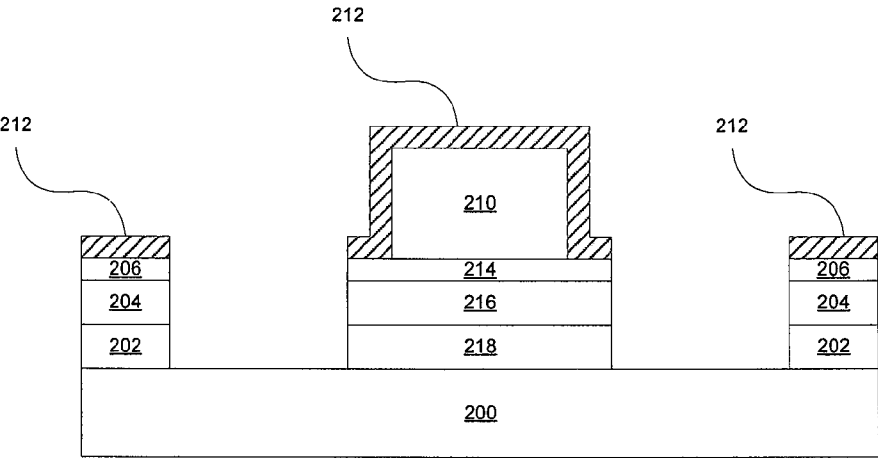


FIG._2F

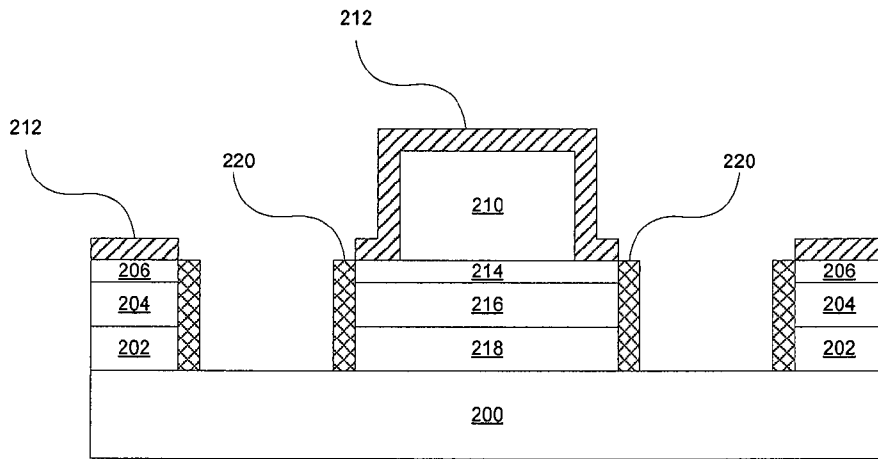


FIG._2G

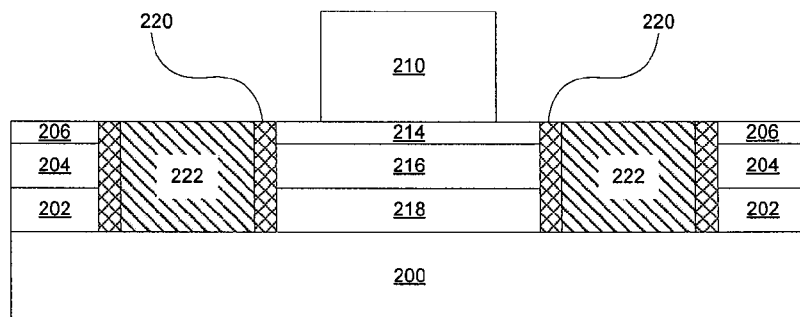
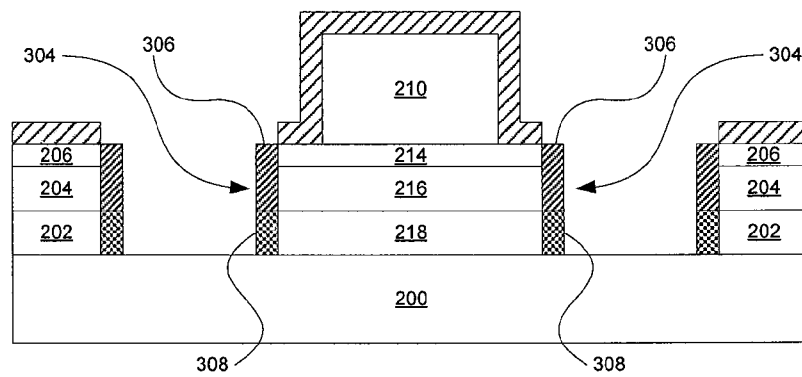
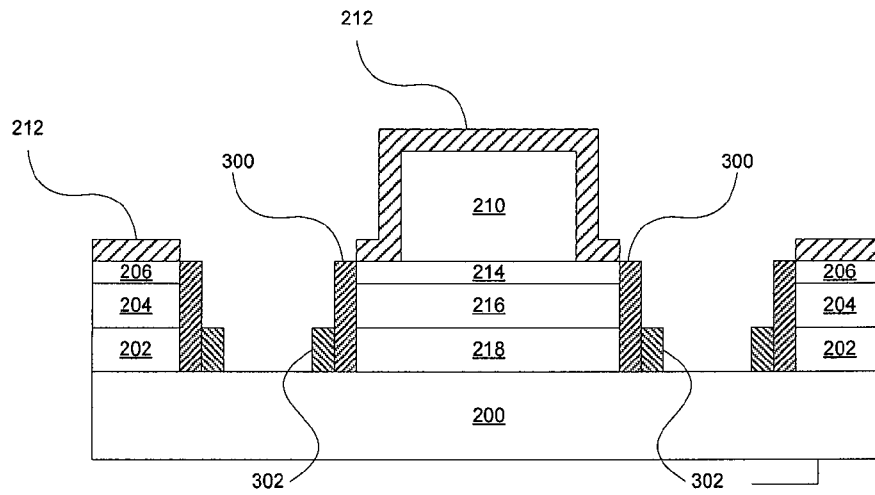


FIG._2H



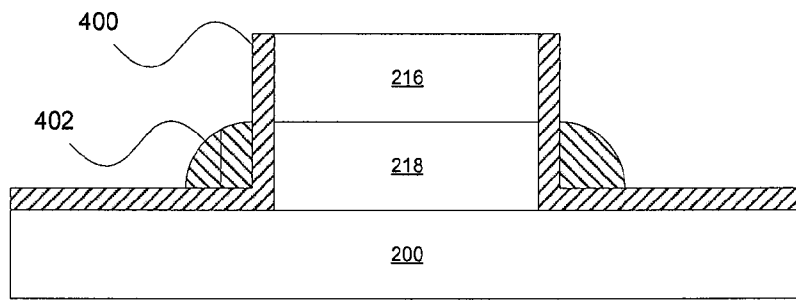


FIG. 4A

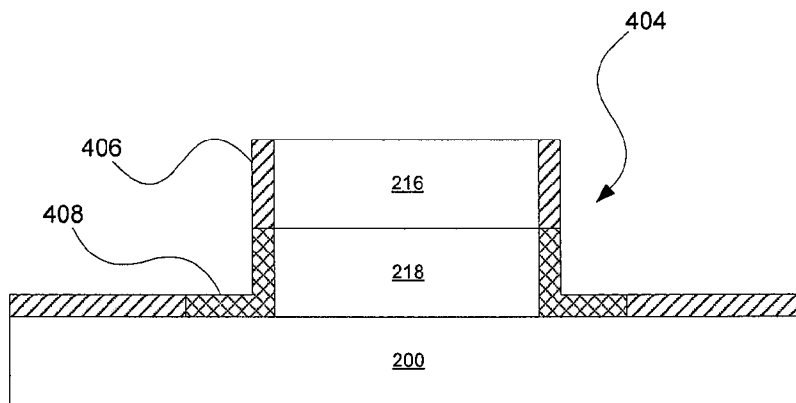


FIG. 4B