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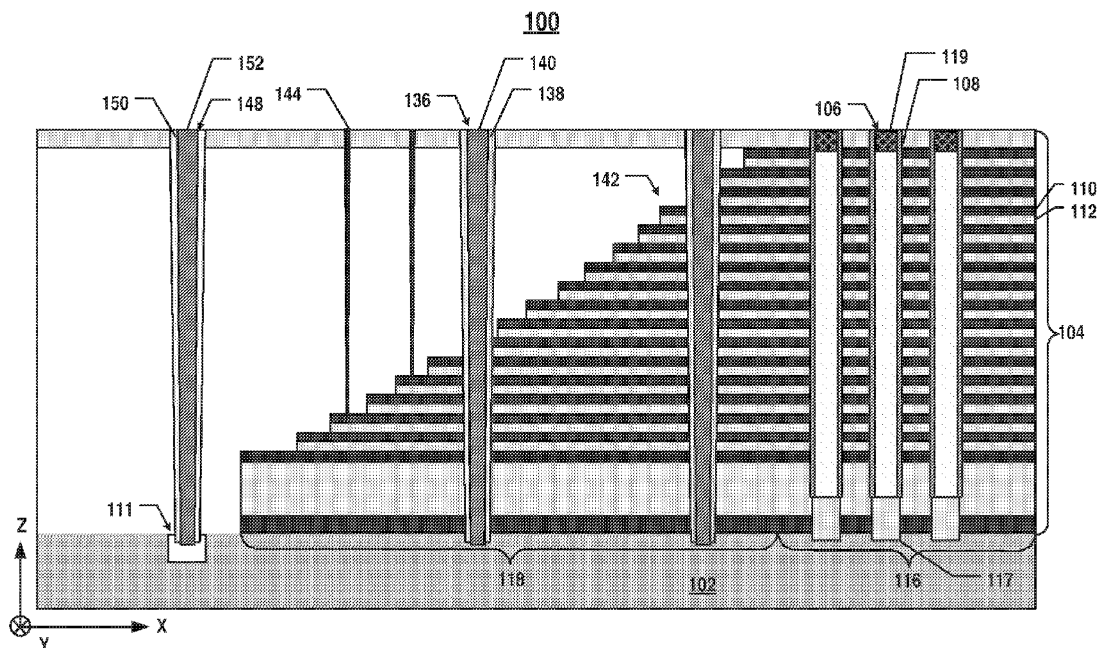
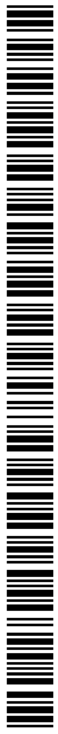


FIG. 1

(57) Abstract: Embodiments of three-dimensional (3D) memory devices having through stair contacts (TSCs) and methods for forming the same are disclosed. In an example, a method for forming a 3D memory device (100) is disclosed. A dielectric stack (104) including a plurality of interleaved dielectric layers (112) and sacrificial layers (110) is formed on a substrate (102). A staircase structure (142) is formed on one side of the dielectric stack (104). A dummy hole extending vertically through the staircase structure (142) and reaching the substrate (102) is formed. A spacer (138) having a hollow core is formed in the dummy hole. A TSC (136) in contact with the substrate (102) is formed by depositing a conductor layer (140) in the hollow core of the spacer (138). The TSC (136) extends vertically through the staircase structure (142).



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THREE-DIMENSIONAL MEMORY DEVICES HAVING THROUGH STAIR CONTACTS AND METHODS FOR FORMING THE SAME

BACKGROUND

[0001] Embodiments of the present disclosure relate to three-dimensional (3D) memory devices and fabrication methods thereof.

[0002] Planar memory cells are scaled to smaller sizes by improving process technology, circuit design, programming algorithm, and fabrication process. However, as feature sizes of the memory cells approach a lower limit, planar process and fabrication techniques become challenging and costly. As a result, memory density for planar memory cells approaches an upper limit.

[0003] A 3D memory architecture can address the density limitation in planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array.

SUMMARY

[0004] Embodiments of 3D memory devices and fabrication methods thereof are disclosed herein.

[0005] In one example, a method for forming a 3D memory device is provided. A dielectric stack including a plurality of interleaved dielectric layers and sacrificial layers is formed on a substrate. A staircase structure is formed on one side of the dielectric stack. A dummy hole extending vertically through the staircase structure and reaching the substrate is formed. A spacer having a hollow core is formed in the dummy hole. A TSC in contact with the substrate is formed by depositing a conductor layer in the hollow core of the spacer. The TSC extends vertically through the staircase structure.

[0006] In another example, a method for forming a 3D memory device is provided. A dielectric stack including a plurality of interleaved dielectric layers and sacrificial layers is formed on a substrate. A staircase structure is formed on one side of the dielectric stack. A dummy channel structure reaching the substrate is formed. The dummy channel structure extends vertically through the staircase structure. A spacer is formed by removing part of the dummy channel structure. The spacer has a hollow core. A TSC in

contact with the substrate is formed by depositing a conductor layer in the hollow core of the spacer. The TSC extends vertically through the staircase structure.

[0007] In a different example, a 3D memory device is provided. The 3D memory device includes a substrate, a memory stack on the substrate including a plurality of interleaved conductor layers and dielectric layers, a staircase structure on one side of the memory stack, and a TSC extending vertically through the staircase structure of the memory stack. The TSC is in contact with the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0009] FIG. 1 illustrates a cross-section of an exemplary 3D memory device, according to some embodiments of the present disclosure.

[0010] FIGS. 2A–2C illustrate an exemplary fabrication process for forming channel structures and staircase structures of a 3D memory device, according to some embodiments of the present disclosure.

[0011] FIGS. 3A–3E illustrate exemplary fabrication processes for forming TSCs, peripheral contacts, and word line contacts of a 3D memory device, according to various embodiments of the present disclosure.

[0012] FIGS. 4A–4D illustrate another exemplary fabrication process for forming TSCs, peripheral contacts, and word line contacts of a 3D memory device, according to some embodiments of the present disclosure.

[0013] FIGS. 5A-5C are flowcharts of exemplary methods for forming a 3D memory device, according to some embodiments.

[0014] FIG. 6 illustrates related art using different patterns to form dummy channel structures and TSCs in separate fabrication steps.

[0015] Embodiments of the present disclosure will be described with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0016] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the pertinent art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the pertinent art that the present disclosure can also be employed in a variety of other applications.

[0017] It is noted that references in the specification to "one embodiment," "an embodiment," "an example embodiment," "some embodiments," etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the pertinent art to effect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0018] In general, terminology may be understood at least in part from usage in context. For example, the term "one or more" as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as "a," "an," or "the," again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context. In addition, the term "based on" may be understood as not necessarily intended to convey an exclusive set of factors and may, instead, allow for existence of additional factors not necessarily expressly described, again, depending at least in part on context.

[0019] It should be readily understood that the meaning of "on," "above," and "over" in the present disclosure should be interpreted in the broadest manner such that "on" not only means "directly on" something but also includes the meaning of "on" something with an intermediate feature or a layer therebetween, and that "above" or "over" not only means the meaning of "above" or "over" something but can also include the meaning it is "above" or "over" something with no intermediate feature or layer therebetween (i.e., directly on something).

[0020] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0021] As used herein, the term "substrate" refers to a material onto which subsequent material layers are added. The substrate itself can be patterned. Materials added on top of the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0022] As used herein, the term "layer" refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer can extend laterally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which interconnect lines and/or via contacts are formed) and one or more dielectric layers.

[0023] As used herein, the term "nominal/nominally" refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term "about" indicates the value of a given quantity that can vary based on a particular technology node associated with the subject semiconductor device. Based on the particular technology node, the term

"about" can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., ±10%, ±20%, or ±30% of the value).

[0024] As used herein, the term "3D memory device" refers to a semiconductor device with vertically oriented strings of memory cell transistors (referred to herein as "memory strings," such as NAND memory strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term "vertical/vertically" means nominally perpendicular to the lateral surface of a substrate.

[0025] In some 3D memory devices, through stair contacts (TSCs) are used for providing vertical interconnects between a memory device and a peripheral device. In addition, dummy channel structures are used for providing structural support for the memory device. In existing fabrication processes, TSCs and dummy channel structures are formed in separate steps using different patterns. Because each pattern consumes its own share of real estate on a die, the available area on the die for other patterns becomes limited.

[0026] FIG. 6 illustrate related art using different patterns to form dummy channel structures and TSCs in separate fabrication steps. As shown in FIG. 6, a memory device 600 includes a memory stack 604 above a substrate 602. Memory stack 604 may include an array of memory strings 606 and may include a staircase structure 642. An array of dummy channel structures 602 can be formed by first etching an array of dummy holes using a dummy pattern, and then filling the dummy holes with a dielectric layer to form the dummy channel structure 602. After forming dummy channel structure 602, sacrificial layer 610 that are initially formed as part of a dielectric stack including interleaved dielectric layer 612 and sacrificial layer 610 can be replaced by conductor layers to form word lines. After the word lines are formed, a TSC pattern can be used to etch an array of TSC holes, which are subsequently filled by a conductor layer to form TSC 608. The above-described fabrication processes utilize different patterns (a dummy channel structure pattern and a TSC pattern) to form dummy channel structure 602 and TSC 608, respectively, in separate fabrication steps.

[0027] Various embodiments in accordance with the present disclosure provide a 3D memory device having TSCs sharing the same pattern for forming the dummy channel structures, which improves the efficiency of die usage. For example, by combining two separate patterns into a single pattern, the available area on the die may be increased,

allowing placement of additional patterns. Moreover, various embodiments of methods for forming the 3D memory device disclosed herein can allow TSCs to be formed in the same fabrication process(es) for making other structures (e.g., peripheral contacts) and thus, further simplify the fabrication flow and reduce process cost.

[0028] FIG. 1 illustrates a cross-section of an exemplary 3D memory device 100, according to some embodiments of the present disclosure. 3D memory device 100 can include a substrate 102, which can include silicon (e.g., single crystalline silicon), silicon germanium (SiGe), gallium arsenide (GaAs), germanium (Ge), silicon on insulator (SOI), or any other suitable materials. In some embodiments, substrate 102 is a thinned substrate (e.g., a semiconductor layer), which was thinned from a normal thickness by grinding, wet/dry etching, chemical mechanical polishing (CMP), or any combination thereof.

[0029] 3D memory device 100 can include a memory stack 104 above substrate 102. Memory stack 104 can be a stacked storage structure through which memory strings (e.g., NAND memory strings 106) are formed. In some embodiments, memory stack 104 includes a plurality of conductor/dielectric layer pairs stacked vertically above substrate 102. Each conductor/dielectric layer pair can include a conductor layer 110 and a dielectric layer 112. That is, memory stack 104 can include interleaved conductor layers 110 and dielectric layers 112 stacked vertically. As shown in FIG. 1, each NAND memory string 106 extends vertically through interleaved conductor layers 110 and dielectric layers 112 in memory stack 104. In some embodiments, 3D memory device 100 is a NAND Flash memory device in which memory cells are provided at intersections of NAND memory strings 106 and conductor layers 110 (functioning as word lines) of 3D memory device 100. The number of conductor/dielectric layer pairs in memory stack 104 (e.g., 32, 64, 96, or 128) can set the number of memory cells in 3D memory device 100.

[0030] Conductor layers 110 can each have the same thickness or have different thicknesses. Similarly, dielectric layers 112 can each have the same thickness or have different thicknesses. Conductor layers 110 can include conductive materials including, but not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), polycrystalline silicon (polysilicon), doped silicon, silicides, or any combination thereof. Dielectric layers 112 can include dielectric materials including, but not limited to, silicon oxide,

silicon nitride, silicon oxynitride, or any combination thereof. In some embodiments, conductor layers 110 include metals, such as W, and dielectric layers 112 include silicon oxide. It is understood that a silicon oxide film (not shown), such as an in-situ steam generation (ISSG) silicon oxide, can be formed between substrate 102 (e.g., a silicon substrate) and memory stack 104, according to some embodiments.

[0031] It is noted that *x*, *y*, and z axes are added to FIG. 1 to further illustrate the spatial relationship of the components in 3D memory device 100 (*y*-direction points into the page). The *x*-, *y*-, and *z*-directions are perpendicular to one another. Substrate 102 includes two lateral surfaces (e.g., a top surface and a bottom surface) extending laterally in the *x*-direction and *y*-direction (the lateral direction) in the *x*-*y* plane. As used herein, whether one component (e.g., a layer or a device) is "on," "above," or "below" another component (e.g., a layer or a device) of a semiconductor device (e.g., 3D memory device 100) is determined relative to the substrate (e.g., substrate 102) of the semiconductor device in the *z*-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the *z*-direction. The same notion for describing spatial relationship is applied throughout the present disclosure.

[0032] In some embodiments, 3D memory device 100 is part of a monolithic 3D memory device, in which the components of the monolithic 3D memory device (e.g., memory cells and peripheral devices) are formed on a single substrate (e.g., substrate 102). Peripheral devices 111, such as any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 100, can be formed on substrate 102 as well, outside of memory stack 104. Peripheral device 111 can be formed "on" substrate 102, where the entirety or part of peripheral device 111 is formed in substrate 102 (e.g., below the top surface of substrate 102) and/or directly on substrate 102. Peripheral device 111 can include one or more of a page buffer, a decoder (e.g., a row decoder and a column decoder), a sense amplifier, a driver, a charge pump, a current or voltage reference, or any active or passive components of the circuits (e.g., transistors, diodes, resistors, or capacitors). Isolation regions (e.g., shallow trench isolations (STIs)) and doped regions (e.g., source regions and drain regions of the transistors) can be formed in substrate 102 as well, outside of memory stack 104. It is understood that in some embodiments, peripheral devices 111 are formed above or below NAND memory strings 106, as opposed to on the side of NAND memory strings 106 as

shown in FIG. 1. It is further understood that in some embodiments, 3D memory device 100 is part of a non-monolithic 3D memory device, in which the components are formed separately on different substrates and then bonded in a face-to-face manner, a face-to-back manner, or a back-to-back manner. Peripheral devices 111 can be formed on a separate substrate different from substrate 102.

[0033] As shown in FIG. 1, memory stack 104 can include an inner region 116 (also known as a "core array region") and an outer region 118 (also known as a "staircase region"). In some embodiments, inner region 116 is the center region of memory stack 104 where an array of NAND memory strings 106 are formed through the conductor/dielectric layer pairs, and outer region 118 is the remaining region of memory stack 104 surrounding inner region 116 (including the sides and edges) without NAND memory strings 106.

[0034] As shown in FIG. 1, each NAND memory string 106 can include a channel structure 108 extending vertically through the conductor/dielectric layer pairs in inner region 116 of memory stack 104. Channel structure 108 can include a channel hole filled with semiconductor materials (e.g., forming a semiconductor channel) and dielectric materials (e.g., forming a memory film). In some embodiments, the semiconductor channel includes silicon, such as amorphous silicon, polysilicon, or single crystalline silicon. In some embodiments, the memory film is a composite layer including a tunneling layer, a storage layer (also known as a "charge trap/storage layer"), and a blocking layer. Each NAND memory string 106 can have a cylinder shape (e.g., a pillar shape). The semiconductor channel, tunneling layer, storage layer, and blocking layer are arranged along a direction from the center toward the outer surface of the pillar in this order, according to some embodiments. The tunneling layer can include silicon oxide, silicon oxynitride, or any combination thereof. The storage layer can include silicon nitride, silicon oxynitride, silicon, or any combination thereof. The blocking layer can include silicon oxide, silicon oxynitride, high dielectric constant (high-k) dielectrics, or any combination thereof.

[0035] In some embodiments, NAND memory strings 106 include a plurality of control gates (each being part of a word line/conductor layer 110) for NAND memory strings 106. Conductor layer 110 in each conductor/dielectric layer pair can function as a control gate for memory cells of NAND memory string 106. Conductor layer 110 can include

multiple control gates for multiple NAND memory strings 106 and can extend laterally as a word line ending in outer region 118 of memory stack 104.

[0036] In some embodiments, NAND memory string 106 includes two plugs 117 and 119 at a respective end in the vertical direction. Each plug 117 or 119 can be in contact with a respective end of channel structure 108. Plug 117 can include a semiconductor material, such as silicon, that is epitaxially grown from substrate 102. Plug 117 can function as the channel controlled by a source select gate of NAND memory string 106. Plug 117 can be at the lower end of NAND memory string 106 and in contact with channel structure 108 (e.g., on the lower end of channel structure 108). As used herein, the "upper end" of a component (e.g., NAND memory string 106) is the end father away from substrate 102 in the z-direction, and the "lower end" of the component (e.g., NAND memory string 106) is the end closer to substrate 102 in the z-direction when substrate 102 is positioned in the lowest plane of 3D memory device 100.

[0037] Plug 119 can include semiconductor materials (e.g., polysilicon) or conductor materials (e.g., metals). In some embodiments, plug 119 includes an opening filled with titanium/titanium nitride (Ti/TiN as a barrier layer) and tungsten (as a conductor). By covering the upper end of channel structure 108 during the fabrication of 3D memory device 100, plug 119 can function as an etch stop layer to prevent etching of dielectrics filled in channel structure 108, such as silicon oxide and silicon nitride. In some embodiments, plug 119 functions as the drain of NAND memory string 106.

[0038] As shown in FIG. 1, at least on one side in the lateral direction (e.g., in the x-direction), outer region 118 of memory stack 104 can include a staircase structure 142. In some embodiments, another staircase structure (not shown) is disposed on the opposite side of memory stack 104 in the x-direction. Each "level" of staircase structure 142 can include one or more conductor/dielectric layer pairs, each including conductor layer 110 and dielectric layer 112. The top layer in each level of staircase structure 142 can be conductor layer 110 for interconnection in the vertical direction. In some embodiments, each two adjacent levels of staircase structure 142 are offset by a nominally same distance in the vertical direction and a nominally same distance in the lateral direction. For each two adjacent levels of staircase structure 142, the first level (and conductor layer and dielectric layer therein) that is closer to substrate 102 can extend laterally further than the

second level (and conductor layer and dielectric layer therein), thereby forming a "landing area" on the first level for interconnection in the vertical direction.

[0039] Staircase structure 142 can be used for landing word line contacts 144. The lower end of each word line contact 144 can be in contact with top conductor layer 110 (word line) in a respective level of staircase structure 142 to individually address a corresponding word line of 3D memory device 100. Word line contact 144 can include an opening (e.g., a via hole or a trench) extending vertical through one or more dielectric layers and filled with conductive materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof.

[0040] As shown in FIG. 1, 3D memory device 100 further includes TSCs 136 each extending vertically through the conductor/dielectric layer pairs in staircase structure 142. Each TSC 136 can extend vertically through interleaved conductor layers 110 and dielectric layers 112. In some embodiments, TSC 136 can extend through the entire thickness of staircase structure 142 (e.g., all the conductor/dielectric layer pairs in the vertical direction at a lateral position of staircase structure 142) and reach substrate 102. In some embodiments, TSC 136 further extends through at least part of substrate 102. TSC 136 can carry electrical signals from and/or to 3D memory device 100, such as part of the power bus, with shorten interconnect routing. In some embodiments, TSC 136 can provide electrical connections between 3D memory device 100 and peripheral device 111 and/or between back-end-of-line (BEOL) interconnects (not shown) and peripheral device 111. TSC 136 can also provide mechanical support to staircase structure 142.

[0041] TSC 136 can be formed by filling materials in a vertical opening through staircase 142. In some embodiments, TSC 136 includes a conductor layer 140 surrounded by a spacer 138. For example, the sidewall of TSC 136 may be in contact with spacer 138. Conductor layer 140 can include conductive materials, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. Spacer 138 can electrically insulate conductor layer 140 of TSC 136 from surrounding conductor layers 110 in staircase structure 142. In some embodiments, TSC 136 has a substantially circular shape in the plan view, and conductor layer 140 and spacer 138 are disposed radially from the center of TSC 136 in this order. Spacer 138 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

[0042] As shown in FIG. 1, 3D memory device 100 can further include peripheral contacts 148 extending vertically through one or more dielectric layers and in contact with peripheral devices 111 outside of memory stack 104. Peripheral contact 148 can provide electrical connections with peripheral devices 111. Peripheral contact 148 can be formed by filling materials in a vertical opening. In some embodiments, similar to TSC 136, peripheral contact 148 may include a conductor layer 152 surrounded by a spacer 150. Conductor layer 152 can include conductive materials, including, but not limited to, W, Co, Cu, Al, doped silicon, silicides, or any combination thereof. In some embodiments, peripheral contact 148 has a substantially circular shape in the plan view, and conductor layer 152 and spacer 150 are disposed radially from the center of peripheral contact 148 in this order. Spacer 150 can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof. In some embodiments, spacer 150 and spacer 138 have nominally the same thickness in the lateral direction (e.g., radial direction). In some embodiments, both spacer 150 and spacer 138 include silicon oxide. It is understood that peripheral devices 111 may not be formed on substrate 102, and peripheral contacts 148 may be in a different configuration in some embodiments, for example, in which 3D memory device 100 is a non-monolithic 3D memory device.

[0043] It is understood that 3D memory device 100 can include additional components and structures not shown in FIG. 1 including, but not limited to, other local contacts and interconnects in one or more BEOL interconnect layers above memory stack 104 and/or below substrate 102.

[0044] FIGS. 2A–2C illustrate an exemplary fabrication process for forming channel structures and staircase structures of a 3D memory device, according to some embodiments of the present disclosure. FIGS. 3A–3E illustrate an exemplary fabrication process for forming TSCs, peripheral contacts, and word line contacts of a 3D memory device, according to various embodiments of the present disclosure. FIGS. 4A–4D illustrate another exemplary fabrication process for forming TSCs, peripheral contacts, and word line contacts of a 3D memory device, according to some embodiments of the present disclosure. FIGS. 5A-5C are flowcharts of exemplary methods 500, 500’, and 500” for forming a 3D memory device, according to some embodiments. Examples of the 3D memory device depicted in FIGS. 2-5 include 3D memory device 100 depicted in

FIG. 1. FIGS. 2-5 will be described together. It is understood that the operations shown in methods 500, 500', and 500" are not exhaustive and that other operations can be performed as well before, after, or between any of the illustrated operations. Further, some of the operations may be performed simultaneously, or in a different order than shown in FIGS. 5A-5C.

[0045] Referring to FIG. 5A, method 500 starts at operation 502, in which a dielectric stack including a plurality of interleaved dielectric layers and sacrificial layers is formed on a substrate. The substrate can be a silicon substrate. Method 500 proceeds to operation 504, as illustrated in FIG. 5A, in which a channel structure extending vertically through the dielectric stack is formed. Method 500 proceeds to operation 506, in which a staircase structure is formed on one side of the dielectric stack.

[0046] As illustrated in FIG. 2A, a dielectric deck 204 including a plurality of interleaved dielectric layers and sacrificial layers is formed on a silicon substrate 202. In some embodiments, sacrificial layers 206 and dielectric layers 208 are alternatingly deposited by one or more thin film deposition processes including, but not limited to, physical vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), or any combination thereof. In some embodiments, sacrificial layers 206 include silicon nitride, and dielectric layers 208 include silicon oxide. It is understood that the sequence of depositing sacrificial layers 206 and dielectric layers 208 is not limited. The deposition can start with sacrificial layer 206 or dielectric layer 208 and can end with sacrificial layer 206 or dielectric layer 208.

[0047] As illustrated in FIG. 2B, an array of channel structures 210 are formed, each of which extends vertically through interleaved sacrificial layers 206 and dielectric layers 208 in dielectric deck 204. In some embodiments, fabrication processes to form channel structure 210 include forming a channel hole through interleaved sacrificial layers 206 and dielectric layers 208 in dielectric deck 204 using dry etching/and or wet etching, such as deep reactive-ion etching (DRIE), followed by filling the channel hole with a plurality of layers, such as a dielectric layer and a semiconductor layer, using thin film deposition processes. In some embodiments, the dielectric layer is a composite dielectric layer, such as a combination of multiple dielectric layers including, but not limited to, a tunneling layer, a storage layer, and a blocking layer. The tunneling layer can include dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or

any combination thereof. The storage layer can include materials for storing charge for memory operation. The storage layer materials can include, but not limited to, silicon nitride, silicon oxynitride, a combination of silicon oxide and silicon nitride, or any combination thereof. The blocking layer can include dielectric materials including, but not limited to, silicon oxide or a combination of silicon oxide/silicon oxynitride/silicon oxide (ONO). The blocking layer can further include a high-k dielectric layer, such as an aluminum oxide (Al_2O_3) layer. The semiconductor layer can include polysilicon, serving as a semiconductor channel. The semiconductor layer and dielectric layer can be formed by processes such as ALD, CVD, PVD, or any combination thereof.

[0048] In some embodiments, dielectric stack 204 may be a joined by another dielectric stack to form a multi-stack structure through a joint layer 212. As illustrated in FIG. 2B, joint layer 212 can be formed on dielectric deck 204 by depositing a dielectric layer, such as a silicon oxide layer, using thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof. An array of inter-deck plugs 214 can be formed in joint layer 212 and in contact with the array of channel structures 210, respectively. Inter-deck plugs 214 can be formed by patterning and etching openings through joint layer 212, followed by deposition of semiconductor materials, such as polysilicon, using thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof. In the following, embodiments of the present disclosure are described with respect to a single-stack structure for conciseness and simplicity. It is understood that technical solutions disclosed herein are applicable to multi-stack structure as well.

[0049] As illustrated in FIG. 2C, staircase structures 224 are formed on the sides of dielectric stack 218. Staircase structure 224 can be formed by the so-called "trim-etch" processes, which, in each cycle, trim (e.g., etching incrementally and inwardly, often from all directions) a patterned photoresist layer, followed by etching the exposed portions of the dielectric/sacrificial layer pair using the trimmed photoresist layer as an etch mask to form one step of staircase structure 224.

[0050] Method 500 proceeds to operation 508, as illustrated in FIG. 5A, in which a dummy channel structure extending vertically through the staircase structure is formed. In some embodiments, dummy channel structures are formed as intermediate structures that are later replaced by TSCs. As illustrated in FIG. 3B, an array of dummy channel

structures 302 are formed through a staircase structure 342 of a dielectric stack 304. Dielectric stack 304 includes interleaved dielectric layers 312 and sacrificial layers 310.

[0051] Dummy channel structure 302 can extend vertically through staircase structure 342 and have a vertical opening filled with the same materials as those in channel structure 108. Different from channel structures 108, a contact is not formed on dummy channel structure 302 to provide electrical connections with other components of a 3D memory device such as 3D memory device 100, according to some embodiments. In some embodiments, dummy channel structure 302 is fully filled with dielectric materials including, but not limited to, silicon oxide, silicon nitride, silicon oxynitride, or any combination thereof.

[0052] Dummy channel structure 302 can be used for balancing load in certain processes during fabrication (e.g., etching and chemical mechanical polishing (CMP)) and for providing mechanical support to memory array structures, e.g., staircase structure 342. Embodiments of the present disclosure can form TSCs from dummy channel structures, thereby using the same pattern to form both the dummy channel structures and TSCs. The resulting TSCs can provide the balancing and supporting functions of the dummy channel structures.

[0053] As shown in FIG. 3A, dummy channel structure 302 can be formed by first etching a dummy hole 322 through one or more dielectric layers in staircase structure 342 using wet etching and/or dry etching, such as DRIE. In some embodiments, dummy hole 322 may extend vertically through all of the dielectric layers in staircase structure 342 and expose part of silicon substrate 202 (e.g., dummy hole 322 may extend to silicon substrate 202). In some embodiments, dummy hole 322 may extend into silicon substrate 202 (e.g., part of silicon substrate 202 may be etched away during the etching process).

[0054] In some embodiments, a dummy hole 324 outside dielectric stack 304 may be formed simultaneously (e.g., in the same fabrication steps) with forming dummy hole 322. Dummy hole 324 may be used to form a peripheral contact providing interconnect to a peripheral device 311. In some embodiments, dummy holes 322 and 324 may have a nominally circular shape in plan view, as shown in FIG. 3A. In some embodiments, the size of dummy holes 322 and 324 may be nominally the same.

[0055] Referring back to FIG. 3B, dummy holes 322 shown in FIG. 3A may be filled (deposited) with a dielectric layer 352, such as a silicon oxide layer, to form dummy

channel structures 302 using one or more thin film deposition processes, such as ALD, CVD, PVD, or any combination thereof. In some embodiments, dummy channel structures 302 are formed simultaneously with channel structures 210 in the same fabrication steps, such that dummy holes 322 is filled with at least some of the materials filling in channel structures 210.

[0056] In some embodiments, a dummy channel structure 303 outside dielectric stack 304 is formed simultaneously (e.g., in the same fabrication steps) with forming dummy channel structure 302 by depositing a dielectric layer 354 in dummy hole 324. Dielectric layer 354 may have the same material as dielectric layer 352.

[0057] In some embodiments, dummy holes 322/324 may be fully filled with dielectric layer 352/354, respectively. In other embodiments, dummy holes 322 or 324 may be partially filled, as shown in FIG. 3B. In such cases, the resulting dummy channel structure 302/303 may have the top, bottom, and sidewall portions deposited with dielectric layer 352/354. The center region may not be fully filled.

[0058] Method 500 proceeds to operation 510, as illustrated in FIG. 5, in which a plurality of word lines are formed by replacing the sacrificial layers in the dielectric stack with conductor layers. As shown in FIG. 3C, sacrificial layers 310 are replaced by conductor layers (functioned as word lines) 309. The replacement of sacrificial layers 310 with conductor layers 309 can be performed by wet etching sacrificial layers 310 (e.g., silicon nitride) selective to dielectric layers 304 (e.g., silicon oxide) and filling the structure with conductor layers 309 (e.g., W). Conductor layers 309 can be deposited by PVD, CVD, ALD, electrochemical depositions, or any combination thereof. Conductor layers 309 can include conductive materials including, but not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. As a result, after the gate replacement processes, dielectric stack 304 in FIGS. 3A-3B becomes a memory stack 305 including the conductor/dielectric layer pairs, i.e., interleaved conductor layers 309 and dielectric layers 312, on silicon substrate 202.

[0059] Method 500 proceeds to operation 512, in which an opening extending vertically through a center portion of the dummy channel structure is etched to form a spacer. Referring to FIG. 3D, an opening 372 (TSC hole) is etched through dummy channel structure 302 (shown in FIGS. 3B-3C) to form a spacer 362. In some embodiments, opening 372/spacer 362 may extend vertically through the interleaved dielectric layers

312 and conductor layer 309 in staircase structure 342 to reach silicon substrate 202. In some embodiments, a second opening 374 (peripheral contact hole) may be simultaneously formed from dummy channel structure 303 (shown in FIGS. 3B-3C). Opening 372/374 may be etched using wet etching and/or drying etching process, such as DRIE. For example, a center portion of dummy channel structure 302/303 may be removed by etching to form spacer 362/364 with a hollow core, as shown in FIG. 3D. In some embodiments, the sidewalls of spacers 362 and 364 may have a nominally same thickness. The depths of TSC hole 372 and peripheral contact hole 374 in the vertical direction can be nominally the same. The lateral dimensions of TSC hole 372 and peripheral contact hole 374, such as the diameters, can be nominally the same or different in various embodiments. For example, the diameter of TSC hole 372 can be greater than the diameter of peripheral contact hole 374, according to some embodiments.

[0060] As shown in FIG. 3D, TSC hole 372 and peripheral contact hole 374 can reach to silicon substrate 202, and the lower end of peripheral contact hole 374 can be in contact with peripheral device 311 formed on silicon substrate 202. In some embodiments, peripheral device 311 includes transistors, which can be formed by a plurality of processes including, but not limited to, photolithography, dry/wet etch, thin film deposition, thermal growth, implantation, CMP, and any other suitable processes. In some embodiments, doped regions are formed in silicon substrate 202 by ion implantation and/or thermal diffusion, which function, for example, as source regions and/or drain regions of the transistors. In some embodiments, isolation regions (e.g., STIs) are also formed in silicon substrate 202 by wet etching and/or dry etching and thin film deposition processes. The fabrication process for forming peripheral device 311 can occur at any fabrication stage prior to the etching of peripheral contact hole 374.

[0061] Because opening 372/374 is etched from dummy channel structure 302/303 by removing part of the dielectric layer deposited thereon, the remaining portion, including the sidewall of the dummy channel structure 302/303 after opening 372/274 is formed, becomes spacer 362/364. Spacer 362/264 can provide mechanical support to memory stack 305, including staircase structure 342, similar to dummy channel structure 302/303. In addition, spacer 362/364 can function as an insulation layer surround the conductor layer deposited into opening 372/374 to form a TSC/peripheral contact.

[0062] In some embodiments, opening 372/374 (defined by the inner wall of spacer 362/364) may have a nominally circular shape in plan view, as shown in FIG. 3D. In some embodiments, the sidewalls of spacer 362 and 364 may have a nominally same thickness. In some embodiments, spacer 362 and 364 may have the same or different size. For example, the diameter of spacer 364 (e.g., measured from the inner or outer sidewall) may be smaller than the diameter of spacer 362.

[0063] Method 500 proceeds to operation 514, as illustrated in FIG. 5, in which word line contacts and TSCs are simultaneously formed. In some embodiments, a conductor layer is deposited in an opening to form a TSC. In some embodiments, the conductor layer is a composite layer including an adhesion/barrier layer and a conductor. As illustrated in FIG. 3E, a conductor layer 382 is deposited in opening 372 (as shown in FIG. 3D) to fill the remaining space of opening 372, thereby forming a TSC 336 extending vertically through staircase structure 342. In some embodiments, a conductor can be formed in the remaining space of opening 372 by depositing metals, such as tungsten, using one or more thin film deposition processes, such as ALD, CVD, PVD, electrochemical depositions, or any combination thereof. A conductor layer 384 can be simultaneously formed in opening 374 (as shown in FIG. 3D) to form a peripheral contact 348 in contact with peripheral device 311, using the same deposition processes. In some embodiments, conductor layers 382 and 384 may use the same material (e.g., tungsten (W)). The excess conductor layer after deposition can be removed by CMP.

[0064] Word line contacts 344 can be formed simultaneously (e.g., in the same fabrication steps) with TSCs. Each word line contact 344 is in contact with a respective one of conductor layers 309 of the conductor/dielectric layer pairs in staircase structure 342. Word line contacts 344 are formed through one or more dielectric layers by first etching vertical openings (e.g., by wet etching and/or dry etching), followed by filling the openings with conductive materials using ALD, CVD, PVD, electrochemical depositions, or any combination thereof. In some embodiments, other conductive materials are filled in the openings to function as an adhesion/barrier layer. Etching of dielectric layers to form the openings of word line contacts 344 can be controlled by etch stop at a different material. For example, etching of dielectric layers can be stopped when reaching to conductor layers 309 in staircase structure 342.

[0065] In some embodiments, TSC 336, word line contact 344, and peripheral contact 348 may have a nominally circular shape in a plan view, as shown in FIG. 3E. TSC 336, word line contact 344, and peripheral contact 348 may have the same or different sizes. For example, TSC 336 and peripheral contact 348 may have a larger diameter than that of word line contact 344, according to some embodiments.

[0066] FIG. 5B is a flowchart of another exemplary method 500' for forming a 3D memory device, according to some embodiments of the present disclosure. Operations 502', 504', 506', and 508' are similar to operations 502, 504, 506, and 508, respectively, and thus are not repeated. Method 500' proceeds to operation 520, as illustrated in FIG. 5B, in which an opening is etched extending vertically through a center portion of the dummy channel structure to form a spacer. Operation 520 is similar to operation 512, with a difference that etching of the opening in operation 520 is performed before forming word lines. As illustrated in FIG. 4A, opening 372/374 are etched before sacrificial layer 310 are replaced by conductor layer 309.

[0067] Method 500' proceeds to operation 522, as illustrated in FIG. 5B, in which a TSC is formed extending vertically through the staircase structure by depositing a conductor layer in the opening. Operation 522 is similar to 514 in terms of forming the TSC. Unlike operation 514, in which word line contacts are formed simultaneously with TSCs, in operation 522, word line contacts are not formed because word lines are not yet formed prior to operation 522. Referring to FIG. 4B, TSCs 336 is formed before sacrificial layers 310 are replaced by conductor layer 309.

[0068] Method 500' proceeds to operation 524, as illustrated in FIG. 5B, in which word lines are formed by replacing the sacrificial layers in the dielectric stack with conductor layers. Operation 524 is similar to operation 510. Referring to FIG. 4C, word lines 309 are formed by replacing sacrificial layer 310 with conductor layer 309. Note that in FIG. 4C, TSC 336 and peripheral contact 348 have been formed.

[0069] Method 500' proceeds to operation 526, as illustrated in FIG. 5B, in which word line contacts are formed. Operation 526 is similar to operation 514 in terms of forming word lines. As illustrated in FIG. 4D, word line contacts 344 are formed after TSC 336 and peripheral contact 348 are formed.

[0070] FIG. 5C is a flowchart of a further exemplary method 500" for forming a 3D memory device, according to some embodiments of the present disclosure. Operations

502", 504", and 506" are similar to operations 502, 504, and 506, respectively, and thus are not repeated. Method 500" proceeds to operation 530, as illustrated in FIG. 5C, in which a dummy hole is formed extending vertically through the staircase structure. As shown in FIG. 3A, dummy hole 322 may be formed through one or more dielectric layers in staircase structure 342 using wet etching and/or dry etching, such as DRIE. In some embodiments, dummy hole 322 may extend vertically through all of the dielectric layers in staircase structure 342 and reach silicon substrate 202. In some embodiments, dummy hole 322 may extend into silicon substrate 202 (e.g., part of silicon substrate 202 may be etched away during the etching process).

[0071] In some embodiments, a dummy hole 324 outside dielectric stack 304 may be formed simultaneously (e.g., in the same fabrication steps) with forming dummy hole 322. Dummy hole 324 may be used to form a peripheral contact providing interconnect to a peripheral device 311. In some embodiments, dummy holes 322 and 324 may have a nominally circular shape in plan view, as shown in FIG. 3A. In some embodiments, the size of dummy holes 322 and 324 may be nominally the same.

[0072] Method 500" proceeds to operation 532, as illustrated in FIG. 5C, in which a spacer having a hollow core is formed in the dummy hole. As shown in FIGS. 3B-3D, spacer 362 may be formed by depositing a dielectric layer 352 into dummy hole 322, followed by removing part of the dielectric layer 352 to form spacer 362, as described above in connection with steps 512 and 520. In some embodiments, spacer 362 may be formed directly by depositing dielectric layer 352 into dummy hole 322, without an additional etching operation to remove part of the deposited dielectric material to form spacer 362. Spacer 364 may be formed in a similar manner.

[0073] Method 500" proceeds to operation 534, as illustrated in FIG. 5C, in which a TSC is formed extending vertically through the staircase structure by depositing a conductor layer in the hollow core of the spacer. Operation 534 is similar to operation 522.

[0074] Method 500" proceeds to operation 536, as illustrated in FIG. 5C, in which word lines are formed by replacing the sacrificial layers in the dielectric stack with conductor layers. Operation 536 is similar to operation 524. Referring to FIG. 4C, word lines 309 are formed by replacing sacrificial layer 310 with conductor layer 309. Note that in FIG. 4C, TSC 336 and peripheral contact 348 have been formed.

[0075] Method 500" proceeds to operation 538, as illustrated in FIG. 5C, in which word line contacts are formed. Operation 538 is similar to operation 526. As illustrated in FIG. 4D, word line contacts 344 are formed after TSC 336 and peripheral contact 348 are formed.

[0076] According to one aspect of the present disclosure, a method for forming a 3D memory device is provided. A dielectric stack including a plurality of interleaved dielectric layers and sacrificial layers is formed on a substrate. A staircase structure is formed on one side of the dielectric stack. A dummy hole extending vertically through the staircase structure and reaching the substrate is formed. A spacer having a hollow core is formed in the dummy hole. A TSC in contact with the substrate is formed by depositing a conductor layer in the hollow core of the spacer. The TSC extends vertically through the staircase structure.

[0077] In some embodiments, prior to forming the spacer, a plurality of word lines are formed by replacing the sacrificial layers in the dielectric stack with conductor layers.

[0078] In some embodiments, a plurality of word line contacts each in contact with a respective one of the word lines are formed simultaneously with forming the TSC.

[0079] In some embodiments, after forming the TSC, a plurality of word lines are formed by replacing the sacrificial layers in the dielectric stack with conductor layers.

[0080] In some embodiments, a plurality of word line contacts each in contact with a respective one of the word lines are formed.

[0081] In some embodiments, to form the spacer, a dielectric layer is formed in the dummy hole.

[0082] In some embodiments, the dielectric layer includes silicon oxide.

[0083] In some embodiments, the dielectric layer forms the spacer.

[0084] In some embodiments, to form the spacer, the hollow core is etched through the dielectric layer deposited in the dummy hole.

[0085] In some embodiments, a second dummy hole outside the dielectric stack is formed simultaneously with the dummy hole.

[0086] In some embodiments, a peripheral contact is formed by depositing a second conductor layer in the second dummy hole simultaneously with forming the TSC. The peripheral contact is in contact with the substrate.

[0087] In some embodiments, the first and second conductor layers include the same material.

[0088] In some embodiments, the TSC has a nominally circular shape in a plan view.

[0089] In some embodiments, the conductor layer includes tungsten (W).

[0090] In some embodiments, the dielectric layers in the interleaved dielectric layers and sacrificial layers include silicon oxide, and the sacrificial layers in the interleaved dielectric layers and sacrificial layers include silicon nitride.

[0091] According to another aspect of the present disclosure, a method for forming a 3D memory device is provided. A dielectric stack including a plurality of interleaved dielectric layers and sacrificial layers is formed on a substrate. A staircase structure is formed on one side of the dielectric stack. A dummy channel structure reaching the substrate is formed. The dummy channel structure extends vertically through the staircase structure. A spacer is formed by removing part of the dummy channel structure. The spacer has a hollow core. A TSC in contact with the substrate is formed by depositing a conductor layer in the hollow core of the spacer. The TSC extends vertically through the staircase structure.

[0092] In some embodiments, prior to forming the spacer, a plurality of word lines are formed by replacing the sacrificial layers in the dielectric stack with conductor layers.

[0093] In some embodiments, a plurality of word line contacts each in contact with a respective one of the word lines are formed simultaneously with forming the TSC.

[0094] In some embodiments, after forming the TSC, a plurality of word lines are formed by replacing the sacrificial layers in the dielectric stack with conductor layers.

[0095] In some embodiments, a plurality of word line contacts each in contact with a respective one of the word lines are formed.

[0096] In some embodiments, prior to forming the dummy channel structure, a dummy hole extending vertically through the staircase structure and exposing part of the substrate is formed.

[0097] In some embodiments, to form the dummy channel structure, a dielectric layer is deposited in the dummy hole.

[0098] In some embodiments, the dielectric layer includes silicon oxide.

[0099] In some embodiments, to form the spacer, an opening is etched through the dielectric layer deposited in the dummy hole.

[0100] In some embodiments, to form the spacer, part of the dielectric layer deposited in the dummy hole is removed.

[0101] In some embodiments, a second spacer outside the dielectric stack is formed simultaneously with the spacer.

[0102] In some embodiments, a peripheral contact is formed by depositing a second conductor layer in the second spacer simultaneously with forming the TSC. The peripheral contact is in contact with the substrate.

[0103] In some embodiments, the first and second conductor layers include the same material.

[0104] In some embodiments, the spacer and the second space have a nominally same thickness.

[0105] In some embodiments, the conductor layer includes tungsten (W).

[0106] In some embodiments, the dielectric layers in the interleaved dielectric layers and sacrificial layers include silicon oxide, and the sacrificial layers in the interleaved dielectric layers and sacrificial layers include silicon nitride.

[0107] According to yet another aspect of the present disclosure, a 3D memory device is provided. The 3D memory device includes a substrate, a memory stack on the substrate including a plurality of interleaved conductor layers and dielectric layers, a staircase structure on one side of the memory stack, and a TSC extending vertically through the staircase structure of the memory stack. The TSC is in contact with the substrate.

[0108] In some embodiments, the 3D memory device further includes a peripheral contact outside of the memory stack. The peripheral contact is in contact with the substrate.

[0109] In some embodiments, the peripheral contact and the TSC include the same material.

[0110] In some embodiments, a sidewall of each of the TSC and peripheral contact is surrounded by a spacer with a nominally same thickness.

[0111] In some embodiments, the spacer includes silicon oxide.

[0112] In some embodiments, the 3D memory device further includes a plurality of word line contacts each in contact with a respective one of the conductor layers in the staircase structure.

[0113] The foregoing description of the specific embodiments will so reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0114] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0115] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0116] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A method for forming a three-dimensional (3D) memory device, comprising:

forming a dielectric stack on a substrate, the dielectric stack comprising a plurality of interleaved dielectric layers and sacrificial layers;

forming a staircase structure on at least one side of the dielectric stack;

forming a dummy hole extending vertically through the staircase structure and reaching the substrate;

forming a spacer in the dummy hole, the spacer having a hollow core; and

forming a through stair contact (TSC) in contact with the substrate by depositing a conductor layer in the hollow core of the spacer, the TSC extending vertically through the staircase structure.

2. The method of claim 1, further comprising prior to forming the TSC, forming a plurality of word lines by replacing the sacrificial layers in the dielectric stack with conductor layers.

3. The method of claim 2, further comprising forming a plurality of word line contacts each in contact with a respective one of the word lines simultaneously with forming the TSC.

4. The method of claim 1, further comprising after forming the TSC, forming a plurality of word lines by replacing the sacrificial layers in the dielectric stack with conductor layers.

5. The method of claim 4, further comprising forming a plurality of word line contacts each in contact with a respective one of the word lines.

6. The method of any one of claims 1 to 5, wherein forming the spacer comprising depositing a dielectric layer in the dummy hole.

7. The method of claim 6, wherein the dielectric layer comprises silicon oxide.

8. The method of claim 6 or 7, wherein the dielectric layer forms the spacer.

9. The method of claim 6 or 7, wherein forming the spacer comprises etching the hollow core through the dielectric layer deposited in the dummy hole.

10. The method of any one of claims 1 to 9, further comprising forming a second dummy hole outside the dielectric stack simultaneously with forming the dummy hole.

11. The method of claim 10, further comprising forming a peripheral contact by depositing a second conductor layer in the second dummy hole simultaneously with forming the TSC, wherein the peripheral contact is in contact with the substrate.

12. The method of claim 11, wherein the first and second conductor layers comprise a same material.

13. The method of any one of claims 1 to 12, wherein the TSC has a nominally circular shape in a plan view.

14. The method of any one of claims 1 to 13, wherein the conductor layer comprises tungsten (W).

15. The method of any one of claims 1 to 14, wherein:

the dielectric layers in the interleaved dielectric layers and sacrificial layers comprise silicon oxide; and

the sacrificial layers in the interleaved dielectric layers and sacrificial layers comprise silicon nitride.

16. A method for forming a three-dimensional (3D) memory device, comprising:

forming a dielectric stack comprising a plurality of interleaved dielectric layers and sacrificial layers on a substrate;

forming a staircase structure on at least one side of the dielectric stack;

forming a dummy channel structure reaching the substrate, the dummy channel structure extending vertically through the staircase structure;

forming a spacer by removing part of the dummy channel structure, the spacer having a hollow core; and

forming a through stair contact (TSC) in contact with the substrate by depositing a conductor layer in the hollow core of the spacer, the TSC extending vertically through the staircase structure.

17. The method of claim 16, further comprising prior to forming the spacer, forming a plurality of word lines by replacing the sacrificial layers in the dielectric stack with conductor layers.

18. The method of claim 17, further comprising forming a plurality of word line contacts each in contact with a respective one of the word lines simultaneously with forming the TSC.

19. The method of claim 16, further comprising after forming the TSC, forming a plurality of word lines by replacing the sacrificial layers in the dielectric stack with conductor layers.

20. The method of claim 19, further comprising forming a plurality of word line contacts each in contact with a respective one of the word lines.

21. The method of any one of claims 16 to 20, further comprising prior to forming the dummy channel structure, forming a dummy hole extending vertically through the staircase structure and exposing part of the substrate.

22. The method of claim 21, wherein forming the dummy channel structure comprises depositing a dielectric layer in the dummy hole.

23. The method of claim 22, wherein the dielectric layer comprises silicon oxide.

24. The method of claims 22 or 23, wherein forming the spacer comprises etching an opening through the dielectric layer deposited in the dummy hole.

25. The method of any one of claims 22 to 24, wherein forming the spacer comprises removing part of the dielectric layer deposited in the dummy hole.

26. The method of any one of claims 16 to 25, further comprising forming a second spacer outside the dielectric stack simultaneously with forming the spacer.

27. The method of claim 26, further comprising forming a peripheral contact by depositing a second conductor layer in the second spacer simultaneously with forming the TSC, wherein the peripheral contact is in contact with the substrate.

28. The method of claim 27, wherein the first and second conductor layers comprise a same material.

29. The method of any one of claims 26 to 28, wherein the spacer and the second spacer have a nominally same thickness.

30. The method of any one of claims 16 to 29, wherein the conductor layer comprises tungsten (W).

31. The method of any one of claims 16 to 30, wherein:

the dielectric layers in the interleaved dielectric layers and sacrificial layers comprise silicon oxide; and

the sacrificial layers in the interleaved dielectric layers and sacrificial layers comprise silicon nitride.

32. A three-dimensional (3D) memory device, comprising:

a substrate;

a memory stack on the substrate comprising a plurality of interleaved conductor layers and dielectric layers;

a staircase structure on one side of the memory stack; and

a through stair contact (TSC) extending vertically through the staircase structure of the memory stack, wherein the TSC is in contact with the substrate.

33. The 3D memory device of claim 32, further comprising:

a peripheral contact outside of the memory stack, wherein the peripheral contact is in contact with the substrate.

34. The 3D memory device of claim 33, wherein the peripheral contact and the TSC comprise a same material.

35. The 3D memory device of claim 33 or 34, wherein a sidewall of each of the TSC and peripheral contact is surrounded by a spacer with a nominally same thickness.

36. The 3D memory device of claim 35, wherein the spacer comprises silicon oxide.

37. The 3D memory device of any one of claims 32 to 36, further comprising:

a plurality of word line contacts each in contact with a respective one of the conductor layers in the staircase structure.

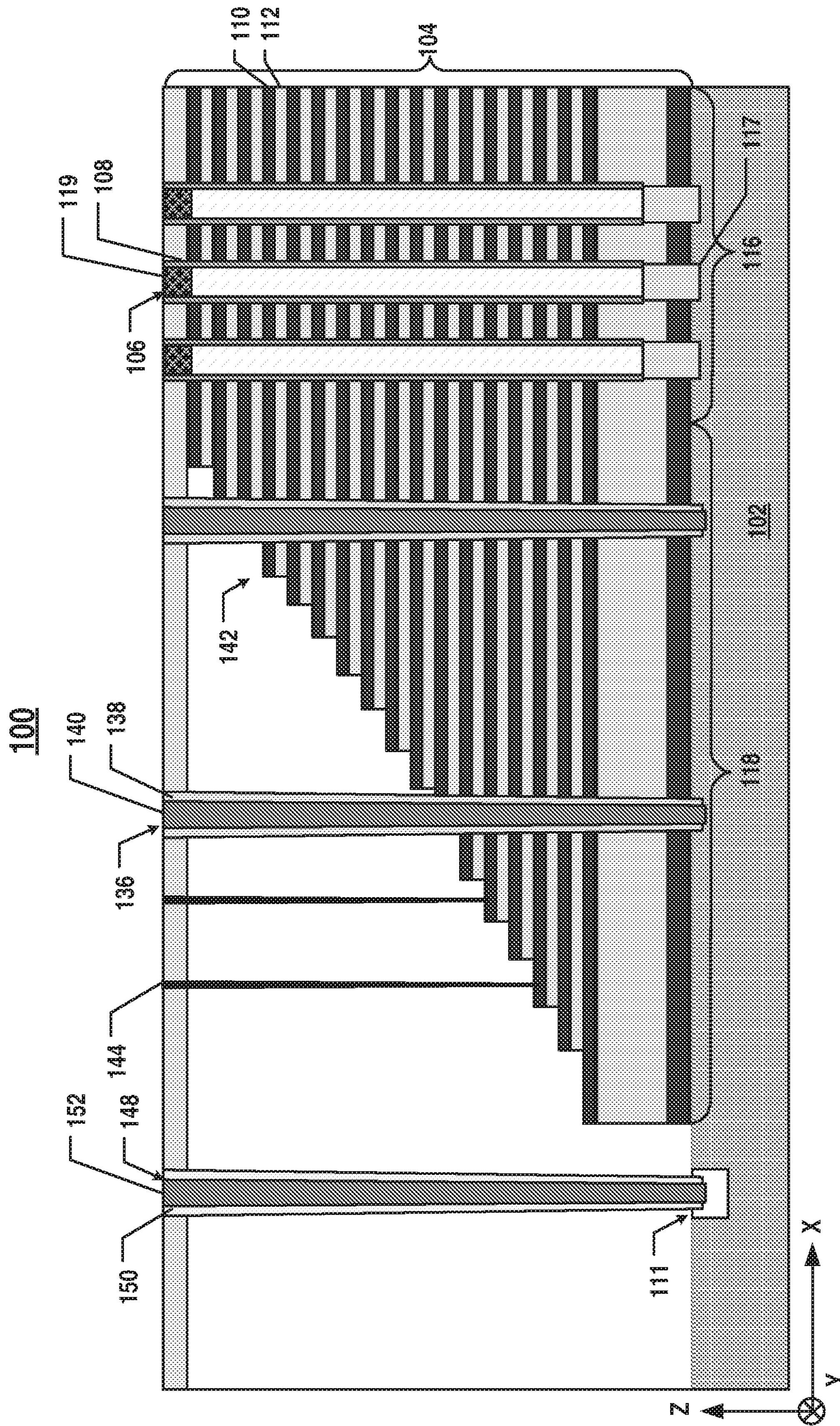

FIG. 1

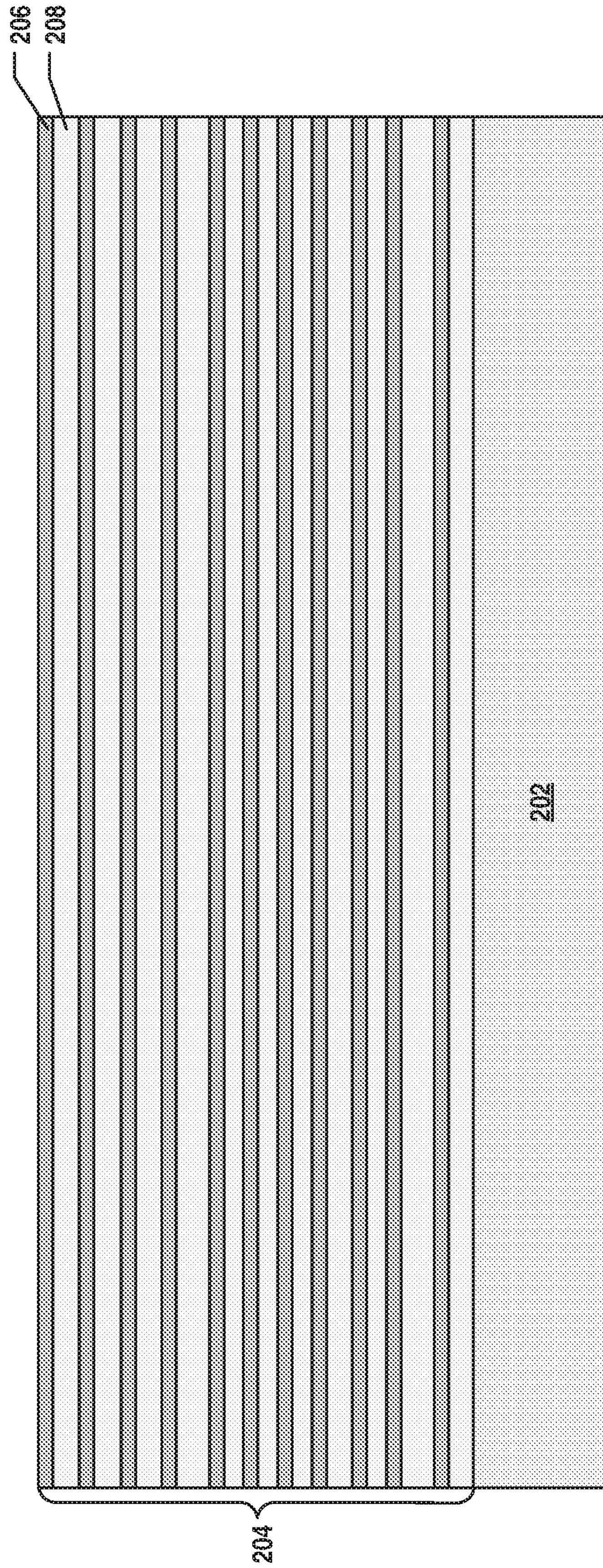

FIG. 2A

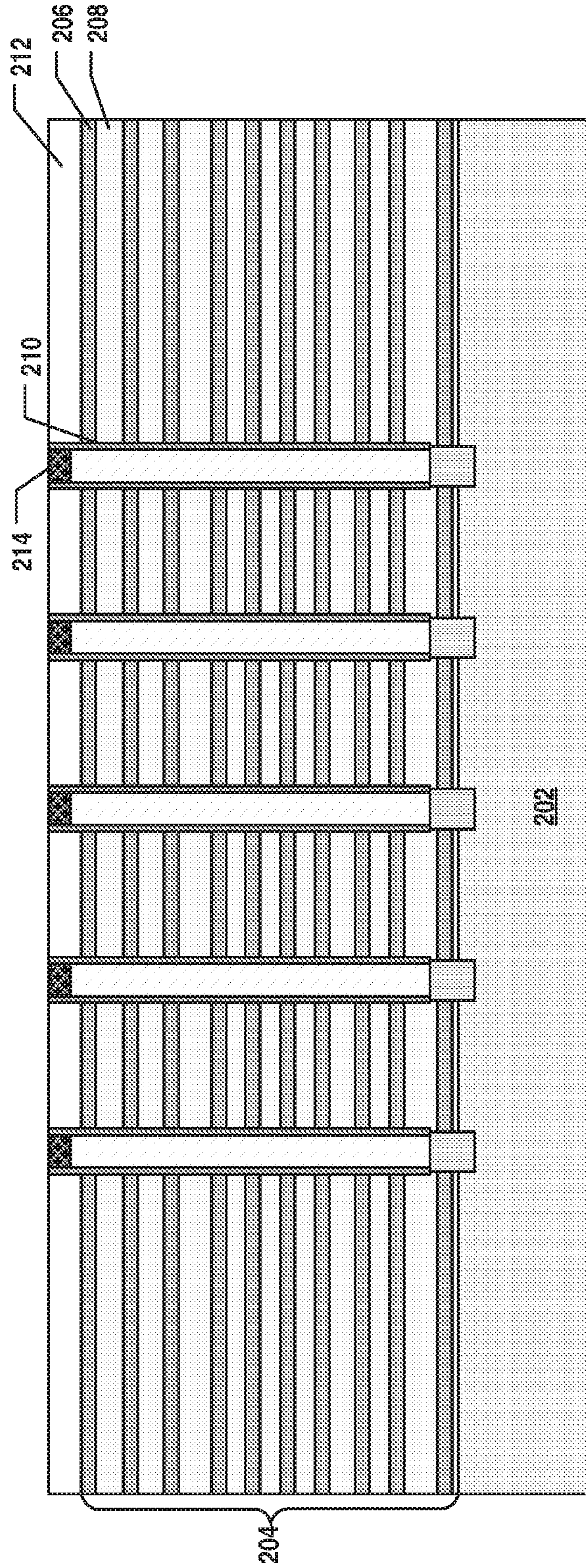

FIG. 2B

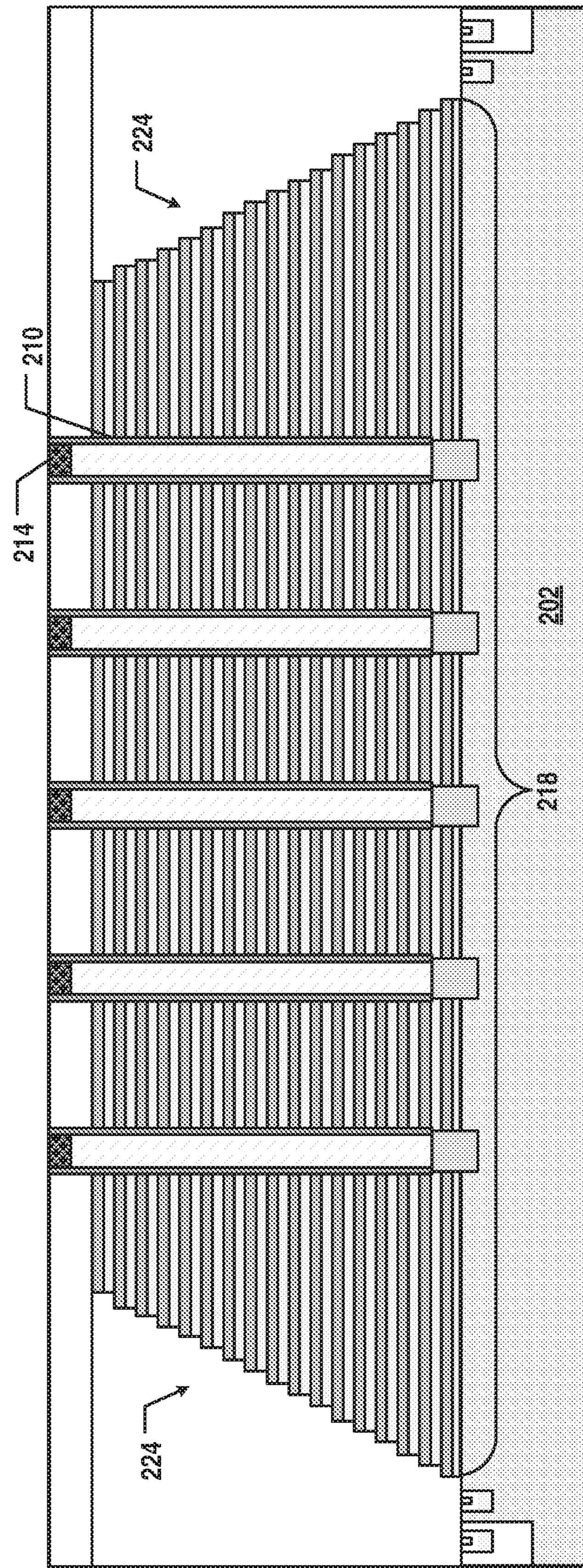

FIG. 2C

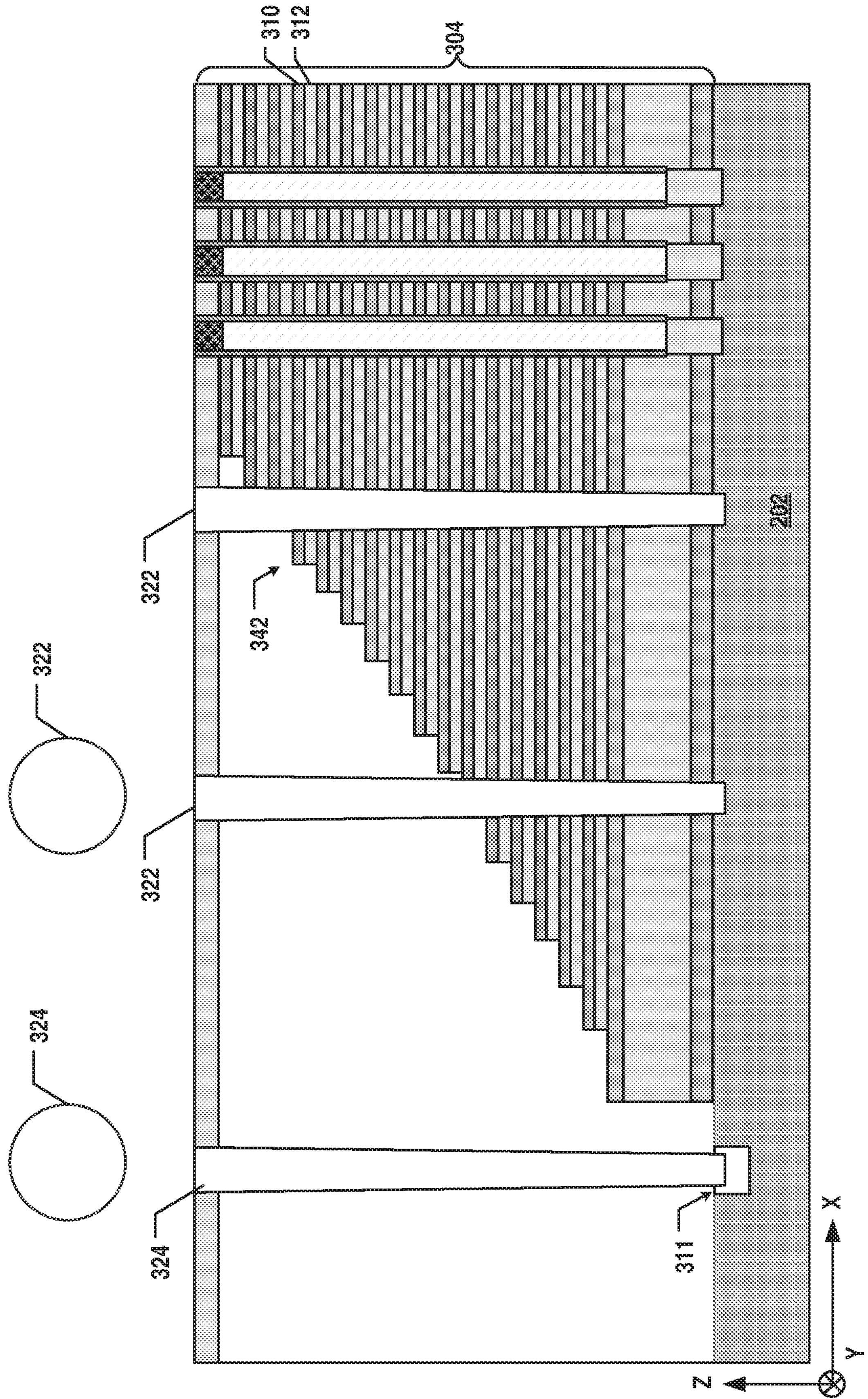
310
312
304
322
322
342
322
324
324
311
202
X
Y
Z
FIG. 3A

FIG. 3B

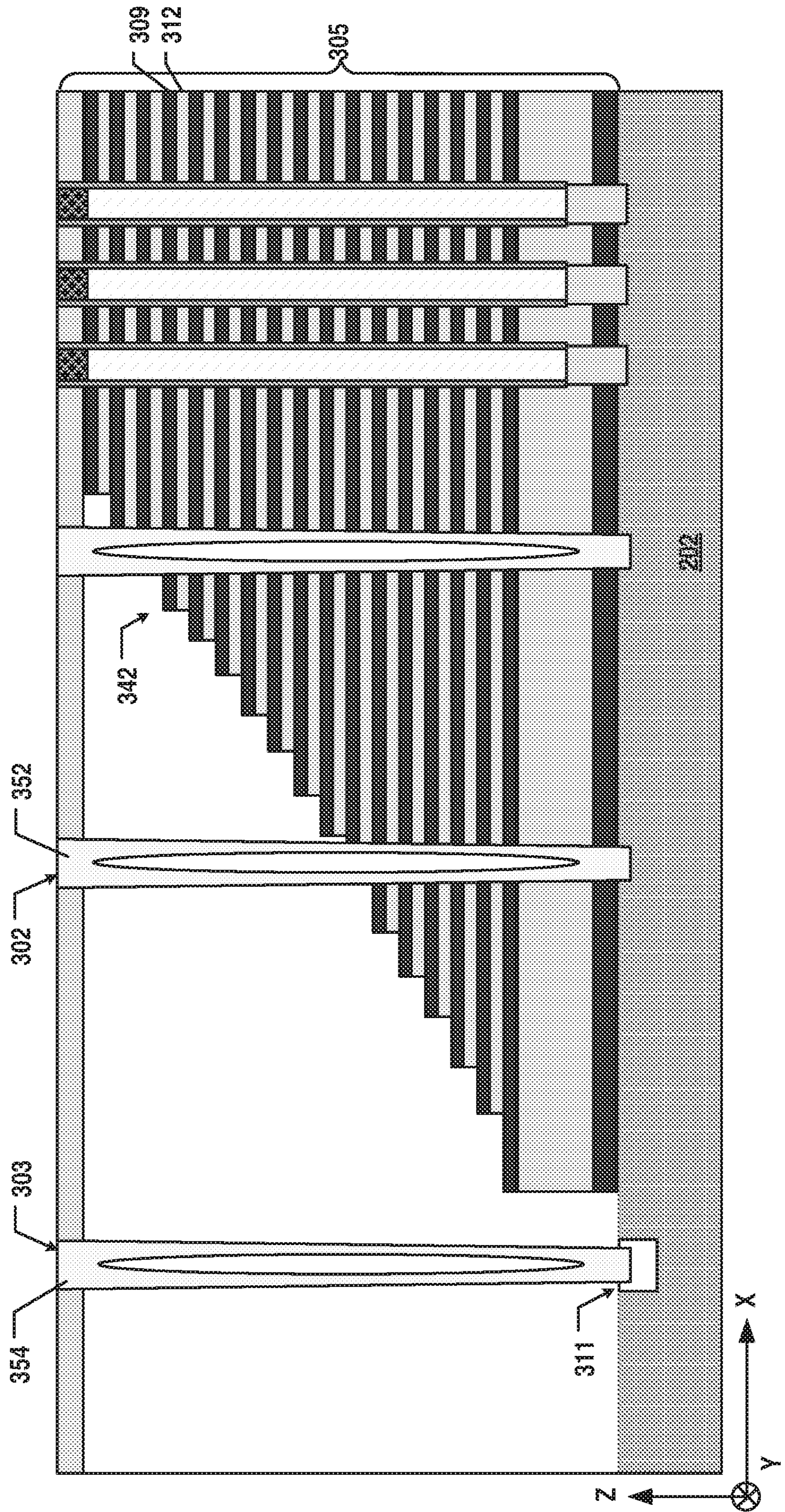

FIG. 3C

FIG. 3D

FIG. 3E

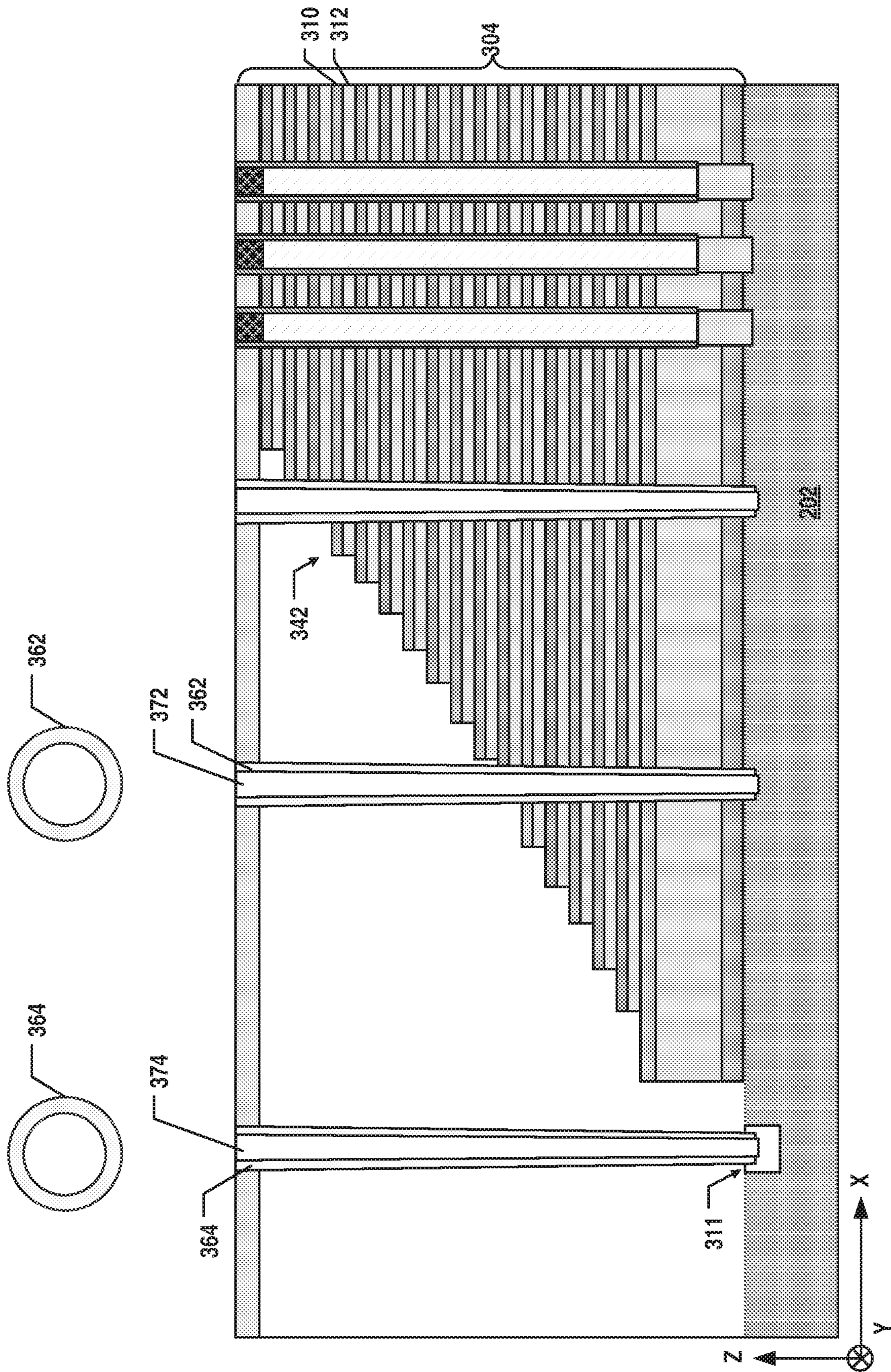

FIG. 4A

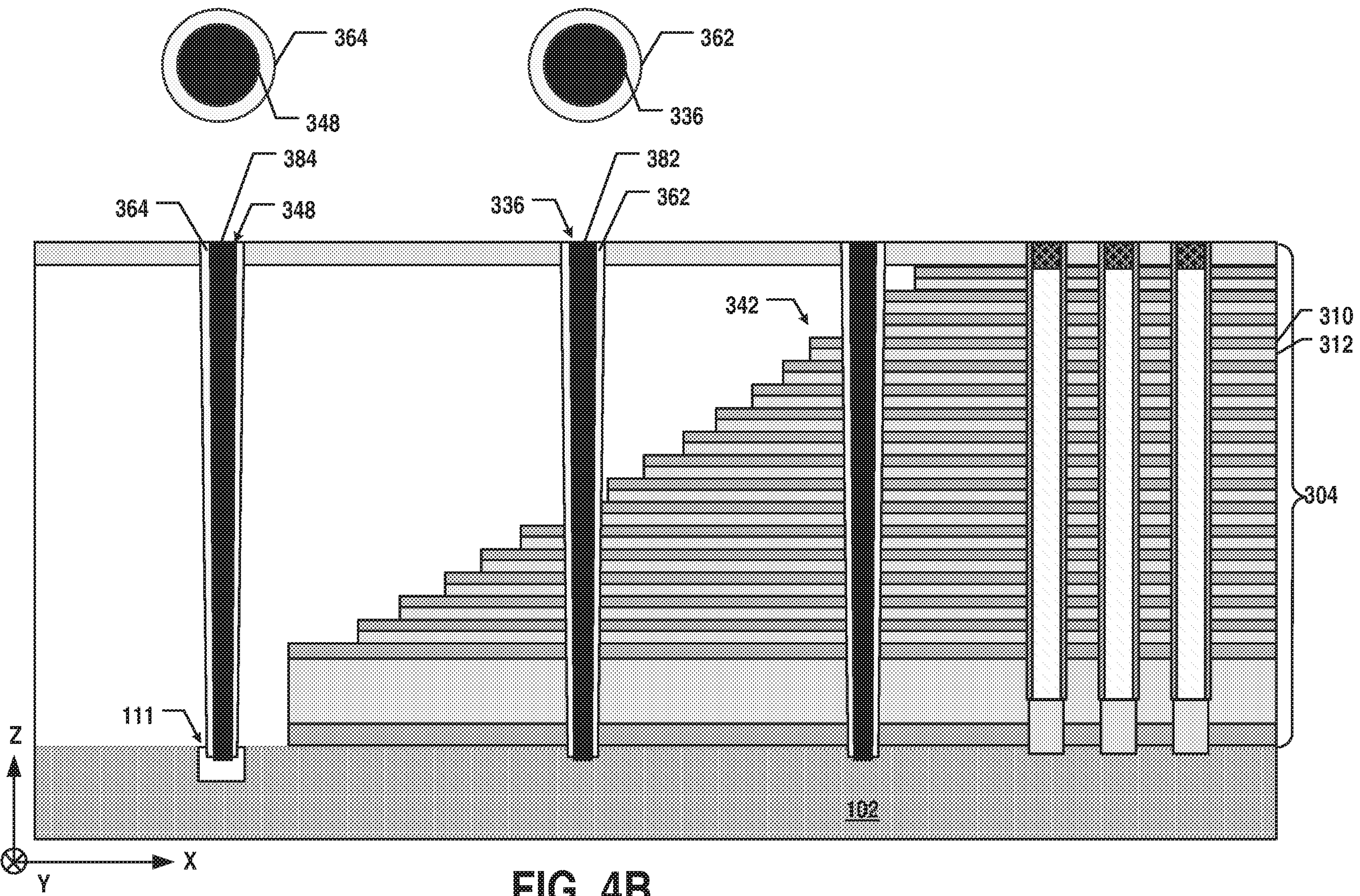

FIG. 4B

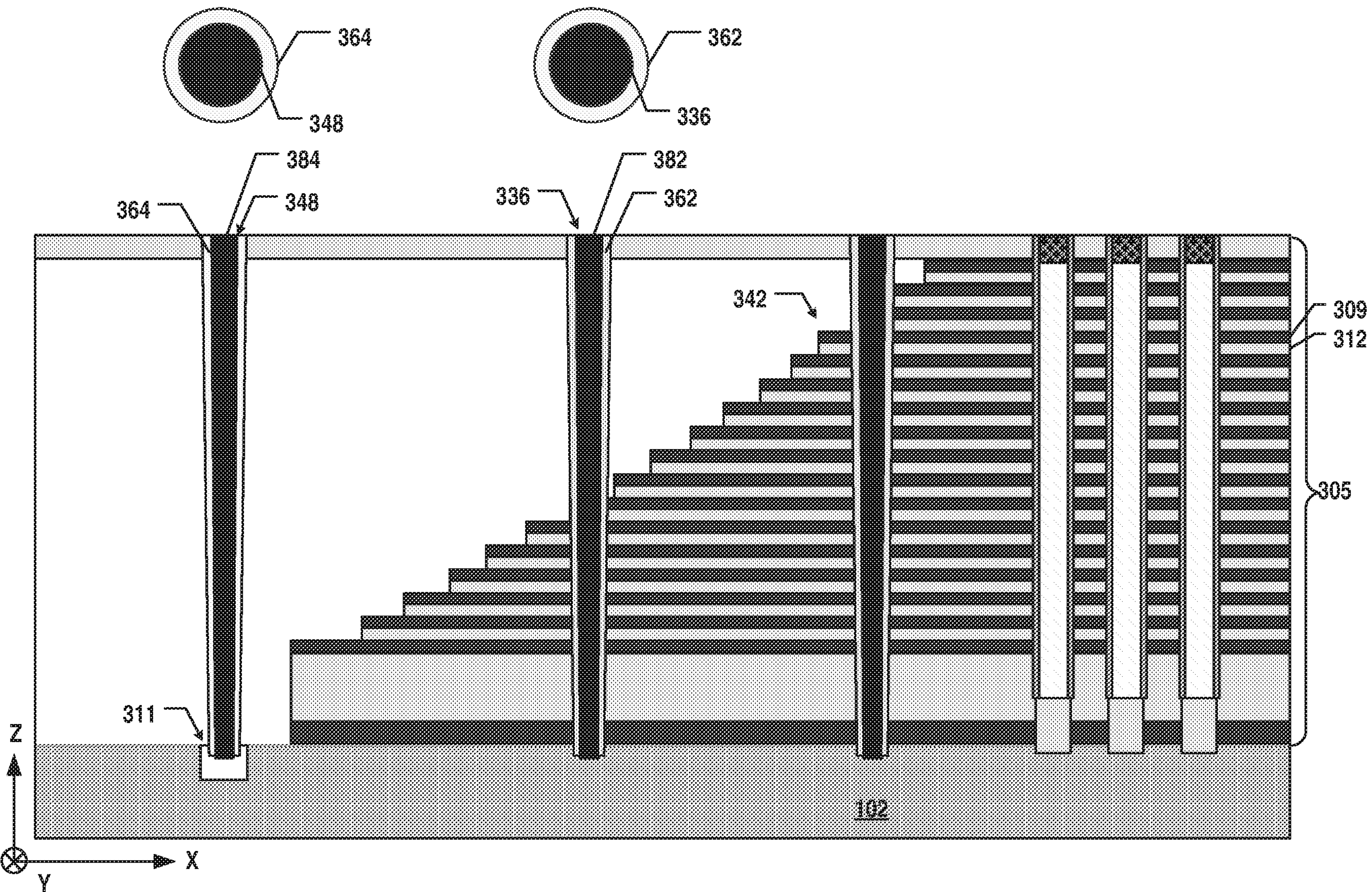

FIG. 4C

FIG. 4D

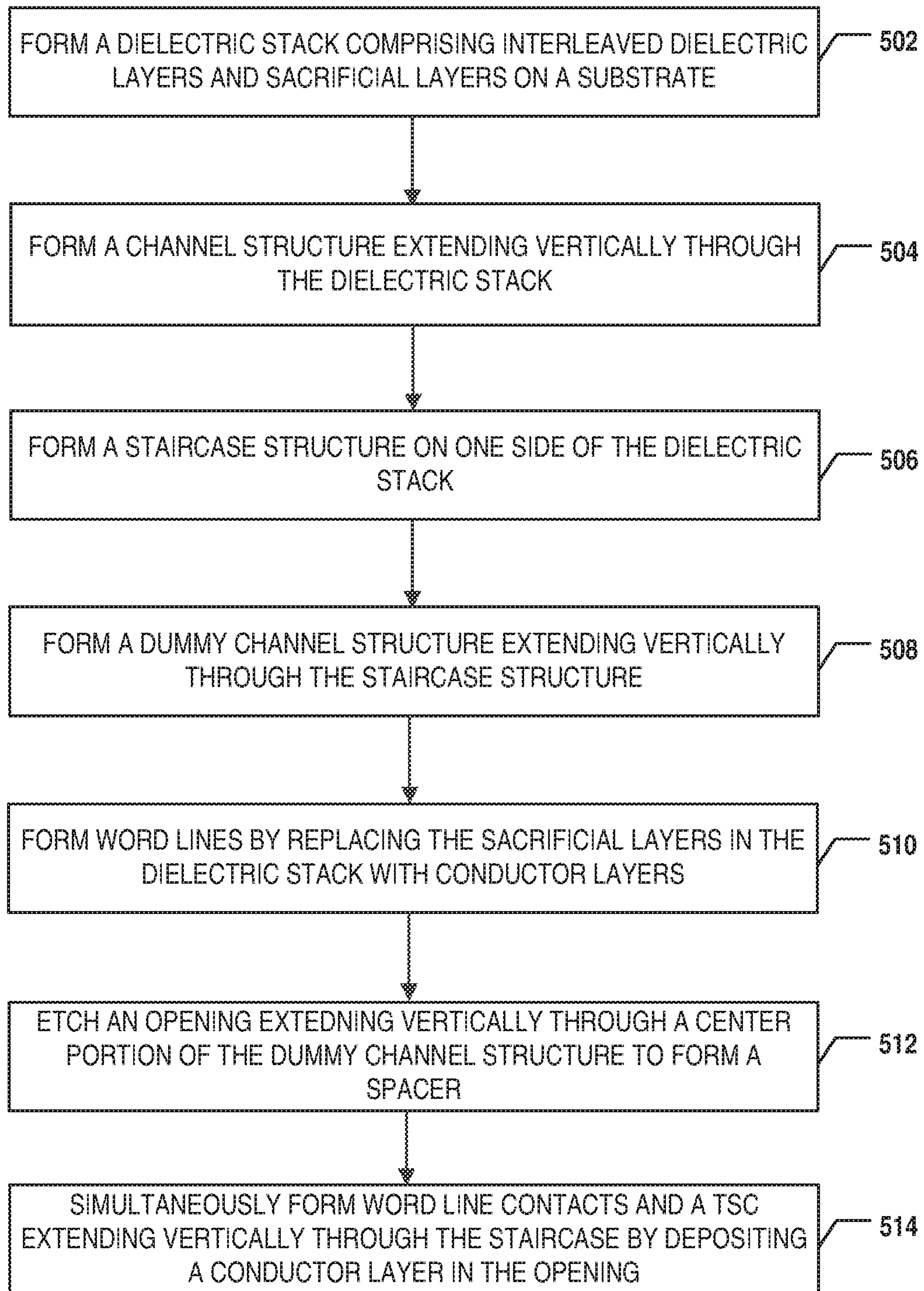

FIG. 5A

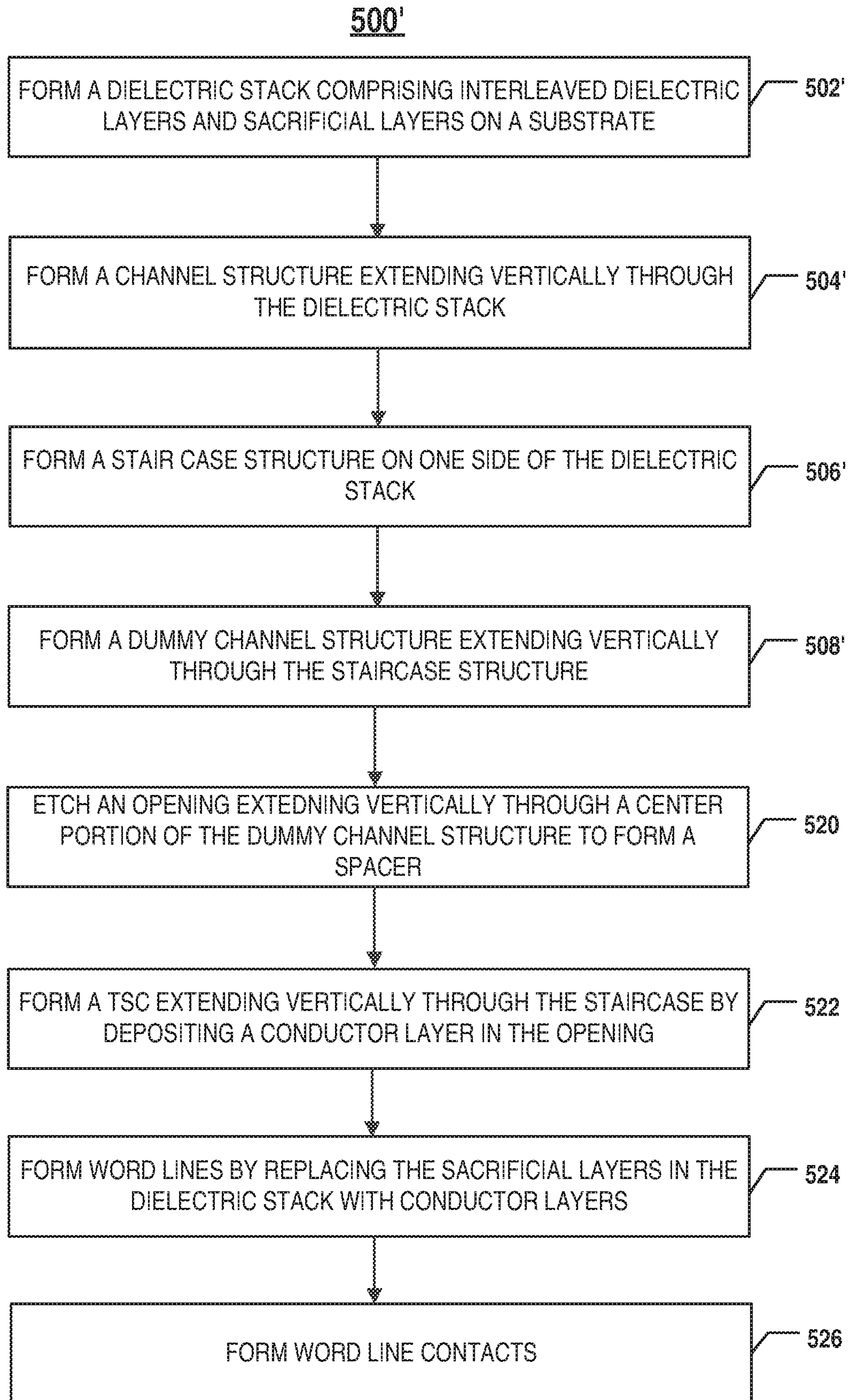

FIG. 5B

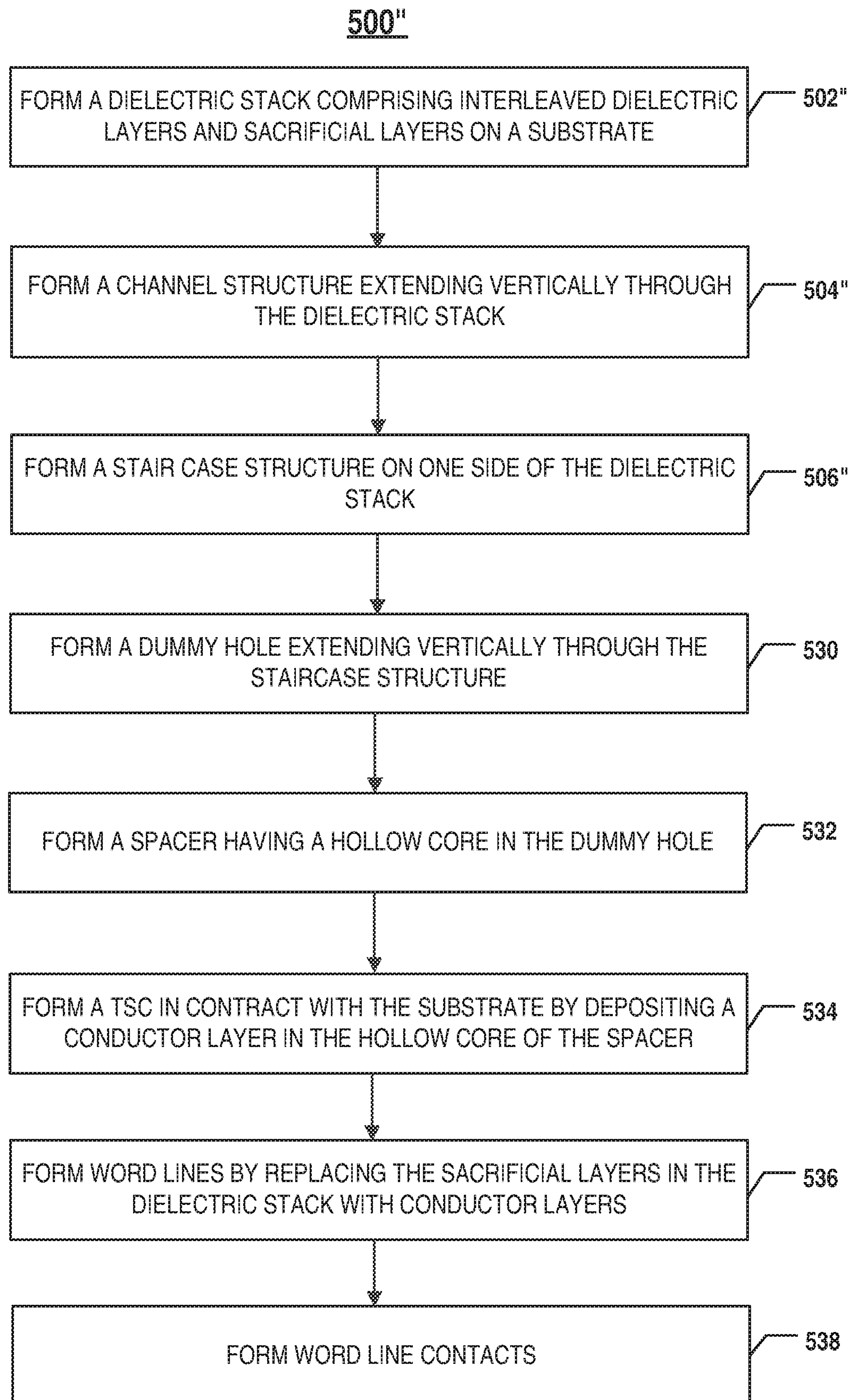

FIG. 5C

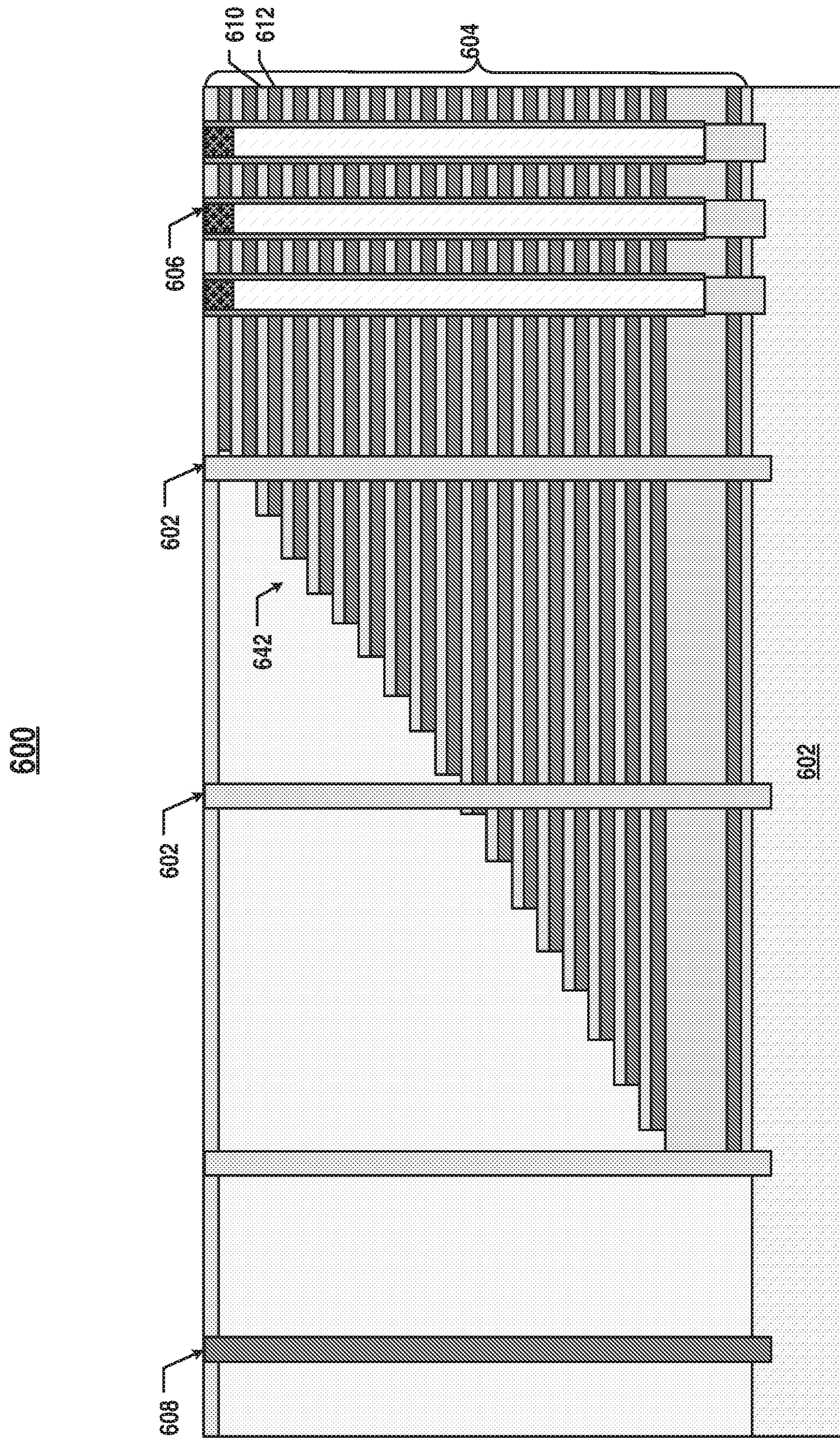

FIG. 6 (Related Art)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2019/070009

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i; H01L 23/538(2006.01)i; H01L 27/11548(2017.01)i; H01L 27/11551(2017.01)i; H01L 27/11575(2017.01)i; H01L 27/11578(2017.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L21/-;H01L23/-;H01L27/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNABS;CNTXT;DWPI;Three?Dimensional,3D,memory,dielectric,staircase,sacrificial,conduct+,vertically through,dummy,tsc, through stair contact,layer+,hollow core,stack,insult+,spacer+,deposit+,hole,etch+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN 108377660 A (ANDISK TECHNOLOGIES LL) 07 August 2018 (2018-08-07) para.[132], [173], [374-377], Fig.72A-75C	1-37
X	CN 109075175 A (ANDISK TECHNOLOGIES LL) 21 December 2018 (2018-12-21) para.[56-67], [125-146], Fig.9A-10E	1-37
A	CN 108431956 A (ANDISK TECHNOLOGIES LL) 21 August 2018 (2018-08-21) para.[95-119], Fig.10-14	1-37
A	WO 2018194750 A1 (ANDISK TECHNOLOGIES LL) 25 October 2018 (2018-10-25) para.[130-144]Fig.14-15	1-37
A	CN 108766971 A (TZE MEMORY TECHNOLOGIES CO., LTD) 06 November 2018 (2018-11-06) para.[65-77], Fig.1	1-37

☐ Further documents are listed in the continuation of Box C.   ☑ See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 September 2019	**26 September 2019**

Name and mailing address of the ISA/CN	Authorized officer
National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088 China	**FENG,Xue**
Facsimile No. **(86-10)62019451**	Telephone No. **(86-10)53962909**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2019/070009

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				US	9818759	B2	14 November 2017
				US	10381371	B2	13 August 2019
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				US	2017179154	A1	22 June 2017
				US	10038006	B2	31 July 2018
				JP	6463872	B2	06 February 2019
				US	2017179153	A1	22 June 2017
				JP	2018534765	A	22 November 2018
				WO	2017112014	A1	29 June 2017
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				US	2017179151	A1	22 June 2017
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				US	2017352678	A1	07 December 2017
				WO	2017213720	A1	14 December 2017
				EP	3420591	A1	02 January 2019
CN	108431956	A	21 August 2018	US	10269620	B2	23 April 2019
				US	2017236746	A1	17 August 2017
				WO	2017142806	A1	24 August 2017
WO	2018194750	A1	25 October 2018	US	10115632	B1	30 October 2018
				US	2018301374	A1	18 October 2018
CN	108766971	A	06 November 2018		None		