(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 October 1998 (01.10.1998)

PCT

(10) International Publication Number
WO 98/043193 A3

(51) International Patent Classification[6]: G06F 9/45, 15/16, 15/78, 15/80

(21) International Application Number: PCT/US98/05975

(22) International Filing Date: 20 March 1998 (20.03.1998)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

60/041,044	21 March 1997 (21.03.1997)	US
60/071,516	15 January 1998 (15.01.1998)	US

(71) Applicant *(for all designated States except US)*: **UNIVERSITY OF MARYLAND** [US/US]; 4312 Knox Road, College Park, MD 20742-8621 (US).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **VISHKIN, Uzi** [US/US]; 2 Dundee Court, Rockville, MD 20850 (US).

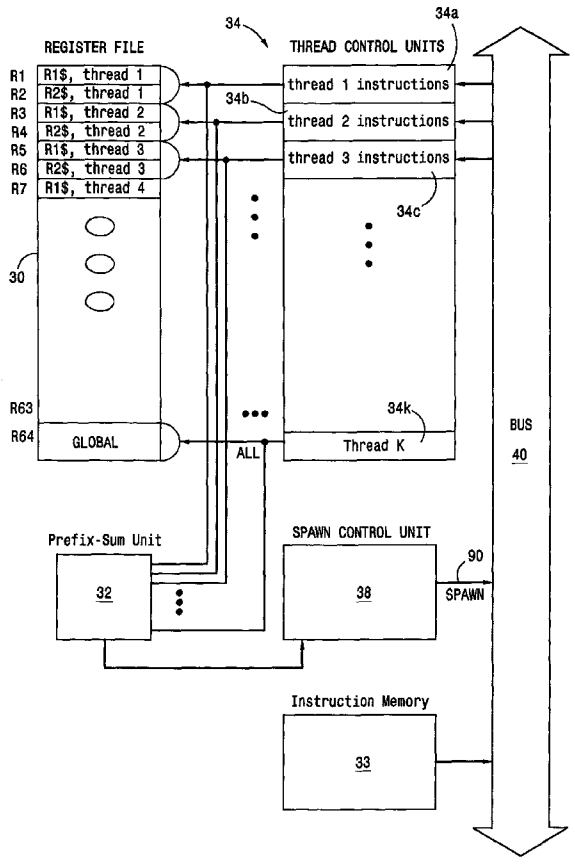
(74) Agent: **OLIVER, Eric**; Dickstein Shapiro Morin & OSHINSKY LLP, 2101 L Street N.W., Washington, DC 20037-1526 (US).

(81) Designated States *(national)*: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: SPAWN-JOIN INSTRUCTION SET ARCHITECTURE FOR PROVIDING EXPLICIT MULTITHREADING



(57) Abstract: The invention presents a unique computational paradigm that provides the tools to take advantage of the parallelism inherent in parallel algorithms to the full spectrum from algorithms through architecture to implementation. The invention provides a new processing architecture that extends the standard instruction set of the conventional uniprocessor architecture. The architecture used to implement this new computational paradigm includes a thread control unit (34), a spawn control unit (38), and an enabled instruction memory (50). The architecture initiates multiple threads and executes them in parallel. Control of the threads is provided such that the threads may be suspended or allowed to execute each at its own pace.

WO 98/043193 A3

Published:
— *with international search report*

(88) Date of publication of the international search report:
7 August 2003

(15) Information about Correction:

Previous Correction:
see PCT Gazette No. 09/1999 of 4 March 1999, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/05975

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 9/45, 15/16, 15/78, 15/80
US CL :395/800.22, 800.23, 800.24, 706, 670
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/800.22, 800.23, 800.24, 706, 670

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, IEEE Publications

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,404,469 A (CHUNG et al) 04 April 1995, figures 1 and 5.	1-3, 14-15, 18-19
Y	US 5,404,469 A (CHUNG et al) 04 April 1995, cols. 1-10.	1-20
X	US 5,546,593 A (KIMURA et al) 13 August 1996, figures 1, 2(a), 2(b), 2(c).	1-3, 14-15, 18-19
Y	US 5,546,593 A (KIMURA et al) 13 August 1996, cols. 1-17.	1-20
Y, P	US 5,729,710 A (MAGEE et al) 17 March 1998, cols. 1-66.	1-20
Y	US 5,590,326 A (MANABE) 31 December 1996, cols. 1-12.	1-20

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 25 JANUARY 1999	Date of mailing of the international search report 14 APR 2003
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer JOHN FOLLANSBEE Telephone No. (703) 305-8498

Form PCT/ISA/210 (second sheet)(July 1992)★

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/05975

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,519,867 A (MOELLER et al) 21 May 1996, cols. 1-37.	1-20
Y	HALSTEAD. Robert. H. MASA: A Multithreaded Processor Architecture for Parallel Symbolic Computing IEEE. 1988. pages 443-451.	1-20
Y	YU. Ge. et. al Transaction Management for a Distributed Object Storage System WAKASHI-Design, Implementation and Performance IEEE. 1996, pages 460-468.	1-20
Y	D'HOLLANDER. Erick. H. Partitioning and Labeling of Loops by Unimodular Transformations IEEE. 1992, pages 465-476.	1-20