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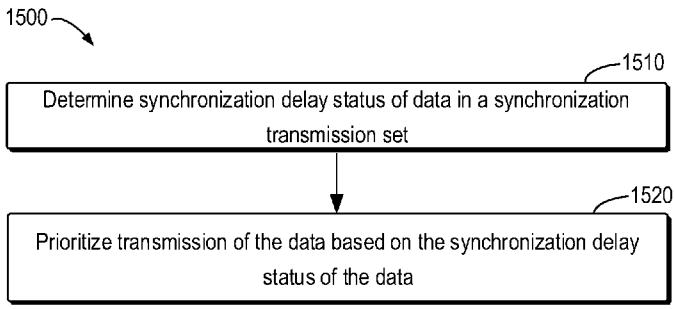

Fig. 15

(57) Abstract: Various aspects of the present disclosure relate to logical channel prioritization based on synchronization delay status. In one aspect, a UE determines synchronization delay status of data in a first synchronization transmission set. In turn, the UE prioritizes transmission of the data based on the synchronization delay status of the data.

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LOGICAL CHANNEL PRIORITIZATION based on synchronization delay status

TECHNICAL FIELD

[0001] The present disclosure relates to wireless communications, and more specifically to user equipment (UE) and methods for supporting logical channel prioritization (LCP) based on synchronization delay status.

BACKGROUND

[0002] A wireless communications system may include one or multiple network communication devices, such as base stations, which may be otherwise known as an eNodeB (eNB), a next-generation NodeB (gNB), or other suitable terminology. Each network communication devices, such as a base station may support wireless communications for one or multiple user communication devices, which may be otherwise known as UE, or other suitable terminology. The wireless communications system may support wireless communications with one or multiple user communication devices by utilizing resources of the wireless communication system (e.g., time resources (e.g., symbols, slots, subframes, frames, or the like) or frequency resources (e.g., subcarriers, carriers). Additionally, the wireless communications system may support wireless communications across various radio access technologies including third generation (3G) radio access technology, fourth generation (4G) radio access technology, fifth generation (5G) radio access technology, among other suitable radio access technologies beyond 5G (e.g., sixth generation (6G)).

[0003] The tactile and multi-modal communication service can be applied in multiple fields, such as industry, robotics and telepresence, virtual reality, augmented reality, healthcare, road traffic, serious gaming, education, culture and smart grid. These services support applications enabling input from more than one sources and/or output to more than one destinations to convey information more effectively. The input and output may be different modalities which may include at least one of the following: video/audio media; information received by sensors about the environment, such as brightness, temperature, humidity and so on; or haptic (or tactile) data which can be feelings when touching a surface (such as pressure, texture, vibration, temperature), or kinaesthetic senses (such as gravity, pull forces, sense of position awareness).

[0004] For immersive multi-modal virtual reality (VR) applications, synchronization between different media components is critical in order to avoid having a negative impact on the user experience (i.e., viewers detecting lack of synchronization), particularly when the synchronization threshold between two or more modalities is less than the latency key performance indicator (KPI) for the application.

[0005] Logical channel prioritization (LCP) procedure does not consider synchronization delay status but a priority of a logical channel. When remaining synchronization delay of data of a first logical channel is below a threshold, and a priority of the first logical channel is lower than a priority of a second logical channel which does not have synchronization delay requirement, the data of the first logical channel may not be multiplexed to a medium access control (MAC) protocol data unit (PDU) for an uplink (UL) grant during the MAC PDU assembling procedure, and the data may be discarded. Thus, the user experience is impacted.

SUMMARY

[0006] The present disclosure relates to UEs and methods that support logical channel prioritization based on synchronization delay status. With the UEs and methods, logical channel prioritization based on synchronization delay status may be achieved. Thus, the user experience may be improved.

[0007] Some implementations of a UE described herein may include a processor and a transceiver coupled to the processor, wherein the processor is configured to: determine synchronization delay status of data in a synchronization transmission set; and prioritize transmission of the data based on the synchronization delay status of the data.

[0008] In some implementations, the processor is configured prioritize transmission of the data based on the synchronization delay status of the data by: prioritize transmission of a first type of data in the synchronization transmission set, wherein the synchronization delay status comprises first remaining synchronization delay of the first type of data, the first remaining synchronization delay of the first type of data is below a first threshold.

[0009] In some implementations, the processor is configured to prioritize the transmission of the data by: prioritizing the transmission of the data based on the synchronization delay status of the data and a value which is maintained for a first logical channel (LCH) having the data.

[0010] In some implementations, the processor is configured to prioritize the transmission of the data by: prioritizing the transmission of the data based on the synchronization delay status of the data regardless of a value which is maintained for a first LCH having the data.

[0011] In some implementations, the processor is configured to prioritize the transmission of the data by one of the following: prioritizing transmission of data of a first LCH, wherein the first LCH has a first type of data, first remaining synchronization delay of the first type of data is below a first threshold; prioritizing transmission of all the data in the synchronization transmission set; or prioritizing transmission of the first type of data in the synchronization transmission set.

[0012] In some implementations, the processor is configured to prioritize the transmission of the first type of data by: increasing at least a first priority level for the first type of data to a target priority level.

[0013] In some implementations, the processor is further configured to: receive a configuration for the target priority level via the transceiver from a network entity; and determine the target priority level based on the configuration.

[0014] In some implementations, the configuration for the target priority level comprises one of the following: an absolute target priority value, a priority offset value, or a factor.

[0015] In some implementations, the processor is configured to increase at least the first priority level for the first type of data to the target priority level by one of the following: increasing a second priority level for a first LCH to the target priority level, wherein the first LCH has the first type of data; increasing only the first priority level for the first type of data to the target priority level; or increasing a third priority level for the synchronization transmission set to the target priority level, wherein the synchronization transmission set comprises the first type of data.

[0016] In some implementations, both a first LCH and a second LCH have the first type of data, and the first LCH has the synchronization transmission set; and the processor is configured to prioritize the transmission of the first type of data in the synchronization transmission set by prioritizing transmission of the first type of data in the first LCH based on determining one of the following: a first priority level for the first LCH is higher than

a second priority level for the second LCH; or the first remaining synchronization delay of the first type of data in the first LCH is less than second remaining synchronization delay of the first type of data in the second LCH.

[0017] In some implementations, the processor is further configured to: receive, via the transceiver from a network entity, a first indication indicating whether to prioritize transmission of the data based on the synchronization delay status of the data.

[0018] In some implementations, the data comprises a first type of data, wherein first remaining synchronization delay of the first type of data is below a first threshold among the multiple thresholds.

[0019] In some implementations, the processor is configured to prioritize the transmission of the data by: receiving, via the transceiver from a network entity, a second indication indicating to prioritize the transmission of the first type of data based on the first threshold; and prioritizing, based on the second indication, the transmission of the first type of data based on the first threshold.

[0020] In some implementations, the data further comprises a third type of data, wherein third remaining time of the third type of data is below a second threshold among the multiple thresholds.

[0021] In some implementations, the processor is configured to prioritize the transmission of the data by: increasing a first priority level for the first type of data to a first target priority level; and increasing a second priority level for the third type of data to a second target priority level.

[0022] In some implementations, a first logical channel (LCH) has the first type of data, and a second LCH has the third type of data.

[0023] In some implementations, a first logical channel (LCH) has both the first type of data and the third type of data.

[0024] In some implementations, the processor is configured to prioritize the transmission of the data by: prioritizing the transmission of one of the first type of data and the third type of data.

[0025] Some implementations of a UE described herein may include a processor and a transceiver coupled to the processor, wherein the processor is configured to: determine

delay status of data based on at least one of multiple thresholds; and prioritize transmission of the data based on one of the multiple thresholds.

[0026] In some implementations, the processor is configured to maximize transmission of the data by one of the following: maximizing transmission of data of a first logical channel (LCH), wherein the first LCH has a first type of data, first remaining synchronization delay of the first type of data is below a first threshold; maximizing transmission of all the data in the synchronization transmission set; or maximizing transmission of the first type of data in the synchronization transmission set.

[0027] Some implementations of a UE described herein may include a processor and a transceiver coupled to the processor, wherein the processor is configured to: determine synchronization delay status of data in a synchronization transmission set; and maximize transmission of the data based on determining that an uplink grant is enough to accommodate the data.

[0028] Some implementations of a method described herein may include: determining synchronization delay status of data in a synchronization transmission set; and prioritizing transmission of the data based on the synchronization delay status of the data.

[0029] Some implementations of a method described herein may include: determining delay status of data based on at least one of multiple thresholds; and prioritizing transmission of the data based on one of the multiple thresholds.

[0030] Some implementations of a method described herein may include: determining synchronization delay status of data in a synchronization transmission set; and maximizing transmission of the data based on determining that an uplink grant is enough to accommodate the data.

[0031] Some implementations of a processor described herein may include at least one memory and a controller coupled with the at least one memory and configured to cause the controller to: determine synchronization delay status of data in a synchronization transmission set; and prioritize transmission of the data based on the synchronization delay status of the data.

[0032] Some implementations of a processor described herein may include at least one memory and a controller coupled with the at least one memory and configured to

cause the controller to: determine delay status of data based on at least one of multiple thresholds; and prioritize transmission of the data based on one of the multiple thresholds.

[0033] Some implementations of a processor described herein may include at least one memory and a controller coupled with the at least one memory and configured to cause the controller to: determine synchronization delay status of data in a synchronization transmission set; and maximize transmission of the data based on determining that an uplink grant is enough to accommodate the data.

[0034] It is to be understood that the summary section is not intended to identify key or essential features of embodiments of the present disclosure, nor is it intended to be used to limit the scope of the present disclosure. Other features of the present disclosure will become easily comprehensible through the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] Fig. 1 illustrates an example of a wireless communications system that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure;

[0036] Fig. 2 illustrates an example of a legacy logical channel prioritization;

[0037] Fig. 3 illustrates a flowchart of a process for multiplexing a MAC PDU of a logical channel in accordance with aspects of the present disclosure;

[0038] Fig. 4 illustrates a signaling chart illustrating an example process that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure;

[0039] Fig. 5 illustrates an example of a synchronization transmission set in accordance with some implementations of the present disclosure;

[0040] Figs. 6 and 7 illustrate a flowchart of a method that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure, respectively;

[0041] Fig. 8 illustrates an example of data of a first LCH in accordance with aspects of the present disclosure;

[0042] Fig. 9 illustrates a flowchart of a method that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure;

[0043] Fig. 10 illustrates a signaling chart illustrating an example process that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure;

[0044] Figs. 11A, 11B and 11C illustrate an example of data of a first LCH in accordance with aspects of the present disclosure, respectively;

[0045] Fig. 12 illustrates a signaling chart illustrating an example process that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure;

[0046] Fig. 13 illustrates an example of a device that supports logical channel prioritization based on synchronization delay status in accordance with some aspects of the present disclosure;

[0047] Fig. 14 illustrates an example of a processor that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure; and

[0048] Figs. 15, 16 and 17 illustrate a flowchart of a method that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure, respectively.

DETAILED DESCRIPTION

[0049] Principles of the present disclosure will now be described with reference to some embodiments. It is to be understood that these embodiments are described only for the purpose of illustration and help those skilled in the art to understand and implement the present disclosure, without suggesting any limitation as to the scope of the disclosure. The disclosure described herein may be implemented in various manners other than the ones described below.

[0050] In the following description and claims, unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skills in the art to which this disclosure belongs.

[0051] References in the present disclosure to "one embodiment," "an example embodiment," "an embodiment," "some embodiments," and the like indicate that the embodiment(s) described may include a particular feature, structure, or characteristic, but it is not necessary that every embodiment includes the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment(s). Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0052] It shall be understood that although the terms "first" and "second" or the like may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. For example, a first element could also be termed as a second element, and similarly, a second element could also be termed as a first element, without departing from the scope of embodiments. As used herein, the term "and/or" includes any and all combinations of one or more of the listed terms.

[0053] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of example embodiments. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises", "comprising", "has", "having", "includes" and/or "including", when used herein, specify the presence of stated features, elements, and/or components etc., but do not preclude the presence or addition of one or more other features, elements, components and/ or combinations thereof.

[0054] Aspects of the present disclosure are described in the context of a wireless communications system.

[0055] Fig. 1 illustrates an example of a wireless communications system 100 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure. The wireless communications system 100 may include one at least one of network entities 102 (also referred to as network equipment (NE)), one or more terminal devices or UEs 104, a core network 106, and a packet data network 108. The wireless communications system 100 may support various

radio access technologies. In some implementations, the wireless communications system 100 may be a 4G network, such as an LTE network or an LTE-advanced (LTE-A) network. In some other implementations, the wireless communications system 100 may be a 5G network, such as an NR network. In other implementations, the wireless communications system 100 may be a combination of a 4G network and a 5G network, or other suitable radio access technology including institute of electrical and electronics engineers (IEEE) 802.11 (Wi-Fi), IEEE 802.16 (WiMAX), IEEE 802.20. The wireless communications system 100 may support radio access technologies beyond 5G. Additionally, the wireless communications system 100 may support technologies, such as time division multiple access (TDMA), frequency division multiple access (FDMA), or code division multiple access (CDMA), etc.

[0056] The network entities 102 may be dispersed throughout a geographic region to form the wireless communications system 100. One or more of the network entities 102 described herein may be or include or may be referred to as a network node, a base station (BS), a network element, a radio access network (RAN) node, a base transceiver station, an access point, a NodeB, an eNodeB (eNB), a next-generation NodeB (gNB), or other suitable terminology. A network entity 102 and a UE 104 may communicate via a communication link 110, which may be a wireless or wired connection. For example, a network entity 102 and a UE 104 may perform wireless communication (e.g., receive signaling, transmit signaling) over a Uu interface. The network entities 102 may be collectively referred to as network entities 102 or individually referred to as a network entity 102. Hereinafter, some implementations of the present disclosure will be described by taking a base station as an example of the network entity 102. Thus, the network entity 102 may be used interchangeably with the network entity 102.

[0057] A network entity 102 may provide a geographic coverage area 112 for which the network entity 102 may support services (e.g., voice, video, packet data, messaging, broadcast, etc.) for one or more UEs 104 within the geographic coverage area 112. For example, a network entity 102 and a UE 104 may support wireless communication of signals related to services (e.g., voice, video, packet data, messaging, broadcast, etc.) according to one or multiple radio access technologies. In some implementations, a network entity 102 may be moveable, for example, a satellite associated with a non-terrestrial network. In some implementations, different geographic coverage areas 112 associated with the same or different radio access technologies may overlap, but the

different geographic coverage areas 112 may be associated with different network entities 102. Information and signals described herein may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0058] The one or more UEs 104 may be dispersed throughout a geographic region of the wireless communications system 100. A UE 104 may include or may be referred to as a mobile device, a wireless device, a remote device, a remote unit, a handheld device, or a subscriber device, or some other suitable terminology. In some implementations, the UE 104 may be referred to as a unit, a station, a terminal, or a client, among other examples. Additionally, or alternatively, the UE 104 may be referred to as an internet-of-things (IoT) device, an internet-of-everything (IoE) device, or machine-type communication (MTC) device, among other examples. In some implementations, a UE 104 may be stationary in the wireless communications system 100. In some other implementations, a UE 104 may be mobile in the wireless communications system 100.

[0059] The one or more UEs 104 may be devices in different forms or having different capabilities. Some examples of UEs 104 are illustrated in Fig. 1. A UE 104 may be capable of communicating with various types of devices, such as the network entities 102, other UEs 104, or network equipment (e.g., the core network 106, the packet data network 108, a relay device, an integrated access and backhaul (IAB) node, or another network equipment), as shown in Fig. 1. Additionally, or alternatively, a UE 104 may support communication with other network entities 102 or UEs 104, which may act as relays in the wireless communications system 100.

[0060] A UE 104 may also be able to support wireless communication directly with other UEs 104 over a communication link 114. For example, a UE 104 may support wireless communication directly with another UE 104 over a device-to-device (D2D) communication link. In some implementations, such as vehicle-to-vehicle (V2V) deployments, vehicle-to-everything (V2X) deployments, or cellular-V2X deployments, the communication link 114 may be referred to as a sidelink. For example, a UE 104 may support wireless communication directly with another UE 104 over a PC5 interface.

[0061] A network entity 102 may support communications with the core network 106, or with another network entity 102, or both. For example, a network entity 102 may interface with the core network 106 through one or more backhaul links 116 (e.g., via an S1, N2, N2, or another network interface). The network entities 102 may communicate with each other over the backhaul links 116 (e.g., via an X2, Xn, or another network interface). In some implementations, the network entities 102 may communicate with each other directly (e.g., between the network entities 102). In some other implementations, the network entities 102 may communicate with each other or indirectly (e.g., via the core network 106). In some implementations, one or more network entities 102 may include subcomponents, such as an access network entity, which may be an example of an access node controller (ANC). An ANC may communicate with the one or more UEs 104 through one or more other access network transmission entities, which may be referred to as a radio heads, smart radio heads, or transmission-reception points (TRPs).

[0062] In some implementations, a network entity 102 may be configured in a disaggregated architecture, which may be configured to utilize a protocol stack physically or logically distributed among two or more network entities 102, such as an integrated access backhaul (IAB) network, an open radio access network (O-RAN) (e.g., a network configuration sponsored by the O-RAN Alliance), or a virtualized RAN (vRAN) (e.g., a cloud RAN (C-RAN)). For example, a network entity 102 may include one or more of a central unit (CU), a distributed unit (DU), a radio unit (RU), a RAN intelligent controller (RIC) (e.g., a near-real time RIC (Near-RT RIC), a non-real time RIC (Non-RT RIC)), a service management and orchestration (SMO) system, or any combination thereof.

[0063] An RU may also be referred to as a radio head, a smart radio head, a remote radio head (RRH), a remote radio unit (RRU), or a transmission reception point (TRP). One or more components of the network entities 102 in a disaggregated RAN architecture may be co-located, or one or more components of the network entities 102 may be located in distributed locations (e.g., separate physical locations). In some implementations, one or more network entities 102 of a disaggregated RAN architecture may be implemented as virtual units (e.g., a virtual CU (VCU), a virtual DU (VDU), a virtual RU (VRU)).

[0064] Split of functionality between a CU, a DU, and an RU may be flexible and may support different functionalities depending upon which functions (e.g., network layer

functions, protocol layer functions, baseband functions, radio frequency functions, and any combinations thereof) are performed at a CU, a DU, or an RU. For example, a functional split of a protocol stack may be employed between a CU and a DU such that the CU may support one or more layers of the protocol stack and the DU may support one or more different layers of the protocol stack. In some implementations, the CU may host upper protocol layer (e.g., a layer 3 (L3), a layer 2 (L2)) functionality and signaling (e.g., radio resource control (RRC), service data adaption protocol (SDAP), packet data convergence protocol (PDCP)). The CU may be connected to one or more DUs or RUs, and the one or more DUs or RUs may host lower protocol layers, such as a layer 1 (L1) (e.g., physical (PHY) layer) or an L2 (e.g., radio link control (RLC) layer, medium access control (MAC) layer) functionality and signaling, and may each be at least partially controlled by the CU.

[0065] Additionally, or alternatively, a functional split of the protocol stack may be employed between a DU and an RU such that the DU may support one or more layers of the protocol stack and the RU may support one or more different layers of the protocol stack. The DU may support one or multiple different cells (e.g., via one or more RUs). In some implementations, a functional split between a CU and a DU, or between a DU and an RU may be within a protocol layer (e.g., some functions for a protocol layer may be performed by one of a CU, a DU, or an RU, while other functions of the protocol layer are performed by a different one of the CU, the DU, or the RU).

[0066] A CU may be functionally split further into CU control plane (CU-CP) and CU user plane (CU-UP) functions. A CU may be connected to one or more DUs via a midhaul communication link (e.g., F1, F1-c, F1-u), and a DU may be connected to one or more RUs via a fronthaul communication link (e.g., open fronthaul (FH) interface). In some implementations, a midhaul communication link or a fronthaul communication link may be implemented in accordance with an interface (e.g., a channel) between layers of a protocol stack supported by respective network entities 102 that are in communication via such communication links.

[0067] The core network 106 may support user authentication, access authorization, tracking, connectivity, and other access, routing, or mobility functions. The core network 106 may be an evolved packet core (EPC), or a 5G core (5GC), which may include a control plane entity that manages access and mobility (e.g., a mobility management entity

(MME), an access and mobility management functions (AMF)) and a user plane entity that routes packets or interconnects to external networks (e.g., a serving gateway (S-GW), a packet data network (PDN) gateway (P-GW), or a user plane function (UPF)). In some implementations, the control plane entity may manage non-access stratum (NAS) functions, such as mobility, authentication, and bearer management (e.g., data bearers, signal bearers, etc.) for the one or more UEs 104 served by the one or more network entities 102 associated with the core network 106.

[0068] The core network 106 may communicate with the packet data network 108 over one or more backhaul links 116 (e.g., via an S1, N2, N2, or another network interface). The packet data network 108 may include an application server 118. In some implementations, one or more UEs 104 may communicate with the application server 118. A UE 104 may establish a session (e.g., a PDU session, or the like) with the core network 106 via a network entity 102. The core network 106 may route traffic (e.g., control information, data, and the like) between the UE 104 and the application server 118 using the established session (e.g., the established PDU session). The PDU session may be an example of a logical connection between the UE 104 and the core network 106 (e.g., one or more network functions of the core network 106).

[0069] In the wireless communications system 100, the network entities 102 and the UEs 104 may use resources of the wireless communications system 100 (e.g., time resources (e.g., symbols, slots, subframes, frames, or the like) or frequency resources (e.g., subcarriers, carriers)) to perform various operations (e.g., wireless communications). In some implementations, the network entities 102 and the UEs 104 may support different resource structures. For example, the network entities 102 and the UEs 104 may support different frame structures. In some implementations, such as in 4G, the network entities 102 and the UEs 104 may support a single frame structure. In some other implementations, such as in 5G and among other suitable radio access technologies, the network entities 102 and the UEs 104 may support various frame structures (i.e., multiple frame structures). The network entities 102 and the UEs 104 may support various frame structures based on one or more numerologies.

[0070] One or more numerologies may be supported in the wireless communications system 100, and a numerology may include a subcarrier spacing and a cyclic prefix. A first numerology (e.g., μ=0) may be associated with a first subcarrier spacing (e.g., 15

kHz) and a normal cyclic prefix. In some implementations, the first numerology (e.g., μ=0) associated with the first subcarrier spacing (e.g., 15 kHz) may utilize one slot per subframe. A second numerology (e.g., μ=1) may be associated with a second subcarrier spacing (e.g., 30 kHz) and a normal cyclic prefix. A third numerology (e.g., μ=2) may be associated with a third subcarrier spacing (e.g., 60 kHz) and a normal cyclic prefix or an extended cyclic prefix. A fourth numerology (e.g., μ=3) may be associated with a fourth subcarrier spacing (e.g., 120 kHz) and a normal cyclic prefix. A fifth numerology (e.g., μ=4) may be associated with a fifth subcarrier spacing (e.g., 240 kHz) and a normal cyclic prefix.

[0071] A time interval of a resource (e.g., a communication resource) may be organized according to frames (also referred to as radio frames). Each frame may have a duration, for example, a 10 millisecond (ms) duration. In some implementations, each frame may include multiple subframes. For example, each frame may include 10 subframes, and each subframe may have a duration, for example, a 1 ms duration. In some implementations, each frame may have the same duration. In some implementations, each subframe of a frame may have the same duration.

[0072] Additionally or alternatively, a time interval of a resource (e.g., a communication resource) may be organized according to slots. For example, a subframe may include a number (e.g., quantity) of slots. The number of slots in each subframe may also depend on the one or more numerologies supported in the wireless communications system 100. For instance, the first, second, third, fourth, and fifth numerologies (i.e., μ=0, μ=1, μ=2, μ=3, μ=4) associated with respective subcarrier spacings of 15 kHz, 30 kHz, 60 kHz, 120 kHz, and 240 kHz may utilize a single slot per subframe, two slots per subframe, four slots per subframe, eight slots per subframe, and 16 slots per subframe, respectively. Each slot may include a number (e.g., quantity) of symbols (e.g., OFDM symbols). In some implementations, the number (e.g., quantity) of slots for a subframe may depend on a numerology. For a normal cyclic prefix, a slot may include 14 symbols. For an extended cyclic prefix (e.g., applicable for 60 kHz subcarrier spacing), a slot may include 12 symbols. The relationship between the number of symbols per slot, the number of slots per subframe, and the number of slots per frame for a normal cyclic prefix and an extended cyclic prefix may depend on a numerology. It should be understood that reference to a first numerology (e.g., μ=0) associated with a first subcarrier spacing (e.g., 15 kHz) may be used interchangeably between subframes and slots.

[0073] In the wireless communications system 100, an electromagnetic (EM) spectrum may be split, based on frequency or wavelength, into various classes, frequency bands, frequency channels, etc. By way of example, the wireless communications system 100 may support one or multiple operating frequency bands, such as frequency range designations FR1 (410 MHz – 7.125 GHz), FR2 (24.25 GHz – 52.6 GHz), FR3 (7.125 GHz – 24.25 GHz), FR4 (52.6 GHz – 114.25 GHz), FR4a or FR4-1 (52.6 GHz – 71 GHz), and FR5 (114.25 GHz – 300 GHz). In some implementations, the network entities 102 and the UEs 104 may perform wireless communications over one or more of the operating frequency bands. In some implementations, FR1 may be used by the network entities 102 and the UEs 104, among other equipment or devices for cellular communications traffic (e.g., control information, data). In some implementations, FR2 may be used by the network entities 102 and the UEs 104, among other equipment or devices for short-range, high data rate capabilities.

[0074] FR1 may be associated with one or multiple numerologies (e.g., at least three numerologies). For example, FR1 may be associated with a first numerology (e.g., μ=0), which includes 15 kHz subcarrier spacing; a second numerology (e.g., μ=1), which includes 30 kHz subcarrier spacing; and a third numerology (e.g., μ=2), which includes 60 kHz subcarrier spacing. FR2 may be associated with one or multiple numerologies (e.g., at least 2 numerologies). For example, FR2 may be associated with a third numerology (e.g., μ=2), which includes 60 kHz subcarrier spacing; and a fourth numerology (e.g., μ=3), which includes 120 kHz subcarrier spacing.

[0075] As described above, for immersive multi-modal VR applications, synchronization between different media components is critical in order to avoid having a negative impact on the user experience (i.e., viewers detecting lack of synchronization), particularly when the synchronization threshold between two or more modalities is less than the latency KPI for the application. Table 1 provides an example of typical synchronization thresholds for immersive multi-modality VR applications.

Table 1

Media components	**synchronization threshold (note 1)**	
audio-tactile	audio delay: 50 ms	tactile delay: 25 ms
visual-tactile	visual delay:	tactile delay:

	15 ms	50 ms
NOTE 1: for each media component, "delay" refers to the case where that media component is delayed compared to the other.		

[0076] In Table 1, for each media component, "delay" refers to the case where that one media component is delayed compared to the other. For example, the "visual delay" of 15 ms refers to the case where tactile data arrived at a UE first (e.g., at an access stratum (AS) of the UE first) and visual data is delayed by 15 ms compared to the tactile data. Alternatively, the "visual delay" of 15 ms refers to the case where tactile data is transmitted to a base station first and visual data is delayed by 15 ms compared to the tactile data. That is, a synchronization threshold between the tactile data and the visual data is equal to 15 ms.

[0077] As described above, an LCP procedure does not consider synchronization delay status but a priority of a logical channel. When remaining synchronization delay of data of a first logical channel is below a threshold, and a priority of the first logical channel is lower than a priority of a second logical channel which does not have synchronization delay requirement, the data of the first logical channel may not be multiplexed to a MAC PDU for a UL grant during the MAC PDU assembling procedure, and the data may be discarded. Thus, the user experience is impacted. This will be described with reference to Fig. 2.

[0078] Fig. 2 illustrates an example of a legacy LCP. In the example of Fig. 2, a priority of an LCH #1 is represented by P1, a priority of an LCH #2 is represented by P2, and a priority of an LCH #3 is represented by P3. P1 is higher than P2, and P2 is higher than P3.

[0079] Remaining time of data of the LCH #1 is equal to 10ms and the LCH #1 does not have synchronization delay requirement.

[0080] Tactile data is carried on the LCH #2 and visual data is carried on the LCH #3. The tactile data and the visual data are comprised in a synchronization transmission set.

[0081] The tactile data arrived at a UE at time T1 and the visual data arrived at the UE at time (T1+12ms). As shown in Table 1, a synchronization threshold between the tactile data and the visual data is equal to 15 ms. Thus, remaining synchronization delay of the visual data of the LCH #3 is equal to 15 minus 12 (ms). That is, remaining

synchronization delay of the visual data of the LCH #3 is equal to 3ms. Thus, the UE should transmit the visual data of the LCH #3 within 3ms after transmitting the tactile data of the LCH #2.

[0082] Because P1 is higher than P2 and P2 is higher than P3, the UE may first allocate resources for the data of the LCH #1 and the LCH #2 for a UL grant. In other words, the data of the LCH #1 and the LCH #2 is multiplexed to a MAC PDU for the UL grant first. If the UL grant is exhausted after the data of the LCH #1 and the LCH #2 was multiplexed, the data of the LCH #3 will not be multiplexed to the MAC PDU for the UL grant. If the remaining synchronization delay of the visual data of the LCH #3 is equal to or less than a threshold and the visual data of the LCH#3 is not timely multiplexed to a MAC PDU for transmission, the visual data of the LCH #3 may be discarded. Thus, the user experience is impacted.

[0083] Fig. 3 illustrates a flowchart of a process 300 for multiplexing a MAC PDU of a logical channel in accordance with aspects of the present disclosure.

[0084] In the process 300, each LCH *j* has a token bucket (also referred to as "bucket") and a value which is maintained for the LCH *j*. The value which is maintained for the LCH *j* is presented by *Bj*.

[0085] A bucket size maximum capacity of the token bucket 305 is equal to a product prioritized bit rate (PBR) and bucket size duration (BSD) (i.e., PBR*BSD). The bucket size of the token bucket 305 is also referred to as a maximum capacity of the token bucket 305.

[0086] *Bj* may represent the number of tokens in the token bucket for the LCH *j*. *Bj* is initialized to zero when the LCH j is established. For each LCH *j*, the UE 104 shall increment *Bj* by the product PBR ×T before every instance of the LCP procedure, where T is the time elapsed since *Bj* was last incremented. If the value of *Bj* is greater than the bucket size (i.e., PBR ×BSD), the UE 104 sets *Bj* to the bucket size.

[0087] As shown in Fig. 3, at 310, the UE 104 inject PBR×T tokens to the token bucket 305 at every instance of an LCP procedure.

[0088] At 320, the UE 104 increments Bj by the product PBR ×T, where T is the time elapsed since *Bj* was last incremented.

[0089] At 330, the UE 104 determines whether *Bi* is greater than zero.

[0090] If *Bj* is greater than zero, the UE 104 decrements *Bj* by the total size of MAC SDUs served to logical channel *j* at 340. The total size of MAC SDUs served to logical channel *j* is represented by Tsdu.

[0091] At 350, the UE 104 multiplex an SDU 315 in a MAC PDU.

[0092] At 360, the UE 104 determines whether PBR is met.

[0093] If PBR is met, the UE 104 processes the next LCH at 370.

[0094] If PBR is not met, the process 300 proceeds to block 395. At 395, the UE 104 receives packets from upper layer.

[0095] If the UE 104 determines *Bj* is not greater than zero at 330, the UE 104 determines, at 380, there are no available tokens in the token bucket 305 and the SDU 315 will not be multiplexed in the MAC PDU.

[0096] At 390, the UE 104 determines the processing of this LCH is completed, and then the next logical channel with lower priority will be processed.

[0097] In view of the above, the present disclosure provides a solution that supports logical channel prioritization based on synchronization delay status. In this solution, a UE determines synchronization delay status of data in a first synchronization transmission set. In turn, the UE prioritizes transmission of the data based on the synchronization delay status of the data. In this way, logical channel prioritization based on synchronization delay status may be achieved. Thus, the user experience may be improved.

[0098] Hereinafter, principle of the present disclosure will be described with reference to Figs. 4 to 10.

[0099] Fig. 4 illustrates a signaling chart illustrating an example process 400 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure. For the purpose of discussion, the process 400 will be described with reference to Fig. 1. The process 400 may involve the UE 104 and the network entity 102 in Fig. 1.

[0100] As shown in Fig. 4, the UE 104 determines 420 synchronization delay status of data in a synchronization transmission set.

[0101] In some implementations, the synchronization transmission set may comprise packets associated with one or multiple QoS flows. An example of a synchronization transmission set will be described later with reference to Fig. 5.

[0102] In some implementations, a set of packets which are carried by one or multiple QoS flows and need synchronization transmission may be defined as a synchronization transmission set.

[0103] In some implementations, the UE 104 may identify packets in a synchronization transmission set from the upper layer.

[0104] In some implementations, the synchronization transmission set may be referred to as synchronization PDU sets. For example, the synchronization transmission set may comprise at least two PDU sets and each of the at least two PDU sets is associated with a QoS flow.

[0105] In some implementations, the synchronization transmission set may comprise one or more PDUs associated with a first QoS flow as well as one or more PDUs associated with a second QoS flow. The first QoS flow and the second QoS flow are QoS flows that are indicated by synchronization transmission association of QoS flows.

[0106] Alternatively, in some implementations, the synchronization transmission set may comprise one or more PDU sets associated with the first QoS flow as well as one or more PDUs associated with the second QoS flow.

[0107] Alternatively, in some implementations, the synchronization transmission set may comprise one or more PDU sets associated with the first QoS flow as well as one or more PDU sets associated with the second QoS flow.

[0108] In some implementations, a PDU set may comprise one or more PDUs carrying the payload of one unit of information generated at an application level. For example, the unit of information may be a frame or video slice for XR services. In some implementations, all PDUs in a PDU set are needed by an application layer of the UE 104 to use the corresponding unit of information. In other implementations, the application layer can still recover parts or all of the information unit when some PDUs are missing.

[0109] In some implementations, the synchronization transmission set may comprise one or more data bursts associated with the first QoS flow as well as one or more data bursts associated with the second QoS flow. In some implementations, a data burst may

be a set of multiple PDUs generated and sent by an application in a short period of time. Alternatively, in some implementations, a data burst may comprise one or multiple PDU sets.

[0110] In some implementations, the synchronization transmission set may be carried on one data radio bearer (DRB). Alternatively, the synchronization transmission set may be carried on multiple DRBs. For example, the multiple DRBs may comprise a first DRB and a second DRB. For example, one part of data in the synchronization transmission set is carried on the first DRB, and another part of data in the synchronization transmission set is carried on the second DRB.

[0111] In some implementations, the data in the synchronization transmission set may comprise a first type of data. The synchronization delay status of the data may comprise first remaining synchronization delay of the first type of data. The first remaining synchronization delay of the first type of data is below a first threshold. In other words, the first remaining synchronization delay of the first type of data is equal to or less than the first threshold.

[0112] In some implementations, in order to determine the synchronization delay status of the data in the synchronization transmission set, the UE 104 may determine a synchronization delay status per packet of an LCH. For example, a packet of the LCH may comprise a PDCP SDU corresponding a PDU in the synchronization transmission set.

[0113] In some implementations, if remaining synchronization delay of a packet is below the first threshold, the UE 104 may consider the packet as the first type of data. Hereinafter, the first type of data is also referred to as synchronization delay critical data. The first threshold may be configured by the network entity 102 or predefined.

[0114] In some implementations, the UE 104 may determine the remaining synchronization delay of the packet based on a synchronization timer. For example, the UE 104 may start the synchronization timer at a PDCP layer of the UE 104 upon reception the packet from upper layer. The UE 104 may determine the remaining synchronization delay of the packet as remaining time of the synchronization timer. In such implementations, the first threshold may be configured separately from *remainingTimeThreshold* which is the threshold on remaining time for triggering a delay status report (DSR) for a logical channel group (LCG).

[0115] Alternatively, in some implementations, the UE 104 may reuse *remainingTimeThreshold* as the first threshold. In such implementations, the synchronization delay status is same as the delay status based on remaining time of a discard timer (i.e., remaining discard time). That is to say, the synchronization delay critical data is same as the delay critical data.

[0116] In some implementations, the first threshold may be configured per UE by the network entity 102. For example, the network entity 102 may configure a percentage. Then, the UE 104 may determine the first threshold as a product of a base threshold * the percentage. The base threshold may be a value of a discarding timer for a DRB carrying the synchronization delay critical data. For example, the base threshold may be equal to 50ms and the percentage may be equal to 20%. The UE 104 may determine the first threshold as a product of 50*20% (ms). That is, the UE 104 may determine the first threshold as 10ms.

[0117] Alternatively, in some implementations, the synchronization transmission set may comprise a packet #1 of an LCH #1 and a packet #2 of a LCH #2. The packet #1 arrives at the UE 104 before the packet #2. The UE 104 may determine remaining synchronization delay of the packet #2 based on the relative arrival time between the packet #1 and the packet #2. The packet #1 of the LCH #1 may be a packet of the LCH #1 which arrives at the UE 104 first or a packet of the LCH #1 which arrives at the UE 104 last. The packet #2 of the LCH #2 may be a packet of the LCH #2 which arrives at the UE 104 first or a packet of the LCH #2 which arrives at the UE 104 last.

[0118] Alternatively, in some implementations, the synchronization transmission set may comprise a packet #1 of an LCH #1 and a packet #2 of a LCH #2. The packet #1 arrives at the UE 104 before the packet #2. The UE 104 may determine remaining synchronization delay of the packet #2 based on the relative transmission time between the packet #1 and the packet #2. The packet #1 of the LCH #1 may be a packet of the LCH #1 which is transmitted by the UE 104 first or a packet of the LCH #1 which is transmitted by the UE 104 last. The packet #2 of the LCH #2 may be a packet of the LCH #2 which is transmitted by the UE 104 first or a packet of the LCH #2 which is transmitted by the UE 104 last.

[0119] Alternatively, in some implementations, the synchronization transmission set may comprise a packet #1 of an LCH #1 and a packet #2 of a LCH #2. The packet #1 is

transmitted by the UE 104 before the packet #2 arrives at the UE 104. The UE 104 may determine remaining synchronization delay of the packet #2 based on a time difference between arrival time of the packet #2 and transmission time of the packet #1. The packet #1 of the LCH #1 may be a packet of the LCH #1 which is transmitted by the UE 104 first or a packet of the LCH #1 which is transmitted by the UE 104 last. The packet #2 of the LCH #2 may be a packet of the LCH #2 which is transmitted by the UE 104 first or a packet of the LCH #2 which is transmitted by the UE 104 last.

[0120] With continued reference to Fig. 4, the UE 104 prioritizes 430 transmission of the data in the synchronization transmission set based on the synchronization delay status of the data.

[0121] For example, the UE 104 may prioritize transmission of part of data in the synchronization transmission set based on the synchronization delay status of the data. Alternatively, the UE 104 may prioritize transmission of all the data in the synchronization transmission set based on the synchronization delay status of the data.

[0122] In some implementations, optionally, the UE 104 may receive 410, from the network entity 102, a first indication indicating whether to prioritize transmission of the data based on the synchronization delay status of the data. If the first indication indicates to prioritize transmission of the data based on the synchronization delay status of the data, the UE 104 may prioritize the transmission of the data in the synchronization transmission set based on the synchronization delay status of the data.

[0123] In some implementations, the first indication may indicate, per LCH, DRB, or QoS flow, to prioritize transmission of the data based on the synchronization delay status of the data.

[0124] With the process 400, logical channel prioritization based on synchronization delay status may be achieved. Thus, the user experience may be improved.

[0125] Fig. 5 illustrates an example of a synchronization transmission set in accordance with some implementations of the present disclosure. As shown in Fig. 5, a synchronization transmission set comprises one or more PDU sets associated with a first QoS flow as well as one or more PDUs associated with a second QoS flow. The first QoS flow may be a video flow and the second QoS flow may be a tactile flow. For example, a synchronization (SYNC) transmission set 500 comprises a PDU set 510 of the video flow

as well as PDUs 520 and 522 of the tactile flow. The PDU set 510 comprises PDUs 512, 514 and 516. The PDUs 512, 514 and 516 of the video flow are carried on a first DRB. The PDUs 520 and 522 are carried on a second DRB.

[0126] In some implementations, the UE 104 may prioritize the transmission of the data in the synchronization transmission set by prioritizing transmission of data of a first LCH. The synchronization transmission set is carried on the first LCH. The first LCH has the synchronization transmission set and the synchronization transmission set has the first type of data.

[0127] Alternatively, in some implementations, the UE 104 may prioritize the transmission of the data by prioritizing transmission of all the data in the synchronization transmission set.

[0128] Alternatively, in some implementations, the UE 104 may prioritize the transmission of the data by prioritizing transmission of the first type of data in the synchronization transmission set.

[0129] In some implementations, the UE 104 may prioritize the transmission of the first type of data by increasing at least a first priority level for the first type of data to a target priority level.

[0130] In some implementations, the UE 104 may receive a configuration for the target priority level from the network entity 102. In turn, the UE 104 may determine the target priority level based on the configuration.

[0131] In some implementations, the configuration for the target priority level may comprise an absolute target priority value. For example, the absolute target priority value may be an absolute target priority value for the first type of data. The UE 104 may increase the first priority level for the first type of data based on the absolute target priority value. In such implementations, the UE 104 may increase the first priority level for the first type of data to the absolute target priority value.

[0132] Alternatively, in some implementations, the configuration for the target priority level may comprise a priority offset value. For example, the priority offset value may be a priority offset value for the first type of data. The UE 104 may increase the first priority level for the first type of data by the priority offset value. For example, the first priority level for the first type of data may be configured by the network entity 102 via an

RRC signaling. The UE 104 may determine the target priority level for the first type of data as the first priority level minus the priority offset value (i.e., a difference between the first priority level and the priority offset value).

[0133] Alternatively, in some implementations, the configuration for the target priority level may comprise a factor. For example, the factor may be a factor for the first type of data. The UE 104 may increase the first priority level for the first type of data based on the factor. For example, the UE 104 may determine the target priority level based on the following: floor (factor * the first priority level), where "floor" represents a rounding down operation.

[0134] Alternatively or additionally, in some implementations, the UE 104 may increase the first priority level for the first type of data based on mapping between the factor and the first remaining synchronization delay of the first type of data. The mapping between the factor and the first remaining synchronization delay of the first type of data may be configured by the network entity 102.

[0135] In some implementations, the configuration for the target priority level may be configured by the network entity 102 per LCH, DRB or QoS flow.

[0136] In some implementations, the UE 104 may prioritize the transmission of the data in the synchronization transmission set based on the synchronization delay status of the data and a value which is maintained for a first LCH having the data. As used herein, a value which is maintained for an LCH j is represented by Bj. This will be described with reference to Fig. 6.

[0137] Fig. 6 illustrates a flowchart of a method 600 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure. The method 600 may be considered as an example implementation of the action 420 in Fig. 4. For the purpose of discussion, the method 600 will be described from the perspective of the UE 104 with reference to Fig. 1.

[0138] Generally, in the method 600, the UE 104 prioritizes the transmission of the data in the synchronization transmission set based on the synchronization delay status of the data and the value which is maintained for the first LCH having the data. In order to prioritize the transmission of the data in the synchronization transmission set, the UE 104 may increase at least the first priority level for the first type of data to the target priority

level during the first round of resource allocation procedure (i.e., based on a value of Bj >0).

[0139] As shown in Fig. 6, at 610, the UE 104 may increase at least the first priority level for the first type of data in the synchronization transmission set to the target priority level. The UE 104 may increase at least the first priority level for the first type of data during the second round of resource allocation procedure (i.e., regardless of the value of Bj).

[0140] In some implementations, the UE 104 may increase at least the first priority level for the first type of data to the target priority level by increasing a second priority level for a first LCH to the target priority level. The first LCH has the first type of data. Alternatively, the UE 104 may increase at least the first priority level for the first type of data to the target priority level by increasing only the first priority level for the first type of data to the target priority level. Alternatively, the UE 104 may increase at least the first priority level for the first type of data to the target priority level by increasing a third priority level for the synchronization transmission set to the target priority level. The synchronization transmission set comprises the first type of data. Such implementations will be described later with reference to Fig. 8.

[0141] At 620, the UE 104 may allocate resources to data of LCHs for a UL grant with Bj > 0 in a decreasing priority order. For example, the UE 104 may allocate resources to the data of LCHs for the UL grant with Bj > 0 in the decreasing priority order by performing the process 300 in Fig. 3.

[0142] In some implementations, the UE 104 may prioritize the transmission of the data in the synchronization transmission set based on the synchronization delay status of the data regardless of the value which is maintained for the first LCH having the data. As used herein, a value which is maintained for an LCH *j* is represented by *Bj*. This will be described with reference to Fig. 7.

[0143] Fig. 7 illustrates a flowchart of a method 700 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure. The method 700 may be considered as an example implementation of the action 420 in Fig. 4. For the purpose of discussion, the method 700 will be described from the perspective of the UE 104 with reference to Fig. 1.

[0144] Generally, in the method 700, the UE 104 prioritizes the transmission of the data in the synchronization transmission set based on the synchronization delay status of the data regardless of the value which is maintained for the first LCH having the data. In order to prioritize the transmission of the data in the synchronization transmission set, the UE 104 may increase at least the first priority level for the first type of data to the target priority level during the second round of resource allocation procedure after the first round of resource allocation procedure.

[0145] As shown in Fig. 7, at 710, the UE 104 may perform the first round of resource allocation procedure to allocate resources to data of LCHs for a UL grant with $Bj > 0$ in a decreasing priority order. For example, the UE 104 may allocate resources to the data of LCHs for the UL grant with $Bj > 0$ in the decreasing priority order by performing the process 300 in Fig. 3.

[0146] At 720, the UE 104 decrements Bj by the total size of MAC SDUs served to LCH j.

[0147] At 730, if any resources remain, the UE 104 may increase at least the first priority level for the first type of data in the synchronization transmission set to the target priority level. In other words, the UE 104 may increase at least the first priority level for the first type of data during the second round of resource allocation procedure.

[0148] If the UE 104 has increased, at 710, at least the first priority level for the first type of data in the synchronization transmission set to the target priority level, the UE 104 may not increase, at 730, at least the first priority level for the first type of data in the synchronization transmission set to the target priority level again. In this case, the UE 104 uses the target priority level at 730.

[0149] Similar to the action 610 in Fig. 6, in some implementations, the UE 104 may increase at least the first priority level for the first type of data to the target priority level by increasing a second priority level for a first LCH to the target priority level. The first LCH has the first type of data. Alternatively, the UE 104 may increase at least the first priority level for the first type of data to the target priority level by increasing only the first priority level for the first type of data to the target priority level. Alternatively, the UE 104 may increase at least the first priority level for the first type of data to the target priority level by increasing a third priority level for the synchronization transmission set

to the target priority level. The synchronization transmission set comprises the first type of data. Such implementations will be described later with reference to Fig. 8.

[0150] At 740, the UE 104 may allocate resources to data of LCHs for a UL grant (regardless of the value of *Bj*) in a decreasing priority order.

[0151] Fig. 8 illustrates an example of data of a first LCH in accordance with aspects of the present disclosure. As shown in Fig. 8, the first LCH has a first synchronization transmission set and a second synchronization transmission set.

[0152] The first synchronization transmission set comprises the first type of data (i.e., synchronization delay critical data) and a second type of data. Second remaining synchronization delay of the second type of data is above the first threshold. Hereinafter, the second type of data is also referred to as non-synchronization delay critical data.

[0153] The second synchronization transmission set only comprises the non-synchronization delay critical data.

[0154] In some implementations, the UE 104 may increase at least the first priority level for the synchronization delay data to the target priority level by increasing a priority level for the first LCH to the target priority level. In other words, the UE 104 may increase a priority level for all the data of the first LCH to the target priority level.

[0155] Alternatively, the UE 104 may increase at least the first priority level for the synchronization delay data to the target priority level by increasing only the first priority level for the synchronization delay data in the first synchronization transmission set to the target priority level. The UE 104 may keep the first priority level for the non-synchronization delay data of the first LCH unchanged. That is, the UE 104 may keep the first priority level for the non-synchronization delay data in the first and second synchronization transmission sets unchanged.

[0156] Alternatively, the UE 104 may increase at least the first priority level for the synchronization delay data to the target priority level by increasing a priority level for the first synchronization transmission set to the target priority level. In other words, the UE 104 may increase a priority level for all the data in the first synchronization transmission set to the target priority level. That is, he UE 104 may increase a priority level for the synchronization delay data and the non-synchronization delay data in the first synchronization transmission set to the target priority level.

[0157] In some implementations, the UE 104 may prioritize transmission for an LCH with the first type of data over another LCH without the first type of data. This will be described later with reference to Fig. 9.

[0158] Fig. 9 illustrates a flowchart of a method 900 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure. The method 900 may be considered as an example implementation of the action 420 in Fig. 4. For the purpose of discussion, the method 900 will be described from the perspective of the UE 104 with reference to Fig. 1.

[0159] As shown in Fig. 9, at 910, the UE 104 may divide LCHs into at least two groups. For example, the UE 104 may divide LCHs into a first group of LCHs and a second group of LCHs. Each of the LCHs in the first group comprises the first type of data. Each of the LCHs in the second group does not comprise the first type of data.

[0160] At 920, in order to prioritize transmission of data of the LCHs in the first group over data of the LCHs in the second group, the UE 104 may increase priority levels at least for the first type of data of the LCHs in the first group to the target priority level.

[0161] In some implementations, the UE 104 may increase priority levels for the data of the LCHs in the first group to the target priority level during the first round of resource allocation procedure.

[0162] Alternatively, the UE 104 may increase priority levels for the data of the LCHs in the first group to the target priority level during the second round of resource allocation procedure.

[0163] At 930, the UE 104 may allocate resources to the LCHs in the first group before allocating resources to the LCHs in the second group.

[0164] For example, during the first round of resource allocation procedure, the UE 104 may allocate resources to data of the LCHs in the first group and the second group for a UL grant with $Bj > 0$ in decreasing priority order of the LCHs.

[0165] For another example, during the second round of resource allocation procedure, the UE 104 may allocate resources to data of the LCHs in the first group and the second group for a UL grant regardless of the value of Bj in decreasing priority order of the LCHs.

[0166] In some implementations, the first group may comprise a first LCH and a second LCH. Each of the first LCH and the second LCH comprises the first type of data.

[0167] In such implementations, the UE 104 may allocate resources to the data of the first LCH and the second LCH selected for the UL grant with Bj >0 in a decreasing priority (e.g., original priority level or target priority level) order. For example, if a first priority level for the first LCH is higher than a second priority level for the second LCH, the UE 104 may allocate resources to the data of the first LCH before allocating resources to the data of the second LCH. The first priority level may be an original priority level for the first LCH, and the second priority level may be an original priority level for the second LCH. The original priority level may be configured by the network entity 102 via an RRC signalling.

[0168] Alternatively, in such implementations, the UE 104 may allocate resources to the data of the first LCH and the second LCH selected for the UL grant with Bj >0 in an increasing order of remaining synchronization delays. For example, if the first remaining synchronization delay of the first type of data in the first LCH is less than second remaining synchronization delay of the first type of data in the second LCH, the UE 104 may allocate resources to the data of the first LCH before allocating resources to the data of the second LCH.

[0169] Alternatively, at 930, the UE 104 may allocate resources to the first type of data (i.e., the synchronization delay critical data) before allocating resources to the second type of data (i.e., non-synchronization delay critical data). For example, if the first LCH has the synchronization delay critical data and the non-synchronization delay critical data, the UE 104 may only increase the priority level for the synchronization delay critical data to the target priority level.

[0170] Alternatively, at 930, the UE 104 may allocate resources to a synchronization transmission set comprising the synchronization delay critical data before allocating resources to a synchronization transmission set comprising the non-synchronization delay critical data. For example, the first LCH has a first synchronization transmission set and a second synchronization transmission set. The first synchronization transmission set comprises the synchronization delay critical data. The second synchronization transmission set does not comprise the synchronization delay critical data. That is, the second synchronization transmission set only comprises the non-synchronization delay

critical data. The UE 104 may only increase the priority level for the first synchronization set comprising the synchronization delay critical data to the target priority level.

[0171] Fig. 10 illustrates a signaling chart illustrating an example process 1000 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure. For the purpose of discussion, the process 1000 will be described with reference to Fig. 1. The process 1000 may involve the UE 104 and the network entity 102 in Fig. 1.

[0172] As shown in Fig. 10, the UE 104 determines 1020 delay status of data based on at least one of multiple thresholds.

[0173] In turn, the UE 104 prioritizes 1030 transmission of the data based on one of the multiple thresholds.

[0174] In some implementations, the data may comprise data in a synchronization transmission set. In such implementations, the UE 104 may determine the delay status of the data by determining synchronization delay status of the data in the synchronization transmission set, as described with reference to Figs. 4 to 9. Implementations of determining synchronization delay status of the data in the synchronization transmission set are omitted for brevity.

[0175] In some implementations, the data may comprise the first type of data (i.e., the synchronization delay critical data) as described above with reference to Figs. 4 to 9. The first remaining synchronization delay of the first type of data is below the first threshold among the multiple thresholds. In such implementations, the UE 104 may determine the delay status of the data by determining the first remaining synchronization delay of the first type of data based on at least one of multiple thresholds.

[0176] Alternatively, in some implementations, the UE 104 may determine the delay status of the data by determining delay status of data in an LCH. In such implementations, the UE 104 may determine the delay status of the data by determining remaining time of a discard timer for the data based on at least one of multiple thresholds.

[0177] In some implementations, the data may further comprise a third type of data. Third remaining time of a discard timer for the third type of data is below a second threshold among the multiple thresholds. In such implementations, the UE 104 may determine the delay status of the data by determining the third remaining time of the

discard timer for the third type of data. Hereinafter, the third type of data is also referred to as delay critical data.

[0178] In some implementations, the UE 104 may prioritize the transmission of one of the first type of data and the third type of data.

[0179] In some implementations, a first LCH has both the first type of data and the third type of data. Alternatively, the first LCH has the first type of data, and a second LCH has the third type of data.

[0180] In some implementations, optionally, the UE 104 may receive 1010 a second indication from the network entity 102.

[0181] In some implementations, the second indication may indicate to prioritize the transmission of the first type of data based on the first threshold. This will be described with reference to Fig. 11A.

[0182] Fig. 11A illustrates an example of data of a first LCH in accordance with aspects of the present disclosure. As shown in Fig. 11A, the first LCH has both the first type of data and the third type of data. In other words, the first LCH has both the synchronization delay critical data and the delay critical data.

[0183] The second indication may indicate to prioritize the transmission of the synchronization delay critical data based on the first threshold. In such implementations, the UE 104 may prioritize, based on the second indication, the transmission of the synchronization delay critical data based on the first threshold. Such implementations may simplify implementation of the UE 104.

[0184] In some implementations, in order to prioritize the transmission of the first type of data (i.e., the synchronization delay critical data), the UE 104 may increase a first priority level for the first type of data to a first target priority level. For example, the UE 104 may increase the first priority level for the first type of data by performing the process 400 or any of the methods 600, 700 and 900.

[0185] In some implementations, the network entity 102 may configure the multiple thresholds by configuring multiple *remainingTimeThresholds*. One of *remainingTimeThresholds* may be used as the first threshold.

[0186] In some implementations, the synchronization delay status of the synchronization delay critical data may be the same as the delay status of the delay critical data based on remaining time of a discard timer (i.e., remaining discard time). That is to say, the synchronization delay critical data may be the same as the delay critical data.

[0187] In some implementations, the network entity 102 may configure the UE 104 to prioritize at least the transmission of the synchronization delay critical data based on which *remainingTimeThreshold*.

[0188] In some implementations, the network entity 102 may configure the UE 104 to prioritize at least the transmission of the synchronization delay critical data based on one of multiple *remainingTimeThresholds*.

[0189] For example, *remainingTimeThresholds* may comprise *remainingTimeThreshold#1* and *remainingTimeThreshold#2*. *RemainingTimeThreshold#1* is equal to 5ms and *remainingTimeThreshold#2* is equal to 10ms. The network entity 102 may configure the UE 104 to prioritize the transmission of the synchronization delay critical data based on *remainingTimeThreshold#2*.

[0190] If remaining synchronization delay of data in a synchronization transmission set is equal to 6ms, the UE 104 may determine the remaining synchronization delay is above *remainingTimeThreshold#1* (5ms) and below *remainingTimeThreshold#2* (10ms). In other words, the UE 104 may determine the delay status of the data based on two thresholds among the multiple thresholds. In this case, the synchronization delay critical data may comprise the data with remaining synchronization delay above *remainingTimeThreshold#1* (5ms) and below *remainingTimeThreshold#2* (10ms).

[0191] Alternatively, if remaining synchronization delay of data in the synchronization transmission set is equal to 6ms, the UE 104 may determine the remaining synchronization delay is below *remainingTimeThreshold#2* (10ms). In other words, the UE 104 may determine the delay status of the data based on one of the multiple thresholds. In this case, the synchronization delay critical data may comprise the data with remaining synchronization delay below *remainingTimeThreshold#2*.

[0192] It shall be noted that in other implementations, the UE 104 may determine the delay status of the data based on more than two thresholds among the multiple thresholds.

[0193] Alternatively, in some implementations, the second indication may indicate to prioritize the transmission of the third type of data based on the second threshold. This will be described with reference to Fig. 11B.

[0194] Fig. 11B illustrates an example of data of a first LCH in accordance with aspects of the present disclosure. As shown in Fig. 11B, the first LCH has both the first type of data and the third type of data. In other words, the first LCH has both the synchronization delay critical data and the delay critical data.

[0195] The second indication may indicate to prioritize the transmission of the delay critical data based on the second threshold. In such implementations, the UE 104 may prioritize, based on the second indication, the transmission of the delay critical data based on the second threshold. Such implementations may simplify implementation of the UE 104.

[0196] In some implementations, the UE 104 may prioritize, by default, the transmission of the delay critical data based on the smallest threshold among the multiple thresholds for the LCH carrying the data. In such implementations, the UE 104 does not need receive the second indication which indicates the UE 104 to prioritize the transmission of the delay critical data based on which threshold.

[0197] In some implementations, in order to prioritize the transmission of the third type of data (i.e., the delay critical data), the UE 104 may increase a second priority level for the third type of data to a second target priority level.

[0198] Alternatively, in some implementations, the second indication may indicate to prioritize the transmission of the first type of data based on the first threshold and to prioritize the transmission of the third type of data based on the second threshold. This will be described with reference to Fig. 11C.

[0199] Fig. 11C illustrates an example of data of a first LCH in accordance with aspects of the present disclosure. As shown in Fig. 11C, the first LCH has both the first type of data and the third type of data. In other words, the first LCH has both the synchronization delay critical data and the delay critical data.

[0200] The second indication may indicate to prioritize the transmission of the first type of data based on the first threshold and to prioritize the transmission of the third type of data based on the second threshold. In such implementations, the UE 104 may prioritize,

based on the second indication, the transmission of the synchronization delay critical data based on the first threshold and the transmission of the delay critical data based on the second threshold.

[0201] In some implementations, in order to prioritize the transmission of the first type of data (i.e., the synchronization delay critical data), the UE 104 may increase a first priority level for the first type of data to a first target priority level. For example, the UE 104 may increase the first priority level for the first type of data by performing the process 400 or any of the methods 600, 700 and 900.

[0202] In some implementations, in order to prioritize the transmission of the third type of data (i.e., the delay critical data), the UE 104 may increase a second priority level for the third type of data to a second target priority level.

[0203] In some implementations, if one data belongs to the first type of data and the third type of data, the UE 104 may use the highest target priority level of the data after the UE 104 may separately increase the priority level for the data to the target priority level.

[0204] In some implementations, if the first LCH has both the synchronization delay critical data and the delay critical data, the UE 104 may only prioritize the transmission of the third type of data (i.e., the delay critical data). In this case, the UE 104 may only increase a second priority level for the third type of data to a second target priority level. Such implementations may simplify implementation of the UE 104.

[0205] It shall be noted that some implementations of the present disclosure which have been described with reference to Figs. 4 to 9 may be applied to the process 1000. Details of these implementations are omitted for brevity.

[0206] Fig. 12 illustrates a signaling chart illustrating an example process 1200 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure. For the purpose of discussion, the process 1200 will be described with reference to Fig. 1. The process 1200 may involve the UE 104 and the network entity 102 in Fig. 1.

[0207] As shown in Fig. 12, the UE 104 determines 1210 synchronization delay status of data in a synchronization transmission set.

[0208] The action 1210 in Fig. 12 is similar to the action 420 in Fig. 4. Details of this action is omitted for brevity.

[0209] In turn, the UE 104 maximizes transmission of the data in the synchronization transmission set if a UL grant is enough to accommodate the data. For example, the UE 104 may maximize the transmission of the synchronization delay critical data as possible if the synchronization transmission set fits into resources of the associated MAC entity.

[0210] With the process 1200, the UE 104 maximizes transmission of the data in the synchronization transmission set to guarantee the synchronization threshold for multi-modality VR applications.

[0211] In some implementations, the network entity 102 may configure the UE 104 to maximize transmission of the data in the synchronization transmission set per QoS flow, LCH or DRB.

[0212] In some implementations, remaining synchronization delay of a packet in the synchronization transmission set is separate from remaining time of a discard timer for the packet. In such implementations, the UE 104 may determine the remaining synchronization delay of a packet in the synchronization transmission set.

[0213] If the remaining synchronization delay of the packet is below the first threshold, the UE 104 may consider the packet as the first type of data, i.e., the synchronization delay critical data.

[0214] In turn, the UE 104 may maximize transmission of data of a first LCH if a UL grant is enough to accommodate the data of the first LCH. The first LCH has the first type of data, and the first remaining synchronization delay of the first type of data is below the first threshold.

[0215] Alternatively, the UE 104 may maximize transmission of all the data in the synchronization transmission set if the UL grant is enough to accommodate all the data in the synchronization transmission set.

[0216] Alternatively, the UE 104 may maximize transmission of the first type of data in the synchronization transmission set if the UL grant is enough to accommodate the first type of data.

[0217] In some implementations, remaining synchronization delay of a packet in the synchronization transmission set is the same as remaining time of a discard timer for the packet. In such implementations, the UE 104 may determine the remaining time of a discard timer for the packet in the synchronization transmission set. For example, the UE 104 may set and start the discard timer for the packet in the synchronization transmission set. For another example, the UE 104 may set and start the discard timer for the synchronization transmission set.

[0218] If the remaining time is below the first threshold, the UE 104 may consider the packet as the first type of data. In this case, the first type of data comprises the delay critical data. That is, the first type of data is the same as the third type of data.

[0219] In turn, the UE 104 may maximize transmission of data of a first LCH if a UL grant is enough to accommodate the data of the first LCH. The first LCH has the first type of data, and the first remaining synchronization delay of the first type of data is below the first threshold.

[0220] Alternatively, the UE 104 may maximize transmission of all the data in the synchronization transmission set if the UL grant is enough to accommodate all the data in the synchronization transmission set.

[0221] Alternatively, the UE 104 may maximize transmission of the first type of data in the synchronization transmission set if the UL grant is enough to accommodate the first type of data.

[0222] In some implementations, in order to maximize the transmission of the data in the synchronization transmission set, the UE 104 may determine Bj based on a size of the synchronization delay critical data, a size of the synchronization transmission set or a size of data of an LCH having the synchronization delay critical data. In turn, the UE 104 may allocate resources to data of LCHs for a UL grant with $Bj > 0$ in a decreasing priority order.

[0223] It shall be noted that some implementations of the present disclosure which have been described with reference to Figs. 4 to 9 may be applied to the process 1200. Details of these implementations are omitted for brevity.

[0224] Fig. 13 illustrates an example of a device 1300 that supports logical channel prioritization in accordance with aspects of the present disclosure. The device 1300 may

be an example of a network entity 102 or a UE 104 as described herein. The device 1300 may support wireless communication with one or more network entities 102, UEs 104, or any combination thereof. The device 1300 may include components for bi-directional communications including components for transmitting and receiving communications, such as a processor 1302, a memory 1304, a transceiver 1306, and, optionally, an I/O controller 13014. These components may be in electronic communication or otherwise coupled (e.g., operatively, communicatively, functionally, electronically, electrically) via one or more interfaces (e.g., buses).

[0225] The processor 1302, the memory 1304, the transceiver 1306, or various combinations thereof or various components thereof may be examples of means for performing various aspects of the present disclosure as described herein. For example, the processor 1302, the memory 1304, the transceiver 1306, or various combinations or components thereof may support a method for performing one or more of the operations described herein.

[0226] In some implementations, the processor 1302, the memory 1304, the transceiver 1306, or various combinations or components thereof may be implemented in hardware (e.g., in communications management circuitry). The hardware may include a processor, a digital signal processor (DSP), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA) or other programmable logic device, a discrete gate or transistor logic, discrete hardware components, or any combination thereof configured as or otherwise supporting a means for performing the functions described in the present disclosure. In some implementations, the processor 1302 and the memory 1304 coupled with the processor 1302 may be configured to perform one or more of the functions described herein (e.g., executing, by the processor 1302, instructions stored in the memory 1304).

[0227] For example, the processor 1302 may support wireless communication at the device 1300 in accordance with examples as disclosed herein. The processor 1302 may be configured to operable to support a means for performing the following: determining synchronization delay status of data in a synchronization transmission set; and prioritizing transmission of the data based on the synchronization delay status of the data.

[0228] Alternatively, in some implementations, the processor 1302 may be configured to operable to support a means for performing the following: determining

delay status of data based on at least one of multiple thresholds; and prioritizing transmission of the data based on one of the multiple thresholds.

[0229] Alternatively, in some implementations, the processor 1302 may be configured to operable to support a means for performing the following: determining synchronization delay status of data in a synchronization transmission set; and maximizing transmission of the data based on determining that an uplink grant is enough to accommodate the data.

[0230] The processor 1302 may include an intelligent hardware device (e.g., a general-purpose processor, a DSP, a CPU, a microcontroller, an ASIC, an FPGA, a programmable logic device, a discrete gate or transistor logic component, a discrete hardware component, or any combination thereof). In some implementations, the processor 1302 may be configured to operate a memory array using a memory controller. In some other implementations, a memory controller may be integrated into the processor 1302. The processor 1302 may be configured to execute computer-readable instructions stored in a memory (e.g., the memory 1304) to cause the device 1300 to perform various functions of the present disclosure.

[0231] The memory 1304 may include random access memory (RAM) and read-only memory (ROM). The memory 1304 may store computer-readable, computer-executable code including instructions that, when executed by the processor 1302 cause the device 1300 to perform various functions described herein. The code may be stored in a non-transitory computer-readable medium such as system memory or another type of memory. In some implementations, the code may not be directly executable by the processor 1302 but may cause a computer (e.g., when compiled and executed) to perform functions described herein. In some implementations, the memory 1304 may include, among other things, a basic I/O system (BIOS) which may control basic hardware or software operation such as the interaction with peripheral components or devices.

[0232] The I/O controller 13014 may manage input and output signals for the device 1300. The I/O controller 13014 may also manage peripherals not integrated into the device M02. In some implementations, the I/O controller 13014 may represent a physical connection or port to an external peripheral. In some implementations, the I/O controller 13014 may utilize an operating system such as iOS®, ANDROID®, MS-WINDOWS®, OS/2®, UNIX®, LINUX®, or another known operating system. In some

implementations, the I/O controller 13014 may be implemented as part of a processor, such as the processor 1302. In some implementations, a user may interact with the device 1300 via the I/O controller 13014 or via hardware components controlled by the I/O controller 13014.

[0233] In some implementations, the device 1300 may include a single antenna 1310. However, in some other implementations, the device 1300 may have more than one antenna 1310 (i.e., multiple antennas), including multiple antenna panels or antenna arrays, which may be capable of concurrently transmitting or receiving multiple wireless transmissions. The transceiver 1306 may communicate bi-directionally, via the one or more antennas 1310, wired, or wireless links as described herein. For example, the transceiver 1306 may represent a wireless transceiver and may communicate bi-directionally with another wireless transceiver. The transceiver 1306 may also include a modem to modulate the packets, to provide the modulated packets to one or more antennas 1310 for transmission, and to demodulate packets received from the one or more antennas 1310. The transceiver 1306 may include one or more transmit chains, one or more receive chains, or a combination thereof.

[0234] A transmit chain may be configured to generate and transmit signals (e.g., control information, data, packets). The transmit chain may include at least one modulator for modulating data onto a carrier signal, preparing the signal for transmission over a wireless medium. The at least one modulator may be configured to support one or more techniques such as amplitude modulation (AM), frequency modulation (FM), or digital modulation schemes like phase-shift keying (PSK) or quadrature amplitude modulation (QAM). The transmit chain may also include at least one power amplifier configured to amplify the modulated signal to an appropriate power level suitable for transmission over the wireless medium. The transmit chain may also include one or more antennas 1310 for transmitting the amplified signal into the air or wireless medium.

[0235] A receive chain may be configured to receive signals (e.g., control information, data, packets) over a wireless medium. For example, the receive chain may include one or more antennas 1310 for receive the signal over the air or wireless medium. The receive chain may include at least one amplifier (e.g., a low-noise amplifier (LNA)) configured to amplify the received signal. The receive chain may include at least one demodulator configured to demodulate the receive signal and obtain the transmitted data by reversing

the modulation technique applied during transmission of the signal. The receive chain may include at least one decoder for decoding the processing the demodulated signal to receive the transmitted data.

[0236] Fig. 14 illustrates an example of a processor 1400 that supports logical channel prioritization in accordance with aspects of the present disclosure. The processor 1400 may be an example of a processor configured to perform various operations in accordance with examples as described herein. The processor 1400 may include a controller 1402 configured to perform various operations in accordance with examples as described herein. The processor 1400 may optionally include at least one memory 1404, such as L1/L2/L3 cache. Additionally, or alternatively, the processor 1400 may optionally include one or more arithmetic-logic units (ALUs) 1406. One or more of these components may be in electronic communication or otherwise coupled (e.g., operatively, communicatively, functionally, electronically, electrically) via one or more interfaces (e.g., buses).

[0237] The processor 1400 may be a processor chipset and include a protocol stack (e.g., a software stack) executed by the processor chipset to perform various operations (e.g., receiving, obtaining, retrieving, transmitting, outputting, forwarding, storing, determining, identifying, accessing, writing, reading) in accordance with examples as described herein. The processor chipset may include one or more cores, one or more caches (e.g., memory local to or included in the processor chipset (e.g., the processor 1400) or other memory (e.g., random access memory (RAM), read-only memory (ROM), dynamic RAM (DRAM), synchronous dynamic RAM (SDRAM), static RAM (SRAM), ferroelectric RAM (FeRAM), magnetic RAM (MRAM), resistive RAM (RRAM), flash memory, phase change memory (PCM), and others).

[0238] The controller 1402 may be configured to manage and coordinate various operations (e.g., signaling, receiving, obtaining, retrieving, transmitting, outputting, forwarding, storing, determining, identifying, accessing, writing, reading) of the processor 1400 to cause the processor 1400 to support various operations in accordance with examples as described herein. For example, the controller 1402 may operate as a control unit of the processor 1400, generating control signals that manage the operation of various components of the processor 1400. These control signals include enabling or disabling functional units, selecting data paths, initiating memory access, and coordinating timing of operations.

[0239] The controller 1402 may be configured to fetch (e.g., obtain, retrieve, receive) instructions from the memory 1404 and determine subsequent instruction(s) to be executed to cause the processor 1400 to support various operations in accordance with examples as described herein. The controller 1402 may be configured to track memory address of instructions associated with the memory 1404. The controller 1402 may be configured to decode instructions to determine the operation to be performed and the operands involved. For example, the controller 1402 may be configured to interpret the instruction and determine control signals to be output to other components of the processor 1400 to cause the processor 1400 to support various operations in accordance with examples as described herein. Additionally, or alternatively, the controller 1402 may be configured to manage flow of data within the processor 1400. The controller 1402 may be configured to control transfer of data between registers, arithmetic logic units (ALUs), and other functional units of the processor 1400.

[0240] The memory 1404 may include one or more caches (e.g., memory local to or included in the processor 1400 or other memory, such RAM, ROM, DRAM, SDRAM, SRAM, MRAM, flash memory, etc. In some implementation, the memory 1404 may reside within or on a processor chipset (e.g., local to the processor 1400). In some other implementations, the memory 1404 may reside external to the processor chipset (e.g., remote to the processor 1400).

[0241] The memory 1404 may store computer-readable, computer-executable code including instructions that, when executed by the processor 1400, cause the processor 1400 to perform various functions described herein. The code may be stored in a non-transitory computer-readable medium such as system memory or another type of memory. The controller 1402 and/or the processor 1400 may be configured to execute computer-readable instructions stored in the memory 1404 to cause the processor 1400 to perform various functions. For example, the processor 1400 and/or the controller 1402 may be coupled with or to the memory 1404, the processor 1400, the controller 1402, and the memory 1404 may be configured to perform various functions described herein. In some examples, the processor 1400 may include multiple processors and the memory 1404 may include multiple memories. One or more of the multiple processors may be coupled with one or more of the multiple memories, which may, individually or collectively, be configured to perform various functions herein.

[0242] The one or more ALUs 1406 may be configured to support various operations in accordance with examples as described herein. In some implementation, the one or more ALUs 1406 may reside within or on a processor chipset (e.g., the processor 1400). In some other implementations, the one or more ALUs 1406 may reside external to the processor chipset (e.g., the processor 1400). One or more ALUs 1406 may perform one or more computations such as addition, subtraction, multiplication, and division on data. For example, one or more ALUs 1406 may receive input operands and an operation code, which determines an operation to be executed. One or more ALUs 1406 be configured with a variety of logical and arithmetic circuits, including adders, subtractors, shifters, and logic gates, to process and manipulate the data according to the operation. Additionally, or alternatively, the one or more ALUs 1406 may support logical operations such as AND, OR, exclusive-OR (XOR), not-OR (NOR), and not-AND (NAND), enabling the one or more ALUs 1406 to handle conditional operations, comparisons, and bitwise operations.

[0243] The processor 1400 may support wireless communication in accordance with examples as disclosed herein. The processor 1400 may be configured to operable to support a means for performing the following: determining synchronization delay status of data in a synchronization transmission set; and prioritizing transmission of the data based on the synchronization delay status of the data.

[0244] Alternatively, in some implementations, the processor 1400 may be configured to operable to support a means for performing the following: determining delay status of data based on at least one of multiple thresholds; and prioritizing transmission of the data based on one of the multiple thresholds.

[0245] Alternatively, in some implementations, the processor 1400 may be configured to operable to support a means for performing the following: determining synchronization delay status of data in a synchronization transmission set; and maximizing transmission of the data based on determining that an uplink grant is enough to accommodate the data.

[0246] Fig. 15 illustrates a flowchart of a method 1500 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure. The operations of the method 1500 may be implemented by a device or its components as described herein. For example, the operations of the method 1500

may be performed by the UE 104 as described herein. In some implementations, the device may execute a set of instructions to control the function elements of the device to perform the described functions. Additionally, or alternatively, the device may perform aspects of the described functions using special-purpose hardware.

[0247] At 1510, the method may include determining synchronization delay status of data in a synchronization transmission set. The operations of 1510 may be performed in accordance with examples as described herein. In some implementations, aspects of the operations of 1510 may be performed by a device as described with reference to Fig. 1.

[0248] At 1520, the method may include prioritizing transmission of the data based on the synchronization delay status of the data. The operations of 1520 may be performed in accordance with examples as described herein. In some implementations, aspects of the operations of 1520 may be performed by a device as described with reference to Fig. 1.

[0249] Fig. 16 illustrates a flowchart of a method 1600 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the present disclosure. The operations of the method 1600 may be implemented by a device or its components as described herein. For example, the operations of the method 1600 may be performed by the UE 104 as described herein. In some implementations, the device may execute a set of instructions to control the function elements of the device to perform the described functions. Additionally, or alternatively, the device may perform aspects of the described functions using special-purpose hardware.

[0250] At 1610, the method may include determining delay status of data based on at least one of multiple thresholds. The operations of 1610 may be performed in accordance with examples as described herein. In some implementations, aspects of the operations of 1610 may be performed by a device as described with reference to Fig. 1.

[0251] At 1620, the method may include prioritizing transmission of the data based on one of the multiple thresholds. The operations of 1620 may be performed in accordance with examples as described herein. In some implementations, aspects of the operations of 1620 may be performed by a device as described with reference to Fig. 1.

[0252] Fig. 17 illustrates a flowchart of a method 1700 that supports logical channel prioritization based on synchronization delay status in accordance with aspects of the

present disclosure. The operations of the method 1700 may be implemented by a device or its components as described herein. For example, the operations of the method 1700 may be performed by the UE 104 as described herein. In some implementations, the device may execute a set of instructions to control the function elements of the device to perform the described functions. Additionally, or alternatively, the device may perform aspects of the described functions using special-purpose hardware.

[0253] At 1710, the method may include determining synchronization delay status of data in a synchronization transmission set. The operations of 1710 may be performed in accordance with examples as described herein. In some implementations, aspects of the operations of 1710 may be performed by a device as described with reference to Fig. 1.

[0254] At 1720, the method may include maximizing transmission of the data based on determining that an uplink grant is enough to accommodate the data. The operations of 1720 may be performed in accordance with examples as described herein. In some implementations, aspects of the operations of 1720 may be performed by a device as described with reference to Fig. 1.

[0255] It shall be noted that implementations of the present disclosure which have been described with reference to Figs. 1 to 12 are also applicable to the device 1300, the processor 1400 and the methods 1500, 1600 and 1700.

[0256] It should be noted that the methods described herein describes possible implementations, and that the operations and the steps may be rearranged or otherwise modified and that other implementations are possible. Further, aspects from two or more of the methods may be combined.

[0257] The various illustrative blocks and components described in connection with the disclosure herein may be implemented or performed with a general-purpose processor, a DSP, an ASIC, a CPU, an FPGA or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general-purpose processor may be a microprocessor, but in the alternative, the processor may be any processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices (e.g., a combination of a DSP and a microprocessor, multiple microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0258] The functions described herein may be implemented in hardware, software executed by a processor, firmware, or any combination thereof. If implemented in software executed by a processor, the functions may be stored on or transmitted over as one or more instructions or code on a computer-readable medium. Other examples and implementations are within the scope of the disclosure and appended claims. For example, due to the nature of software, functions described herein may be implemented using software executed by a processor, hardware, firmware, hardwiring, or combinations of any of these. Features implementing functions may also be physically located at various positions, including being distributed such that portions of functions are implemented at different physical locations.

[0259] Computer-readable media includes both non-transitory computer storage media and communication media including any medium that facilitates transfer of a computer program from one place to another. A non-transitory storage medium may be any available medium that may be accessed by a general-purpose or special-purpose computer. By way of example, non-transitory computer-readable media may include RAM, ROM, electrically erasable programmable ROM (EEPROM), flash memory, compact disk (CD) ROM or other optical disk storage, magnetic disk storage or other magnetic storage devices, or any other non-transitory medium that may be used to carry or store desired program code means in the form of instructions or data structures and that may be accessed by a general-purpose or special-purpose computer, or a general-purpose or special-purpose processor.

[0260] As used herein, including in the claims, an article "a" before an element is unrestricted and understood to refer to "at least one" of those elements or "one or more" of those elements. The terms "a," "at least one," "one or more," and "at least one of one or more" may be interchangeable. As used herein, including in the claims, "or" as used in a list of items (e.g., a list of items prefaced by a phrase such as "at least one of" or "one or more of" or "one or both of") indicates an inclusive list such that, for example, a list of at least one of A, B, or C means A or B or C or AB or AC or BC or ABC (i.e., A and B and C). Also, as used herein, the phrase "based on" shall not be construed as a reference to a closed set of conditions. For example, an example step that is described as "based on condition A" may be based on both a condition A and a condition B without departing from the scope of the present disclosure. In other words, as used herein, the phrase "based

on" shall be construed in the same manner as the phrase "based at least in part on. Further, as used herein, including in the claims, a "set" may include one or more elements.

[0261] The description herein is provided to enable a person having ordinary skill in the art to make or use the disclosure. Various modifications to the disclosure will be apparent to a person having ordinary skill in the art, and the generic principles defined herein may be applied to other variations without departing from the scope of the disclosure. Thus, the disclosure is not limited to the examples and designs described herein but is to be accorded the broadest scope consistent with the principles and novel features disclosed herein.

WHAT IS CLAIMED IS:

1. A user equipment (UE), comprising:

a processor; and

a transceiver coupled to the processor,

wherein the processor is configured to:

determine synchronization delay status of data in a synchronization transmission set; and

prioritize transmission of the data based on the synchronization delay status of the data.

2. The UE of claim 1, wherein the processor is configured prioritize transmission of the data based on the synchronization delay status of the data by:

prioritize transmission of a first type of data in the synchronization transmission set, wherein the synchronization delay status comprises first remaining synchronization delay of the first type of data, the first remaining synchronization delay of the first type of data is below a first threshold.

3. The UE of claim 1, wherein the processor is configured to prioritize the transmission of the data by:

prioritizing the transmission of the data based on the synchronization delay status of the data and a value which is maintained for a first logical channel (LCH) having the data.

4. The UE of claim 1, wherein the processor is configured to prioritize the transmission of the data by:

prioritizing the transmission of the data based on the synchronization delay status of the data regardless of a value which is maintained for a first logical channel (LCH) having the data.

5. The UE of claim 1, wherein the processor is configured to prioritize the transmission of the data by one of the following:

prioritizing transmission of data of a first LCH, wherein the first LCH has a first type of data, first remaining synchronization delay of the first type of data is below a first threshold;

prioritizing transmission of all the data in the synchronization transmission set; or

prioritizing transmission of the first type of data in the synchronization transmission set.

6. The UE of claim 2, wherein the processor is configured to prioritize the transmission of the first type of data by:

increasing at least a first priority level for the first type of data to a target priority level.

7. The UE of claim 6, wherein the processor is further configured to:

receive a configuration for the target priority level via the transceiver from a network entity;

determine the target priority level based on the configuration.

8. The UE of claim 7, wherein the configuration for the target priority level comprises one of the following:

an absolute target priority value,

a priority offset value, or

a factor.

9. The UE of claim 6, wherein the processor is configured to increase at least the first priority level for the first type of data to the target priority level by one of the following:

increasing a second priority level for a first logical channel (LCH) to the target priority level, wherein the first LCH has the first type of data;

increasing only the first priority level for the first type of data to the target priority level; or

increasing a third priority level for the synchronization transmission set to the target priority level, wherein the synchronization transmission set comprises the first type of data.

10. The UE of claim 1, wherein the processor is further configured to:

receive, via the transceiver from a network entity, a first indication indicating whether to prioritize transmission of the data based on the synchronization delay status of the data.

11. A user equipment (UE), comprising:

a processor; and

a transceiver coupled to the processor,

wherein the processor is configured to:

determine delay status of data based on at least one of multiple thresholds; and

prioritize transmission of the data based on one of the multiple thresholds.

12. The UE of claim 11, wherein the data comprises a first type of data, wherein first remaining synchronization delay of the first type of data is below a first threshold among the multiple thresholds.

13. The UE of claim 12, wherein the processor is configured to prioritize the transmission of the data by:

receiving, via the transceiver from a network entity, a second indication indicating to prioritize the transmission of the first type of data based on the first threshold; and

prioritizing, based on the second indication, the transmission of the first type of data based on the first threshold.

14. The UE of claim 12, wherein the data further comprises a third type of data, wherein third remaining time of the third type of data is below a second threshold among the multiple thresholds.

15. The UE of claim 14, wherein the processor is configured to prioritize the transmission of the data by:

increasing a first priority level for the first type of data to a first target priority level; and

increasing a second priority level for the third type of data to a second target priority level.

16. The UE of claim 14, wherein a first logical channel (LCH) has both the first type of data and the third type of data.

17. The UE of claim 16, wherein the processor is configured to prioritize the transmission of the data by:

prioritizing the transmission of one of the first type of data and the third type of data.

18. A user equipment (UE), comprising:

a processor; and

a transceiver coupled to the processor,

wherein the processor is configured to:

determine synchronization delay status of data in a synchronization transmission set; and

maximize transmission of the data based on determining that an uplink grant is enough to accommodate the data.

19. The UE of claim 18, wherein the processor is configured to maximize transmission of the data by one of the following:

maximizing transmission of data of a first logical channel (LCH), wherein the first LCH has a first type of data, first remaining synchronization delay of the first type of data is below a first threshold;

maximizing transmission of all the data in the synchronization transmission set; or

maximizing transmission of the first type of data in the synchronization transmission set.

20. A processor for wireless communication, comprising:

at least one memory; and

a controller coupled with the at least one memory and configured to cause the controller to:

determine synchronization delay status of data in a synchronization transmission set; and

prioritize transmission of the data based on the synchronization delay status of the data.

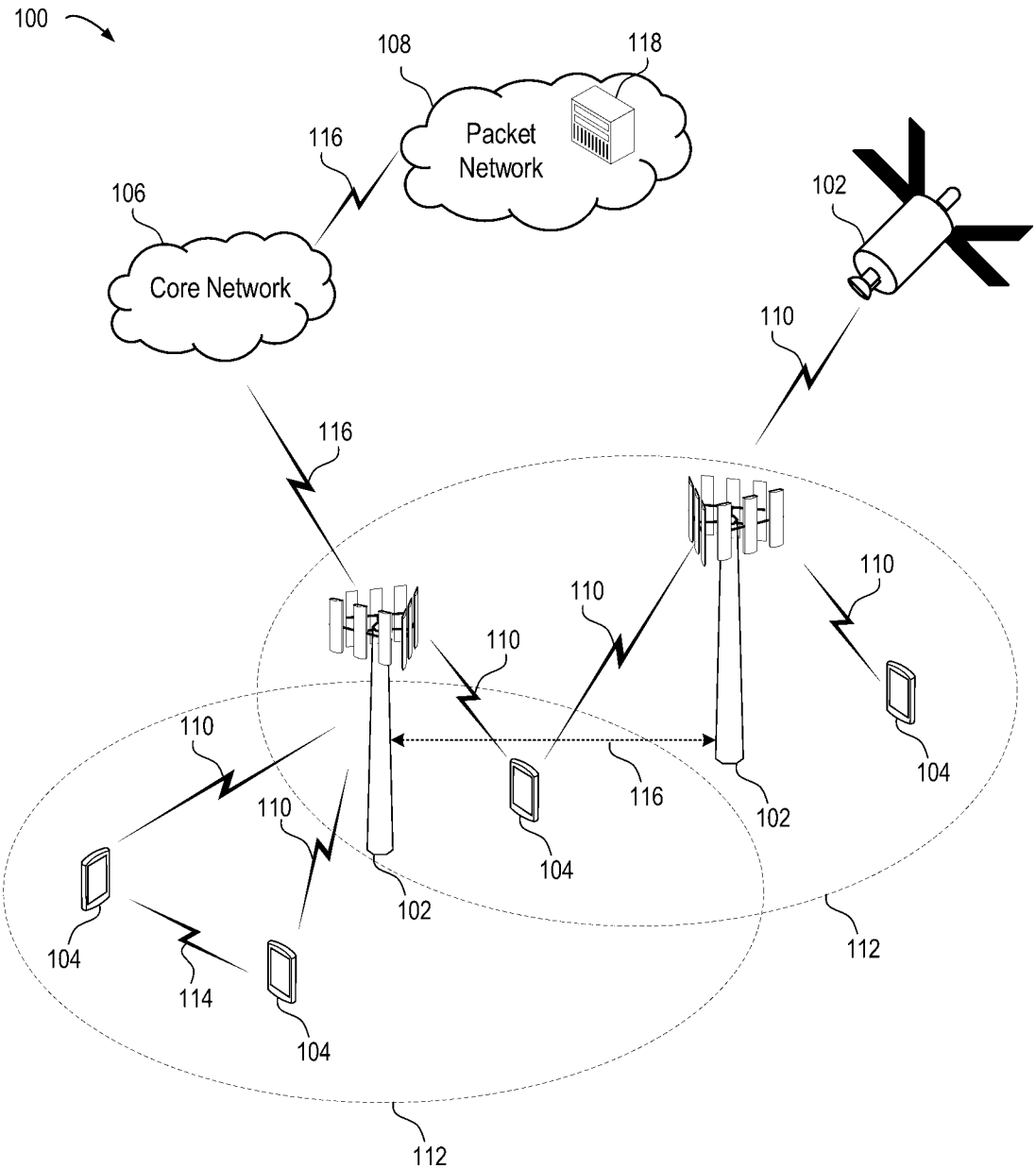
100
108
118
Packet Network
116
106
Core Network
102
110
116
110
110
110
110
110
104
116
102
104
110
102
104
114
104
112
112

Fig. 1

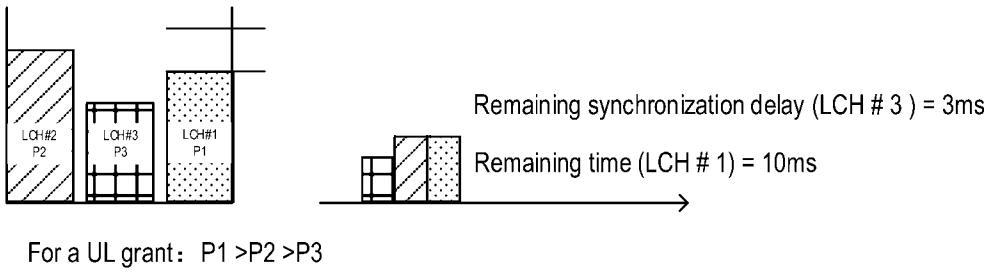
LCH#2
P2
LCH#3
P3
LCH#1
P1
Remaining synchronization delay (LCH # 3) = 3ms
Remaining time (LCH # 1) = 10ms
For a UL grant：P1 >P2 >P3

Fig. 2

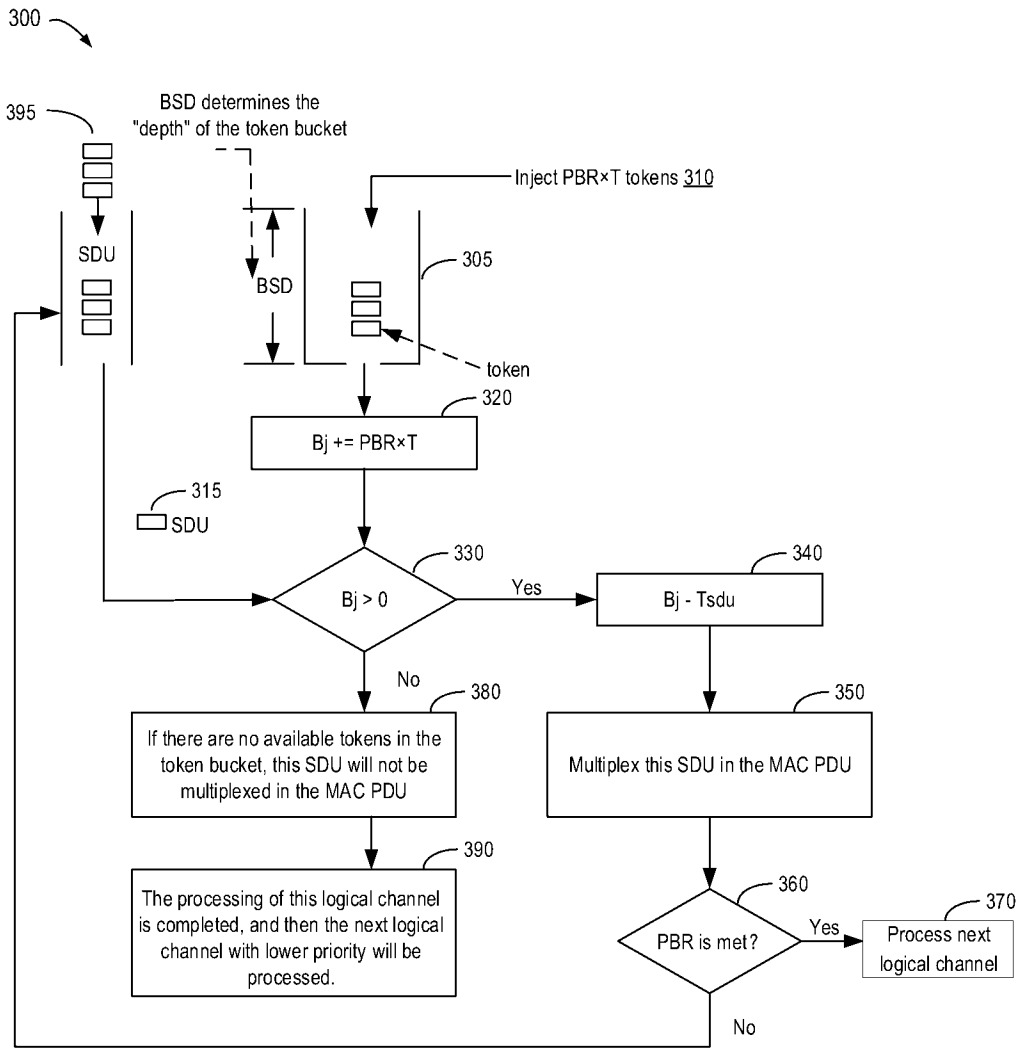
300
395
BSD determines the "depth" of the token bucket
Inject PBR×T tokens 310
SDU
BSD
305
token
320
Bj += PBR×T
315
SDU
330
Bj > 0
Yes
340
Bj - Tsdu
No
380
If there are no available tokens in the token bucket, this SDU will not be multiplexed in the MAC PDU
350
Multiplex this SDU in the MAC PDU
390
The processing of this logical channel is completed, and then the next logical channel with lower priority will be processed.
360
PBR is met?
Yes
370
Process next logical channel
No

Fig. 3

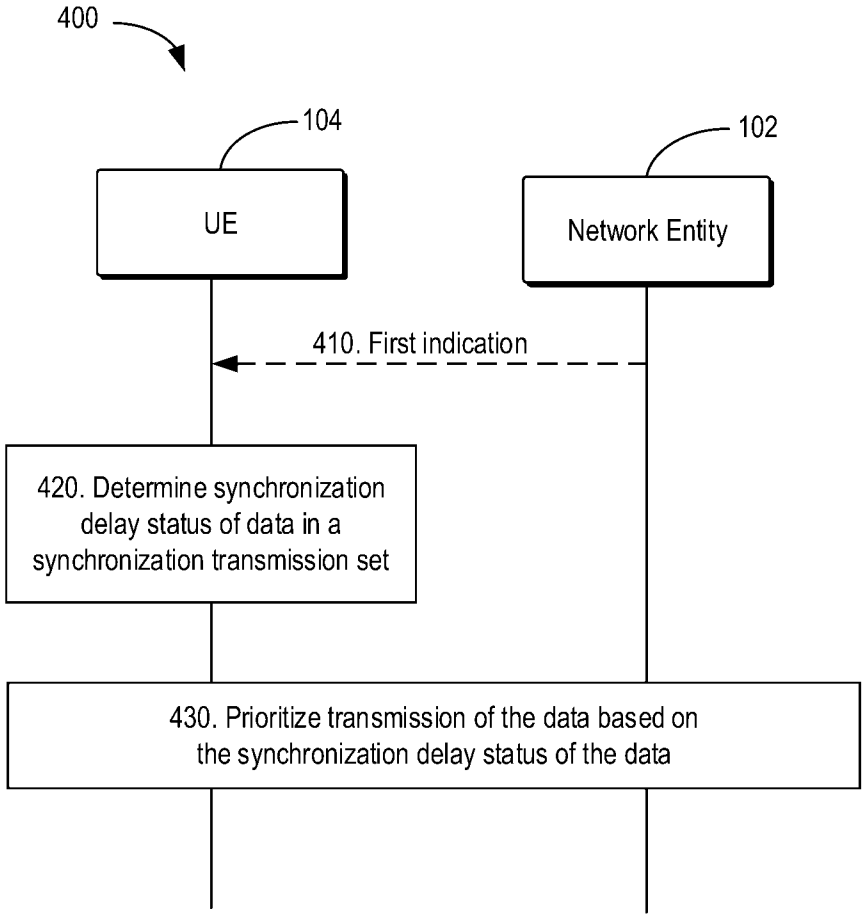
400
104
UE
102
Network Entity
410. First indication
420. Determine synchronization delay status of data in a synchronization transmission set
430. Prioritize transmission of the data based on the synchronization delay status of the data

Fig. 4

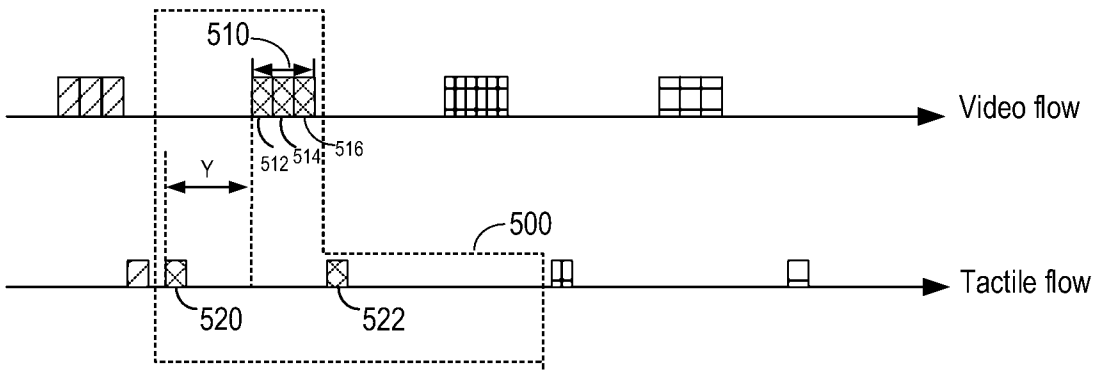
510
Video flow
512
514
516
Y
500
Tactile flow
520
522

Fig. 5

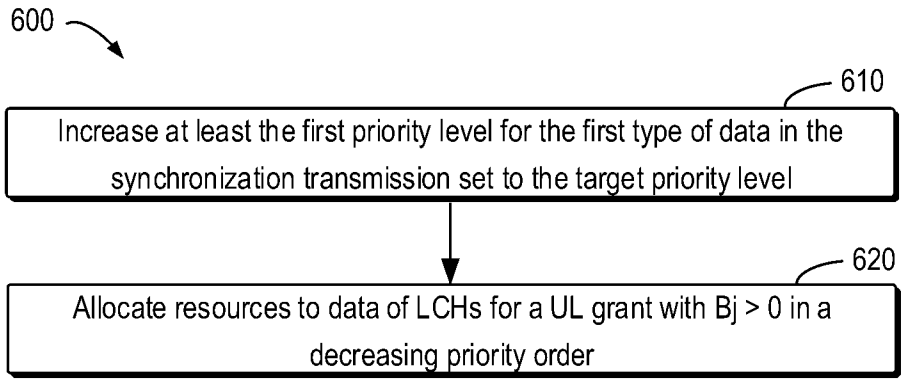
600
610
Increase at least the first priority level for the first type of data in the synchronization transmission set to the target priority level
620
Allocate resources to data of LCHs for a UL grant with Bj > 0 in a decreasing priority order

Fig. 6

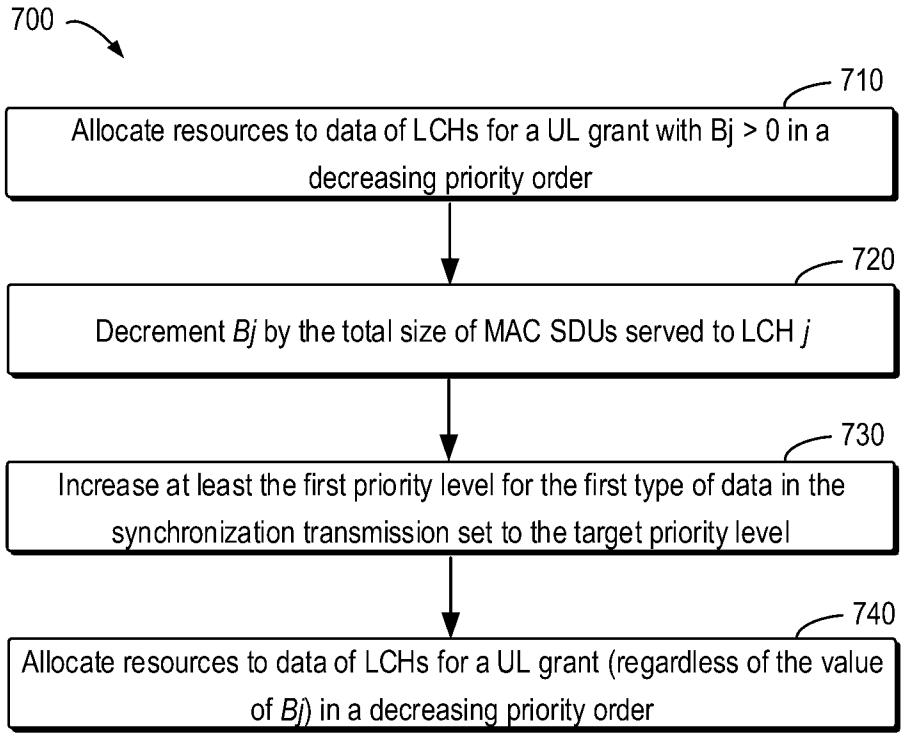
700
710
Allocate resources to data of LCHs for a UL grant with Bj > 0 in a decreasing priority order
720
Decrement Bj by the total size of MAC SDUs served to LCH j
730
Increase at least the first priority level for the first type of data in the synchronization transmission set to the target priority level
740
Allocate resources to data of LCHs for a UL grant (regardless of the value of Bj) in a decreasing priority order

Fig. 7

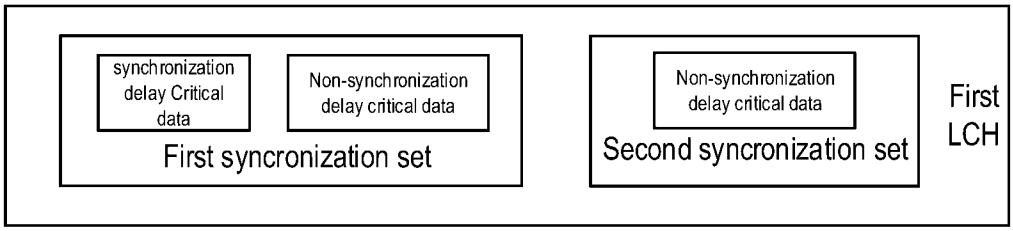
synchronization delay Critical data
Non-synchronization delay critical data
First syncronization set
Non-synchronization delay critical data
Second syncronization set
First LCH

Fig. 8

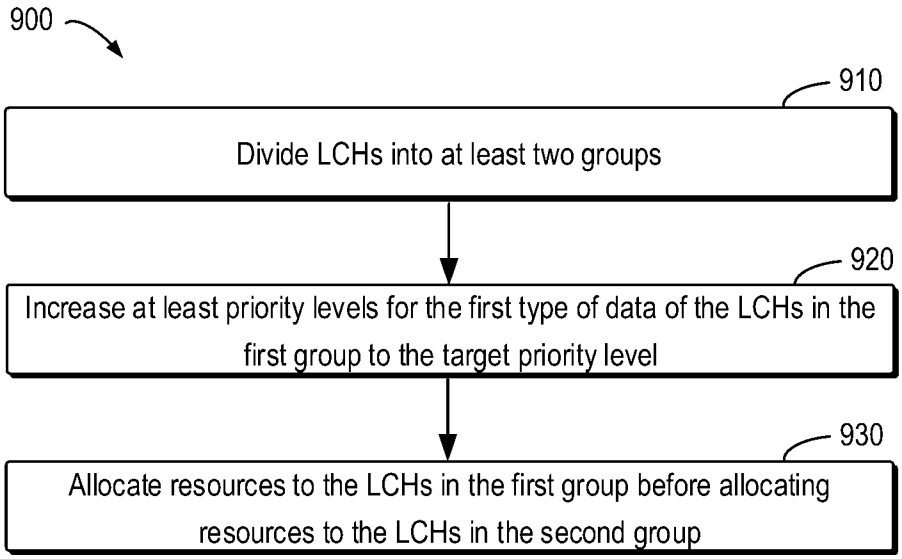
900
910
Divide LCHs into at least two groups
920
Increase at least priority levels for the first type of data of the LCHs in the first group to the target priority level
930
Allocate resources to the LCHs in the first group before allocating resources to the LCHs in the second group

Fig. 9

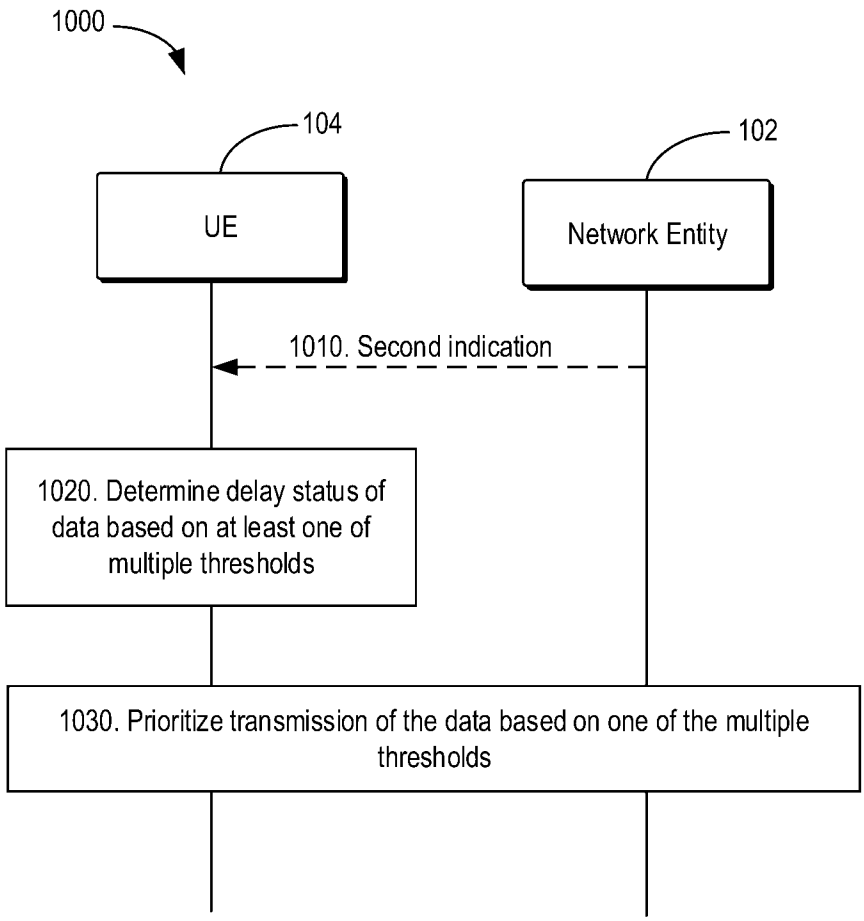
1000
104
102
UE
Network Entity
1010. Second indication
1020. Determine delay status of data based on at least one of multiple thresholds
1030. Prioritize transmission of the data based on one of the multiple thresholds

Fig. 10

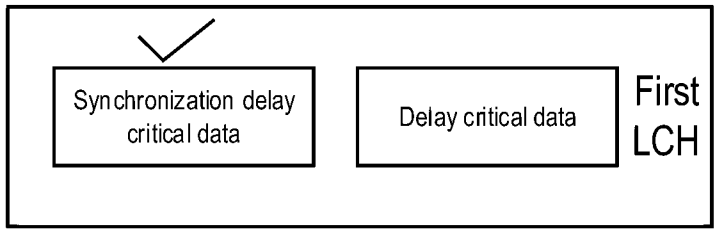

Fig. 11A

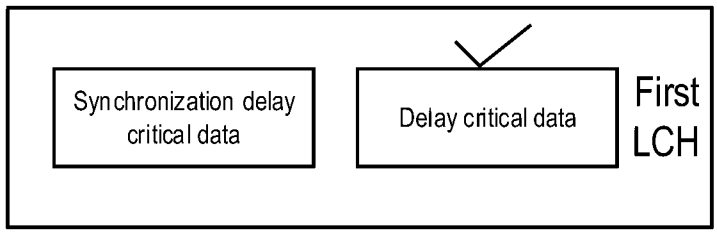

Fig. 11B

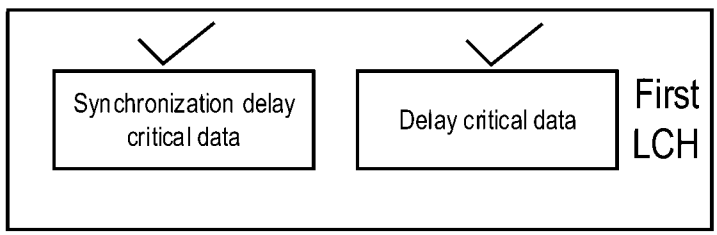

Fig. 11C

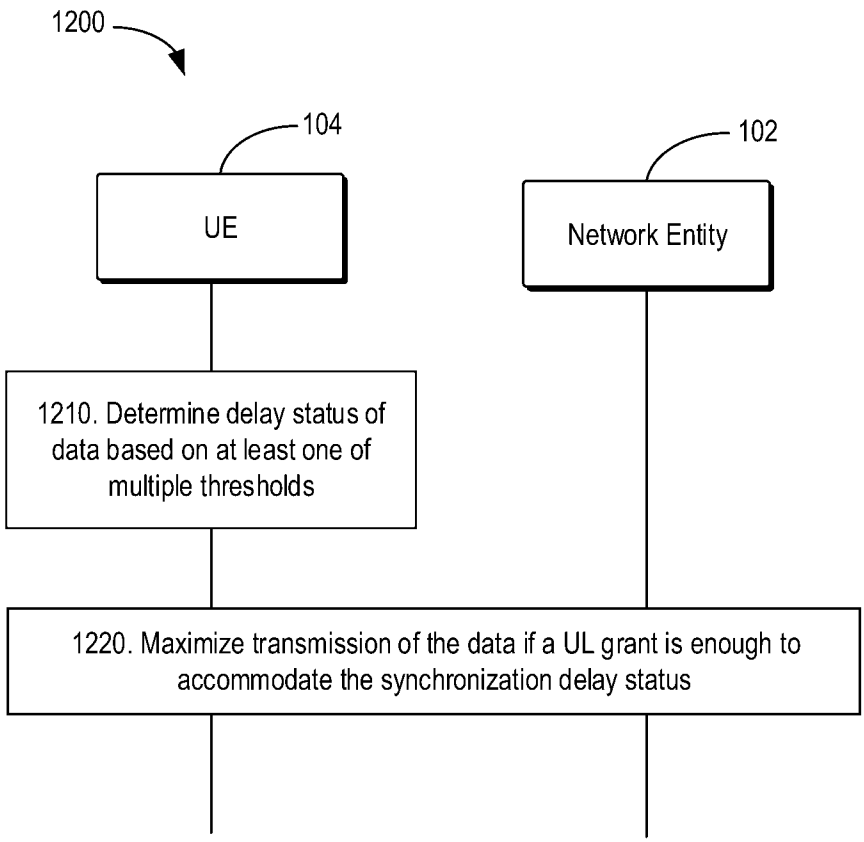
1200
104
102
UE
Network Entity
1210. Determine delay status of data based on at least one of multiple thresholds
1220. Maximize transmission of the data if a UL grant is enough to accommodate the synchronization delay status

Fig. 12

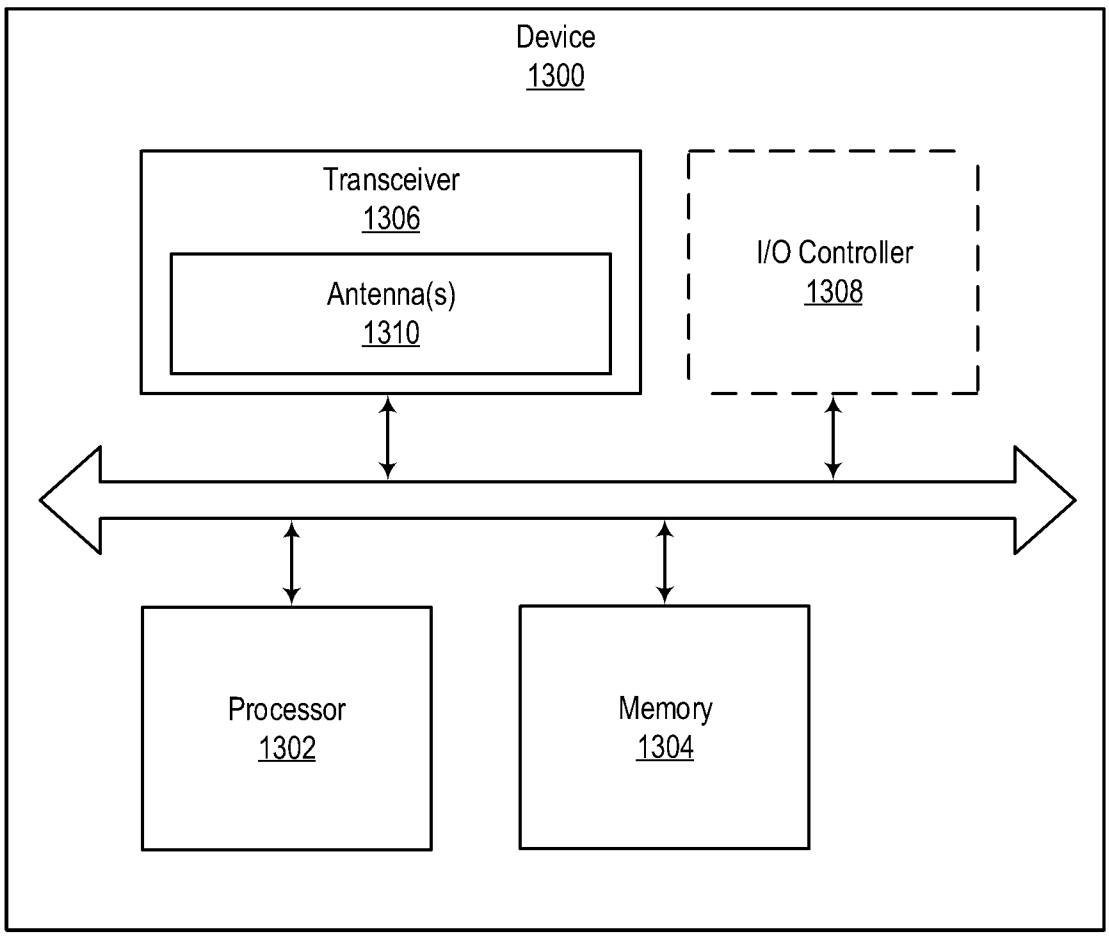
Device
1300
Transceiver
1306
Antenna(s)
1310
I/O Controller
1308
Processor
1302
Memory
1304

Fig. 13

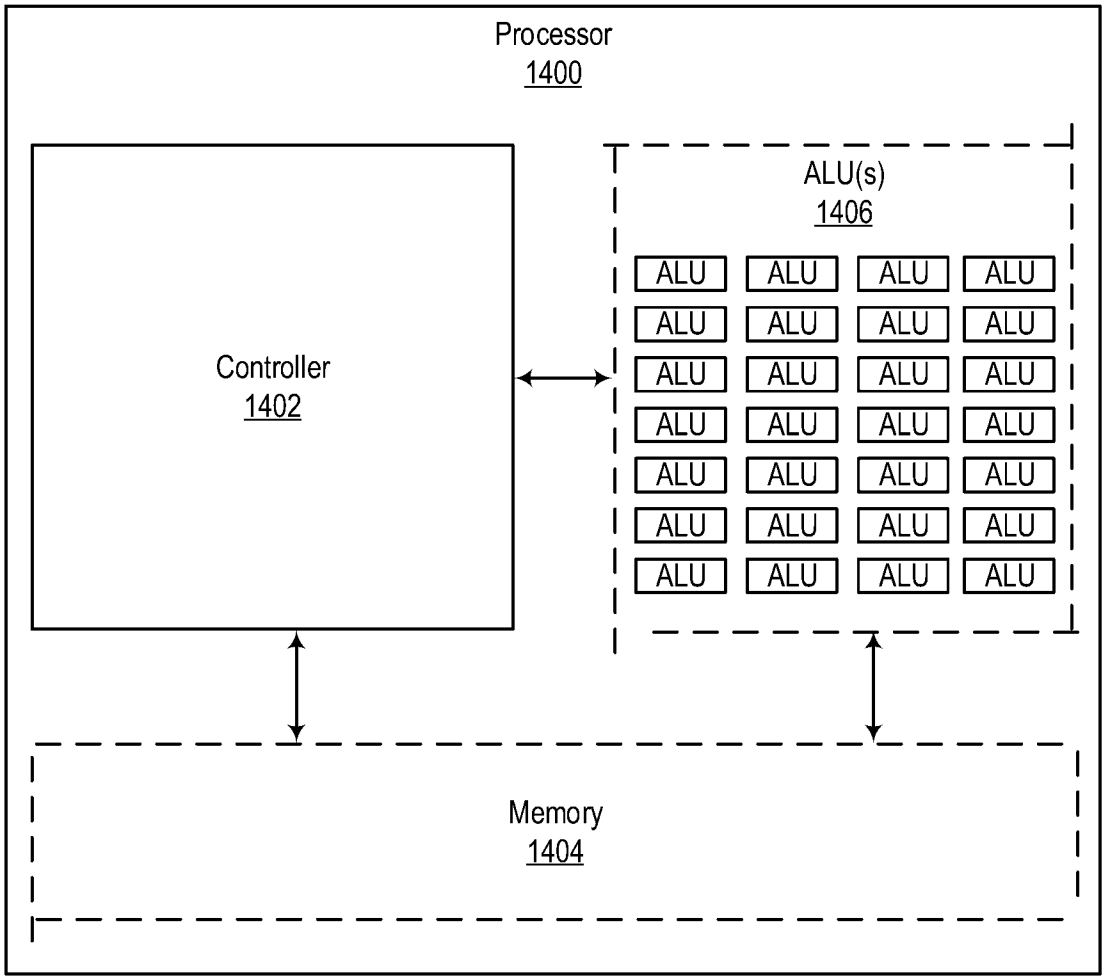

Fig. 14

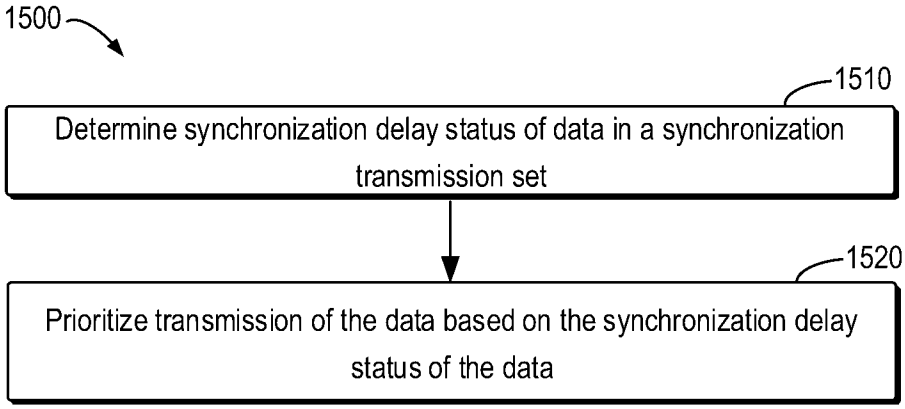

Fig. 15

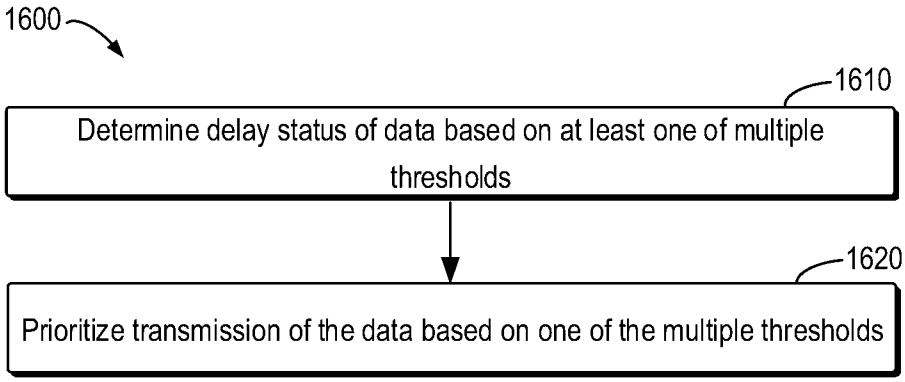

Fig. 16

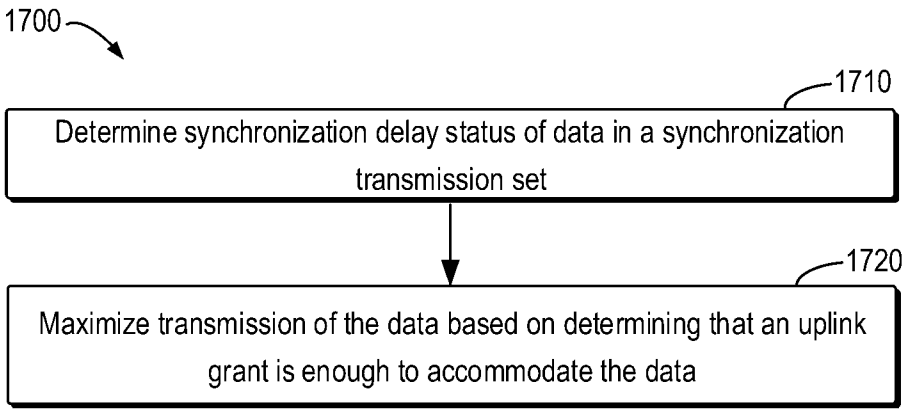

Fig. 17

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2024/075563

A. CLASSIFICATION OF SUBJECT MATTER

H04W56/00(2009.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC:H04W

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

3GPP,CNTXT,DWPI,ENTXT,ENTXTC,OETXT,VEN,WPABS: logical channel prioritization, logical channel, ordering, synchronization, delay, prioritization, LCH, LCP, delay status, threshold, maximize

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2024023155 A1 (QUALCOMM INCORPORATED) 18 January 2024 (2024-01-18) description, paragraphs [0047]-[0086], figures 1-7	1-20
A	WO 2023209542 A1 (LENOVO (SINGAPORE) PTE LIMITED) 02 November 2023 (2023-11-02) the whole document	1-20
A	WO 2023154333 A1 (INTERDIGITAL PATENT HOLDINGS, INC.) 17 August 2023 (2023-08-17) the whole document	1-20
A	US 2023122493 A1 (FG INNOVATION COMPANY LIMITED) 20 April 2023 (2023-04-20) the whole document	1-20
A	VIVO. "Left issues for UL/SL prioritization" *3GPP TSG-RAN WG2 Meeting #108 R2-1914923,* 22 November 2019 (2019-11-22), the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☑ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 October 2024	**24 October 2024**

Name and mailing address of the ISA/CN	Authorized officer
CHINA NATIONAL INTELLECTUAL PROPERTY ADMINISTRATION **6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China**	**FU,YuanYuan** Telephone No. **(+86) 010-53961775**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2024/075563

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
US 2024023155 A1	18 January 2024	WO 2024015182 A1	18 January 2024
WO 2023209542 A1	02 November 2023	None	
WO 2023154333 A1	17 August 2023	None	
US 2023122493 A1	20 April 2023	None	