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(54) **BUS-HANDLING**

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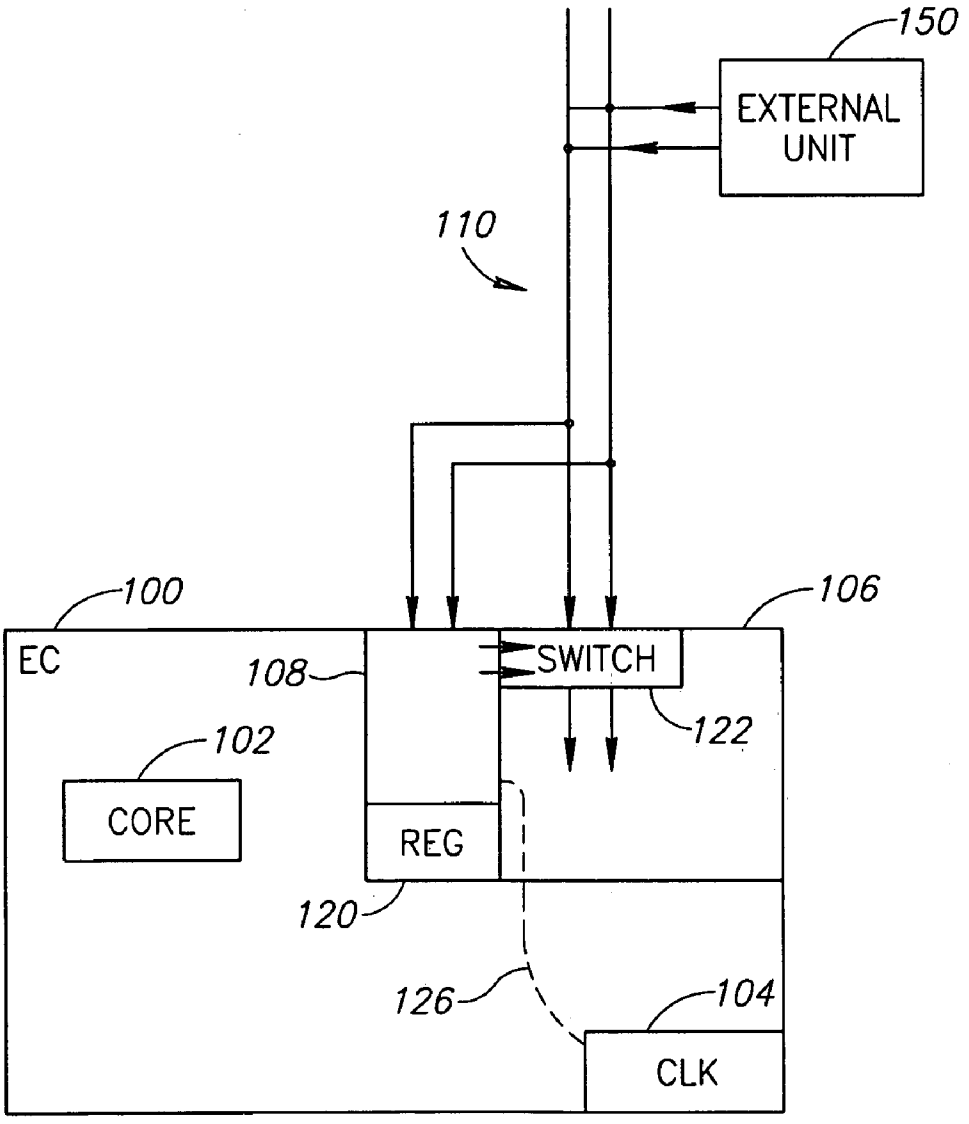
(57) **ABSTRACT**

A processor, comprising a processing unit having an active state and a sleep state in which at least one of its sub-sections is inactive and a communication port adapted to receive signals from external units over a bus, which is configured to be not fully operative when the processor is in the sleep state. The processor additionally includes a bus monitoring unit configured to stall the bus responsive to identifying transmissions on the bus directed to the communication port, while the processing unit is in the sleep state and to indicate to the communication port that a transmission started while it was in the sleep state.



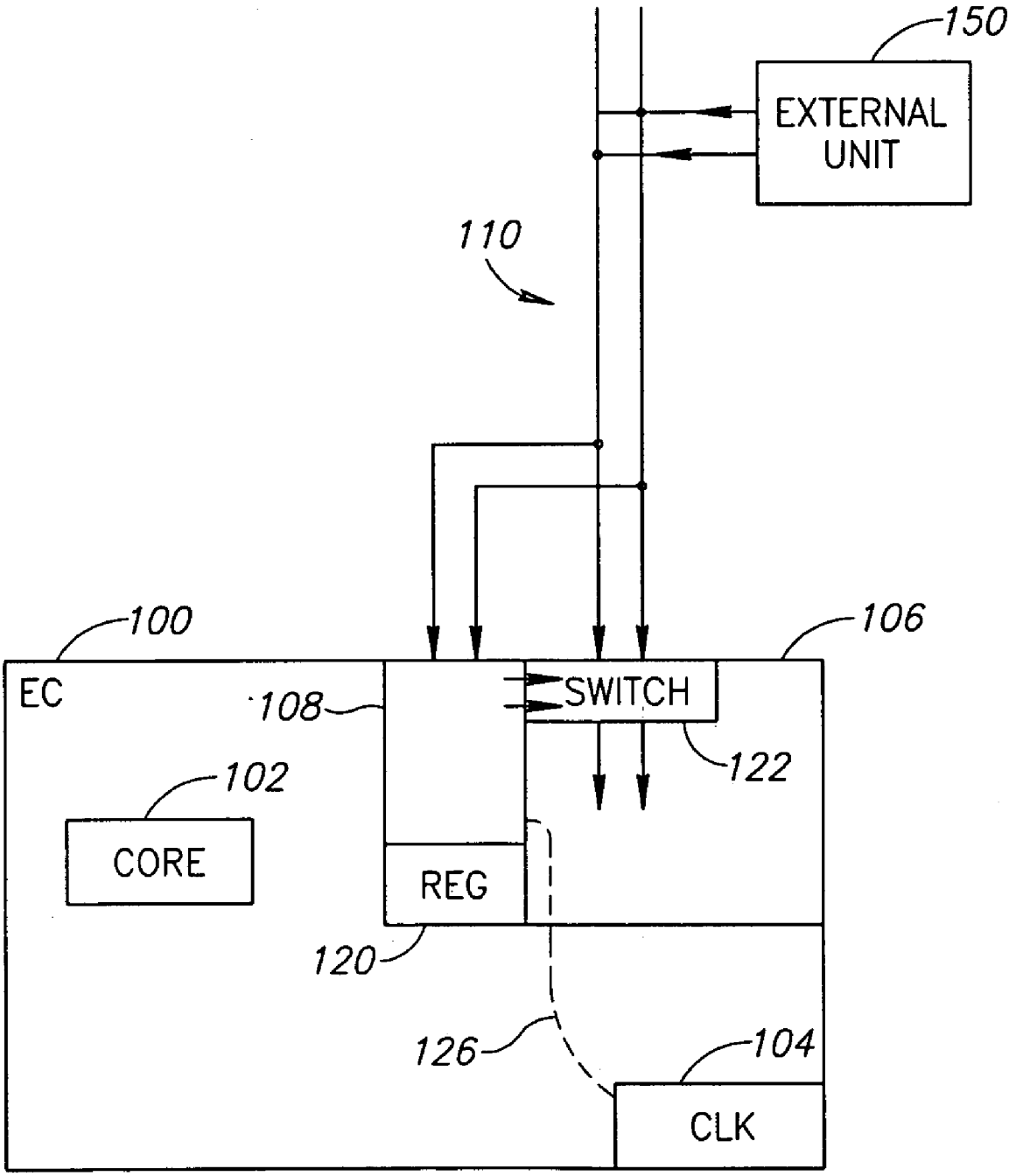

150
EXTERNAL UNIT
110
100
EC
106
108
SWITCH
122
102
CORE
REG
120
126
104
CLK

FIG.1

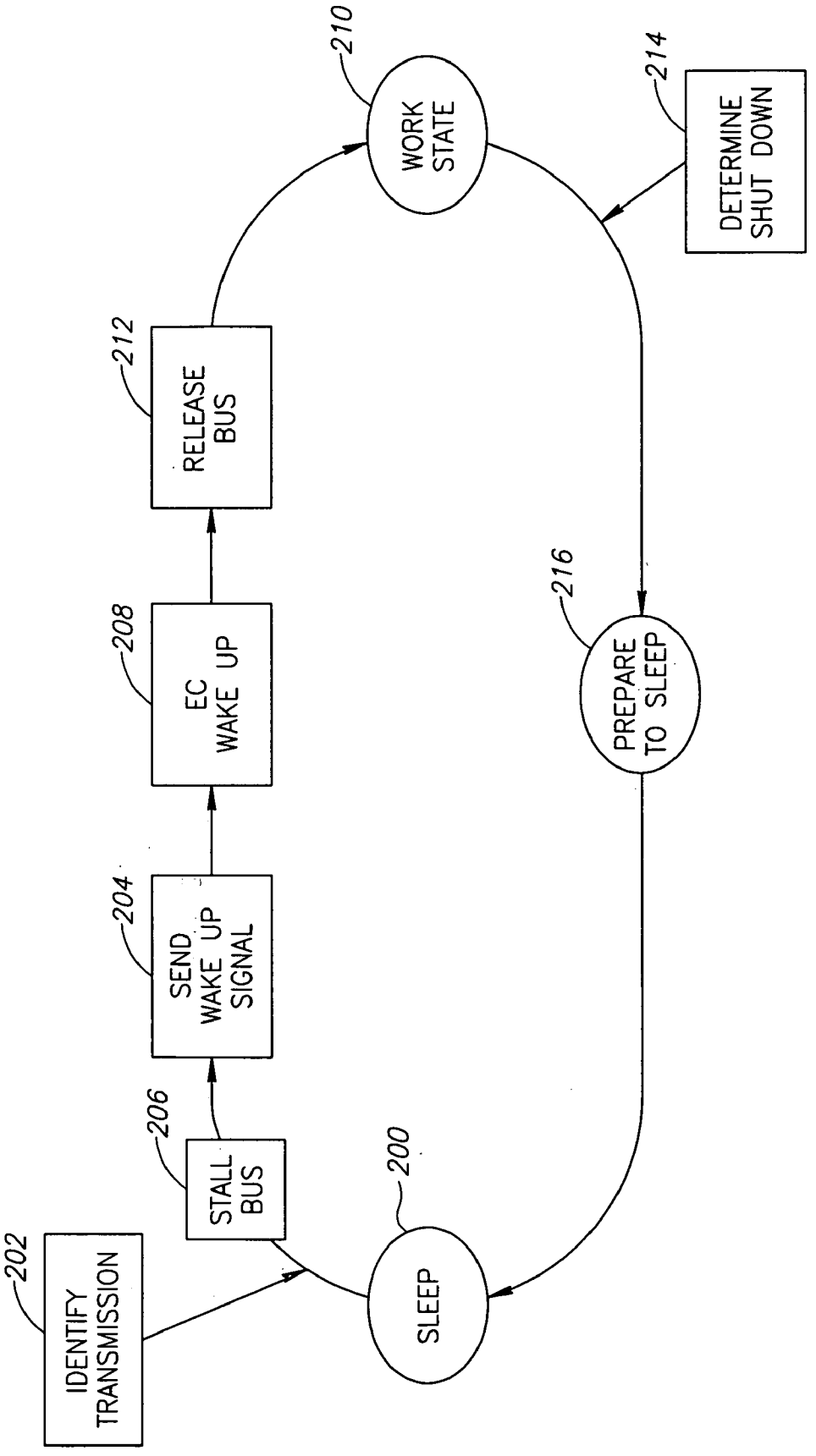

210
WORK STATE
214
DETERMINE SHUT DOWN
212
RELEASE BUS
208
EC WAKE UP
216
PREPARE TO SLEEP
204
SEND WAKE UP SIGNAL
206
STALL BUS
200
SLEEP
202
IDENTIFY TRANSMISSION

FIG.2

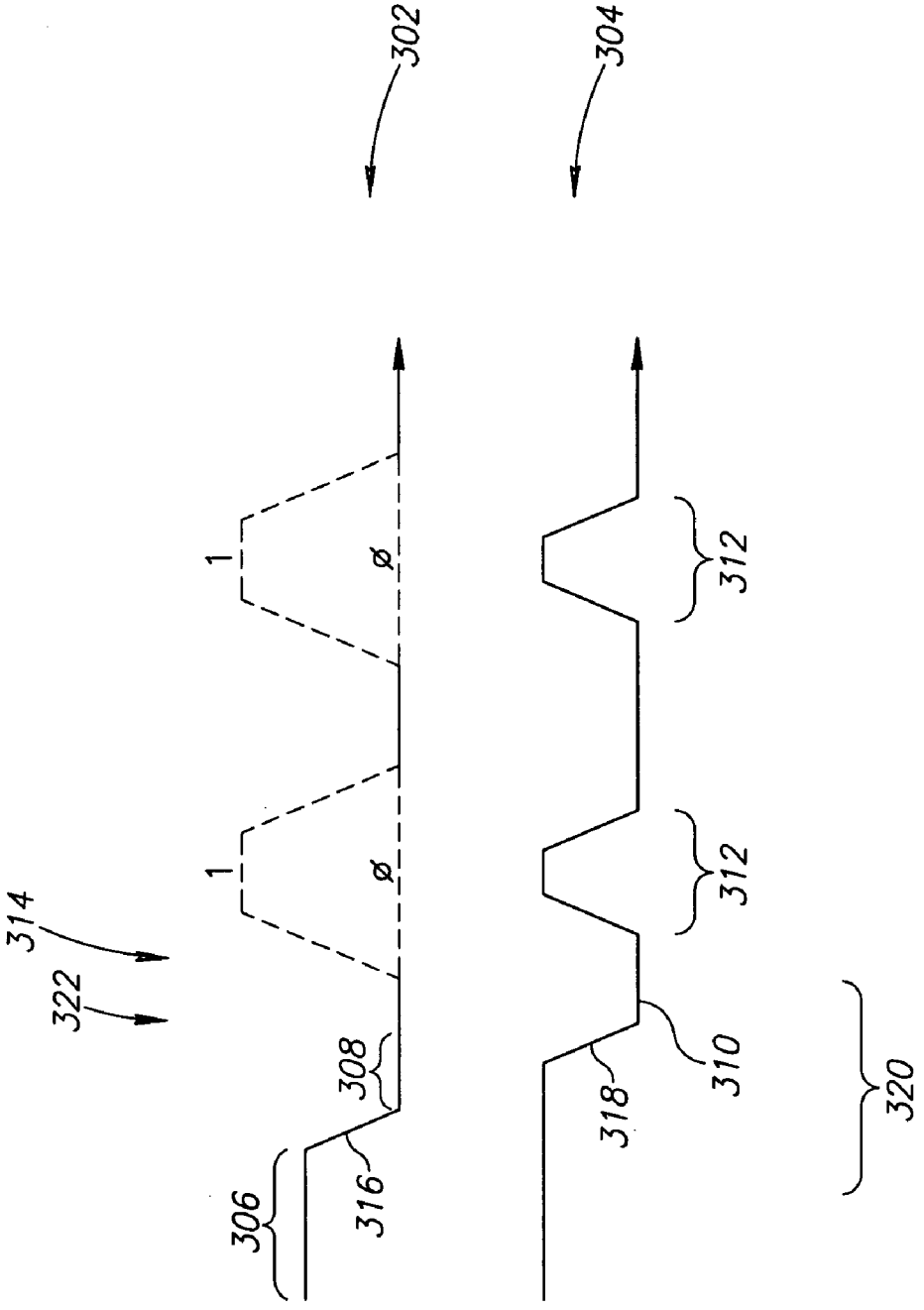


FIG.3

BUS-HANDLING

FIELD OF THE INVENTION

[0001] The present invention relates generally to communications and specifically to wake-up procedures of communication devices.

BACKGROUND

[0002] Many computerized systems, such as portable computers, are battery operated and measures are taken to reduce their power consumption. One method used to reduce power consumption is shutting down units which are not currently in use. The unit which is shut down generally disables its clock and waits for a signal instructing it to wake up, i.e., to enter an active mode.

[0003] US patent publication 2008/0178026 to Chen, titled: "Computer System and Power Saving Method Thereof", the disclosure of which is incorporated herein by reference, describes a system in which when a chipset and a processor are in a power saving mode a bus connecting the chipset and processor is disabled. When the chipset needs to send data to the processor it enables the bus, transmits the data and then moves back to the sleep state.

[0004] EP patent 1 594 253 to Bogavac Davor, titled: "Method and Device to Wake-up Nodes in a Serial Databus", the disclosure of which is incorporated herein by reference, describes another system with nodes that wake up responsive to transmissions from a master unit, each unit waking up only for specific transmissions directed to it.

[0005] The waking up process may take time, referred to as a "wake up latency". In some cases, the source of transmitted data is not aware that the receiving unit is asleep and the sleeping unit is configured to wake up immediately when it identifies that signals are being transmitted on the bus. If the wake up latency is not sufficiently short, however, the sleeping unit will wake up only after at least part of the data from the source was transmitted and the transmission will be lost. While some sources may be configured to receive retransmission requests, other sources may not be so adapted and the data they transmit is permanently lost if the receiving unit does not awake fast enough.

[0006] U.S. Pat. No. 7,363,523 to Kurts et al., titled: "Method and Apparatus for Controlling Power Management State Transitions", the disclosure of which is incorporated herein by reference, suggests having a plurality of low power states for a processor, involving different extents of processor units shut down. When a bus signal is received, the processor does not move to a full scale operation state, but rather moves to an intermediate operation state which is sufficient to handle the bus access. The transition to the intermediate state is performed within 35 microseconds.

[0007] U.S. Pat. No. 7,039,819 to Kommrusch et al., titled: "Apparatus and Method for Initiating a Sleep State in a System on a Chip Device", the disclosure of which is incorporated herein by reference, suggests a state having a wake latency of about 1 microsecond.

[0008] Some processors, however, may not be able to wake up with a short enough latency, to catch the beginning of data transmitted on the bus.

[0009] US patent publication 2007/0239920 to Frid, titled: "Method and System for Communication Between a Secondary Processor and an Auxiliary Display Subsystem of a Notebook", the disclosure of which is incorporated herein by reference, suggests including a low power auxiliary display in a portable computer, which can be used instead of waking up the main processor and display of the computer. This solution, however, still requires substantial power amounts for the auxiliary display, and it would be desired to have a sleep state also for the auxiliary display in order to further reduce power consumption.

[0010] U.S. Pat. No. 6,892,332 to Gulick, titled: "Hardware Interlock Mechanism Using a Watchdog Timer", the disclosure of which is incorporated herein by reference, describes a system in which wake-ups are performed periodically and not responsive to external signals. Such a system is susceptible both to unnecessary wake ups and to delayed responses to external requests.

SUMMARY OF THE INVENTION

[0011] An aspect of some embodiments of the present invention relates to a bus monitoring unit, which is adapted to identify transmissions on the bus and to stall the bus responsive thereto in order to prevent transmissions thereon, until a device serviced by the bus monitoring unit is prepared to receive the transmissions.

[0012] In some embodiments of the invention, in addition to stalling the bus, the bus monitoring unit initiates a wake up of the serviced device, responsive to identifying the transmission on the bus.

[0013] When the serviced device is awake, the bus is released from the stalling. In some embodiments of the invention, before releasing the bus, the bus monitoring unit notifies the serviced device that it was stalled during a transmission, so that the serviced device adjusts itself to continue receiving the transmission that was stopped in the middle when the bus was stalled.

[0014] Alternatively or additionally, the bus monitoring device provides the serviced device with signals which imitate the beginning of a transmission which was missed while the serviced device was in the sleep mode, before the bus was stalled.

[0015] There is therefore provided in accordance with an exemplary embodiment of the invention, a processor, comprising a processing unit having an active state and a sleep state in which at least one of its sub-sections is inactive, a communication port adapted to receive signals from external units over a bus, which is configured not to be fully operative in the sleep state and a bus monitoring unit configured to stall the bus responsive to identifying transmissions on the bus directed to the communication port, while the processing unit is in the sleep state and to indicate to the communication port that a transmission started while it was in the sleep state.

[0016] Optionally, the bus monitoring unit is configured to provide a wakeup signal to the processing unit, responsive to identifying a transmission on the bus that is directed to the communication port. Optionally, the bus monitoring unit is configured to provide the wakeup signal and to stall the bus, substantially concurrently. Alternatively, the bus monitoring unit is configured to provide the wakeup signal before stalling the bus. Optionally, the bus monitoring unit comprises an asynchronous unit which identifies transmissions on the bus without use of a time signal. Optionally, the bus monitoring unit comprises a synchronous unit which identifies transmissions on the bus using a time signal. Optionally, the bus monitoring unit is configured to provide the communication port with an imitation of a beginning portion of a transmission from an external unit, before releasing the bus.

[0017] There is further provided in accordance with an exemplary embodiment of the invention, a method of handling transmissions, comprising identifying a transmission received over a bus, while a port intended to receive the transmission is in a sleep state, moving the port into an operative state and stalling the bus responsive to receiving the transmission, until the port is in the operative state. Optionally, the method includes notifying the port, when it is in the operative state, that a transmission began whilst said port was in the sleep state and/or locally providing an imitation of a beginning of the identified transmission to the port, after it moves into the operative state, before terminating the stalling of the bus.

BRIEF DESCRIPTION OF THE FIGURES

[0018] With specific reference now to the drawings in detail, it is stressed that the particulars shown are by way of example and for purposes of illustrative discussion of the preferred embodiments of the present invention only, and are presented in the cause of providing what is believed to be the most useful and readily understood description of the principles and conceptual aspects of the invention. In this regard, no attempt is made to show structural details of the invention in more detail than is necessary for a fundamental understanding of the invention; the description taken with the drawings making apparent to those skilled in the art how the several forms of the invention may be embodied in practice. In the accompanying drawings:

[0019] FIG. **1** is a schematic illustration of an embedded controller connected to an external unit via a bus, in accordance with an embodiment of the invention;

[0020] FIG. **2** is a state diagram of an embedded controller, in accordance with an exemplary embodiment of the invention; and

[0021] FIG. **3** is a schematic illustration of signals transmitted on a bus, in accordance with an exemplary embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Overview

[0022] FIG. **1** is a schematic illustration of an embedded controller (EC) **100** connected over a bus **110** to an external unit **150**, in accordance with an embodiment of the invention. Embedded controller **100** may be employed, for example, in a notebook computer, to perform control tasks of one or more peripherals, such as a keyboard, a mouse, a screen, a power supply and/or a battery (not shown). Embedded controller **100** includes a processing unit core **102** which manages its operation, and a clock signal generator **104**, which provides a timing signal to the various sub-sections (not all of which are shown) of embedded controller **100**. Controller **100** further includes an SM Bus port **106**, which communicates with one or more external units **150**, via bus **110**.

[0023] In order to reduce power consumption, embedded controller **100** is configured to have a sleep state in which clock signal generator **104** is shut down. A start signal identifier **108** is configured to monitor the signals transmitted on bus **110** while EC **100** is in the sleep state. When in full operation, port **106** optionally handles detection of transmissions on its own and signal identifier **108** is not in use. When a transmission on bus **110** is identified, signal identifier **108** optionally sends a wake up signal **126** to clock **104** and in parallel stalls the transmission on bus **110**, until port **106** is ready to receive the transmission, as is now described in detail.

[0024] FIG. **2** is a state diagram of EC **100**, in accordance with an exemplary embodiment of the invention. When not active, EC **100** enters a sleep state **200** in which it consumes very little or; no power. When a transmission on bus **110** is identified **202**, signal identifier **108** stalls **206** bus **110** and optionally, in parallel or immediately thereafter, sends **204** a wake up signal to clock generator **104**. Responsive to the wake up signal, EC **100** undergoes a wake up procedure **208**. At the end of the wakeup procedure, signal identifier **108** releases **212** the bus and allows EC **100** to handle the incoming transmission and EC **100** enters a work state **210**. When EC **100** is in work state **210** but it is determined **214** that it can be moved to the sleep state in order to reduce power consumption, EC **100** undergoes a prepare-to-sleep procedure **216** and moves into sleep state **200**.

Identification

[0025] Referring in detail to identifying (**202**) a transmission on bus **110**, in some embodiments of the invention, bus **110** is governed by a protocol which requires transmission of a predetermined start signal before transmitting data, and the identifying (**202**) involves identifying at least a portion of the start signal. In some embodiments of the invention, the identification is performed based on the signals on fewer than all the lines of the bus, for example on only a single line, such as only on the data line or only on the clock line of the bus. The extent of the portion to be identified is optionally selected during a design stage, based on a tradeoff between the competing requirements of more accurate identification and of minimizing the resources required for the identification.

[0026] Optionally, signal identifier **108** is an asynchronous unit which does not require a clock signal for its operation, so as to minimize its power consumption. Alternatively, signal identifier **108** is a synchronous unit which operates with a low rate clock signal, such that identification of signals can be based on durations of signal patterns, and consequently is generally more accurate. It will be appreciated that using a synchronous unit for the detection is particularly useful when the bus is expected to be relatively noisy, as it provides a more reliable detection in the presence of noise. Optionally, the low rate clock signal is nonetheless higher than twice the rate of transmission on bus **110**, such that at least two low rate clock cycles are included in each slot **312**, so that signals on the bus can be identified accurately. Alternatively, the low rate clock signal is at a rate lower than twice the bus rate, to reduce further the power consumption, although the determination of the signals on the bus may not be complete.

[0027] FIG. **3** is a schematic illustration of signals transmitted on bus **110**, in accordance with an exemplary embodiment of the invention. In the embodiment of FIG. **3**, bus **110** includes two lines, a data line which carries a data signal **302** and a clock line which carries a clock signal **304**. When the bus is not in use, both bus lines remain at a high voltage level, as illustrated by time segment **306**. At the beginning of each transmission, a start signal **320** is transmitted to indicate the beginning of a new transmission. In generating the start signal **320**, the transmitter first changes the data signal **302** to a low voltage for a period **308** of a predetermined length. Thereafter, clock signal **304** is changed to a low voltage for a predetermined period **310**. Once the transmission of start signal **320** is completed, bits are transmitted in a sequence of slots

312. In each slot 312, clock signal 304 is raised for a predetermined duration and then lowered, to indicate the timing of the slot. Data signal 302 in each slot either has a low voltage, representative of a '0' bit, or a high voltage, representative of a '1' bit.

[0028] With regard to the example of FIG. 3, signal identifier 108 optionally considers a transmission to be identified if a transition of data signal 302 to a low voltage is identified while clock signal 304 is high (e.g., transition 316), followed by transition of clock signal 304 to a low voltage while data signal 302 has a low value (e.g., transit 318). Alternatively, signal identifier 108 considers a transmission to be identified if clock signal 304 moves to a low value while data signal 302 has a low value. In another embodiment, signal identifier 108 considers a transmission to be identified if either clock signal 304 or data signal 302 moves to a low value. This alternative makes signal identifier 108 simpler, possibly at the expense of a higher rate of false transmission identification in the presence of substantial noise levels.

[0029] In embodiments in which signal identifier 108 is a synchronous unit, identification may depend on the duration for which clock signal 304 and/or data signal 302 are in a specific state. For example, an identification of a transmission may require that after transit of signal 302 from a high to low voltage, at least a predetermined period 308, or about a period 308, passes until clock signal 304 moves to a low voltage level.

Bus Stalling

[0030] Referring in detail to stalling (206) bus 110, the stalling is optionally performed by holding the clock line at a low level.

[0031] In some embodiments of the invention, the stalling (206) and the sending (204) of the wake up signal are performed simultaneously. In other embodiments, the stalling of the bus is performed after sending (204) the wake up signal, allowing the external unit 150 to proceed with the transmission until a predetermined desired point, without delaying the beginning of the wake up of controller 100. For example, with reference to FIG. 3, a wake up signal may be sent once point 322 is reached, while the bus is stalled only when point 314 is reached or even only after a predetermined number of slots 312. In one embodiment, the stalling is performed only after a first sequence of bits of the message, indicative of the address of the recipient, is received. In this embodiment, signal identifier receives this first sequence of bits and conveys its contents to port 106 when controller 100 is awake.

[0032] Optionally, both the sending (204) of the wake up signal and the stalling are performed by signal identifier 108. Alternatively, different units perform the wake up and the stalling. For example, the wake up may be performed by a watch dog circuit, for example such as described in U.S. Pat. No. 6,892,332, the disclosure of which is entirely incorporated herein by reference, modified to operate with controller 100. Signal identifier 108 is configured, in such cases, to stall bus 110 until the controller 100 wakes up. Optionally, when a transmission on bus 110 is identified, signal identifier 108 stalls the bus and sets a flag for the watch dog circuit. The next time the watch dog circuit operates, it checks if the flag is set and if so it wakes controller 100. The watch dog circuit optionally operates at a sufficient rate such that the wake-up occurs before the transmitter of external unit 150 times out.

Bus Release

[0033] Referring in detail to releasing 212 the bus 110, in some embodiments of the invention, controller 100 notifies signal identifier 108 when it has completed its wakeup process and following receipt of the notification, signal identifier 108 releases (i.e. un-stalls) bus 110. Alternatively, following stalling of the bus, signal identifier 108 monitors the status of controller 100 to determine when it wakes up. Further alternatively, following the sending of the wakeup signal, signal identifier 108 waits a predetermined period which is required for the wakeup and thereafter it releases the bus, without verifying with controller 100 that it is awake.

[0034] In some embodiments of the invention, after bus 110 is released from being stalled, external unit 150 retransmits the whole stalled message from the beginning, including the predetermined start signal. In such embodiments, once the bus is released from being stalled, port 106 receives the transmitted message as any transmission received while controller 100 is in the awake state, without need for special provisions due to the stalling of the bus.

[0035] In other embodiments, when bus 110 is released, external unit 150 continues to transmit from the point at which it stopped due to the stalling. For example, if the bus was stalled at the time point 314 (FIG. 3), external unit 150 will resume transmission from point 314. As port 106 only moves to the operative state after the bus was stalled, the information transmitted before the bus was stalled was not received by port 106. Therefore, when signal identifier 108 stalls bus 110 in the middle of a transmission, it optionally sets a flag, for example, in a register 120. When port 106 wakes up it checks register 120 to determine whether a transmission is already in progress. If register 120 indicates that a transmission was in progress, port 106 adjusts itself internally as if it had just received the predetermined start portion of the message, transmitted before the bus was stalled.

[0036] Alternatively, in order not to require configuration of port 106 for implementation of the present invention, signal identifier 108 provides port 106 with signals which imitate the start signals missed by port 106 due to its being in the sleep state. Optionally, upon determining that controller 100 is awake, before releasing bus 110, signal identifier 108 sets a switch 122 to disconnect port 106 from bus 110 and to connect it instead to signal identifier 108. Signal identifier 108 then internally transmits to port 106, the portion of the start signal missed because port 106 was asleep. After providing the missed portion of the start signal, signal identifier 108 releases the bus 110 and sets switch 122 to reconnect port 106 to the bus.

[0037] In some embodiments of the invention, signal identifier 108 includes a synchronous portion and an asynchronous portion. The asynchronous portion identifies transmissions on bus 110 while controller 100 is in a sleep state, and the synchronous portion generates the missed portion of the start signal.

[0038] Optionally, the time required for wake up of port 106 and the stalling period are shorter than the time-out period of external unit 150. In some embodiments of the invention, at wake-up, signal identifier 108 determines whether external unit 150 timed out and accordingly determines whether to notify port 106 that the predetermined start portion of the message was already received while it was asleep. If the external portion has already timed-out, such a notification is not provided.

End Remarks

[0039] While the above description relates to an SM bus, the principals of the invention may be applied to other buses

which may be stalled by the receiver. For example, while in the above description the bus is considered idle when it carries a high voltage level, in other embodiments a bus considered idle when it has a low voltage, is used. While the above description relates to a controller of a note book computer, the invention may be implemented in other device using a suitable bus.

[0040] Signal identifier **108** may be configured to operate at all times, or may be disabled by a user in hardware and/or software, at the time of system configuration. Alternatively or additionally, a user may disable signal identifier **108** at any time in which controller **100** is in the operative state. In some embodiments of the invention, signal identifier **108** automatically moves between an operative and inoperative state without user intervention. Optionally, in such embodiments, in prepare-to-sleep procedure **216**, signal identifier **108** is awakened and signal identifier **108** is disabled when controller **100** moves into its operative state.

[0041] It will be appreciated that the above described description of methods and apparatus are to be interpreted as including apparatus for carrying out the methods and methods of using the apparatus. It should be understood that, where appropriate, features and/or steps described with respect to one embodiment may be used with other embodiments and that not all embodiments of the invention have all of the features and/or steps shown in a particular figure or described with respect to a specific embodiment.

[0042] It is noted that at least some of the above described embodiments may include non-limiting details which were provided by way of example for illustration purposes and/or to describe the best mode contemplated by the inventors and therefore may include structure, acts or details of structures and acts that are not essential to the invention. Structure and acts described herein are replaceable by equivalents known in the art, which perform the same function, even if the structure or acts are different. Many alternative implementation details may be used. Therefore, the scope of the invention is limited only by the elements and limitations as used in the claims, wherein the terms "comprise," "include," "have" and their conjugates, shall mean, when used in the claims, "including but not necessarily limited to."

I claim:

1. A processor, comprising:

a processing unit having an active state and a sleep state in which at least one of the sub-sections of the processing unit is inactive;

a communication port adapted to receive signals from external units over a bus, which is configured not to be fully operative in the sleep state; and

a bus monitoring unit configured to stall the bus responsive to identifying transmissions on the bus directed to the communication port, while the processing unit is in the sleep state and to indicate to the communication port that a transmission had started while the port was in the sleep state.

2. A processor according to claim **1**, wherein the bus monitoring unit is configured to provide a wakeup signal to the processing unit, responsive to identifying a transmission on the bus that is directed to the communication port.

3. A processor according to claim **2**, wherein the bus monitoring unit is configured to provide the wakeup signal and to stall the bus, substantially concurrently.

4. A processor according to claim **2**, wherein the bus monitoring unit is configured to provide the wakeup signal before stalling the bus.

5. A processor according to claim **1**, wherein the bus monitoring unit comprises an asynchronous unit which is adapted to identify transmissions on the bus without use of a time signal.

6. A processor according to claim **1**, wherein the bus monitoring unit comprises a synchronous unit which identifies transmissions on the bus using a time signal.

7. A processor according to claim **1**, wherein the bus monitoring unit is configured to provide the communication port with an imitation of a beginning portion of a transmission from an external unit, before releasing the bus.

8. A method of handling transmissions, comprising:

identifying a transmission received over a bus, while a port intended to receive the transmission is in a sleep state;

moving the port into an operative state; and

stalling the bus responsive to receiving the transmission, until the port is in the operative state.

9. The method of claim **8**, comprising notifying the port, when it is in the operative state, that a transmission began whilst the port was in the sleep state.

10. The method of claim **8**, comprising providing locally an imitation of a beginning of the identified transmission to the port, after it moves into the operative state, before releasing the stalling of the bus.

* * * * *