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MODE DETECTOR FOR MULTIMODE MONITOR

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(57) Claim

1. A mode detector of a multimode monitor comprising :

a band separation circuit for separating respective bands of input vertical and horizontal frequencies and for providing logic signals ;

a control signal generation circuit connected to said band separation circuit for providing mode control signals by combining said logic signals of said band separation circuit ; and

a mode control circuit for controlling each mode of the multimode monitor according to said control signals of said control signal generation circuit.

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PATENTS ACT

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Complete specification for the invention entitled:

MODE DETECTOR FOR MULTIMODE MONITOR

The following statement is a full description of this invention, including the best method of performing it known to us :-

MODE DETECTOR FOR MULTIMODE MONITORS

BACKGROUND OF THE INVENTION

The present invention relates to a multimode monitor and, more particularly, to a mode detector of a multimode monitor, which detects a frequency mode applied to the multimode monitor and provides a mode signal to control the multimode monitor.

As the technology related to a computer has been developed, horizontal and vertical frequency bands are more varied. In a VGA(video graphic array) mode, the vertical frequency is generally 60Hz or 70Hz and the horizontal frequency is 31.5 KHz. Also, in an extended VGA mode, each horizontal and vertical frequency is 35.5KHz and 86Hz, respectively. Recently, in a strong VGA mode, 56Hz or 60Hz is used as the vertical frequency and 35.5KHz or 37.5KHz is used as the horizontal frequency. Thus, the multimode monitors are required to convert the mode according to various horizontal and vertical frequencies.

Fig.1 shows an example of a conventional multimode monitor. In the conventional multimode monitor, the input vertical and horizontal frequency signals are converted to a constant voltage level by a vertical frequency-to-voltage converter 10 and a horizontal frequency-to-voltage converter 20, respectively.

According to output voltages of the vertical and horizontal frequency-to-voltage converters 10 and 20, vertical and horizontal

frequency band separators 60 and 30 distinguish bands of respective input vertical and horizontal frequencies to control vertical and horizontal switching circuits 70 and 80, respectively. Then, the vertical and horizontal switching circuits 70 and 80 change respective internal oscillating vertical and horizontal frequencies according to the input vertical and horizontal frequencies. In such multimode monitors, the internal oscillating vertical and horizontal frequencies are respectively synchronized with by the input vertical and horizontal frequencies to focus a screen synchronously with the input frequencies.

However there is a problem that vertical and horizontal sizes, positions, and horizontal pin cushion should be controlled accurately according to the input vertical and horizontal frequency modes so that those are to be controlled manually by users.

SUMMARY OR THE INVENTION

The present invention has an object to provide a mode detector for multimode monitors, which controls the modes of monitor automatically according to the input vertical and horizontal frequency mode under the control of a internal control-signal generation means.

According to the present invention, there is provided a mode detector of a multimode monitor comprising : a band separation circuit for separating respective bands input vertical and horizontal frequencies and for providing logic signals ; a control signal generation circuit connected to said band separation circuit for

providing mode control signals by combining said logic signals of said band separation circuit ; and a mode control circuit for controlling each mode of the multimode monitor according to said control signals of said control signal generation circuit.

BRIEF DESCRIPTION OF DRAWINGS

These and other objects, features, and advantages of the present invention will become more apparent from the following description for the preferred embodiments taken in conjunction with the accompanying drawings, in which :

Fig.1 is a block diagram of a mode detector for a conventional multimode monitor;

Fig.2 is a block diagram of a mode detector for a multimode monitor according to the present invention ; and

Fig.3 a control signal generation circuit according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described in more detail with reference to the accompanying drawings.

Fig.2 shows a block diagram of a mode detector for a multimode monitor according to the present invention, which comprises a band separation circuit 100, a control signal generation circuit 200, and a

mode control circuit 300.

To describe in detail, the band separation circuit 100 distinguishes bands of each input vertical and horizontal frequency to provide logic signals and includes a V-F/V converter (vertical frequency-to-voltage converter) 10 which provides a high level signal when the input vertical frequency is higher than a predetermined frequency, a H-F/V converter (horizontal frequency-to-voltage converter) 20 which provides a dc voltage in proportion to the input horizontal frequency, and a horizontal frequency band separator 30 which provides a logic signal by recognizing the voltage level of the H-F/V converter 20.

As shown in Fig. 3, the control signal generation circuit 200 includes a first logic combination part 40 and a second logic combination part 50. In Fig. 3, the output voltage level of the V-F/V converter 10 becomes low when the input vertical frequency is lower than 60Hz, while it becomes high when the input vertical frequency is higher than 70Hz.

On the other hand, the mode-control circuit 300 enters a video graphic array (VGA) mode when input signals of terminals e, f, g, and h are "0100", where 1 and 0 represent logic-high and logic-low,

respectively. Similarly, the mode control circuit 300 enters the extended video graphic array (EVGA) mode when the input date is "1000", while the mode control circuit 300 enters the strong video graphic array 1 (SVGA-1) mode when the input data is "0010" and the strong video graphic array 2 (SVGA-2) mode when the input data is "0001". Also, the horizontal frequency band separator 30 provides signals "100" through terminals b, c, and d when the input horizontal frequency applied to the H-F/V converter 20 is 31.5KHz. Similarly, the horizontal frequency band separator 30 provides "010" for the input horizontal frequency of 35.5KHz and "011" for the input horizontal frequency of 37.5KHz.

Next, the first logic combination circuit 40 in the control signal generation circuit 200 includes four inverters I1-I4 and an AND gate A1. Two inverters I1 and I2 are connected in series to the output terminal of the V-F/V converter 10, while the other two inverters I3 and I4 are connected in series to the output terminal (d) of the horizontal frequency band separator 30.

Another output terminal (c) of the horizontal frequency b and separator 30 and the output terminal of the inverter are connected to the input terminals

of an AND gate A1, respectively. The second logic combination circuit 50 includes three inverters I5-I7 and three NAND gates NA1-NA3, where output signals of the inverter I2 and the AND gate A1 in the first logic combination part 40 are respectively applied to two input terminals of the NAND gate NA1 in the second logic combination circuit 50 and also the output signals of the inverter I1 are applied to two input terminals of the NAND gate NA2 in the second logic combination part 50.

Also, the output signals of inverters I5-I7 are applied to input terminals (e), (g), and (h) of the mode control circuit 300 respectively. Three pull-up resistors R1-R3 are connected to the

output terminals of the inverters I5~I7, respectively.

On the other hand, the output signal of the terminal (b) of the horizontal frequency band separator 30 is directly applied to the input terminal (f) of the mode control circuit 300. The mode control circuit 300 controls the mode of the monitor according to the combination of the logic signals applied to the input terminals (e), (f), (g), and (h).

If the vertical frequency of 60 or 70 Hz and the horizontal frequency of 31.5KHz are applied to the mode detector in Fig.3 in the VGA mode, the output of the V-F/V converter 10 may be either "1" or "0", that is, "don't-care" state, while the output voltage of the terminal (b) of the horizontal frequency band separator 30 become "1" and the output voltages of the terminals (c) and (d) are commonly "0". Then, an input terminal of the NAND gate NA3 is set to be "0" through the inverters I3 and I4 and thus the output voltage of the NAND gate NA3 becomes "1" independently of the output voltage of the inverter I1. Thus, the input terminal (h) of the mode control circuit 300 is set to be "0". On the other hand, the output voltage of the AND gate A1 becomes "0" since the voltage at the terminal (c) of the horizontal frequency band separator 30 is "0". Then, the output voltages of the NAMD gates NA1 and NA2 become commonly "1" independently of the outputs of the inverters I1 and I2, and thus the input terminals (e) and (g) of the mode control circuit 300 are set to be "0". On the other hand, the input terminal (f) of the mode control circuit 300 is set to be "1" since the voltage level at the output terminal (h) of the horizontal

frequency band separator 30 is "1". Thus, the mode control circuit 300 recognizes that the present vertical and horizontal frequencies are in the VGA mode according to the input signal "0100" at the input terminals (e), (f), (g), and (h) and controls the internal vertical and horizontal oscillating frequencies, the vertical and horizontal sizes, the positions, and the horizontal Pin-cushion of the monitor in the VGA mode.

Similarly, for the vertical frequency of 86Hz and the horizontal frequency of 35.5KHz, the voltage level at the output terminal (a) of the V-F/V converter 10 becomes "1" and the output terminals (b), (c), and (d) of the horizontal frequency band separator 30 become "0", "1", and "0", respectively. In the first and second logic combination circuits 40 and 50, then, the input terminals (e), (f), (g), and (h) of mode control circuit 300 are respectively set to be "1", "0", "0", and "0". Then the mode control circuit 300 recognizes the input vertical and horizontal frequencies are in the EVGA mode and controls the monitor for the EVGA mode.

For the vertical frequency of 56Hz and the horizontal frequency of 35.5KHz, the voltage level at the output terminal of the V-F/V converter 10 become "0" and the voltage level at the terminal of the horizontal frequency band separator 30 becomes "1" and that of the other terminals becomes "0". Thus, the mode control circuit 300 recognizes that the input vertical and horizontal frequencies are in the SVGA-1 mode, so the mode control circuit 300 control the monitor for the SVGA-1 mode.

In the similar manner, at the vertical frequency of 60Hz and the horizontal frequency of 37.5KHz, the mode control circuit 300 controls the monitor in the SVAG-2 mode. The above mentioned operation is summarized by the table 1 as follows :

< Table.1 >

CARD Q2	VGA	EVGA	SVGA-1	SAGA-2
V/H-frequency terminal	V:60.70Hz H:31.5KHz	V:86Hz H:35.5KHz	V:56Hz H:35.5KHz	V:60Hz H:37.5KHz
a	x	1	0	0
b	1	0	0	0
c	0	1	1	1
d	0	0	0	1
e	0	1	0	0
f	1	0	0	0
g	0	0	1	0
h	0	0	0	1

(x : Don't care state)

As mentioned above, the present invention can automatically control the vertical and horizontal synchronized-oscillating frequencies, the vertical and horizontal sizes, and the horizontal pin cushion of the monitor according to the mode of the input vertical and horizontal frequencies by detecting the mode of the input frequencies in the

control signal generation circuit and by providing the combined logic signals of the control signal generation circuit to the mode control circuit.

The invention is in no way limited to the embodiment described hereinabove. Various modifications of the disclosed embodiment as well as other embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of he present invention.

The claims defining the invention are as follows:

1. A mode detector of a multimode monitor comprising :

a band separation circuit for separating respective bands of input vertical and horizontal frequencies and for providing logic signals ;

a control signal generation circuit connected to said band separation circuit for providing mode control signals by combining said logic signals of said band separation circuit ; and

a mode control circuit for controlling each mode of the multimode monitor according to said control signals of said control signal generation circuit.

2. A mode detector of a multimode monitor according to claim 1, wherein said band separation circuit includes :

a vertical frequency-to-voltage converter for providing a high level signal when the input vertical frequency is higher than a predetermined frequency;

a horizontal frequency-to-voltage converter for providing a dc voltage in proportion to the input horizontal frequency; and

a horizontal frequency band separator for providing the logic signals according to the output level of said horizontal frequency-to-voltage converter.

3. A mode detector of a multimode monitor according to claim1, wherein said control signal generation circuit includes a first

logic combination circuit for combining the output of said band separation circuit and a second logic combination circuit for combining the outputs of said first logic combination circuit.

4. A mode detector of a multimode monitor according to either claim 2 or 3, wherein said first logic combination circuit includes:

a first and a second inverter connected in series to said vertical frequency-to-voltage converter;

a third and a fourth inverter connected in series to said horizontal frequency band separator; and

an AND gate connected to said horizontal frequency-band separator and an output of the third inverter, for logically multiplying the two signals inputted therefrom.

5. A mode detector of a multimode monitor according to either claim 3 or 4, wherein said second combination circuit includes:

a NAND gate connected to both outputs of said second inverter and said AND gate, for logically combining two signals provided therefrom;

a NAND gate connected to both outputs of said first inverter and said AND gate, for logically combining two signals provided therefrom; a NAND gate connected to both outputs of said first inverter and said fourth

inverter, for logically combining two signals provided therefrom; and a plurality of inverters connected to outputs of said NAND gates.

6. A mode detector of a multimode monitor substantially as herein before described with particular reference to figs. 2 and 3 of the accompanying drawings.

Dated this 16th day of July 1992

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FIG. 1
(PRIOR ART)

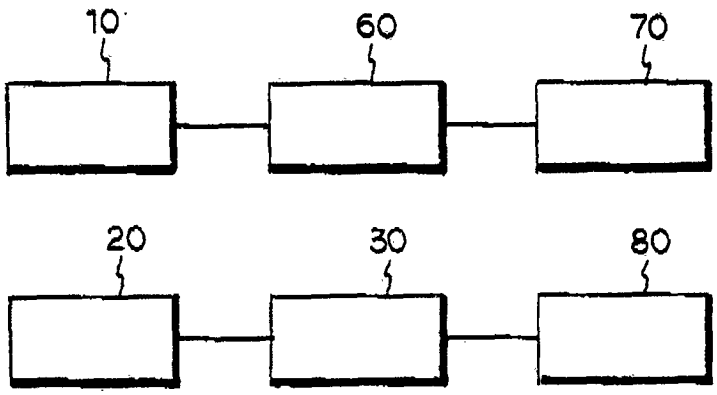

FIG. 2

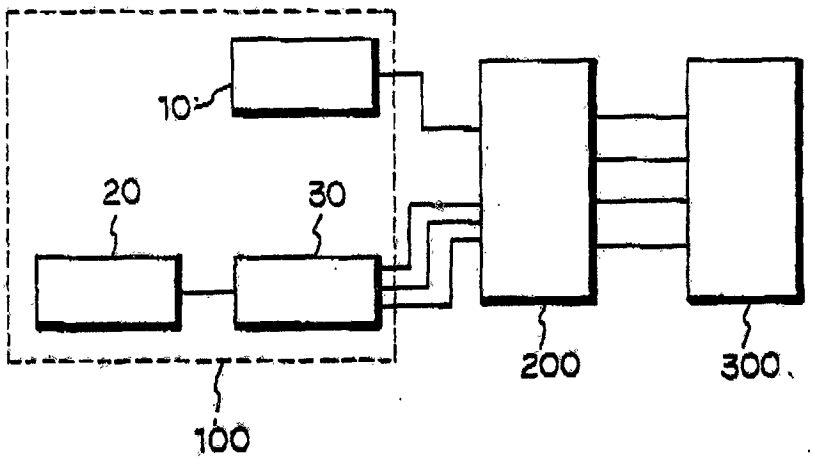

FIG. 3