Aug. 19, 1947. E. BARD ET AL 2,425,981

BALANCED FREQUENCY DISCRIMINATOR

Filed Oct. 27, 1943 2 Sheets-Sheet 1

Fig. 1.

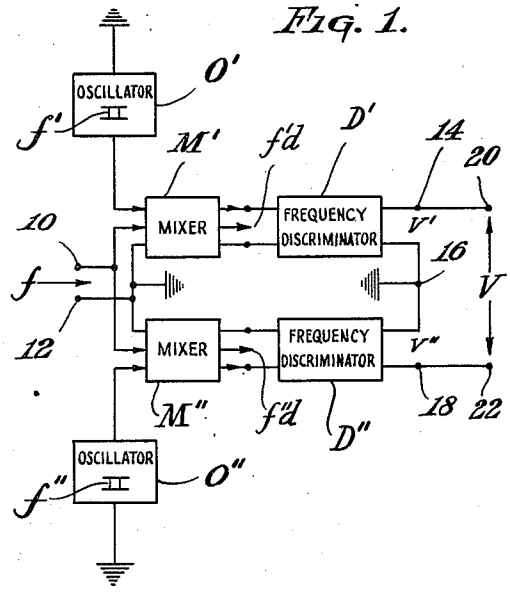

Fig. 1a.

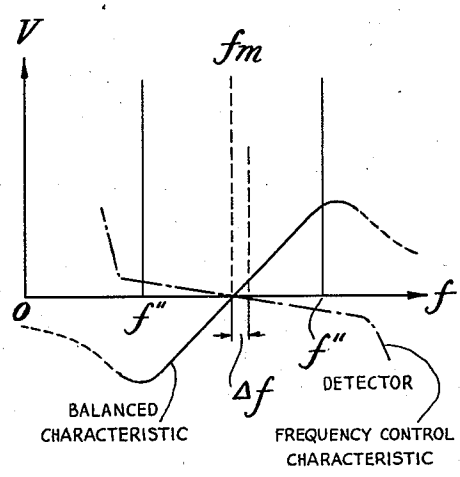

Fig. 2.

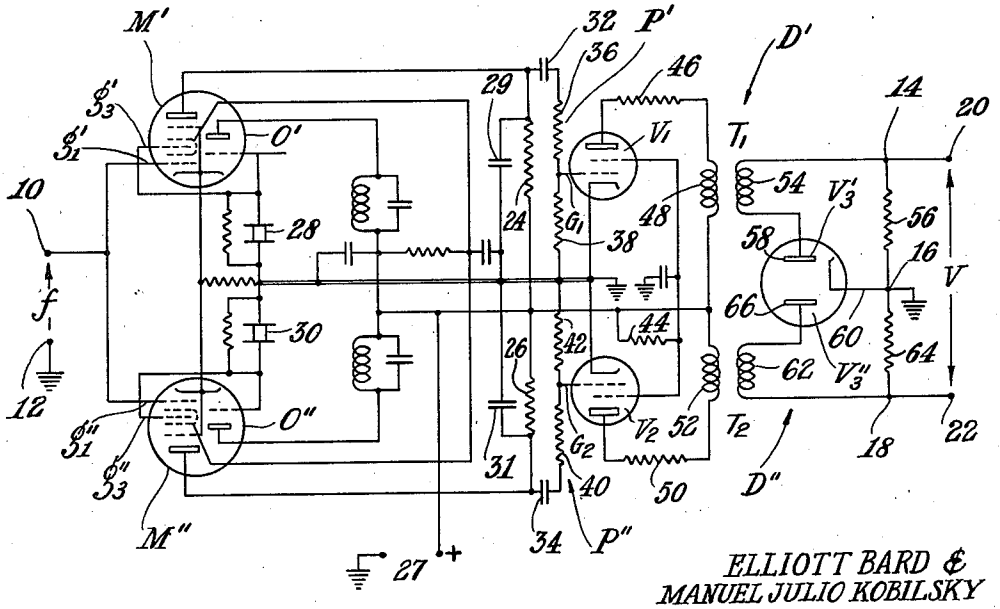

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Fig. 3.

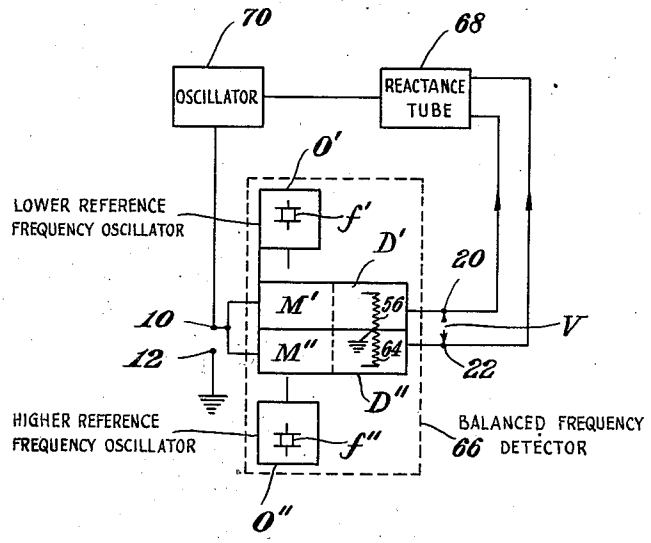
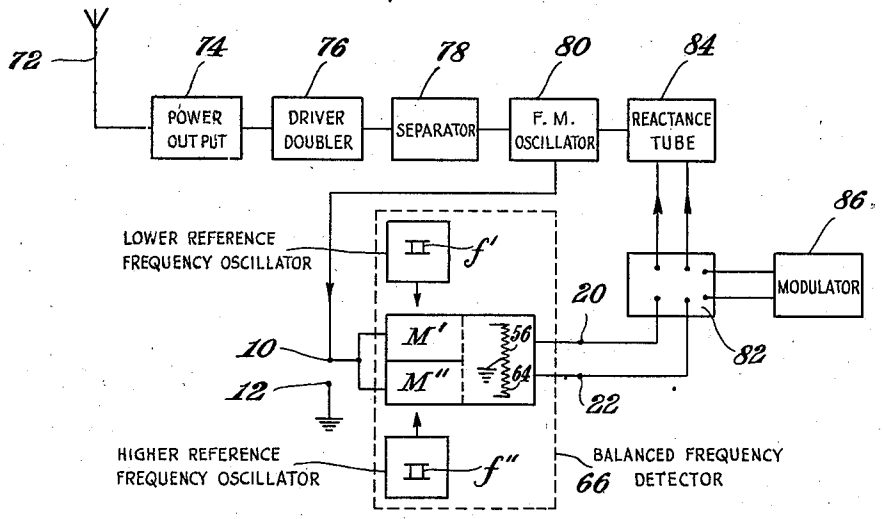


Fig. 4.



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BALANCED FREQUENCY DISCRIMINATOR

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Application October 27, 1943, Serial No. 507,844

6 Claims. (Cl. 250—17)

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This invention relates to improvements in frequency detecting systems and more particularly to balanced frequency detectors especially useful in frequency stabilizing circuits.

As known in the art, the main disadvantage of the common frequency discriminator resides in the critical adjustment of the tuned circuits thereof and in order to avoid this drawback, discriminators of the so-called frequency counter type have been developed which are fully explained in the prior U. S. patent applications of M. Zeigler and M. J. Kobilsky, Serial Number 464,380, filed November 3, 1942, Patent Number 2,406,309, dated August 20, 1946, and M. Zeiler, Serial Number 477,990, filed March 4, 1943. The combination of a frequency counter with a mixer tube and a fixed reference oscillator particularly useful in frequency stabilizing systems, constitutes an unbalanced frequency detector which is easily adjusted and which by utilizing compensating voltage, will provide a zero output for a predetermined frequency independently of the variations in the supply voltages.

However, due to the particular frequency transmission characteristic of the mixer device, the unbalanced frequency detector comprising a frequency counter provides a zero output voltage for a plurality of frequencies, so that in a frequency stabilizing system the frequency discriminator curve thereof crosses the frequency control curve of the system to be stabilized at several points which constitute working points of stable equilibrium, and it has been found in practice that sudden changes in the operating conditions may shift the frequency detector from one working point to another, thus upsetting the normal operation of the whole frequency stabilizing system.

In the prior U. S. patent application of M. Zeigler Serial No. 488,582 filed May 26, 1943, a frequency stabilizing system has been described, which comprises an unbalanced frequency detector system but in which the range of the frequency control has been effectively restricted, by a limiter stage inserted between the frequency discriminator or counter and the reactance tube thereby limiting the operation of the frequency stabilizing system to one stable working point only.

We have found however, that by using two unbalanced frequency detectors in a balanced arrangement and by connecting their out-puts in push-pull or opposition, a frequency detector is obtained which will provide a zero output voltage for solely one predetermined frequency and the frequency detector curve thereof, when used in

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a frequency stabilizing system, will cross the frequency control curve at one point only. In the balanced frequency detector according to the present invention the variable frequency is simultaneously balanced with respect to a lower and a higher fixed reference frequency, respectively, by mixing it with said reference frequencies so as to obtain a first and a second difference frequency respectively. These difference frequencies are then separately applied to frequency discriminators or counters which develop in their output circuits D. C. voltages proportional to the frequency of said difference frequencies. By connecting the output circuits of both frequency discriminators or counters in opposition or "push-pull," a resulting balanced detector output voltage is obtained which, being equal to the difference of the two D. C. voltages, is zero when the variable frequency corresponds to the mean value of the reference frequencies, and which is proportional in magnitude and sign to the deviation of the variable frequency from said mean value.

Therefore the main object of the present invention is to provide a balanced frequency detector which will have a zero output voltage for solely one predetermined frequency value.

A further object of the present invention is to obtain a frequency detector, the detector characteristic of which will be independent of the variations in the supply voltages and/or circuit parameters, due to the balanced arrangement of the components thereof and also to its push-pull output circuit.

A still further object of the present invention is to provide a balanced frequency detector which will have twice the sensitivity of the unbalanced detector of the frequency counter type.

Another object of the present invention is to provide a balanced frequency detector which, when used for frequency stabilization purposes, will furnish a stabilizing system having one working point only.

These and other objects and advantages of the present invention will become apparent from the course of the following description, when read in conjunction with the accompanying drawings, which illustrate one preferred embodiment of the invention, by way of example.

In the drawings:

Fig. 1 is a connection diagram of the basic layout of a balanced frequency detector according to the present invention.

Fig. 1*a* is a graph illustrating the relative position of the detector characteristic of the balanced frequency detector with respect to the fixed

reference frequencies and also with respect to the frequency control characteristic curve of the stabilizing system shown in Fig. 3.

Fig. 2 is a circuit diagram of the balanced frequency detector according to the present invention.

Fig. 3 is a connection diagram illustrating a frequency stabilizing system using a balanced frequency detector according to the present invention.

Fig. 4 is a connection diagram illustrating a frequency modulation transmitter stabilized by means of a balanced frequency detector according to the present invention.

The same reference characters are used to indicate like or corresponding parts or elements throughout the drawings.

Referring now to Fig. 1, it may be seen that the balanced frequency detector according to the present invention comprises a crystal controlled oscillator O' generating a lower fixed reference frequency f' and an oscillator O'' which is also controlled by a crystal and which generates a higher reference frequency f'', oscillators O' and and O'' are coupled to one of the inputs of the mixers M' and M'' respectively, the other inputs of which are connected in parallel and comprise the input terminals 10 and 12 of the balanced frequency detector, to which the variable frequency f is applied.

Due to the abovementioned arrangement, mixer M' develops in its output circuit a first difference frequency F'_d while mixer M'' generates a second difference frequency f''_d, the output circuits of said mixers M' and M'' being coupled to the frequency discriminators or counters D' and D'' respectively, which transform said difference frequencies f'_d and f''_d into D. C. voltages v' and v'' proportional to the frequency f'_d and f''_d, respectively.

In view of the fact that the output terminals 14, 16 and 16,18 of the discriminators D' and D'' respectively are connected in opposition or push-pull, the detector output voltage V developed between output terminals 20 and 22 of the balanced frequency detector will be equal to the difference of said voltages v' and v'' and will also be proportional in magnitude and sign to the deviation of the variable frequency f from the mean value of both reference frequencies f' and f'', as will be explained hereinafter.

Considering the individual response characteristics of the frequency discriminators or counters D' and D'', we can write for the voltages v' and v''

$$(1)\quad v'=k'_1.f'_d+k'_2.(f'_d)^2+k'_3.(f'_d)^3+\ \ldots$$

$$(2)\quad v''=k''_1.f''_d+k''_2.(f''_d)^2+k''_3.(f''_d)^3+\ \ldots$$

where f'_d and f''_d represent the difference frequencies generated by the mixers M' and M'' and k'_1, k'_2, k'_3 and k''_1, k''_2 and k''_3 represent the coefficients of the transfer characteristics of the discriminators D' and D'' respectively.

As both voltages v' and v'' are connected in opposition, detector voltage V will be equal to the difference of v' and v'', or

$$(3)\quad V=k_1.(f'_d-f''_d)+k_2.[(f'_d)^2-(f''_d)^2]+k_3.[(f'_d)^3-(f''_d)^3]+\ \ldots$$

where

$$k_1=k'_1=k''_1;\ k_2=k'_2=k''_2;\ k_3=k'_3=k''_3$$

since both discriminators or frequency counters D' and D'' are arranged to have like transfer characteristics.

Considering Equation 3 it will be evident to those skilled in the art that the detector voltage V, developed between the output terminals 20 and 22 of the balanced frequency detector will be zero only when the difference of the frequencies f'_d and f''_d is zero, viz. when the variable frequency f corresponds to the mean frequency of the fixed reference frequencies f' and f''. Consequently, the balanced frequency detector according to the invention will have a zero detector voltage only when the variable frequency f passes through a point equidistantly located between the reference frequencies f' and f'', as may be seen in the graph shown in Fig. 1*a*.

Since in Equation 3 the higher order terms are of much smaller magnitude than the linear term of the difference frequencies f'_d and f''_d, a deviation of the variable frequency f from its central or mean value f_m will produce between the output terminals 20 and 22 of the balanced detector a voltage $V=2K(f)$, where K represents the transfer constant of the balanced frequency detector and $f=(f'_d-f''_d)$ represents the frequency deviation. Thus the D. C. detector voltage V of the balanced frequency detector will not only be proportional in magnitude to the frequency f but will be either positive or negative depending on whether the variable frequency f is above or below the mean frequency f_m.

It may be seen in Fig. 1 that oscillator O', mixer M', discriminator D' and oscillator O'', mixer M'', discriminator D'' constitute in fact two unbalanced frequency detectors which, due to the location of the reference frequencies f' and f'' with respect to the variable frequency f, and also due to the push-pull connection of the discriminator output circuits, form together a balanced frequency detector which has a zero output voltage for the predetermined mean value of the variable frequency f.

Fig. 2 represents the circuit of the balanced frequency detector based on the diagram of Fig. 1, in which input terminal 12 is connected to ground potential, while input terminal 10 is connected to the signal grids g'_1 and g''_1 of two thermionic mixer tubes M' and M'' respectively, the load resistances 24 and 26 of which are connected to the positive pole of a direct current source 27 from which the other supply voltages for the other electrodes of the tubes are derived as is known in the art.

Injector grids g'_3 and g''_3 of said mixer tubes M' and M'' are coupled to oscillators O' and O'' respectively, constituted by triode tubes controlled by the corresponding quartz crystals 28 and 30. Oscillator O' generates the lower reference frequency f' whereas oscillator O'' generates the higher reference frequency f'', so that in the plate circuits of the mixers M' and M'' the corresponding difference frequencies f'_d and f''_d are developed. The plate circuits of said mixer tubes M' and M'' are provided with filter condensers 29 and 31 respectively, which constitute short-circuits for the reference frequencies f' and f'' so that only the difference frequencies f'_d and f''_d are applied to the inputs of the discriminators D' and D'' which, in the present embodiment of the invention, are constituted by frequency counters of the type described in the prior U. S. patent application Serial No. 477,990.

Said frequency counters D' and D'' comprise a thermionic counter valve V_1 and V_2 and an integrating circuit constituted by a half-wave diode rectifier V'_3, V''_3 respectively, the frequency

counters being coupled to the corresponding mixers M' and M'' through coupling condensers 32 and 34 and potentiometers P' and P'' formed by the resistances 36, 38 and 40, 42 respectively. The screen grids of the tubes V_1 and V_2 are connected through a common voltage-dropping resistance 44 to the positive pole of direct current supply source 27, to which the plate circuits of both tubes are also connected. These plate circuits are constituted by resistance 46, self-inductance 48, and resistance 50, a self-inductance 52 respectively, inductance 48 constituting the primary winding of a transformer T_1, the secondary winding 54 of which, together with a load resistance 56 and the half-wave diode rectifier V'_3 formed by anode 58 and cathode 60, constitutes the integrating circuit of the frequency counter D'.

Inductance 52, inserted in the plate circuit of the counter tube V_2 constitutes the primary winding of a coupling transformer T_2, the secondary winding 62 of which is connected in series with load resistance 64 and the half-wave diode rectifier V''_3 comprising anode 66 and the cathode 60 thus forming the integrating circuit of the frequency counter D''.

The operation of the frequency counters has been fully described in the prior U. S. patent application Serial No. 477,990 where it has been explained that when a sinusoidal voltage is applied to the control grids G_1 or G_2 of the counter tubes V_1 or V_2, the plate current of said tubes flowing through the plate circuits constituted by 48, 46 and 52, 50 respectively, will vary for each half period of like sign of the applied difference frequency so as to generate across the inductances 48 and 52 voltage impulses which, when rectified by the half-wave diode rectifier valves V'_3 and V''_3 and integrated over a time which is sufficiently large compared with the period of the difference frequencies f'_d and f''_d develop across the load resistances 56 and 64 the voltages v' and v'' proportional to the frequency of said difference frequencies f'_d and f''_d.

As may be seen in Fig. 2, the output terminals 20 and 22 of the balanced frequency detector are connected to the ends of said load-resistances 56 and 64, the junction 16 of which is connected to the common cathode 60, so that both load resistances form a push-pull output circuit wherein a detector output voltage V is developed which, being equal to the difference of said voltages v' and v'', is proportional to the deviation of the variable frequency f from the central or mean frequency f_m, as explained hereinbefore.

In short, the balanced frequency detector according to the present invention is formed by two separate unbalanced frequency detectors of the frequency counter type, each constituted by the reference oscillator O' (O'') mixer M' (M'') and counter tube V_1 (V_2) each unbalanced frequency detector being provided with an integrating circuit the load resistances 56 and 64 of which are connected in push-pull or opposition. In view of the balanced arrangement of said frequency detectors and due to the push-pull connection of the frequency counter outputs, a balanced frequency detector is obtained which provides a zero output voltage without the use of a compensating voltage and in which slight variations of the circuit parameters will be automatically compensated. Moreover, the balanced arrangement will compensate for slight and opposite variations of the reference frequencies, thus greatly improving the performance of the novel frequency detector.

The balanced frequency detector according to the present invention is particularly adapted for frequency stabilization purposes by applying to the input thereof the frequency of an oscillator to be stabilized and feeding back the detector output voltage through a reactance tube to the oscillator, the frequency of which should of course be approximately the arithmetic mean of the two fixed reference frequencies f' and f''.

The circuit arrangement for this purpose is shown in block diagram in Fig. 3, in which the balanced frequency detector is represented by the rectangle 66, and in which the output voltage V of the frequency detector is applied to a reactance tube or equivalent device 68 which controls the frequency of an oscillator 70 which in turn is coupled to the input terminals 10, 12 of the balanced frequency detector.

Those skilled in the art will readily understand that in the frequency stabilizing system shown in Fig. 3, the frequency of the oscillator 70 will tend automatically to adjust itself very near to the central or mean frequency f_m of the reference frequencies f' and f'', since every deviation of the oscillator frequency from f_m will produce a corresponding voltage V in the output circuit of the balanced frequency detector 66, and said voltage, acting through reactance tube 68, will tend to readjust the oscillator 70 to its original frequency.

A low pass filter may be included in the output circuit of the balanced frequency detector, to exclude from the output voltage the components of the frequency of the voltage impulses and harmonics thereof, so as to obtain solely a voltage which will vary proportionally to the deviation of the frequency f to be controlled.

In view of the fact that the detector output voltage V has a zero value for only one predetermined frequency, the above described frequency stabilization system has only one working point, viz. the detector characteristic and the frequency control curves cross at one point only, as may be observed in Fig. 1a.

As illustrated in Fig. 4, the novel balanced frequency detector may be also applied to frequency modulated transmission. The transmitter antenna 72 is connected through a power output section 74, a driver or doubler 76 and a separator 78 to an oscillator 80 which is also connected to the input of the balanced frequency detector represented by rectangle 66. The output of the balanced detector is applied through an output low-pass filter 82 to the reactance tube or similar device 84 which controls the frequency of oscillator 80.

The frequency stabilizing circuit of Fig. 4 is substantially that shown in Fig. 3, except for output low-pass filter 82 and modulator 86 connected to the same, so that the balanced frequency detector output, when passing through said low-pass filter 82 is modulated by the intelligence amplified by the modulator 86. The reactance tube 84 therefore acts both as stabilizer and as modulator, and while the balanced frequency detector 66 maintains the oscillator 80 near the central frequency f_m, the output of the oscillator is also frequency modulated by superposition of the intelligence derived from modulator 86.

In the described embodiment of the novel balanced frequency detector, frequency discriminators of the frequency counter type have been utilized which are described in the prior U. S. patent application No. 477,990. However, it is to be un-

derstood that this invention is not limited to the type of the discriminator hereinbefore specifically described for the purpose of illustration and that variations and modifications may be made without departing from the spirit of this invention, and such variations and modifications, or the use of such individual features or subcombination of features as do not depart from the spirit of this invention are, although not specifically described herein, contemplated by and within the scope of the appended claims.

What we claim is:

1. A balanced frequency detector having zero output at a frequency value of a variable frequency wave corresponding to the mean frequency of two fixed reference frequencies, comprising a first crystal-controlled oscillator for generating a wave having the lower of said reference frequencies, a second crystal controlled oscillator for generating a wave having the higher of said reference frequencies, first and second thermionic mixer tubes each having an injector grid, a signal grid and an output electrode, means to connect said signal grids in parallel and to apply thereto said variable frequency wave, means to couple said first and said second oscillators to the injector grids of said first and second mixer tubes respectively, frequency counters coupled to the output electrodes of said mixer tubes for deriving a first and a second voltage proportional to the frequency of the difference frequency waves generated in the output circuits of said first and said second mixer tubes respectively, each of said frequency counters comprising a direct current source, an inductance connected thereto, means to vary the current a like value for each half period of like sign of the respective difference frequency wave and thereby generate voltage impulses across said inductances, and means to integrate the voltage impulses to produce a voltage, and means to connect the respective frequency counters in push-pull to produce an output voltage varying as the difference of the respective derived voltages and which is zero for said mean frequency value of the variable frequency wave and proportional to the deviation of said variable frequency wave from said mean frequency value.

2. A balanced frequency detector having zero output at a frequency value of a variable frequency wave corresponding to the mean frequency of two fixed reference frequencies, comprising a first crystal-controlled oscillator for generating a wave having the lower of said reference frequencies, a second crystal-controlled oscillator for generating a wave having the higher of said reference frequencies, first and second thermionic mixer tubes each having an injector grid, a signal grid and an output electrode, means to connect said signal grids in parallel and to apply thereto said variable frequency wave, means to couple said first and second oscillators to the injector grids of said first and second mixer tubes respectively, and frequency counters coupled to the output electrodes of said mixer tubes, each of said frequency counters comprising a thermionic tube including a cathode, a control grid and an anode, means to couple the control grid to the output electrode of the corresponding mixer tube, a resistance, a self-inductance and a current source connected in series circuit arrangement with said cathode and anode, and voltage integrating means inductively coupled to said anode circuit, said voltage integrating means comprising a half-wave diode rectifier tube and a load resistance coupled thereto, the respective load resistances of the frequency counters being interconnected to produce an output voltage varying as the difference of the voltages developed across each of the load resistances.

3. A balanced frequency detector having zero output at a frequency value of a variable frequency wave corresponding to the mean frequency of two constant reference frequencies, said detector comprising means for generating a wave having the lower of said reference frequencies, means for mixing said variable frequency wave with said lower reference frequency wave to produce a first difference frequency wave, means for generating a wave having the higher of said reference frequencies, means for mixing said variable frequency wave with said higher reference frequency wave to produce a second difference frequency wave, frequency counters coupled to the respective mixing means, each of said frequency counters comprising a thermionic counter tube including a cathode, a control grid and an anode, means to couple the control grid to the corresponding mixing means, a resistance, a self-inductance and a current source connected in series circuit arrangement with said cathode and anode, and voltage integrating means inductively coupled to said anode circuit, each of said voltage integrating means comprising a half-wave diode rectifier tube and a load resistance coupled thereto, the respective load resistances of the frequency counters being connected to produce an output voltage varying as the difference of the voltages developed across each of the load resistances.

4. A balanced frequency detector having zero output at a frequency value of a variable frequency wave corresponding to the mean frequency of two constant reference frequencies, said detector comprising means for generating a wave having the lower of said reference frequencies, means for mixing said variable frequency wave with said lower reference frequency wave to produce a first difference frequency wave, means for generating a wave having the higher of said reference frequencies, means for mixing said variable frequency wave with said higher reference frequency wave to produce a second difference frequency wave, frequency counters coupled to the respective mixing means, each of said frequency counters comprising a thermionic counter tube including a cathode, a control grid, and an anode, means to couple the control grid to the corresponding mixing means, a resistance, a self-inductance and a current source connected in series circuit arrangement with said cathode and anode, a winding inductively coupled to said self-inductance and a diode rectifier and a load resistance coupled to said winding, the respective load resistances of the frequency counters being connected to produce an output voltage varying as the difference of the voltages developed across each of the load resistances.

5. A frequency stabilizing apparatus comprising in combination a source of electrical oscillations the frequency of which is to be stabilized and including frequency adjusting terminals and an output circuit, and a frequency detector comprising two mixers each including two input terminals and an output circuit, and a source of direct current, one of the input terminals of said mixers being connected in parallel to the output circuit of said source of electric oscillations, oscillators for generating a lower fixed reference frequency wave and a higher fixed reference fre-

quency wave, means to couple said oscillators one to each of the other of the input terminals of said mixers, two frequency counters having input terminals coupled to the output circuits of said mixers and connected to said source of direct current, each frequency counter comprising means for impulsively varying said direct current in response to the variations of the difference frequency waves produced in the output circuits of said mixers, a circuit connected to said source of current and including said current varying means and a self-inductance, voltage integrating means coupled to said self-inductance, the output circuits of said voltage integrating means being connected in push-pull and constituting a balanced output circuit for producing a voltage proportional to the frequency variation of said source of electrical oscillations, frequency adjusting means having input terminals connected to the output of said balanced output circuit, and output terminals connected to the frequency adjusting terminals of the source of oscillations, whereby a correcting adjustment is impressed on said source of oscillations is response to variations in the balanced output circuit of the frequency detector.

6. A frequency modulated transmitter comprising in combination an output circuit terminating in a transmitting antenna, a frequency modulated oscillator including modulation terminals and output terminals connected to said output circuit, two mixers each including two input terminals, an output circuit and a source of direct current, one of the input terminals of each mixer being connected in parallel and being coupled to said frequency modulated oscillator, oscillators for generating a lower reference frequency wave and a higher reference frequency wave, means to couple said oscillators one to each of the other of the input terminals of said mixers to produce in the output circuits of said mixers first and second difference frequency waves, two frequency counters having input terminals coupled to the output circuits of said mixers and connected to said source of direct current, each frequency counter comprising means for impulsively varying said direct current in response to variations of the outputs of said mixers, a circuit connected to said source of current and including said current varying means and a self-inductance, voltage integrating means coupled to said self-inductance, the output circuits of said voltage integrating means being connected in push-pull and constituting a balanced output circuit delivering a voltage proportional to the frequency deviation of said source of oscillations from the mean frequency value of said lower and said higher fixed reference frequency waves, a source of voltage proportional to intelligence to be transmitted, a band-pass filter element connected to said intelligence voltage source and to said balanced output circuit, and frequency adjusting means connected between the output terminals of said band-pass filter and the modulation terminals of said frequency modulated oscillator.

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