(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 November 2015 (26.11.2015)

WIPO | PCT

(10) International Publication Number
WO 2015/179062 A1

(51) International Patent Classification:
H01L 27/115 (2006.01) *H01L 21/768* (2006.01)

(21) International Application Number:
PCT/US2015/027308

(22) International Filing Date:
23 April 2015 (23.04.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
14/282,520 20 May 2014 (20.05.2014) US

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

— *with international search report (Art. 21(3))*

(54) Title: POLAR, CHIRAL, AND NON-CENTRO-SYMMETRIC FERROELECTRIC MATERIALS, MEMORY CELLS INCLUDING SUCH MATERIALS, AND RELATED DEVICES AND METHODS

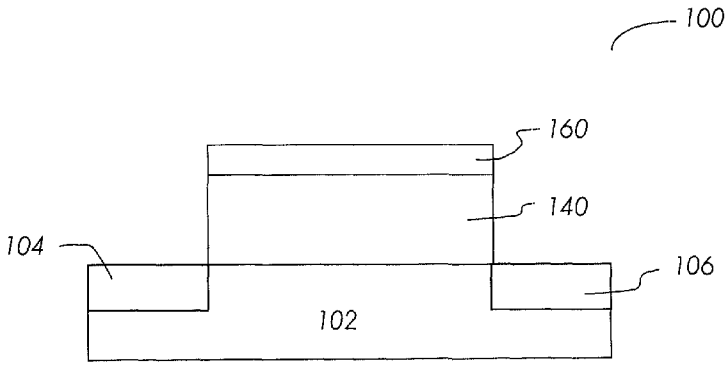


FIG. 1

(57) Abstract: A ferroelectric memory cell comprises a ferroelectric crystalline material having a polar and chiral crystal structure without inversion symmetry through an inversion center. The ferroelectric crystalline material does not consist essentially of an oxide of at least one of hafnium (Hf) and zirconium (Zr).

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POLAR, CHIRAL, AND NON-CENTRO-SYMMETRIC FERROELECTRIC MATERIALS, MEMORY CELLS INCLUDING SUCH MATERIALS, AND RELATED DEVICES AND METHODS

PRIORITY CLAIM

This application claims the benefit of the filing date of United States Patent Application Serial No. 14/282,520, filed May 20, 2014, for "Polar, Chiral, and Non-Centro-Symmetric Ferroelectric Materials, Memory Cells Including Such Materials, and Related Devices and Methods."

TECHNICAL FIELD

Embodiments of the disclosure relate to the field of semiconductor device design and fabrication. More specifically, embodiments of the disclosure relate to methods of forming ferroelectric memory cells including a ferroelectric material and to related semiconductor device structures, such as memory devices.

BACKGROUND

Demands on semiconductor memory devices toward larger storage capacity and faster access speed have continued to increase. Semiconductor memory devices may be categorized into volatile memory devices and non-volatile memory devices. Dynamic Random Access Memory (DRAM) is a prominent volatile memory device, allowing for high speed and high capacity data storage. Examples of non-volatile memory devices include ROM (Read-only-Memory), EEPROM (Electrically Erasable Programmable ROM), FeRAM (Ferroelectric RAM), and MRAM (Magnetoresistive RAM).

With regard to FeRAM devices, a ferroelectric material is used to store information. The FeRAM devices may include a 1T-1C (1 Transistor-1 Capacitor) memo ry cell design, similar in construction to a DRAM memory cell, wherein one capacitor and one access transistor form a memory cell. While the dielectric material of DRAM cell capacitor is a linear dielectric material, the dielectric material of FeRAM cell capacitor includes a ferroelectric dielectric material. The FeRAM devices may include a 1T (1 Transistor) memory cell design, based on a ferroelectric field effect transistor (FeFET). For FeFET memory cell, the gate isolation material includes a ferroelectric dielectric material.

Ferroelectric (FE) materials are electrically polarizable materials that possess at least two polarization states, which polarization states may be switched by the application

of an external electric field. Each polarization state of FE materials remains stable even after the removal of the applied electric field for at least some period of time. Due to this stability of polarization states, FE materials have been used for memory applications. One of the polarization states is considered to be a logic "1" and the other state a logic "0." FE materials have a non-linear relationship between the applied electric field and the apparent stored charge, resulting in a ferroelectric characteristic in the form of a hysteresis loop. Several types of FE memory devices have been reported, such as FeRAM devices, and FeFET for NAND and NOR devices.

Perovskite materials, such as lead zirconate titanate (PZT), have commonly been used as FE materials for the FE memory device applications. However, such conventional FE memory devices often fall short in terms of bit density and scalability because perovskite materials exhibit low remnant polarization (*Pr*). For FeRAM, the thickness of ferroelectric PZT film must be up to 200 nanometers (nm). Thus, the use of conventional FE materials for the sub 20 nm-FE memory devices has been limited. In addition, conventional FE materials, such as PZT, possess limited compatibility with standard semiconductor processing techniques.

Thin films of silicon doped hafnium oxide ($SiHfO_2$) in orthorhombic phase have been investigated as an FE material for FE memory devices. However, the orthorhombic phase of $SiHfO_2$ is not stable, and certain restrictive processing techniques must be utilized in order to stabilize the orthorhombic phase. For example, a titanium nitride (TiN) top electrode may be formed over the thin film of $SiHfO_2$ material, prior to inducing the crystallization of $SiHfO_2$ material through a high temperature annealing process. By crystallizing $SiHfO_2$ material in the presence of an overlying TiN top electrode cap, the orthorhombic phase of $SiHfO_2$ material is formed and stabilized by the mechanically confining (i.e., capping) effect of TiN top electrode, which mechanically strains the underlying $SiHfO_2$ material. It has been reported that by using such $SiHfO_2$ material as the FE material for an FE memory device, the required thickness of the FE material may be reduced to less than 10 nm.

U.S. Patent 8,304823, issued November 6, 2012 to Boescke, discloses a method for manufacturing a ferroelectric memory cell. An amorphous oxide layer of Hf, Zr or (Hf, Zr) is formed over a carrier, and then a covering layer is formed on the amorphous oxide layer. Upon heating the amorphous oxide layer up to a temperature above its crystallization temperature in the confinement of covering layer (i.e., mechanical capping), at least part of

the amorphous oxide layer alters its crystal state from amorphous to crystalline, resulting in a crystallized oxide layer that is suitable as a FE material for an FE memory cell.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a 1T-FeRAM memory cell in accordance with an embodiment of the present disclosure;

FIG. 2 is a cross-sectional view of a 1T-FeRAM memory cell in accordance with another embodiment of the present disclosure;

FIG. 3 is a cross-sectional view of a 1T-FeRAM memory cell in accordance with yet another embodiment of the present disclosure;

FIG. 4A is a cross-sectional view of a 1T-FeRAM memory cell like that of FIG. 1 in a quiescent state, wherein the voltages of Vd, Vg, Vs, and Vb are set to 0 V;

FIG. 4B is a cross-sectional view of a 1T-FeRAM memory cell like that of FIG. 1 in a "write 0" operational state, wherein the gate voltage Vg is set to above 0 V, and Vd, Vs, Vb are set to 0 V;

FIG. 4C is a cross-sectional views of a 1T-FeRAM memory cell like that of FIG. 1 in a "write 1" operational state, wherein the gate voltage Vg is set to below 0 V, and Vd, Vs, Vb are set to 0 V;

FIG. 5 is a cross-sectional view of a 1T-1C FeRAM memory cell in accordance with another embodiment of the present disclosure; and

FIG. 6 is a simplified plan view of a portion of a FeRAM memory cell array in accordance with an embodiment of the present disclosure.

MODE(S) FOR CARRYING OUT THE INVENTION

Semiconductor structures are disclosed that include a ferroelectric material comprising a polar and chiral crystal structure without inversion symmetry about an inversion center, wherein the ferroelectric (FE) crystalline material does not consist essentially of an oxide of at least one of hafnium (Hf) and zirconium (Zr). The ferroelectric crystalline material may be doped, mechanically strained, or both to prevent formation of inversion symmetry through an inversion center. Also disclosed are methods of forming a semiconductor structure that includes such ferroelectric material, and related semiconductor devices.

The following description provides specific details, such as material types, material thicknesses, and processing conditions in order to provide a thorough description of embodiments of the disclosure. However, a person of ordinary skill in the art will understand that the embodiments of the disclosure may be practiced without employing these specific details. Indeed, the embodiments of the disclosure may be practiced in conjunction with conventional fabrication techniques employed in the industry. In addition, the description provided herein does not form a complete process flow for forming a semiconductor device structure, and each of the semiconductor device structures described below do not form a complete semiconductor device. Only those process acts and structures necessary to understand the embodiments of the disclosure are described in detail below. Additional acts to form a complete semiconductor device may be performed by conventional fabrication techniques. Also note, any drawings accompanying the present application are for illustrative purposes only, and are thus not drawn to scale. Additionally, elements common between figures may retain the same numerical designation.

As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise.

As used herein, relational terms, such as "top," "bottom," "over," "under," etc., are used for clarity and convenience in understanding the disclosure and accompanying drawings and do not connote or depend on any specific preference, orientation, or order, except where the context clearly indicates otherwise.

As used herein, the term "substrate" means and includes a foundation material or construction upon which components, such as those within a semiconductor device structure are formed. The substrate may be a semiconductor substrate, a base semiconductor material on a supporting structure, a metal electrode, or a semiconductor substrate having one or more materials, structures, or regions formed thereon. The substrate may be a conventional silicon substrate or other bulk substrate including a semiconductive material. As used herein, the term "bulk substrate" means and includes not only silicon wafers, but also silicon-on-insulator ("SOI") substrates, such as silicon-on-sapphire ("SOS") substrates or silicon-on-glass ("SOG") substrates, epitaxial layers of silicon on a base semiconductor foundation, or other semiconductor or optoelectronic materials, such as silicon-germanium ($Si_{1-x}Ge_x$, where x is, for example, a mole fraction between 0.2 and 0.8), germanium (Ge), gallium arsenide (GaAs), gallium nitride (GaN), or indium phosphide (InP), among others. Furthermore, when reference is

made to a "substrate" in the following description, previous process stages may have been utilized to form materials, regions, or junctions in or on the base semiconductor structure or foundation.

The disclosed ferroelectric materials may be suitable for FeRAM devices. As non-limiting examples, the FeRAM devices may include, but not limited to, a 1T-1C (1 Transistor-1 Capacitor) FE memory cell, or a 1T (1 Transistor) FE memory cell based on a ferroelectric field effect transistor (FeFET).

FIGS. 1–4 show non-limiting examples of 1T-FeRAM memory cells, and FIG. 5 shows a non-limiting example of 1T-1C FeRAM memory cell.

FIG. 1 shows a non-limiting example of the disclosed 1T-FeRAM (FeFET) memory cell that is structurally similar to metal-oxide-semiconductor field-effect transistor (MOSFET) with the linear dielectric oxide material replaced by the disclosed FE crystalline material. The 1T-FeRAM memory cell 100 includes a substrate 102, a source 104, a drain 106, a FE crystalline material 140 over the substrate 102, and a gate electrode material 160 over the FE crystalline material 140.

The FE crystalline material 140 may include a polar and chiral crystal structure without inversion symmetry through an inversion center, wherein the ferroelectric crystalline material does not consist essentially of an oxide of at least one of hafnium (Hf) and zirconium (Zr).

Upon crystallization, the FE crystalline material 140 may form polycrystalline microstructrues, wherein at least some grains or crystals within the polycrystalline microstructure have ferroelectric properties. Some grains or crystals within the polycrystalline microstructure may not exhibit ferroelectric properties. In general, the polar, chiral, non-centro-symmetric phase or phases exhibit ferroelectric characteristics.

In some embodiments, the FE crystalline material 140 may comprise a polar, chiral, non-centro-symmetric phase selected from the group consisting of orthorhombic, tetragonal, cubic, monoclinic, triclinic, trigonal, and hexagonal phases.

In some embodiments, the FE crystalline material 140 may comprise a polar, chiral, non-centro-symmetric phase selected from the group consisting of orthorhombic and tetragonal phases.

In some embodiments, the FE crystalline material 140 may comprise a non-centro-symmetric orthorhombic structure corresponding to a space group selected from the group consisting of $Pca2_1$, $Pbc2_1$, $Pmc2_1$, $Pmn2_1$, and $Pna2_1$.

Non-limiting examples of the FE crystalline materials 140 having a non-centro-symmetric orthorhombic structure corresponding to $Pca2_1$ space group may include, but not limited to, $V_2P_2O_9$, $K_3Mo_3ScO_{12}$, $BaYCo_4O_8$, $CaNa_2Al_4Si_4O_{16}$, or $LaNa_3V_2O_8$.

Non-limiting examples of the FE crystalline materials 140 having a non-centro-symmetric orthorhombic structure corresponding to $Pbc2_1$ space group may include, but not limited to, $V_2P_2O_9$, $K_3Mo_3ScO_{12}$, $BaYCo_4O_8$, $CaNa_2Al_4Si_4O_{16}$, or $LaNa_3V_2O_8$.

Non-limiting examples of the FE crystalline materials 140 having a non-centro-symmetric orthorhombic structure corresponding to $Pmc2_1$space group may include, but not limited to, $SnGa_4Se_7$, SeO_2, $Ti_xTa_yLa_zO_{11}$ where x+y+z = 3, or $In_{11}Mo_{40}O_{62}$. In one embodiment, the FE crystalline material 140 having a non-centro-symmetric orthorhombic structure corresponding to $Pmc2_1$ space group may be $Ti_{1.92}Ta_{1.08}La_3O_{11}$.

Non-limiting examples of the FE crystalline materials 140 having a non-centro-symmetric orthorhombic structure corresponding to $Pmn2_1$ space group may include, but not limited to, $TiSO_5$, V_2O_5, $Sr_5Nb_5O_{16}$, or $ZrMo_2O_8$.

Non-limiting examples of the FE crystalline materials 140 having a non-centro-symmetric orthorhombic structure corresponding to $Pna2_1$ space group may include, but not limited to, $Si_2Y_2O_7$, $Sr_2P_2O_7$, or $Ti_{0.98}Zr_{0.02}RbPO_5$.

In some embodiments, the FE crystalline material 140 may comprise a non-centro-symmetric tetragonal structure corresponding to a space group selected from the group consisting of P422, $P42_12$, $P4_122$, $P4_12_12$, $P4_222$, $P4_22_12$, $P4_322$, and $P4_32_12$.

In some embodiments, the FE crystalline material 140 may be at least substantially free of zirconium and hafnium.

In some embodiments, the FE crystalline material 140 may be doped, mechanically strained, or both to prevent formation of inversion symmetry through an inversion center.

In some embodiments, the FE crystalline material 140 may further comprise a ternary or quaternary oxide material selected from the group consisting of $Ti_{1.1}Zr_{0.893}Hf_{0.008}O_4$, $Ti_{1.92}Ta_{1.08}La_3O_{11}$, $Sr_5Nb_5O_{16}$, $ZrMo_2O_8$, $Si_2Y_2O_7$, and$Ti_{0.98}Zr_{0.02}RbPO_5$.

In some embodiments, the FE crystalline material 140 may include at least one dopant selected from the group consisting of yttrium (Y), lanthanum (La), gadolinium (Gd), niobium (Nb), tantalum (Ta), vanadium (V), phosphorus (P), potassium (K), scandium (Sc), rubidium (Rb), selenium (Se), tin (Sn), magnesium (Mg), calcium (Ca), barium (Ba), and indium (In).

The dopants included in the FE crystalline/polycrystalline material may be utilized to increase the endurance of FE memory cell, lower the coercive-field/voltage (Ec/Vc), modulate the capacitance/dielectric constant and its frequency response, enhance the redox resistance at the interfaces or in the relative bulk, reduce the oxygen vacancy generation/migration and redistribution, as well as to stabilize the FE phase leading to increased remnant/spontaneous polarization.

In some embodiments, the FE crystalline material 140 may comprise a high-k dielectric material doped with at least one metal selected from the group consisting of gadolinium (Gd), lanthanum (La), vanadium (V), phosphorus (P), potassium (K), scandium (Sc), rubidium (Rb), selenium (Se), tin (Sn), magnesium (Mg), calcium (Ca), barium (Ba), and indium (In). The high-k dielectric material comprises hafnium oxide (HfO_x), zirconium oxide (ZrO_x), titanium oxide (TiO_x), hafnium titanium oxide ($HfZrO_x$), hafnium titanium oxide ($HfTiO_x$), or hafnium silicon oxide ($HfSiO_x$). The FE crystalline material 140 may comprise the at least one metal in an amount between about 0.5% and about 30% by weight.

In one embodiment, the FE crystalline material 140 may comprise a high-k dielectric material doped with yttrium (Y), wherein high-k dielectric material comprises hafnium oxide (HfO_x), zirconium oxide (ZrO_x), titanium oxide (TiO_x), hafnium titanium oxide ($HfZrO_x$), hafnium titanium oxide ($HfTiO_x$), or hafnium silicon oxide ($HfSiO_x$). The FE crystalline material 140 may comprise Y in an amount between about 0.5% and about 25% by weight.

In one embodiment, the FE crystalline material 140 may comprise a high-k dielectric material doped with strontium (Sr), wherein high-k dielectric material comprises hafnium oxide (HfO_x), zirconium oxide (ZrO_x), titanium oxide (TiO_x), hafnium titanium oxide ($HfZrO_x$), hafnium titanium oxide ($HfTiO_x$), or hafnium silicon oxide ($HfSiO_x$). The FE crystalline material 140 may comprise Sr in an amount between about 0.05% and about 20% by weight.

In one embodiment, the FE crystalline material 140 may comprise a high-k dielectric material doped with at least one of niobium (Nb) and tantalum (Ta), wherein high-k dielectric material comprises hafnium oxide (HfO_x), zirconium oxide (ZrO_x), titanium oxide (TiO_x), hafnium titanium oxide ($HfZrO_x$), hafnium titanium oxide ($HfTiO_x$), or hafnium silicon oxide ($HfSiO_x$). At least one of Nb and Ta may be present in the FE crystalline material 140 in an amount between about 0.2% and about 10% by weight.

The FE crystalline material 140 may be formed over the substrate 102 by any conventional techniques. Non-limiting examples of the conventional techniques may include, but not limited to, atomic layer deposition (ALD), metal organic atomic layer deposition (MOALD), chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), and physical vapor deposition (PVD).

In some particular embodiments, the FE crystalline material 140 may be formed over the substrate 102 by ALD or MOALD process based on the precursors of the FE metal oxide, oxidant, and, optionally, the dopant capable of interrupting the inversion symmetry of FE metal oxide. The ALD or MOALD process may be performed at a temperature between about 150°C and about 350°C, and a pressure between about 10 mtorr and about 10 torr.

Various known oxidants may be used for the process. By way of non-limiting examples, the oxidant may include, but not limited to, water vapor (H_2O), hydrogen peroxide (H_2O_2), ozone (O_3), or oxygen (O_2).

When the FE crystalline material 140 comprises Zr-based material, the FE crystalline material 140 may be formed by ALD process based on any known Zr-precursors. Non-limiting examples of Zr-precursors may include, but not limited to, $ZrCl_4$, $C_8H_{24}N_4Zr$, or $(C_5H_5)Zr[N(CH_3)_2]_3$.

When the FE crystalline material 140 comprises Hf-based material, the FE crystalline material 140 may be formed by ALD process based on any known Hf precursors. Non-limiting examples of Hf-precursors may include, but not limited to, $HfCl_4$, $C_8H_{24}N_4Hf$, or $(C_5H_5)Hf[N(CH_3)_2]_3$.

When the FE crystalline material 140 comprises Ti-based material, the FE crystalline material 140 may be formed by ALD process based on any known Ti precursors. Non-limiting examples of Ti-precursors may include, but not limited to, $TiCl_4$, $C_8H_{24}N_4Ti$, or $(C_5H_5)Ti[N(CH_3)_2]_3$.

When the FE crystalline material 140 comprises a dopant, the amount of dopant in the FE crystalline material 140 may be defined by varying the cycle ratio of the precursors. The content of dopant may be monitored and determined by any conventional techniques and, therefore is not described in detail herein. Non-limiting examples of such techniques may include, but not limited to, secondary ions mass spectrometry, X-ray photoelectron spectroscopy (XPS), high resolution transmission spectroscopy (HR-TEM), etc. In some embodiments, the amount of dopant in the FE crystalline material 140 may be in a range of

about 0.05% to about 30% by weight. The amount of dopant may depend on the thickness of FE crystalline material 140, the process temperature of 140 or top electrode 160, or the annealing conditions such as post metallization annealing (PMA) conditions. For example, when increasing the thickness of FE crystalline material 140, the amount of dopant may also have to be increased to achieve a desired crystallization having ferroelectric properties.

In some embodiments, the thickness of FE crystalline material 140 may be in a range of about 1 nm to about 100 nm. In some embodiments, the thickness of FE crystalline material 140 may be in a range of about 2 nm to about 20 nm.

The gate electrode material 160 may be formed over the FE crystalline material 140 to provide the semiconductor structure 100. The gate electrode material 160 may be formed over the FE crystalline material 140 by any conventional techniques. Non-limiting examples of such conventional techniques may include, but not limited to, atomic layer deposition (ALD), plasma enhanced atomic layer deposition (PE-ALD), atomic vapor deposition (AVD), ultraviolet assisted atomic layer deposition (UV-ALD), chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), or physical vapor deposition (PVD).

Any conventional gate electrode material may be used for the gate electrode material 160. Such materials may comprise an elemental metal, an alloy of two or more elemental metals, a conductive metal compound, a conductively-doped semiconductor material, or mixtures thereof. Non-limiting examples may include, but not limited to, TiN, TiCN, TiAlN, TiAlCN, Ti-W, Ru-TiN, or RuCN.

Accordingly, the present disclosure describes a ferroelectric memory device including a plurality of memory cells. Each of the memory cells comprises at least one electrode and a ferroelectric crystalline material disposed proximate the at least one electrode. The ferroelectric crystalline material is polarizable by an electric field generated by the at least one electrode in an electrically charged state. The ferroelectric crystalline material has a polar and chiral crystal structure without inversion symmetry through an inversion center. The ferroelectric crystalline material comprises a material selected from the group consisting of hafnium oxide (HfO_x), zirconium oxide (ZrO_x), titanium oxide (TiO_x), hafnium zirconium oxide ($HfZrO_x$), hafnium titanium oxide ($HfTiO_x$), and hafnium silicon oxide ($HfSiO_x$). The ferroelectric crystalline material further comprises least one dopant selected from the group consisting of yttrium (Y), strontium (Sr), niobium (Nb), tantalum (Ta), lanthanum (La), gadolinium (Gd),vanadium (V), phosphorus (P),

potassium (K), scandium (Sc), rubidium (Rb), selenium (Se), tin (Sn), magnesium (Mg), calcium (Ca), barium (Ba), and indium (In).

Furthermore, the present disclosure describes a method of forming a semiconductor structure. The method comprises forming a ferroelectric crystalline material over a substrate, and forming at least one electrode proximate the ferroelectric crystalline material. The ferroelectric crystalline material has a polar and chiral crystal structure without inversion symmetry through an inversion center. The ferroelectric crystalline material does not consist essentially of an oxide of at least one of hafnium (Hf) and zirconium (Zr).

In some embodiments, the method may further comprise annealing the ferroelectric crystalline material and altering a crystal structure of the ferroelectric crystalline material.

The FE crystalline material 140 may be annealed to initiate the crystallization into the desired ferroelectric phase. The annealing of FE crystalline material 140 into the desired ferroelectric phase may be performed by post deposition annealing (PDA) or post metallization annealing (PMA) process.

In the PDA process, the FE crystalline material 140 is annealed into the desired ferroelectric phase prior to the formation of the gate electrode material 160 over the FE crystalline material 140.

In the PMA process, the FE crystalline material 140 is annealed into the desired ferroelectric phase after the gate electrode material 160 is formed over the FE crystalline material 140. In some embodiments, the PMA annealing may be performed by a rapid thermal processing (RTP) annealing technique under ambient nitrogen (N_2) or argon (Ar) condition.

Thus, in some embodiments, the method may further comprise mechanically straining the ferroelectric crystalline material to stabilize the polar and chiral crystal structure of the ferroelectric crystalline material.

Whether the FE crystalline material 140 is annealed by PDA or PMA process depends on various factors, including, but not limited to, the types of high-k dielectric material, the types and amounts of dopants, or the desired structures of FE crystalline phase.

The PDA or PMA annealing conditions may be defined based on various controlling factors. By non-limiting examples, such controlling factor may include, but not limited to, the composition of FE crystalline material 140, the thickness of FE crystalline

material 140, and the composition and thickness of electrode material 160 overlying the FE crystalline material 140 (in case of PMA process). The relatively thinner FE crystalline/polycrystalline material 140 may require a higher annealing temperature and longer annealing times. The annealing requirement is strongly dependent on the choice of FE material 140, such that, in some embodiments of present disclosure, the post metallization anneal may be eliminated, with only a post deposition anneal sufficing. In addition to the thickness of FE crystalline/polycrystalline material 140 and/or electrode material 160, the substrate induced stress may play an important role and may significantly influence the annealing conditions

When the FE crystalline material 140 comprises at least one dopant, the annealing conditions of the FE crystalline material 140 may also be a function of the amount and type of dopant present in the FE crystalline material 140. At relatively higher dopant concentrations, the annealing temperature of the FE crystalline material 140 may be higher than the annealing temperature of the FE crystalline material 140 having a lower amount of the dopant.

In the embodiments wherein the FE crystalline material 140 comprises at least one doped metal selected from the group consisting of gadolinium (Gd), lanthanum (La), vanadium (V), phosphorus (P), potassium (K), scandium (Sc), rubidium (Rb), selenium (Se), tin (Sn), magnesium (Mg), calcium (Ca), barium (Ba), and indium (In), the annealing of the FE crystalline material 140 may be achieved by PMA annealing at a temperature between about 500°C and about 800°C for about 20 seconds to about 600 seconds.

When the FE crystalline material 140 comprises a high-k dielectric material doped with yttrium (Y), the annealing of the FE crystalline material 140 may be achieved by post deposition annealing (PDA) or post metallization annealing (PMA) at a temperature between about 450°C and about 800°C for about 20 seconds to about 600 seconds.

When the FE crystalline material 140 comprises a high-k dielectric material doped with strontium (Sr), the annealing of the FE crystalline material 140 may be achieved by PMA annealing at a temperature between about 450°C and about 800°C for about 20 seconds to about 600 seconds.

When the FE crystalline material 140 comprises a high-k dielectric material doped with at least one of niobium (Nb) and tantalum (Ta), the annealing of the FE crystalline material 140 may be achieved by PMA annealing at a temperature between about 450°C and about 800°C for about 20 seconds to about 300 seconds.

Accordingly, the present disclosure describes a method of forming a semiconductor structure. The method comprises forming a ferroelectric crystalline material over a substrate. The ferroelectric crystalline material has a polar and chiral crystal structure without inversion symmetry through an inversion center. The ferroelectric crystalline material is selected from the group consisting of hafnium oxide (HfO_x), zirconium oxide (ZrO_x), titanium oxide (TiO_x), hafnium zirconium oxide ($HfZrO_x$), hafnium titanium oxide ($HfTiO_x$), and hafnium silicon oxide ($HfSiO_x$). The ferroelectric crystalline material is doped with at least one dopant selected from the group consisting of yttrium (Y), strontium (Sr), niobium (Nb), tantalum (Ta), lanthanum (La), gadolinium (Gd),vanadium (V), phosphorus (P), potassium (K), scandium (Sc), rubidium (Rb), selenium (Se), tin (Sn), magnesium (Mg), calcium (Ca), barium (Ba), and indium (In). The method further comprises forming at least one electrode proximate the ferroelectric crystalline material.

In some embodiments, the FE crystalline material 140 may be annealed and crystallized into a stable ferroelectric crystalline phase, without requiring the capping effect to stabilize such ferroelectric crystalline phase. By way of a non-limiting example, such stable ferroelectric crystalline phase may be orthorhombic $Pbc2_1$ phase. Accordingly, in such embodiments, the crystallization of FE crystalline material 140 is not necessarily performed in the presence of mechanical confinement (capping) such as those described in U.S. Patent 8,304,823 wherein crystallization of FE crystalline material must be performed in the presence of a covering layer.

Thus, in some embodiments, the method of forming a semiconductor structure comprises crystallizing the FE crystalline material 140 into a ferroelectric phase without the presence of capping.

The FE crystalline material 140 may be patterned before crystallizing into the desired ferroelectric phase. Alternatively, the FE crystalline material 140 may be crystallized into the desired ferroelectric phase prior to or at the same time as patterning the FE crystalline material 140. The patterning of the FE crystalline material 140 may be adapted to the intended use of such FE crystalline material 140. By way of non-limiting examples, the FE crystalline material 140 may be patterned to define at least part of a gate stack of a 1T-FeRAM (FeFET) or to define a capacitor dielectric material of 1T-1C FeRAM.

FIG. 2 shows another non-limiting example of the disclosed 1T-FeRAM (FeFET) memory cell. 1T-FeRAM memory cell 200 includes a substrate 202, a source 204, a

drain 206, a FE crystalline material 240 over the substrate 202, an insulating buffer material 220 between the substrate 202 and the FE crystalline material 240, and a gate electrode material 260 over the FE crystalline material 240. In some embodiments, the insulating buffer material 220 may include a crystallized material that is compatible with the substrate 202 and the FE crystalline material 240. In some embodiments, the insulating buffer material may be silicon oxide, such as SiO_2, or silicon oxynitride (SiON). In some embodiments, the thickness of the insulating buffer material 220 may be in a range between about 0.3 nm to about 6 nm. In some embodiments, the thickness of the insulating buffer material 220 may be in a range between about 0.05 nm to about 3 nm.

FIG. 3 shows yet another non-limiting example of the disclosed 1T-FERAM (FeFET) memory cell. 1T-FeRAM memory cell 300 includes a substrate 302, a source 304, a drain 306, a FE crystalline material 340 over the substrate 302, an insulating buffer material 320 between the substrate 302 and the FE crystalline material 340, a gate electrode material 360 over the FE crystalline material 340, and an interfacial material 350 between the FE crystalline material 340 and the gate electrode material 360.

Accordingly, the present disclosure describes a ferroelectric memory cell. The ferroelectric memory cell comprises a ferroelectric crystalline material having a polar and chiral crystal structure without inversion symmetry through an inversion center. The ferroelectric crystalline material does not consist essentially of an oxide of at least one of hafnium (Hf) and zirconium (Zr).

FIGS. 4A–4C illustrate cross-sectional views of the 1T-FeRAM memory cell 400 that comprises a substrate 402, a source 404, a drain 406, a FE crystalline material 440 over the substrate 402, and a gate electrode material 460 over the FE crystalline material 440. The gate electrode material 460 is coupled to a gate voltage Vg; the source 404 is coupled to a source voltage Vs; the drain 406 is coupled to a drain voltage Vd; and a bulk region including source/drain 404/406 embedded therein is coupled to a bulk voltage Vb.

FIG. 4A shows the 1T-FeRAM memory cell 400 in a quiescent state, wherein the voltages of Vd, Vg, Vs, and Vb are set to zero (0) volt (V).

FIG. 4B shows the 1T-FeRAM memory cell 400 in a "write 0" operational state. The binary information state "0" is written to the 1T-FeRAM memory cell 400 by setting the gate voltage Vg to above 0 V, and setting Vd, Vs, Vb to 0 V. Hence, an electric field between the bulk (402, 404, 406) and the gate electrode 460 turns the FE crystalline material 440 to a first polarization state 440B that is associated with the information state

"0." For example, as shown in FIG. 4B, the FE crystalline material 440B polarizes such that its dipole moment has a downward arrow direction. When the applied voltage is removed, the polarization state "0" is preserved.

FIG. 4C shows the 1T-FeRAM memory cell 400 in a "write 1" operation state. By setting gate voltage Vg to below 0 V and Vd, Vs, Vb to 0 V, the electric field between the bulk (402, 404, 406) and the gate electrode 460 is reversed and operational state "write 1" is set. In this operation state, the FE crystalline material 440 is set into a second polarization state 440C that is associated with binary information state "1" and is opposite from the first polarization state 400B. For example, as shown in FIG. 4C, the FE crystalline material 440C polarizes such that its dipole moment has an upward arrow direction. When the applied voltage is removed, the reversed polarization state "1" remains in the FE crystalline material.

Thus, operational states "0" and "1" may be ascribed to different polarization states (440B, 440C) of the FE crystalline material 440. These different polarization states (440B, 440C) result in different threshold voltages of the 1T-FeRAM device.

Under a "read" operational state, the information is read from the 1T-FeRAM memory cell 400 by sensing the current between the source 404 and the drain 406. Read-out from the 1T-FeRAM memory cell 400 may be non-destructive.

FIG. 5 shows a non-limiting example of the disclosed 1T-1C FeRAM memory cell, similar in construction to a DRAM memory cell, wherein one capacitor and one access transistor form a memory cell. While the dielectric material of DRAM cell capacitor is a linear dielectric material, the dielectric material of FeRAM cell capacitor includes a ferroelectric dielectric material.

As shown in FIG. 5, the 1T-1C FeRAM memory cell 500 includes a source 504 and a drain 506 formed within a substrate 502, a conventional transistor acting as an access transistor and comprising a linear dielectric material 545 and a gate electrode 560, and a capacitor 510 coupled to the drain 506 via an interconnection structure 570 (e.g., a contact plug). The capacitor 510 comprises a bottom electrode 590, a top electrode 595, and a FE crystalline material 540 between the bottom and top electrodes 590, 595.

The FE crystalline material 540 may be formed over the bottom electrode 590 using the methods as described earlier for the FE crystalline material 140 of FIG.1. The crystallization of FE crystalline material 540 into the desired ferroelectric phase may be performed before forming a top electrode 595 over the FE crystalline material 540.

Alternatively, the crystallization of FE crystalline material 540 into the desired ferroelectric phase may be performed after or at the same time as forming a top electrode 595 over the FE crystalline material 540.

The bottom and top electrodes 590, 595 may be any conventional electrode materials. The bottom and top electrodes 590, 595 may be formed of the same or different materials. The bottom electrode 590 may be formed as a continuous material, such as at a thickness ranging from about 20 Å to about 200 Å, from about 50 Å to about 130 Å, or from about 40 Å to about 70 Å. In some embodiments, the bottom electrode 590 has a thickness of about 60 Å.

While FIGS. 1–5 show 1T-FeRAM (FeFET) and 1T-1C FeRAM memory cells, it is understood that the present disclosure may be applied to any suitable types of FE memory cells (e.g., 2T-2C FeRAM memory cells). Furthermore, additional acts to form a complete FeRAM device may be performed by conventional fabrication techniques.

The disclosed FE crystalline materials may exhibit significantly higher remnant polarization (*Pr*) than perovskite materials that are conventionally used as the FE materials for FE memory devices. Thus, the disclosed FE crystalline materials may be suitable for various FE memory device applications. By way of non-limiting examples, the disclosed FE crystalline materials may be used for FERAM devices, or FeFET devices for NAND and NOR applications.

The disclosed FE crystalline materials may satisfy the properties required for use in the FE memory devices, such as high polarization, fast switching speeds, low coercive field, high retention, low fatigue, and low imprint, because of their intrinsic microscopic structure. In addition, these FE crystalline materials may fulfill the extrinsic fabrication requirements, such as low processing temperature, good CMOS compatibility, ease of availability, lower cost, better scalability, etc.

It is to be understood that the cross-sectional views of FeRAM memory cells 100, 200, 300, 400, and 500, illustrated in FIGS. 1–5, merely refer to part of the semiconductor devices. Therefore, the semiconductor devices may comprise a plurality of FeRAM memory cells arranged in the form of a ferroelectric memory cell array. Furthermore, additional semiconductor structures may be formed in the substrate. By way of non-limiting examples, these additional semiconductor structures may include, but not limited to, word line drive circuits, bit line drive circuits, source line drive circuits, sense circuits, or control circuits.

FIG. 6 shows a non-limiting example of a portion of a FeRAM memory cell array. The FeRAM memory cell array 600 includes a plurality of memory cells 601, a plurality of digit lines 611 (in dashed lines to show they are buried), and a plurality of word lines 612 (in dashed lines to show they are buried). The FeRAM memory cells 601 are arranged in rows (coupled to a common digit line 611) and in columns (coupled to a common word line 612). Individual FeRAM memory cells 601 are located at a cross-point of a digit line 611 and a word line 612.

Accordingly, the present disclosure describes a ferroelectric memory device including a plurality of memory cells. Each of the memory cells comprises at least one electrode and a ferroelectric crystalline material disposed proximate the at least one electrode. The ferroelectric crystalline material is polarizable by an electric field responsive to an electrical charge of the at least one electrode. The ferroelectric crystalline material has a polar and chiral crystal structure without inversion symmetry through an inversion center. The ferroelectric crystalline material does not consist essentially of an oxide of at least one of hafnium (Hf) and zirconium (Zr).

During use and operation, the FE memory cells of present disclosure may exhibit improved cell performance, such as improved cycling, improved data retention, lower ferroelectric coercivity (E_c), and lower electrical field saturation.

The semiconductor structure of present disclosure comprising the FE crystalline material may find applications in integrated circuit other than memory devices.

While the disclosure is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, the disclosure is not intended to be limited to the particular forms disclosed. Rather, the disclosure is to cover all modifications, equivalents, and alternatives falling within the scope of the disclosure as defined by the following appended claims and their legal equivalents.

CLAIMS

1. A ferroelectric memory cell, comprising:

a ferroelectric crystalline material having a polar and chiral crystal structure without inversion symmetry through an inversion center,

wherein the ferroelectric crystalline material does not consist essentially of an oxide of at least one of hafnium (Hf) and zirconium (Zr).

2. The ferroelectric memory cell of claim 1, wherein the ferroelectric crystalline material has an orthorhombic crystal structure corresponding to a space group selected from the group consisting of $Pca2_1$, $Pbc2_1$, $Pmc2_1$, $Pmn2_1$, and $Pna2_1$.

3. The ferroelectric memory cell of claim 2, wherein the orthorhombic crystal structure has a space group selected from $Pca2_1$ and $Pbc2_1$.

4. The ferroelectric memory cell of claim 3, wherein the ferroelectric crystalline material comprises a material selected from the group consisting of $V_2P_2O_9$, $K_3Mo_3ScO_{12}$, $BaYCo_4O_8$, $CaNa_2Al_4Si_4O_{16}$, and $LaNa_3V_2O_8$.

5. The ferroelectric memory cell of claim 2, wherein the orthorhombic crystal structure has a $Pmc2_1$ space group, and the ferroelectric crystalline material comprises a material selected from the group consisting of $SnGa_4Se_7$, SeO_2, $Ti_xTa_yLa_zO_{11}$, where x+y+z = 3, and $In_{11}Mo_{40}O_{62}$.

6. The ferroelectric memory cell of claim 2, wherein the orthorhombic crystal structure has a $Pmn2_1$ space group, and the ferroelectric crystalline material comprises a material selected from the group consisting of $TiSO_5$, V_2O_5, $Sr_5Nb_5O_{16}$, and $ZrMo_2O_8$.

7. The ferroelectric memory cell of claim 2, wherein the orthorhombic crystal structure has a $Pna2_1$ space group, and the ferroelectric crystalline material comprises a material selected from the group consisting of $Si_2Y_2O_7$, $Sr_2P_2O_7$ and $Ti_{0.98}Zr_{0.02}RbPO_5$.

8. The ferroelectric memory cell of claim 1, wherein the ferroelectric crystalline material has a tetragonal crystal structure corresponding to a space group

selected from the group consisting of P422, $P42_12$, $P4_122$, $P4_12_12$, $P4_222$, $P4_22_12$, $P4_322$, and $P4_32_12$.

9. The ferroelectric memory cell of claim 1, wherein the ferroelectric crystalline material includes at least one dopant selected from the group consisting of yttrium (Y), lanthanum (La), gadolinium (Gd), niobium (Nb), tantalum (Ta), vanadium (V), phosphorus (P), potassium (K), scandium (Sc), rubidium (Rb), selenium (Se), tin (Sn), magnesium (Mg), calcium (Ca), barium (Ba), and indium (In).

10. The ferroelectric memory cell of claim 1, wherein the ferroelectric crystalline material comprises a ternary or quaternary oxide material selected from the group consisting of $Ti_{1.1}Zr_{0.893}Hf_{0.008}O_4$, $Ti_{1.92}Ta_{1.08}La_3O_{11}$, $Sr_5Nb_5O_{16}$, $ZrMo_2O_8$, $Si_2Y_2O_7$, and $Ti_{0.98}Zr_{0.02}RbPO_5$.

11. The ferroelectric memory cell of claim 1, wherein the crystal structure of the ferroelectric crystalline material is selected from the group consisting of orthorhombic, tetragonal, cubic, monoclinic, triclinic, trigonal, and hexagonal crystal structures.

12. The ferroelectric memory cell of claim 1, wherein the ferroelectric crystalline material is at least substantially free of zirconium and hafnium.

13. The ferroelectric memory cell of claim 1, wherein the ferroelectric crystalline material is at least one of doped and mechanically strained to prevent formation of inversion symmetry through an inversion center.

14. A ferroelectric memory device including at least one ferroelectric memory cell of claim 1.

15. A ferroelectric memory cell, comprising:

a ferroelectric crystalline material having a polar and chiral crystal structure without inversion symmetry through an inversion center,

wherein the ferroelectric crystalline material is selected from the group consisting of hafnium oxide (HfO_x), zirconium oxide (ZrO_x), titanium oxide (TiO_x), hafnium zirconium oxide ($HfZrO_x$), hafnium titanium oxide ($HfTiO_x$), and hafnium silicon oxide

($HfSiO_x$), the ferroelectric crystalline material further including at least one dopant selected from the group consisting of yttrium (Y), strontium (Sr), niobium (Nb), tantalum (Ta), lanthanum (La), gadolinium (Gd),vanadium (V), phosphorus (P), potassium (K), scandium (Sc), rubidium (Rb), selenium (Se), tin (Sn), magnesium (Mg), calcium (Ca), barium (Ba), and indium (In).

16. The ferroelectric memory cell of claim 15, wherein the crystal structure of the ferroelectric crystalline material is selected from the group consisting of orthorhombic and tetragonal structures.

17. A ferroelectric memory device including at least one ferroelectric memory cell of claim 15.

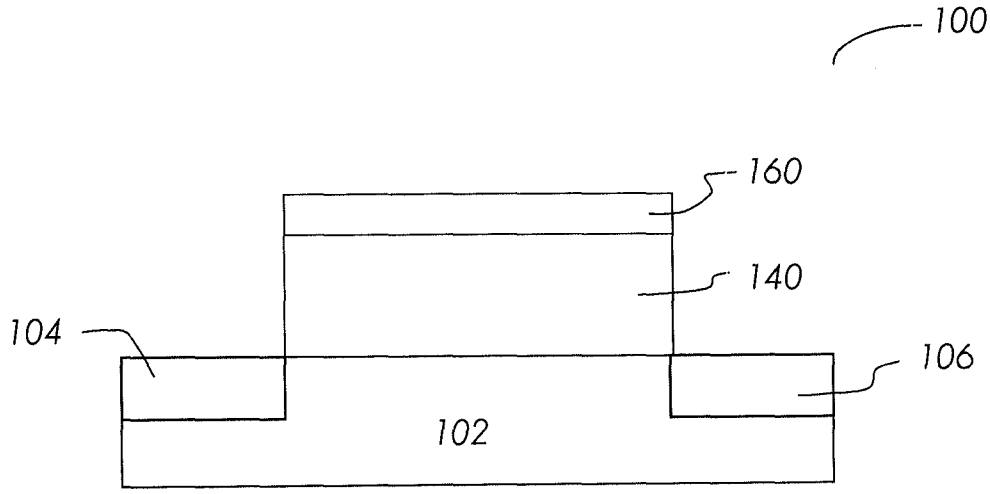


FIG. 1

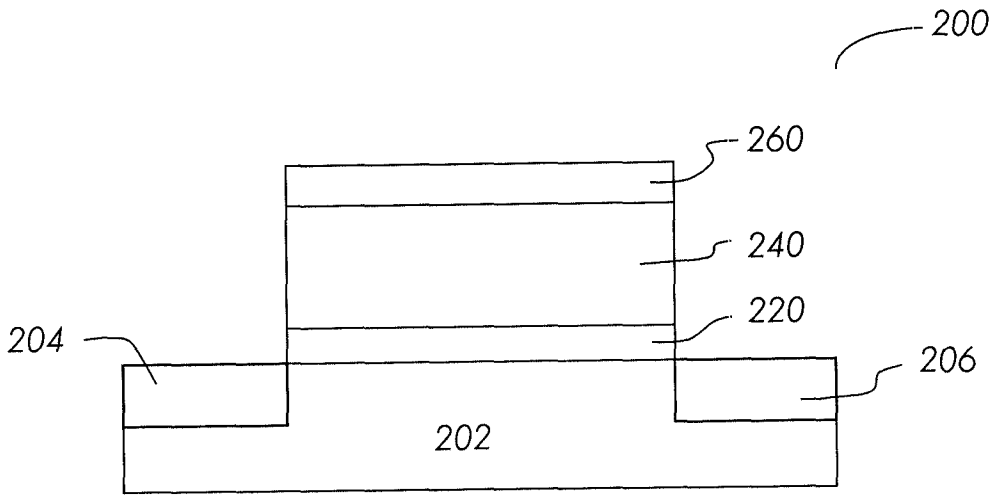


FIG. 2

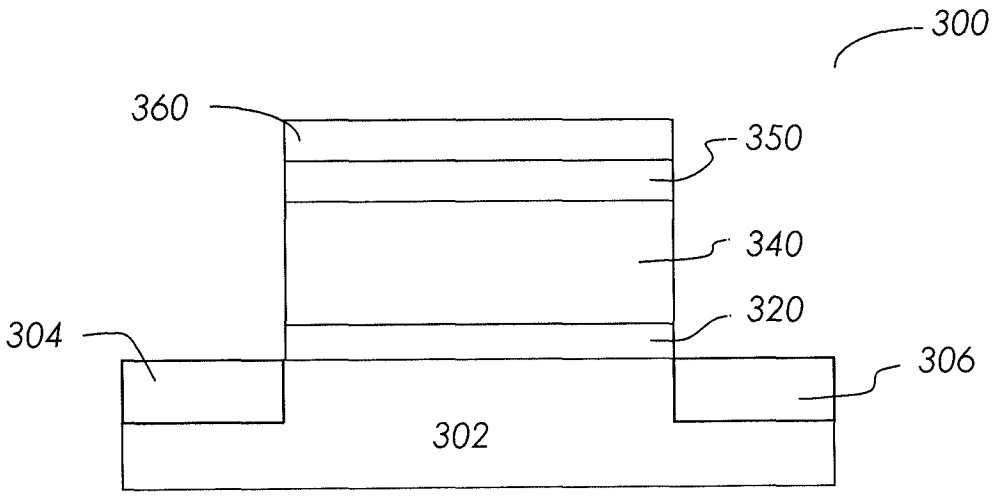

300
360
350
340
320
304
306
302

FIG. 3

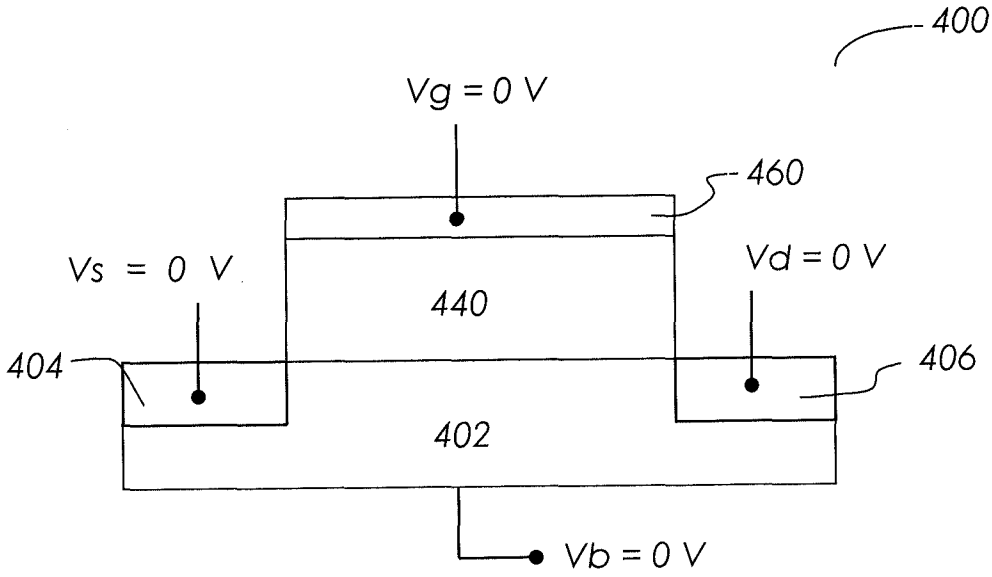

400
Vg = 0 V
460
Vs = 0 V
Vd = 0 V
440
404
406
402
Vb = 0 V

FIG. 4A

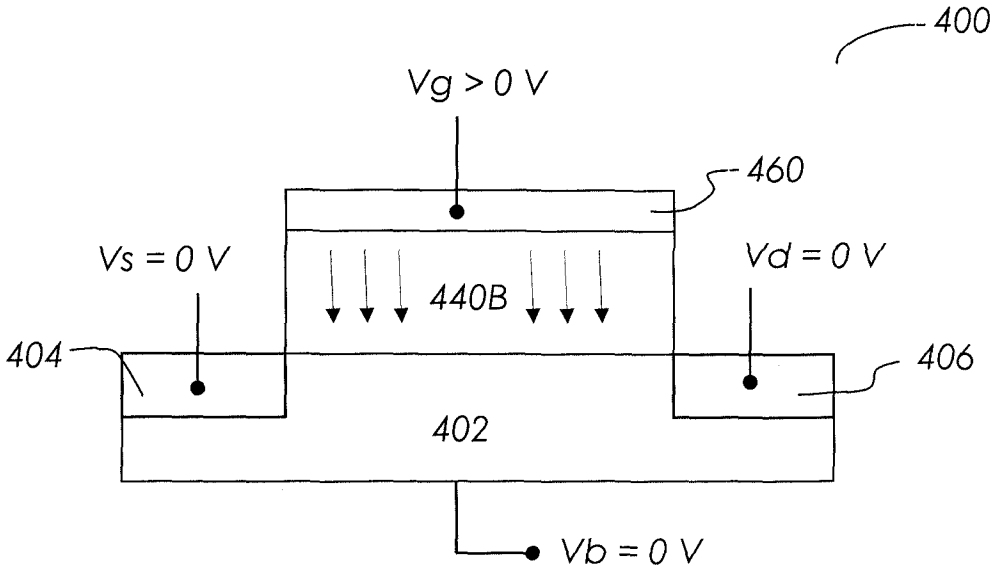

400
Vg > 0 V
460
Vs = 0 V
Vd = 0 V
440B
404
406
402
Vb = 0 V

FIG. 4B

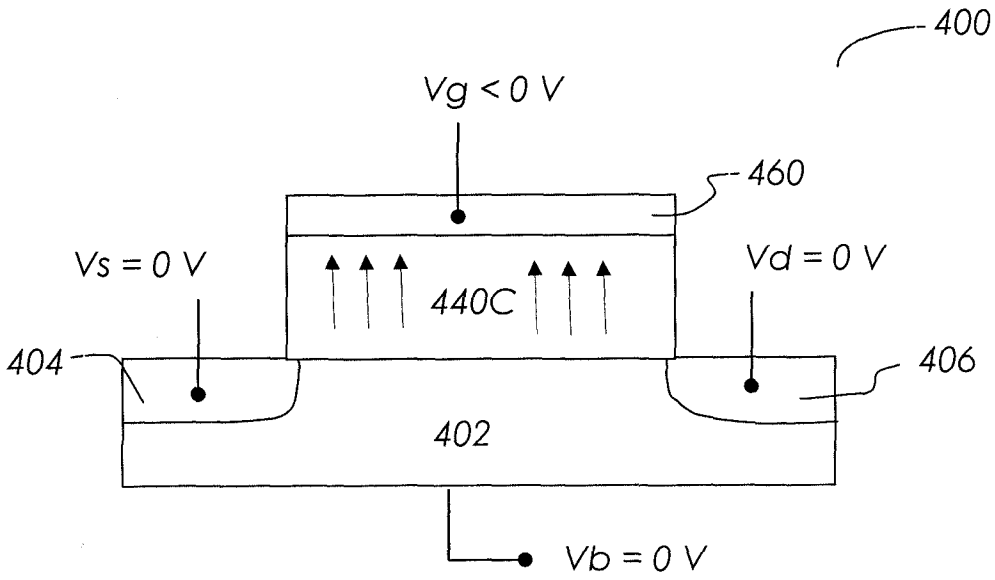

400
Vg < 0 V
460
Vs = 0 V
Vd = 0 V
440C
404
406
402
Vb = 0 V

FIG. 4C

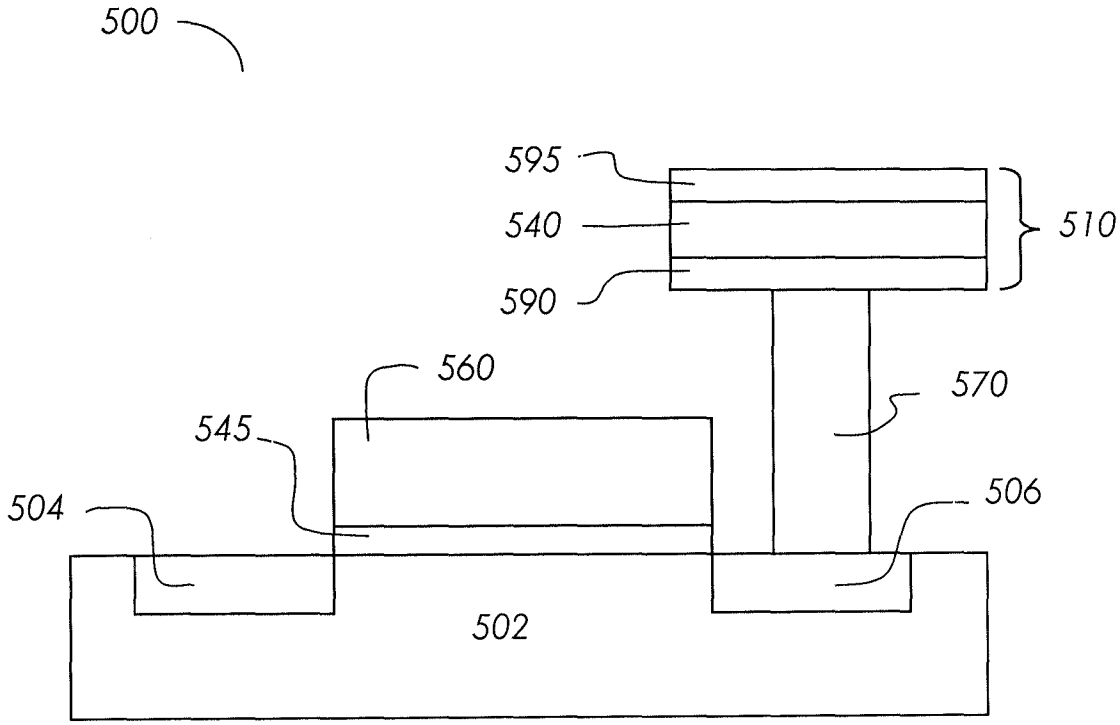


FIG. 5

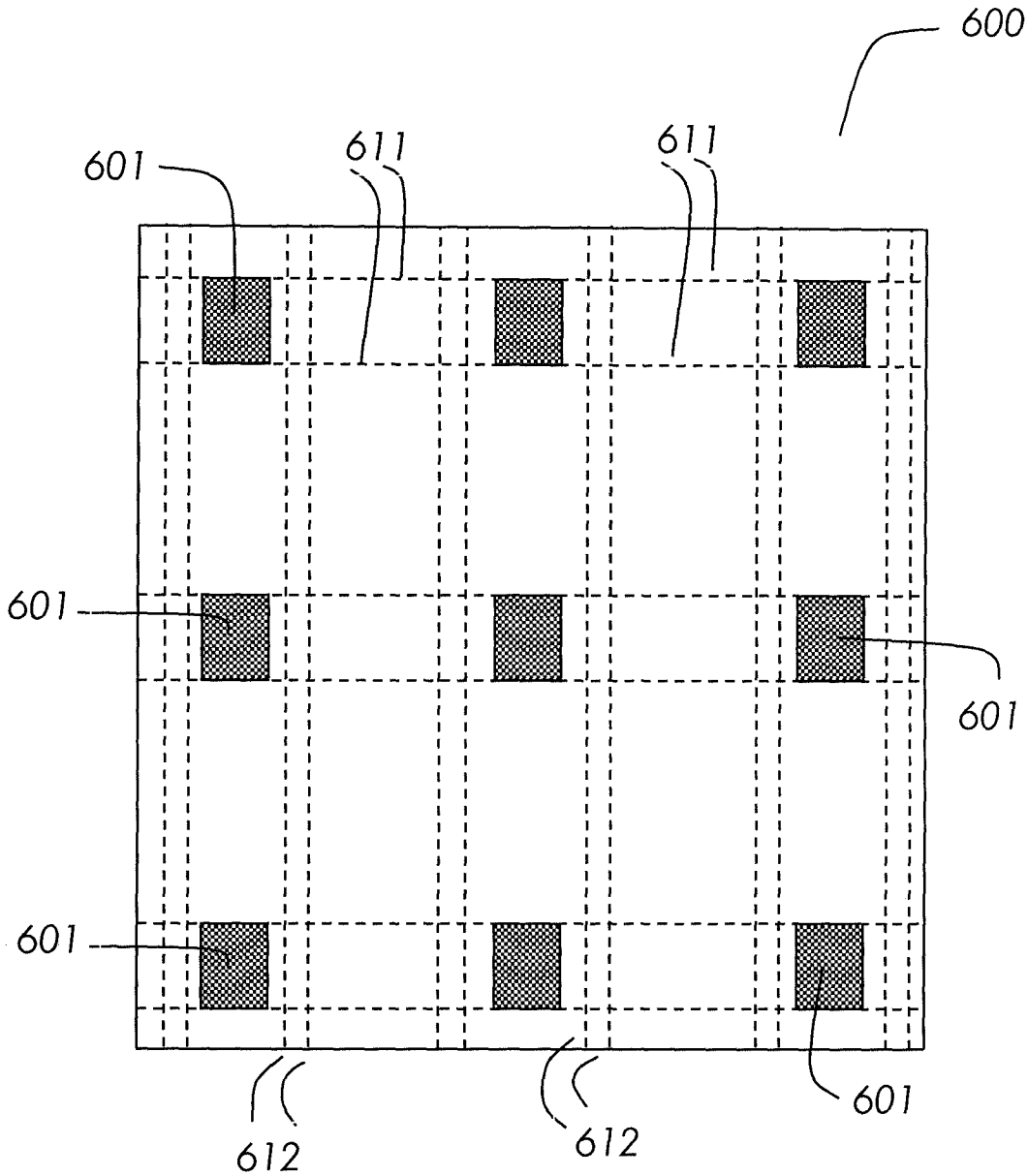


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/027308

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/115(2006.01)i, H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 27/115; H01L 51/30; H01L 43/10; H01L 29/76; A61K 8/19; H01L 49/02; H01L 21/00; H01L 21/768

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: ferroelectric, crystalline, polar, chiral, dopant

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009-0057737 A1 (TIM BOESCKE et al.) 05 March 2009 See abstract, paragraphs [0018]-[0068], claims 9-11 and figures 1A-8.	1,9,11-17
A		2-8,10
A	US 2014-0070289 A1 (KABUSHIKI KAISHA TOSHIBA) 13 March 2014 See abstract, paragraphs [0027]-[0088] and figures 1A-9F.	1-17
A	US 2013-0122722 A1 (JULIE CISSELL et al.) 16 May 2013 See abstract, paragraphs [0013]-[0055] and figure 1.	1-17
A	US 2007-0111335 A1 (HIROMU MIYAZAWA et al.) 17 May 2007 See abstract, paragraphs [0040]-[0100] and figures 1-5.	1-17
A	US 2010-0135937 A1 (STEPHEN O`BRIEN et al.) 03 June 2010 See abstract, paragraphs [0020]-[0073] and figures 1A-3E.	1-17

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 August 2015 (13.08.2015)	**13 August 2015 (13.08.2015)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/027308

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009-0057737 A1	05/03/2009	CN 101645446 A	10/02/2010
		US 7709359 B2	04/05/2010
US 2014-0070289 A1	13/03/2014	JP 2014-053568 A	20/03/2014
US 2013-0122722 A1	16/05/2013	WO 2012-005957 A2	12/01/2012
		WO 2012-005957 A3	12/04/2012
US 2007-0111335 A1	17/05/2007	JP 2005-011931 A	13/01/2005
		JP 3873935 B2	31/01/2007
		US 2005-0017269 A1	27/01/2005
		US 7238978 B2	03/07/2007
		US 7436013 B2	14/10/2008
US 2010-0135937 A1	03/06/2010	WO 2008-118422 A1	02/10/2008