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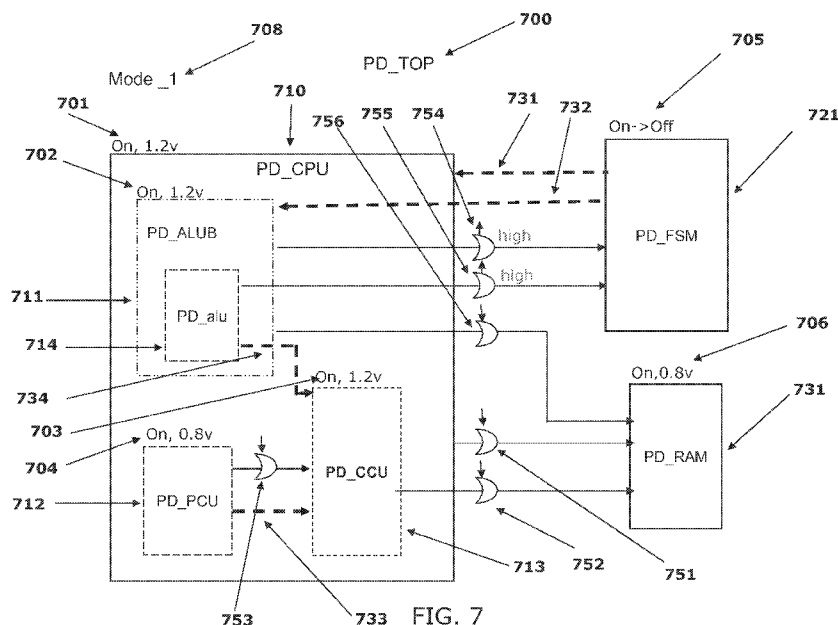
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(54) Title: HIERARCHICAL POWER MAP FOR LOW POWER DESIGN



(57) Abstract: Power information associated with an IC design is displayed graphically and hierarchically using a power map, thereby providing an intuitive way for describing the power distribution among various power domains of the IC and parent-child relationships within the power domains. Each power domain is associated with a power control for controlling the power domain. The status of the power control for each power domain is displayed on the power map. The power map may include a token to set and display current operating mode of the IC design to enable the IC design to be debugged under different operating modes.

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HIERARCHICAL POWER MAP FOR LOW POWER DESIGN

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Patent Application No. 13/718,979,
10 filed December 18, 2012, and entitled "Hierarchical power map for low power
design," which is a continuation-in-part of U.S. Application No. 13/158,471, filed
June 13, 2011, and entitled "Hierarchical power map for low power design," which
claims the benefit of priority of U.S. Provisional Application No. 61/358,002, filed
June 24, 2010, and entitled "Method and system for displaying IC design intent with
15 power domain intent," the contents of all of which are incorporated herein by
reference in their entirety.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to a computer-implemented method for
20 debugging low power integrated circuit (IC) design, and in particular, to a method for
creating an integrated graphic user interface to debug the IC design and provide a map
of its power usage.

[0003] Mobile and consumer electronic devices such as personal mobile computers,
MP3 audio players, notebooks and digital cameras are in wide use. The drive towards
25 low power consumption in increasingly thinner and lighter products require
integration of a number of components on an IC. For example, as more circuits are
integrated on a system-on-chip (SoC) IC to perform increasingly more complex
functions at lower power, the IC becomes more difficult to debug. In many low power
designs, a circuit is divided into many parts, referred to as power domains, each of
30 which may be associated with a power supply. A power domain is a collection of
instances, pins and ports that can share the same power distribution network (voltage).
Some of the power domains can be turned on or off by a power switch. Power

switches are used to turn off unused parts of the design to conserve power consumption.

[0004] An isolation cell is used to isolate signals between two power domains where one is switched on and one is switched off. Such cells are used to isolate
5 signals originating in a power domain that is being switched off. An isolation cell ensures that when a power domain is turned off, its output has a predefined or latched value, thus leaving other active domains unaffected.

[0005] A level shifter is typically required to change one voltage level to another voltage level across different power domains. Therefore, a low power SoC IC, in
10 addition to a number of digital circuits, often includes power network circuitry with a multitude of power components.

[0006] Referring to FIG. 1, a digital circuit design is conventionally implemented in hardware description language (HDL), such as Verilog code 1. The term “power specification” is defined herein as the description of the power intent (intended power
15 behavior) of a circuit design. In order to implement low power network, the power description 2 specified in a power format such as Cadence Common Power Format (CPF) or Unified Power Format (UPF) is generally used to capture the power information so as to allow designers to implement low power network design in a separate file without modifying the Verilog code 1. The power format describes low
20 power intent for design implementation, analysis and verification.

[0007] In order to specify low power design constraints so as to minimize energy consumption, a power supply network is specified to control the distribution of power. Using UPF, one can specify the network at an abstract level. Such a network includes supply ports, supply nets, power switches, and is a high-level abstraction of the
25 electrical network of the power aspect of the chip. Supply ports provide supply interfaces to power domains and switches, whereas supply nets connect supply ports. Since the supply network is specified apart from the logic design, the logic design specification remains independent of power supply network specifications.

[0008] Since traditional hardware description languages (HDL) are not adequate to
30 specify the power design information, a power format, such as UPF, provides a format without changing the existing HDL codes. For instance, UPF provides a command, create_power_domain, for creating a power domain and grouping the design instances

associated with the power domain. Other power components, such as power switches, isolation cells, and level shifters may be created by using the corresponding commands defined by the power formats.

5 [0009] Once the Verilog design and the power design based on the power format are taken into consideration, the IC design can be analyzed and debugged. However, to the extent that a conventional circuit design file is separate from the power network design, to debug a circuit a designer is required to establish a relationship between these two files.

10 [0010] Furthermore, circuit designers are primarily focused on the functionalities of the circuit design and to creat hierarchies based on the functional and logic view of the design. However, power designers prefer to have the design hierarchies in a physical form which can be defined by a power format having a multitude of power domains within the power network design. As a result, it is inefficient and error prone for the designers to debug the entire chip if the low power network design is not
15 viewed in the top level and does not interact with the power designer. A need continues to exist for a more efficient and reliable technique to design low power circuits.

BRIEF SUMMARY OF THE INVENTION

20 [0011] In accordance with embodiments of the present invention, power information is displayed in a graphic window, referred to as a power map, to help users quickly understand the power structure and the relationship between power network design and circuit design to enable easy debugging. The power map includes power domains, isolation cells, level shifters, power switches and power supplies.

25 [0012] One embodiment of the present invention provides a computer-implemented method for generating and displaying a power map, which is a power schematic diagram in a graphic window to show the low power network design based on the low power information defined in a power format in top level, to allow designers debug the low power network design and its associated circuit design, in which the power
30 map comprises a plurality of power domain symbols to represent power domains and to link to the associated parts of the circuit design.

[0013] One embodiment in the present invention is to provide a method to generate and display a power map by the following steps. First, the original circuit design HDL codes, which are some text files, are transformed into internal structure which generally is hierarchical structure called circuit design hierarchies and stored in a knowledge data base generated by a HDL parser, and the original circuit design hierarchies of the knowledge data base are regrouped to new hierarchies which are defined by power specification. In the new hierarchies, instances sharing the same power domain are grouped together. After that, the new hierarchies called power domain circuit design hierarchies are stored in a power data base. Finally, the power map is created from the power data base; it can also display the mismatches or errors between the power specification and the circuit design for those improperly handled signals that connect the power domains.

[0014] The present invention discloses that the power map comprises low power symbols such as power domain symbols, isolation cells, level shifter cells, and power switch cells. Furthermore, the power map is used in conjunction with a simulation result to provide debugging information to the designers, such as displaying the current values of simulation result for signals in the power map at a specific simulation time or displaying the waveforms of simulation result for a period of simulation time in a waveform window by dragging and dropping selected signals in the power map into the waveform window. Moreover, the power map also provides a methodology to detect which HDL signals are not covered by isolation connection and level shifter connection, and will invoke this function automatically when power map is created.

[0015] A feature of the power map, which is displayed in a graphic window, is that it provides some active annotation to easily communicate and interact with users. Accordingly, it is more user friendly to let users debug power network together with digital circuit design in an interactive interface.

[0016] Another object of this invention is to provide a solution to display low power information in a graphic window with a hierarchical representation for power domains to provide an intuitive way to view the parent-child relationships among power domains.

[0017] One embodiment in the present invention is to provide a method to generate and display the power map with a hierarchical representation, wherein the power map comprises a plurality of power domains and each of the plurality of power domains is associated with the part of the circuit design that belongs to the power domain,
5 wherein the plurality of power domains are grouped into a plurality of sets of power domains with a representation to indicate the boundaries and parent-child relationships among the plurality of power domains. In order to present a hierarchical power map, it is necessary that at least one set of power domains contains at least two power domains in which there is a parent power domain and at least one child power
10 domain inside the parent power domain, wherein each of the power domains is associated with a corresponding power control for controlling the power domain, and the status of the power control is displayed on the power map.

[0018] One embodiment of the power map is generated for debugging an IC design having different operating modes, wherein the power map comprises a token to set
15 and display current mode of the IC design. Once the current mode is changed to a new mode, the power domains of the power map will be redrawn under the new mode of the IC design as specified in the low power specification.

[0019] The detailed technology and above preferred embodiments implemented for the present invention are described in the following paragraphs accompanying the
20 appended drawings for people skilled in this field to well appreciate the features of the claimed invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The foregoing aspects and many of the accompanying advantages of this
25 invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description when taken in conjunction with the accompanying drawings, wherein:

[0021] FIG. 1 illustrates a conventional low power digital circuit design methodology;

30 [0022] FIG. 2 is a flowchart of steps performed to create a power map, in accordance with one embodiment of the present invention;

[0023] FIG. 3 illustrates a hierarchical circuit design defined by the power specification after regrouping the original circuit design hierarchy, in accordance with one embodiment of the present invention;

5 [0024] FIG. 4A is a schematic diagram showing a power map, in accordance with one embodiment of the present invention;

[0025] FIG. 4B is a schematic diagram showing an isolation rule, in accordance with one embodiment of the present invention;

[0026] FIG. 4C is a schematic diagram showing a level shifter rule, in accordance with one embodiment of the present invention;

10 [0027] FIG. 4D is a schematic diagram showing a power switch rule, in accordance with one embodiment of the present invention;

[0028] FIG. 5 is a signal value list window, in accordance with one embodiment of the present invention;

15 [0029] FIG. 6 is a waveform window, in accordance with one embodiment of the present invention;

[0030] FIG. 7 illustrates a hierarchical representation of a power map by grouping the power domains of a circuit design according to the power control and parent-child relationships among the power domains, in accordance with one embodiment of the present invention;

20 [0031] FIG. 8 is a flowchart of steps performed in creating a hierarchical representation of a power map, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

25 [0032] Figure 2 is a flowchart for creating a power map of an Integrated Circuit (IC), in accordance with one embodiment of the present invention. At 3, the original text-based circuit design HDL codes are parsed and transformed into an internal structure and stored in a knowledge database. The knowledge database, which may be generated by an HDL parser, is an internal computer-readable data structure (which
30 may have a hierarchical or a flattened structure) of the circuit design, and may be

manipulated or controlled by software. At 4, power designs specified in CPF or UPF are parsed and transformed into internal structure by a CPF or UPF parser. Next, the original circuit design hierarchy in the knowledge database is regrouped into new design hierarchies defined by the power specification having a multitude of power domains. In the new hierarchies, the instances sharing the same power domain are grouped together. It is understood that the original design is not limited to hierarchical or flattened design. If the original circuit design is flattened and stored in the knowledge database, it may be partitioned into multiple power domains. At 5, the new design hierarchies are stored in a power database and transformed into an internal structure which is a computer-readable data structure of the circuit design and the power design. The power database may be manipulated, controlled or modified by software.

[0033] At 6, the power map is created based on the power data base and displayed via a user-friendly GUI (graphical user interface) window. The power map may include many objects such as power domain symbols and isolation cells, described in detail below. If a power domain in a power map is invoked in the user-friendly GUI window, for example, by the user click, the circuit design associated with the power domain is invoked. Therefore, the debugging of the entire chip with power network design and the related HDL code is more efficient and simpler than conventional techniques.

[0034] At 7 static checking may be performed to identify mismatches or errors between the power specification and the circuit design for improperly handled signals that connect the power domains. Such mismatches or errors may be shown to users by annotations, such as dotted lines, symbols, or colored highlights, as illustrated at 8.

[0035] Referring to FIG. 3, frame 9 shows a power map in which the original circuit design hierarchy 11 of HDL is regrouped into new hierarchy 10 defined by a power specification and having a multitude of power domains. Each power domain includes a multitude of instances from the circuit design sharing the same power domain. The original design hierarchy 11 has a top level containing a multitude of instances including a module Power_control with three instances PD_control_1, PD_control_2 and PD_control_3. After regrouping in power map, a top level called PM_top is created. Instance PD_control_1 is associated with and positioned under power domain

PD1, instance PD_control_2 is associated with and positioned under power domain PD2, and instance PD_control_3 is associated with and positioned under power domain PD3.

5 [0036] After new hierarchies are defined by the power specification having a multitude of power domains, they can be stored in a power database, which is an internal computer-readable data structure integrating the circuit design and power network design information. The power database may be manipulated or controlled by software.

10 [0037] After the power data base is generated, the power map may be used to display the power network design, as shown in FIG. 4A. The power map 12 is shown as including a multitude of power domain symbols 13, 14 and 15 connected to grounds 19b, at least one isolation cell 16, at least one level shifter cell 17, at least one power switch cell 18, and at least one power supply 19a.

15 [0038] An isolation cell 16 representing an isolation command includes a multitude of isolation nets 20 for connection with power domains, and an isolation condition net 21 to present the isolation condition expression. Isolation cell 16 is shown as displaying a trigger status symbol positioned on the top-left of the isolation cell 16. If the associated condition's value is "1", the trigger status is successful and the trigger status symbol displays an up-arrow 22a, otherwise the trigger status symbol displays a
20 down-arrow 22b.

[0039] A level shifter cell 17 representing a level shifter command may include a multitude of level shifter nets 23 to connect with power domains.

25 [0040] A power switch cell 18 representing a power switch may include a multitude of power switch nets 24 for connection with a power supply 19a, or with one or more power domains, or with other power switch cells. Moreover, power switch cell 18 also includes a condition pin 26. When a user turns on active annotation, condition value 25 is annotated on condition pin 26. The active annotation provides for interaction and easy communication with the power map. The active annotation can be turned on by an "active annotation mechanism". For example, it may be turned on by clicking a
30 highlighted icon or a symbol, or by selecting an item using a mouse button to annotate the condition value 25 on the condition pin 26.

[0041] Furthermore, in one embodiment, the power map uses a dotted line of red color with mark “iso” 27 to display a signal without proper isolation, and a dotted line of red color with mark “lvs” 28 to display a signal without a level shifter.

[0042] The rules for each power component used in a power map are as follows.

5

Isolation Rule (CPF/UPF)

[0043] Referring to FIG. 4B, the power map uses isolation cell 16 to represent isolation command in a power specification. Isolation cell 16 includes an isolation condition net 21 to present the isolation condition expression. Isolation cell 16 displays an isolation trigger status symbol on the top-left of the isolation cell. If the associated condition’s value is “1”, the trigger status is successful and the trigger status symbol displays an up-arrow; otherwise the trigger status displays a down-arrow 22b.

15 Level Shifter Rule (CPF/UPF)

[0044] Referring to FIG. 4C, the power map uses level shifter cell 17 to represent a level shifter command.

Power Switch (CPF/UPF)

20 Referring to FIG. 4D, the power map uses power switch cell 18 to represent the power switch, thereby showing power switch condition value 25 on condition pin 26 when a user turns on the active annotation (such as by clicking the power switch cell 18).

Non-Covered Connection

25 [0045] A signal connection connecting power domains but not specified by isolation rules and/or level shifter rules in the power specification is called non-covered connection. Referring to FIG. 4A, power map 12 provides a methodology to detect which HDL signals are not covered properly by isolation rules or level shifter rules, thereby to invoke this function automatically when power map 12 is created. In one embodiment, power map 12 uses a dotted line of red color with mark “iso” 27 to display a signal without proper isolation, and a dotted line of red color with mark “lvs” 28 to display a signal without a level shifter.

30

[0046] After the power map is generated, static checking can be performed to detect all mismatches or errors between the power specification and the circuit design to notify the user where such mismatches or errors occur. Mismatches or errors can occur in many ways. For example, the connectivity may be wrong in the
5 isolation/level-shifter cell connection; the control signal may be missing or mismatched in power control signal connected to a power switch; the isolation cells may be useless due to mismatches or missing control signals or there may be improperly covered isolation connections or improperly covered level shifter connections due to missing isolation and/or level shifter cells for the nets connecting
10 to the power domains. Furthermore, in order to ensure that there are both isolation and level shifter connections between two power domains which have HDL signals between them, the power map can create virtual nets (referred to alternatively herein as virtual power rule nets) therebetween to alert designers. For example, if two power domains do not have isolation and/or level shifter connections between them the
15 power map will create a virtual level shifter power rule net and/or a virtual isolation power rule net between them. The impacted signals of each of the two virtual power rule nets are all the HDL signals between the two power domains.

[0047] Referring to FIG. 4A, each power domain symbol can be invoked to link to the part of the circuit design associated with the power domain. In one embodiment,
20 when a user invokes the power domain symbol 13 by clicking it, the part of the circuit design associated with the power domain can be invoked to allow the user view the circuit design in order to debug the entire chip including power network design and the original HDL code.

[0048] The power map is further adapted to display the current values of the
25 simulated signals at any simulation time. In one embodiment, the power map includes a signal value list window 29, as shown in FIG. 5, to make debugging easier. When a user turns on the active annotation, such as by clicking a highlighted icon or a symbol or by selecting an item using a mouse, the signal value list window 29 will display the values of the corresponding simulated signals in the power map for that specific
30 simulation time. Moreover, in one embodiment, the power map using a waveform window 30, as shown in FIG. 6, displays simulation waveforms (for any period of simulation) when a user drags and drops the selected signals in the power map. For example, when a user drags an isolation cell and drops it into the waveform window

30, the nets connecting the isolation level—and considered as variables (VBs)—are added automatically to the waveform window 30, thus resulting in the display of their waveforms automatically for a period of simulation time, as shown in FIG. 6.

Similarly, the waveforms of the power component (e.g., power domain, PD) signals
5 may also be displayed in the waveform window 30. In yet another embodiment, when a user moves the cursor in the waveform window 30 to a certain simulation time, nets in the power map are annotated with values of their associated signals at that specific time. Therefore, in accordance with the embodiments of the present invention, the process of debugging a power network and the digital circuit design is made easier
10 and more efficient than conventional techniques.

[0049] FIG. 7 shows a hierarchical a power map in which the power domains of the circuit design are grouped in accordance with a specification that includes a representation of the power domain boundaries as well as parent-child relationships within the power domains. Each power map is associated with a power control for
15 controlling that power domain. As seen from FIG. 7, the top level of the power map named as PD_TOP 700 is shown as including three sets of parent power domains, namely PD_CPU 710, PD_FSM 721 and PD_RAM 731. Power domain PD_CPU 710 is shown as including three child power domains, namely PD_ALUB 711, PD_PCU 712 and PD_CCU 713, inside a rectangle representing the parent power domain
20 PD_CPU 700. Within the PD_ALUB 711, there is shown one power domain PD_alu 714, thus indicating that there is a parent-child relationship between the parent power domain PD_ALUB 711 and the child power domain PD_alu 714. While FIG. 7 shows three levels of the hierarchy of the power map, it is understood that power map hierarchy may contain many more levels. The top level hierarchy is also shown as
25 including a second power domain set PD_FSM 721; and a third power domain set PD_RAM 731. No child power domain is shown within the power domain PD_FSM 721 or PD_RAM 731. In order to present a hierarchical power map, at least one set of power domains contains at least two power domains, namely a parent power domain and at least one child power domain inside the parent power domain. Each of the
30 power domains is associated with a corresponding power control for controlling that power domain. The status of the power control is displayed on the power map. The power control of a parent power domain can be used to control its child power domains as well. For example, in one embodiment, once the power of a parent power

domain is turned off, all of the child domains inside the parent power domain will be turned off as well. However, if the power of the parent power domain is turned on, each of the child power domains can be turned on automatically or be subject to an additional local power control associated with the child power domain if necessary.

- 5 **[0050]** A status of the first power control 701 of the first set of the power domains PD_CPU 710 is displayed along the first rectangular shape. For example, the status of the first power control PD_CPU 701 shows that the first set of power domains is ON with a voltage level of 1.2V. Likewise, the status of power controls of power domains PD_ALUB 711, PD_PCU 712, PD_CCU 713, PD_FSM 721 and PD_RAM 731 are
- 10 displayed as 702, 704, 703, 705 and 706 respectively. In another example, the status of the power control 705 of power domain PD_FSM 721 shows that the power of PD_FSM 721 is changed from ON to OFF. The status of the power control 706 of power domain PD_RAM 731 shows that the power of PD_RAM 731 is ON with a voltage level of 0.8V. In order to help debug a circuit, static checking may also be
- 15 performed to identify mismatches or errors between the power specification and the circuit design for improperly handled signals that connect the power domains. Such mismatches or errors may be shown to users by one or more annotations, such as dotted lines, symbols, or colored highlights as illustrated in FIG. 7. The connections between power domains or hierarchical blocks of power domains having no isolation
- 20 or level shifter cells may be highlighted with dotted lines, such as connection 731 between the power domain PD_CPU 710 and PD_FSM 721, connection 732 between the power domain PD_ALUB 711 and PD_FSM 721, connection 734 between the power domain PD_alu 714 and PD_CCU 713 and a connection 733 between the power domain PD_PCU 712 and PD_CCU 713.
- 25 **[0051]** The isolation cell 754 is shown as connecting the power domain PD_ALUB 711 to PD_FSM 721, and having a clamp value of logic “high”. Likewise, the isolation cell 755 is shown as connecting the power domain PD_alu 714 to PD_FSM 721 and having a clamp value of logic “high”. The isolation cell 756 is shown as connecting the power domain PD_ALUB 711 to PD_RAM 731. However, the clamp
- 30 value of the isolation cell 756 is not defined and not shown in the power map. Likewise, the clamp values of the isolation cells 751, 752 and 753 are not defined and not shown in FIG. 7. Therefore, the conditions or errors among power domains may be viewed in a hierarchical power map to help with debugging the IC design.

[0052] For circuits having multiple operating modes, to avoid merging all the operating modes into a single power map which may make viewing complex and debugging difficult, each operating mode can have its own power map. As a result, for each mode, a corresponding hierarchical power map can be generated and
5 displayed independently. For example, as shown in FIG. 7, the current operating mode is displayed on the top level of the power map as mode_1 708.

[0053] In one embodiment, the computer-implemented method for creating the power map, in accordance with the present invention, is as follows. As shown in FIG. 8, at 760, the original text-based circuit design HDL codes are parsed and transformed
10 into internal structure and stored in a knowledge database. The knowledge database, which may be generated by a HDL parser, is an internal computer-readable data structure of the circuit design and may be easily manipulated or controlled by software. The knowledge database is generally hierarchical but may have a flattened structure. At 761, power designs specified in CPF or UPF are parsed and transformed
15 into internal structure by a CPF or UPF parser. Thereafter, the original circuit design hierarchy in the knowledge database is regrouped into power domain hierarchies defined by the power specification having a multitude of power domains. At 762, the power domain hierarchies are stored in a power database and transformed into an internal structure which is a computer-readable data structure of the circuit design and
20 the power design and which may be controlled by software. At 763 the power map is created according to the power domain hierarchy of the power database and displayed in a GUI window. The power map includes a multitude of power domains each of which is associated with a part of the circuit. The power map includes a first representation that indicates the boundaries and parent-child relationships among the
25 power domains with at least one of the power domains containing at least one child power domain. Each power domains has a power control for controlling the power domain with the status of the power control displayed on the power map. The power control of a parent power domain can be used to control its child power domains as well. For example, in one embodiment, once the power of a parent power domain is
30 turned off, all of the child domains inside the parent power domain may be turned off as well. However, if the power of the parent power domain is turned on, each of the child power domains can be turned on automatically or be made subject to an additional local power control associated with the child power domain if necessary.

[0054] At 764, static checking may be performed to detect mismatches or errors between the power specification and the circuit design for improperly handled signals that connect the power domains. The mismatches or errors may be displayed to users by one or more annotations such as dotted lines, symbols, or colored highlights as
5 illustrated at 765.

[0055] The above embodiments of the present invention are illustrative and not limitative. Other additions, subtractions or modifications are obvious in view of the present disclosure and are intended to fall within the scope of the appended claims.

WHAT IS CLAIMED IS:

- 1 1. A computer-implemented method for debugging the power
2 aspect of a circuit design specified in a power specification format by displaying a
3 power map that integrates the power specification and the circuit design, the method
4 comprising:
5 generating a knowledge database from the circuit design, when the
6 computer is invoked to debug the circuit design;
7 generating a power database according to the power specification and
8 the knowledge database;
9 generating and displaying the power map according to the power
10 database using the computer, wherein the power map comprises a plurality of power
11 domains each being associated with a different part of the circuit design; and
12 checking and displaying mismatches or errors between the power
13 specification and the circuit design for signals connecting the plurality of power
14 domains, wherein the power map comprises a first representation that indicates
15 boundaries and parent-child relationships among the plurality of power domains,
16 wherein at least one of the plurality of power domains includes at least one child
17 power domain, wherein at least one of the plurality of power domains is associated
18 with a power control for controlling the power domain, and wherein a status of the
19 power control is displayed on the power map.
- 1 2. The computer-implemented method in accordance with claim
2 1, wherein at least a subset of the plurality of power domains has an associated parent
3 power domain and an associated child power domain.
- 1 3. The computer-implemented method in accordance with claim
2 2, wherein the checking and displaying further comprises:
3 displaying a virtual isolation connection net between at least
4 two power domains if there are signals in hardware description language (HDL)
5 between the at least two power domains and there are not any isolation connections
6 between the at least two power domains; and
7 displaying a virtual level shifter connection net between the at
8 least two power domains if there are signals in hardware description language (HDL)

9 between the at least two power domains and there are not any level shifter
10 connections between the at least two power domains.

1 4. The computer-implemented method in accordance with claim
2 2, wherein the power map is used with a simulation result, the computer-implemented
3 method further comprising:

4 displaying current simulation values of signals in the power map; and
5 displaying a status of each power control using an ON or OFF symbol
6 to indicate if the associated power domain is currently powered up or powered down,
7 the status of a power control including a voltage level if the associated power domain
8 is powered up.

1 5. The computer-implemented method in accordance with claim
2 1, wherein the power map further comprises at least one isolation cell representing an
3 isolation command, the at least one isolation cell comprising a plurality of isolation
4 nets for connection to the power domains.

1 6. The computer-implemented method in accordance with claim
2 1, wherein the power map further comprises at least one level shifter cell representing
3 a level shifter command, the at least one level shifter cell comprising a plurality of
4 level shifter nets for connection to the power domains.

1 7. The computer-implemented method in accordance with claim
2 1, wherein the power map further comprises at least one power switch cell
3 representing a power switch, the at least one power switch cell comprising a plurality
4 of power switch nets for connection to a power supply, or the power domains or at
5 least one power switch cell.

1 8. The computer-implemented method in accordance with claim
2 5, wherein the virtual isolation connection net or the virtual level shifter connection
3 net are represented in either dotted or colored lines.

1 9. A computer system adapted to debug the power aspect of a
2 circuit design specified in a power specification format by displaying a power map
3 that integrates the power specification and its corresponding circuit design, the
4 computer system comprising a processor and a computer-readable storage medium

5 adapted to store instruction, wherein said instructions when executed by the processor
6 cause the processor to:
7 generate a knowledge database from the circuit design;
8 generate a power database according to the power specification and the
9 knowledge database;
10 generate and display the power map according to the power database,
11 wherein the power map comprises a plurality of power domains each associated with
12 a different part of the circuit design; and
13 check and display mismatches or errors between the power
14 specification and the circuit design for signals connecting the plurality of power
15 domains, wherein the power map comprises a first representation that indicates
16 boundaries and parent-child relationships among at least a subset of the plurality of
17 power domains, wherein at least one of the plurality of power domains includes at
18 least one child power domain, wherein at least one of the plurality of power domains
19 is associated with a power control for controlling the at least one power domain,
20 wherein the status of the power control is displayed on the power map.

1 10. The computer system of claim 9, wherein at least a subset of
2 the plurality of power domains has an associated parent power domain and an
3 associated child power domain.

1 11. The computer system of claim 10, wherein the check and
2 display further comprises:
3 display a virtual isolation connection net between at least two power
4 domains if there are signals in hardware description language (HDL) between the at
5 least two power domains and there are not any isolation connections between the at
6 least two power domains; and
7 display a virtual level shifter connection net between the at least two
8 power domains if there are signals in hardware description language (HDL) between
9 the at least two power domains and there are not any level shifter connections
10 between the at least two power domains.

1 12. The computer system of claim 10, wherein the power map is
2 used with a simulation result, wherein said instructions when executed by the
3 processor further cause the processor to:

4 display current simulation values of signals in the power map; and
5 display a status of each power control using an ON or OFF symbol to
6 indicate if the associated power domain is currently powered up or powered down, the
7 status of a power control including a voltage level if the associated power domain is
8 powered up.

1 13. The computer system of claim 9, wherein the power map
2 further comprises at least one isolation cell representing an isolation command, the at
3 least one isolation cell comprising a plurality of isolation nets for connection to the
4 power domains.

1 14. The computer system of claim 9, wherein the power map
2 further comprises at least one level shifter cell representing a level shifter command,
3 the at least one level shifter cell comprising a plurality of level shifter nets for
4 connection to the power domains.

1 15. The computer system of claim 9, wherein the power map
2 further comprises at least one power switch cell representing a power switch, the at
3 least one power switch cell comprising a plurality of power switch nets for connection
4 to a power supply, the power domains or at least one power switch cell.

1 16. The computer system of claim 13, wherein the virtual isolation
2 connection net or the virtual level shifter connection net are represented in either
3 dotted or colored lines.

1 17. A computer-readable storage medium comprising instructions
2 that when executed by a processor cause the processor to debug the power aspect of a
3 circuit design specified in a power specification format by displaying a power map
4 that integrates the power specification and its corresponding circuit design, the
5 computer-readable storage medium further comprising instructions that when
6 executed by the processor further cause the processor to:
7 generate a knowledge database from the circuit design;
8 generate a power database according to the power specification and the
9 knowledge database;

10 generate and displaying the power map according to the power
11 database, wherein the power map comprises a plurality of power domains each
12 associated with a different part of the circuit design; and
13 check and display mismatches or errors between the power
14 specification and the circuit design for signals connecting the plurality of power
15 domains, wherein the power map comprises a first representation that indicates
16 boundaries and parent-child relationships among at least a subset of the plurality of
17 power domains, wherein at least one of the plurality of power domains includes at
18 least one child power domain, wherein at least one of the plurality of power domains
19 is associated with a power control for controlling the at least one power domain,
20 wherein the status of the power control is displayed on the power map.

1 18. The computer-readable storage medium 17, wherein at least a
2 subset of the plurality of power domains has an associated parent power domain and
3 an associated child power domain.

1 19. The computer-readable storage medium of claim 18, wherein
2 the check and display further comprises:
3 display a virtual isolation connection net between at least two power
4 domains if there are signals in hardware description language (HDL) between the at
5 least two power domains and there are not any isolation connections between the at
6 least two power domains; and
7 display a virtual level shifter connection net between the at least two
8 power domains if there are signals in hardware description language (HDL) between
9 the at least two power domains and there are not any level shifter connections
10 between the at least two power domains.

1 20. The computer-readable storage medium of claim 18, wherein
2 the power map is used with a simulation result, wherein said instructions when
3 executed by the processor further cause the processor to:
4 display current simulation values of signals in the power map; and
5 display a status of each power control using an ON or OFF symbol to
6 indicate if the associated power domain is currently powered up or powered down, the
7 status of a power control including a voltage level if the associated power domain is
8 powered up.

1 21. The computer-readable storage medium of claim 17, wherein
2 the power map further comprises at least one isolation cell representing an isolation
3 command, the at least one isolation cell comprising a plurality of isolation nets for
4 connection to the power domains.

1 22. The computer-readable storage medium of claim 17, wherein
2 the power map further comprises at least one level shifter cell representing a level
3 shifter command, the at least one level shifter cell comprising a plurality of level
4 shifter nets for connection to the power domains.

1 23. The computer-readable storage medium of claim 17, wherein
2 the power map further comprises at least one power switch cell representing a power
3 switch, the at least one power switch cell comprising a plurality of power switch nets
4 for connection to a power supply, the power domains or at least one power switch
5 cell.

1 24. The computer-readable storage medium of claim 21, wherein
2 the virtual isolation connection net or the named virtual level shifter connection net
3 are represented in either dotted or colored lines.

```
module aaa( )  
.....  
always(@clk)  
.....  
.....  
.....  
end module
```

1

```
create power domain Island Vdd -  
    include scope  
create power domain Island_V1 -  
    elements inst1  
create supply domain Island_V2 -  
    elements inst2  
    create supply net V1SW -domain  
        Island_V1  
create supply net V2 -domain Island_V2  
    create supply port Vddp -domain
```

2

FIG.1
(PRIOR ART)

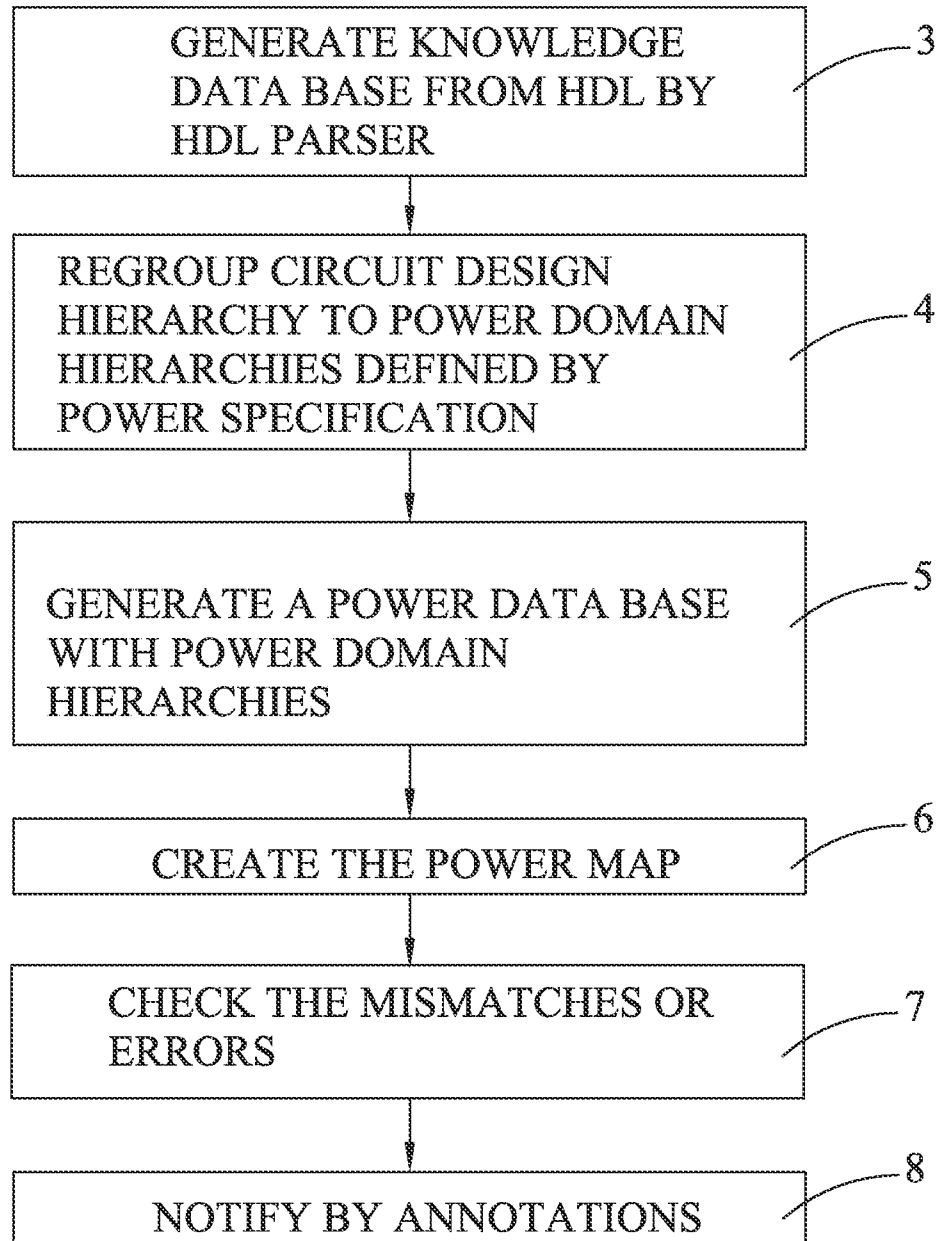


FIG.2

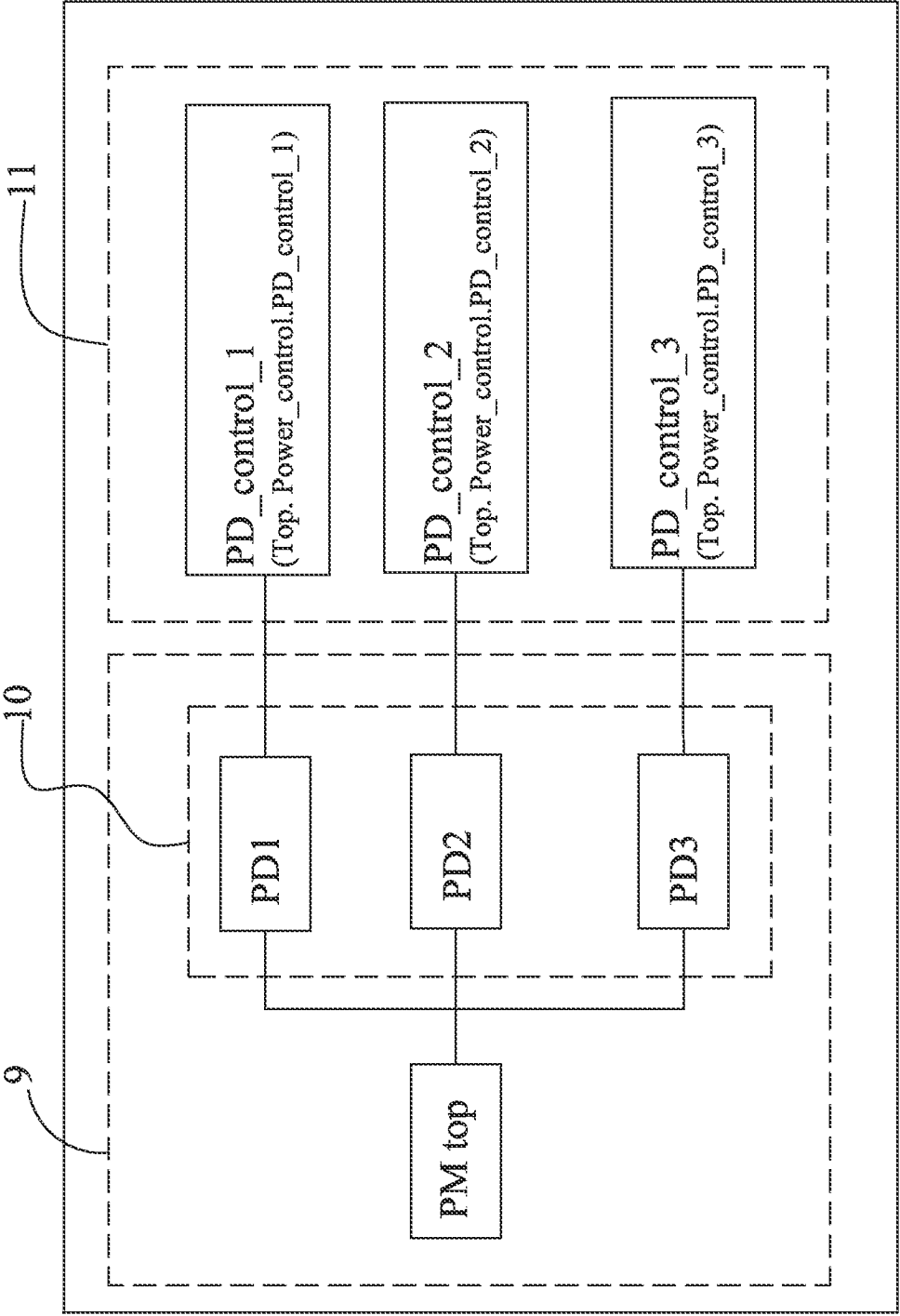


FIG.3

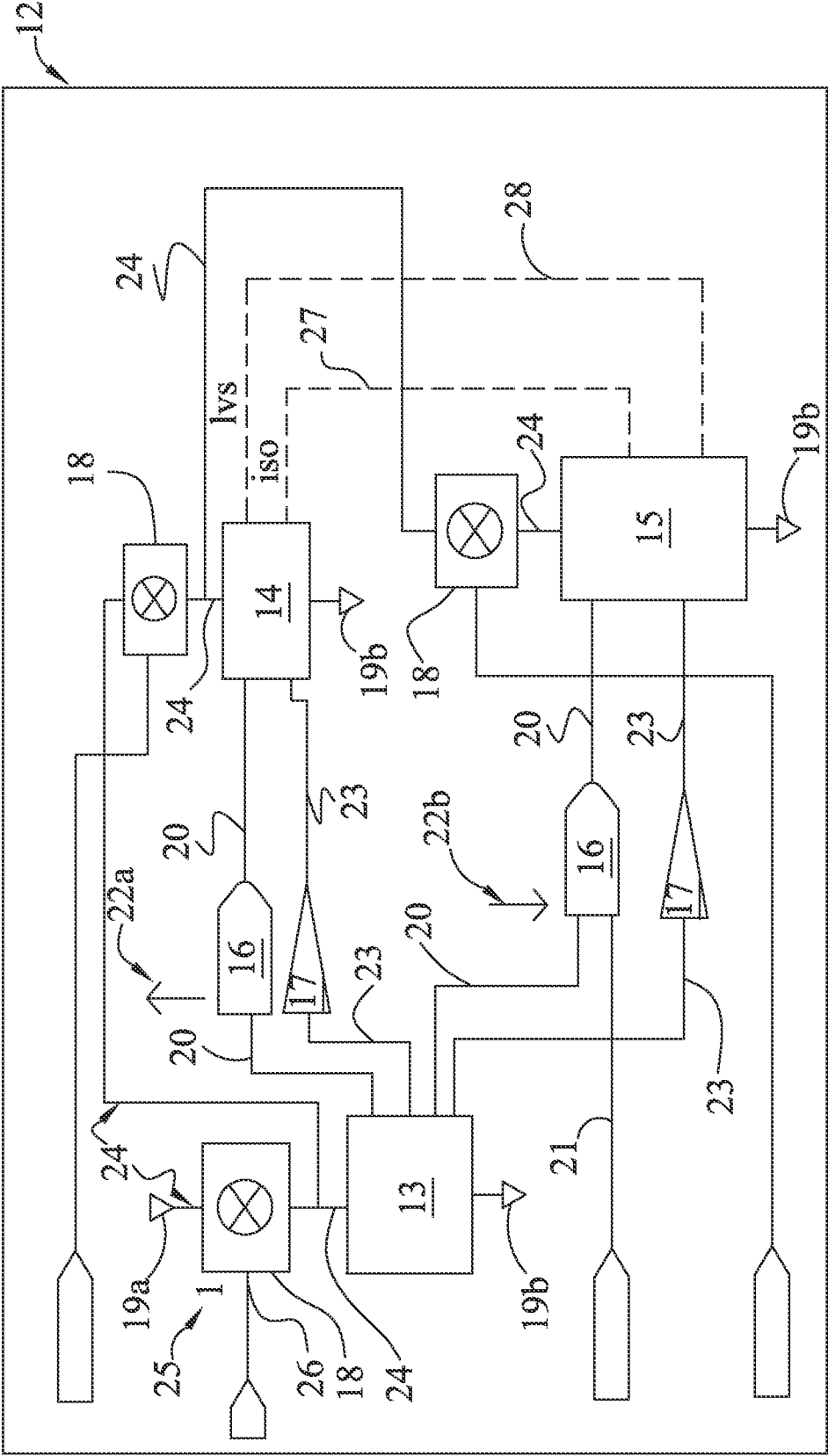


FIG.4A

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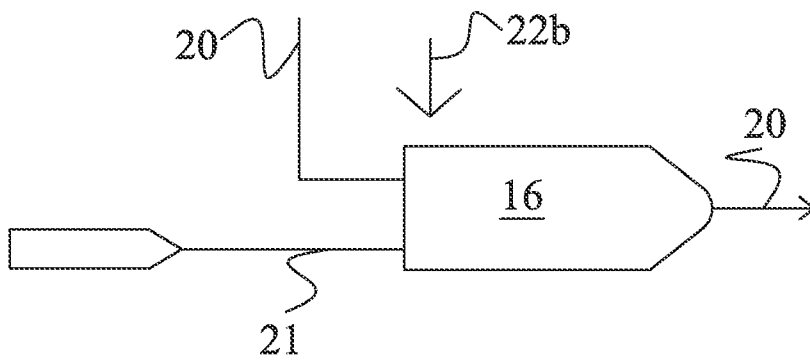


FIG. 4B

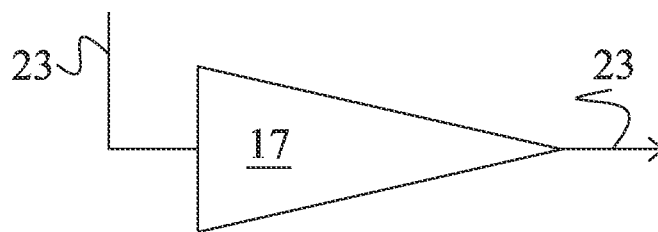


FIG. 4C

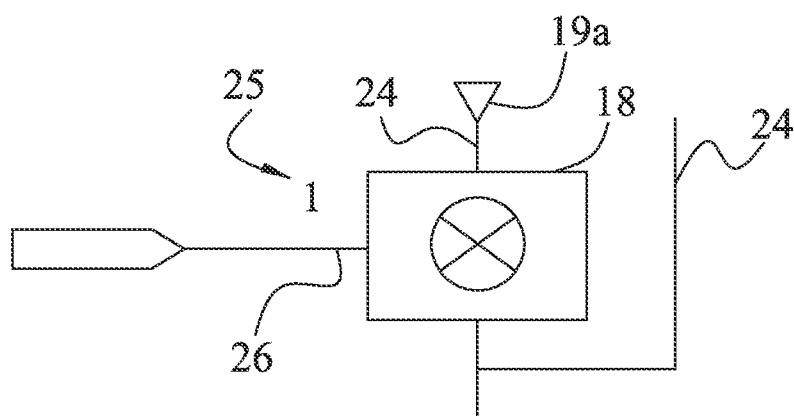


FIG. 4D

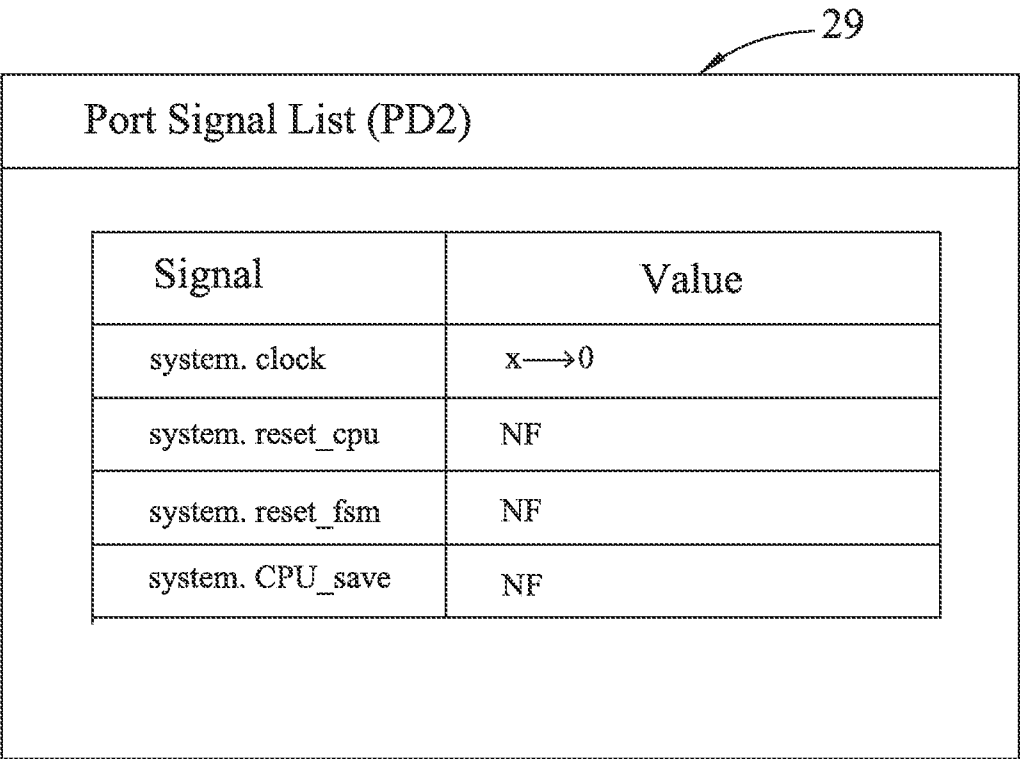


FIG.5

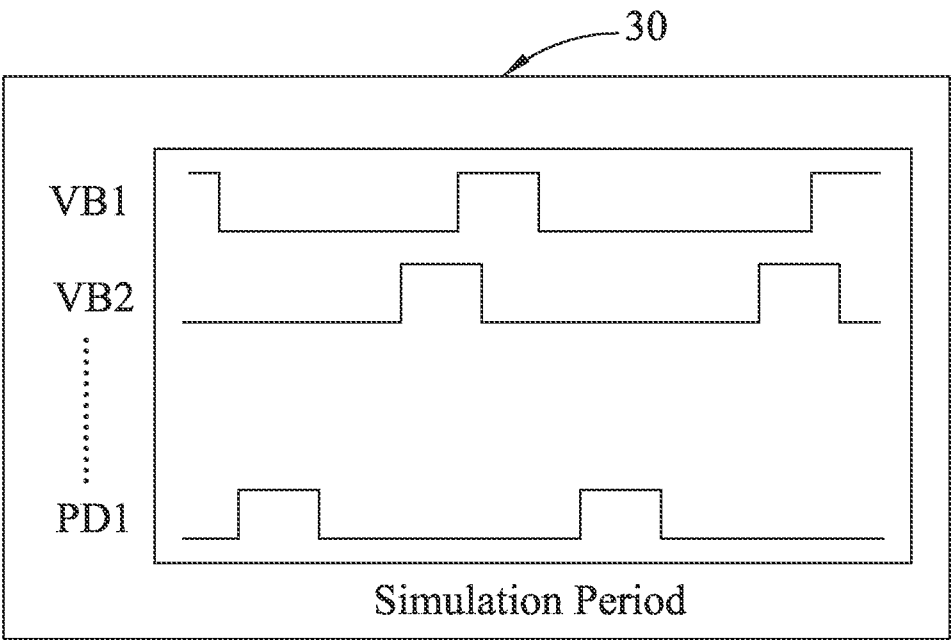


FIG.6

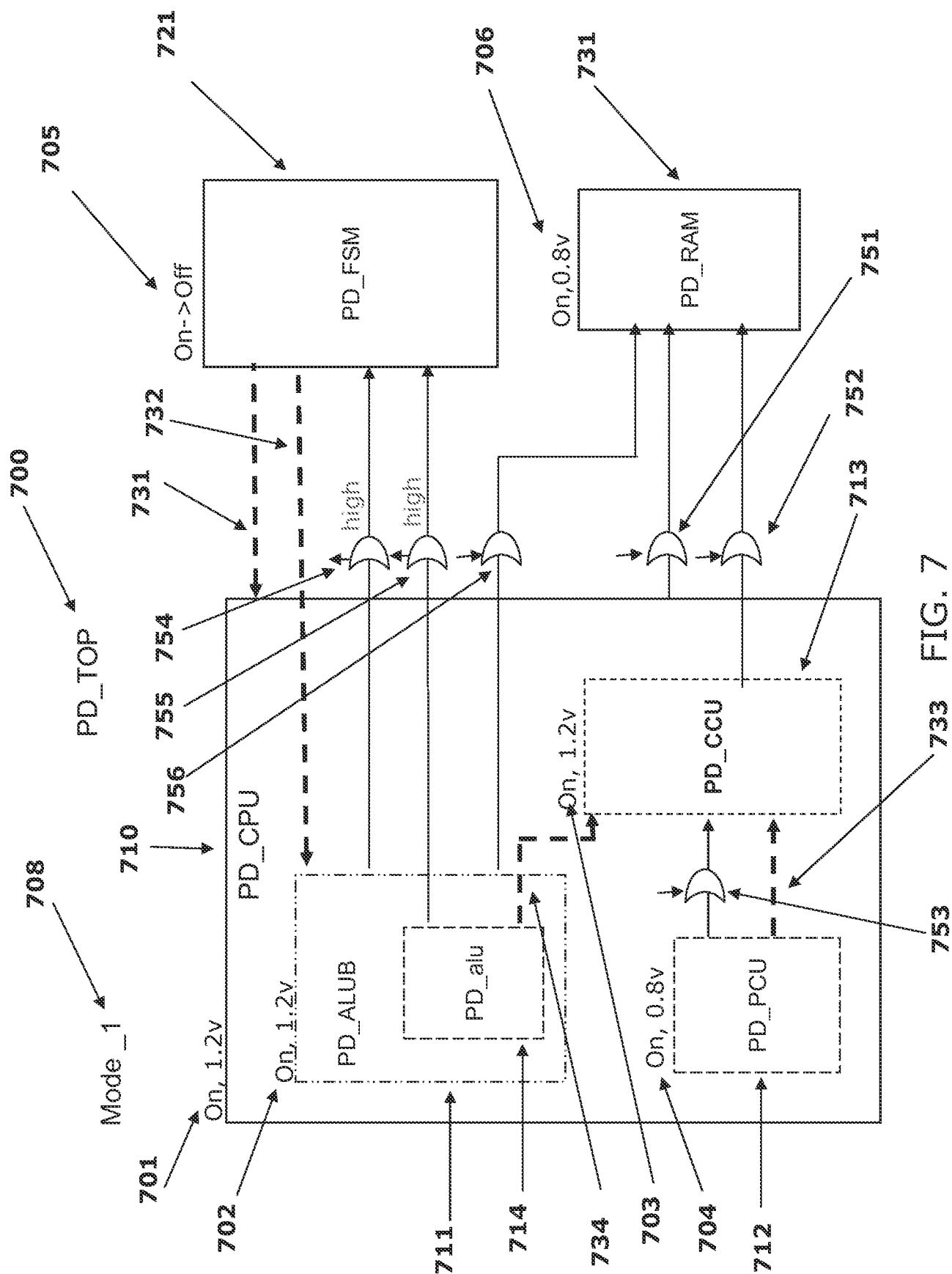


FIG. 7

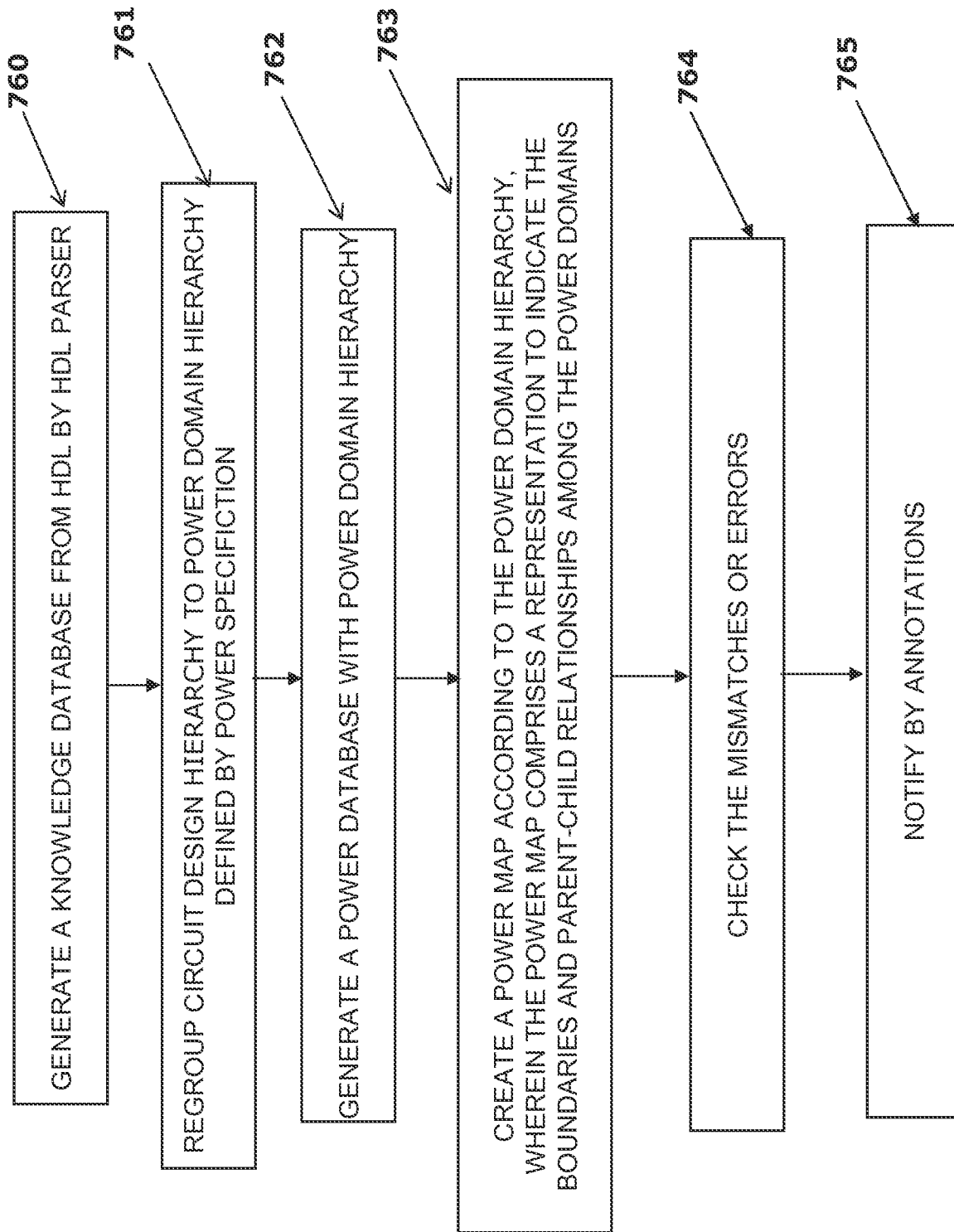


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/076247

A. CLASSIFICATION OF SUBJECT MATTER

G06F 17/50(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 17/50; H02B 001/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: circuit design, power, domain, map, parent-child and similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2011-0320991 A1 (CHIH-NENG HSU et al.) 29 December 2011 See paragraphs [0006], [0030]-[0038]; figures 2-3; and claims 1-2, 5-7, 16.	1-24
Y	US 2008-0126999 A1 (QI WANG) 29 May 2008 See paragraphs [0028]-[0029]; and figure 2.	1-24
A	US 2005-0146228 A1 A1 (WEI CHEN et al.) 07 July 2005 See paragraphs [0044]-[0046]; and figure 3.	1-24
A	US 2012-0198408 A1 (AMIT CHOPRA) 02 August 2012 See paragraphs [0039]-[0045]; and figure 2.	1-24
A	US 2007-0044044 A1 (JOHN WILSON et al.) 22 February 2007 See paragraphs [0062]-[0069]; and figures 6-7.	1-24



Further documents are listed in the continuation of Box C.



See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

26 March 2014 (26.03.2014)

Date of mailing of the international search report

26 March 2014 (26.03.2014)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2013/076247

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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