



US 20190067848A1

(19) **United States**

(12) **Patent Application Publication**

**Aoki**

(10) **Pub. No.: US 2019/0067848 A1**

(43) **Pub. Date: Feb. 28, 2019**

(54) **MEMORY MEZZANINE CONNECTORS**

**H05K 1/18** (2006.01)

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**H01R 12/71** (2006.01)

**H01R 12/72** (2006.01)

**G02B 6/35** (2006.01)

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(52) **U.S. Cl.**

CPC ..... **H01R 12/7076** (2013.01); **H01R 12/82**

(2013.01); **H05K 7/20172** (2013.01); **H01R**

**12/73** (2013.01); **H01R 43/205** (2013.01);

**H01R 43/26** (2013.01); **H01R 12/707**

(2013.01); **H05K 1/115** (2013.01); **H05K**

**1/181** (2013.01); **H01R 12/716** (2013.01);

**H01R 12/722** (2013.01); **G02B 6/354**

(2013.01); **H05K 2201/041** (2013.01); **H05K**

**2201/10159** (2013.01); **H05K 2201/10545**

(2013.01); **H05K 7/1498** (2013.01)

(21) Appl. No.: **15/942,108**

(22) Filed: **Mar. 30, 2018**

**Related U.S. Application Data**

(60) Provisional application No. 62/584,401, filed on Nov.  
10, 2017.

(30) **Foreign Application Priority Data**

Aug. 30, 2017 (IN) ..... 201741030632

**Publication Classification**

(51) **Int. Cl.**

**H01R 12/70** (2006.01)

**H05K 7/14** (2006.01)

**H05K 7/20** (2006.01)

**H01R 12/73** (2006.01)

**H01R 43/20** (2006.01)

**H01R 43/26** (2006.01)

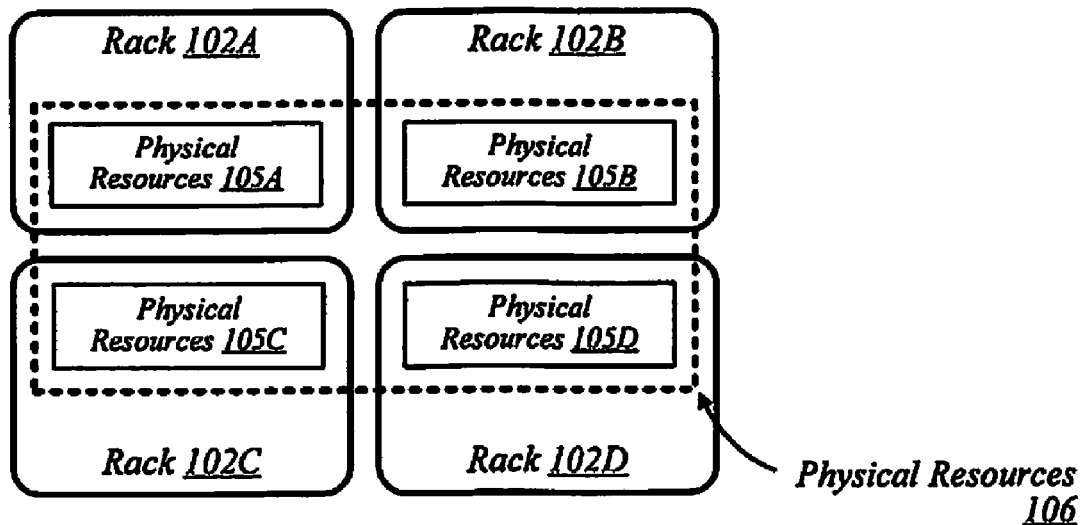
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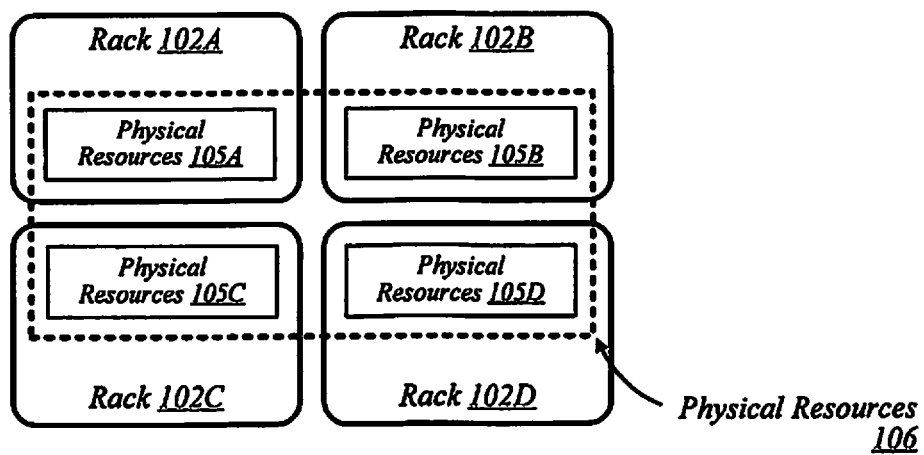
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**ABSTRACT**

Sleds for operation in racks of data centers are disclosed herein. A sled includes a circuit board substrate, one or more physical resources, and one or more memory devices. The circuit board substrate has a top side and a bottom side arranged opposite the top side. The one or more physical resources are coupled to the top side of the circuit board substrate. The one or more memory devices are coupled to the bottom side of the circuit board substrate. Additionally, the sled includes a connector to electrically couple the one or more physical resources to the one or more memory devices.

**Data Center 100**



***Data Center 100*****FIG. 1**

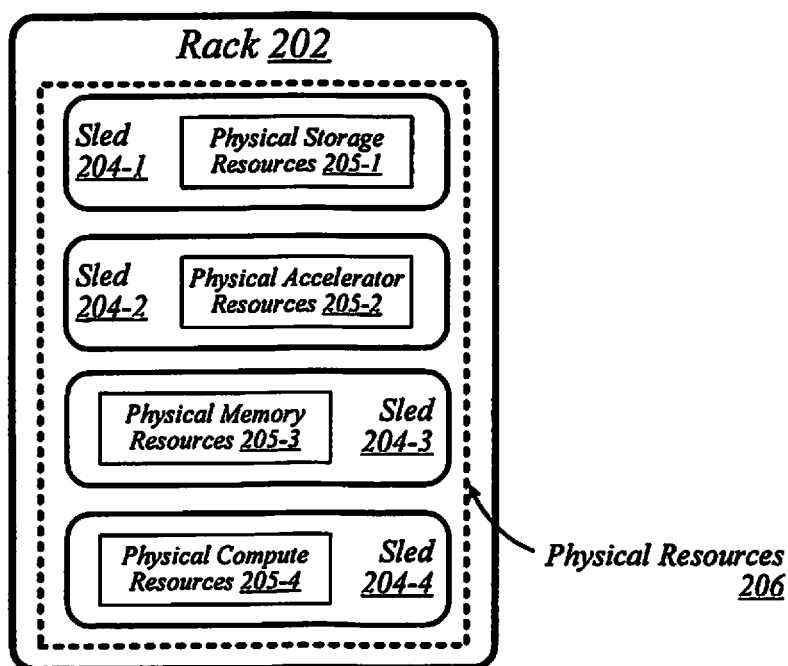
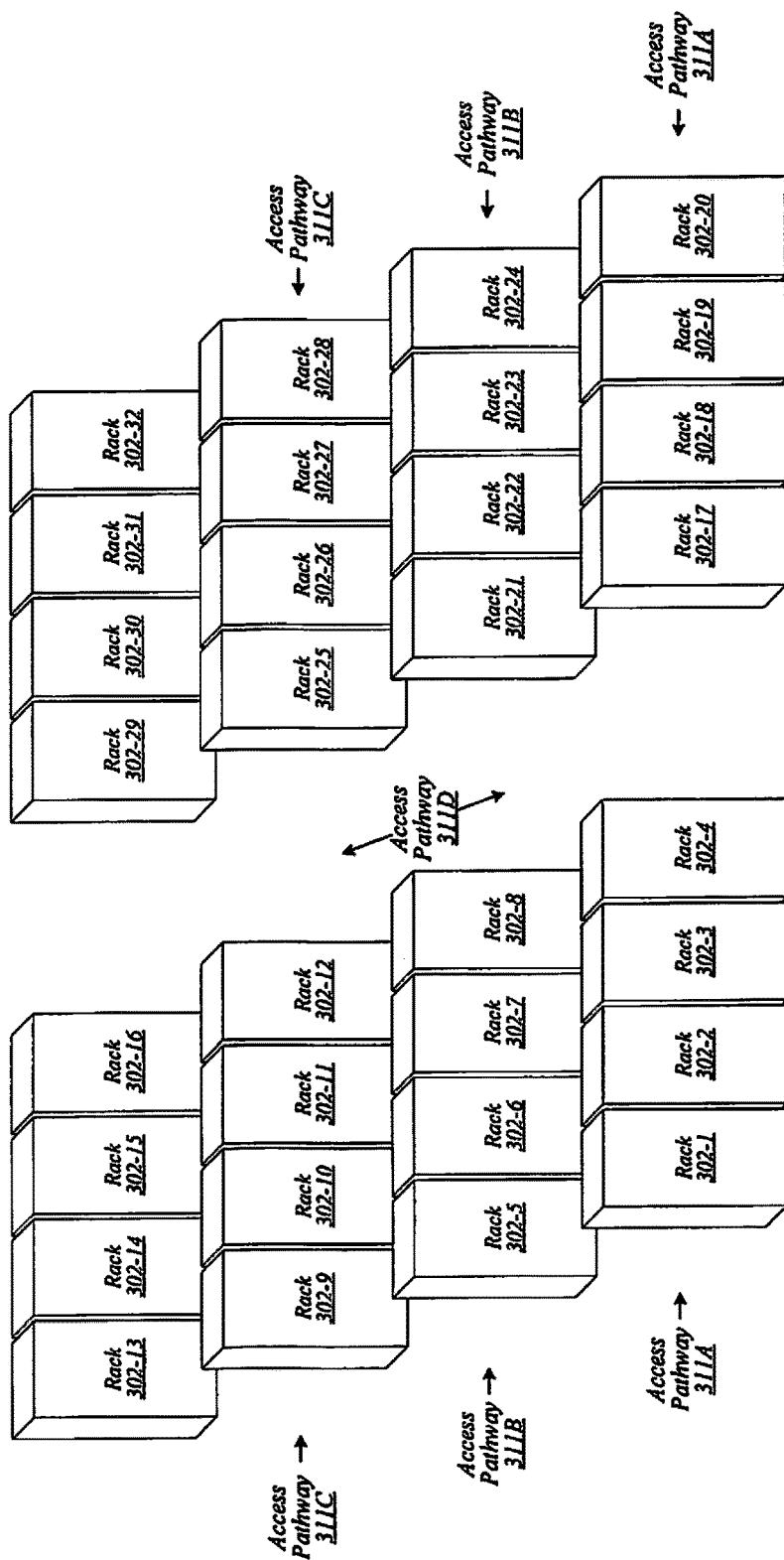
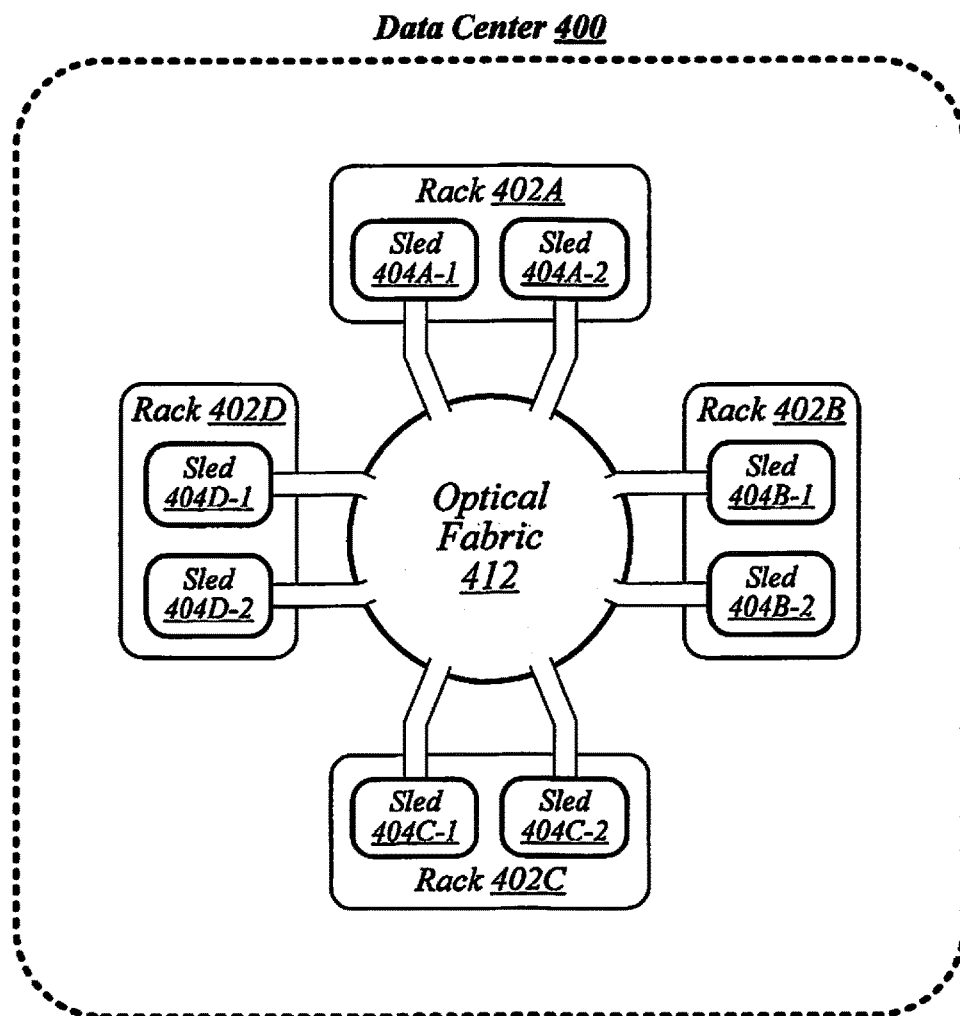


FIG. 2

**Data Center 300**



**FIG. 3**

**FIG. 4**

500

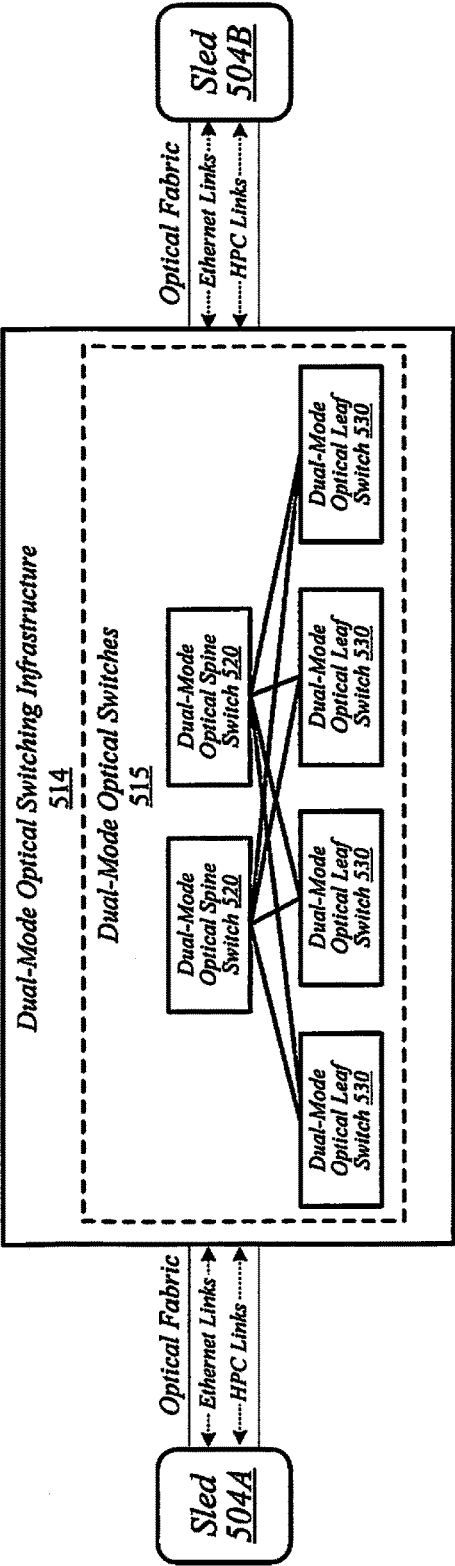
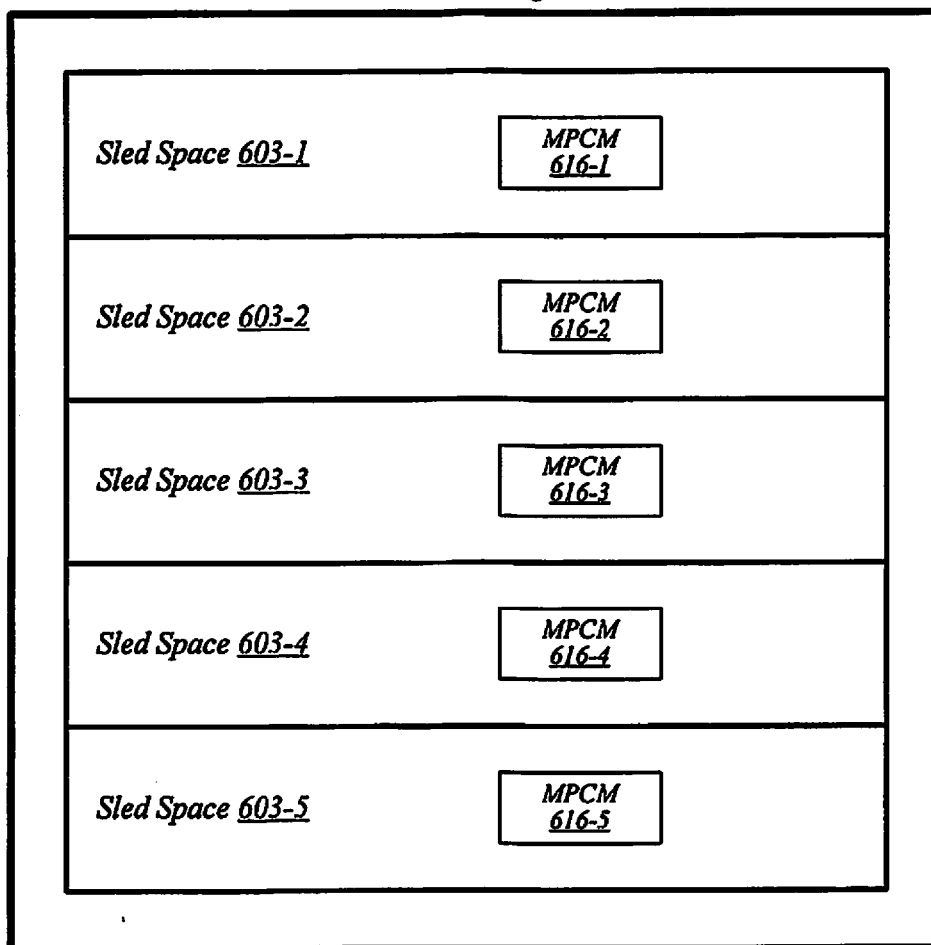


FIG. 5

**600*****Rack Access Region 601*****FIG. 6**

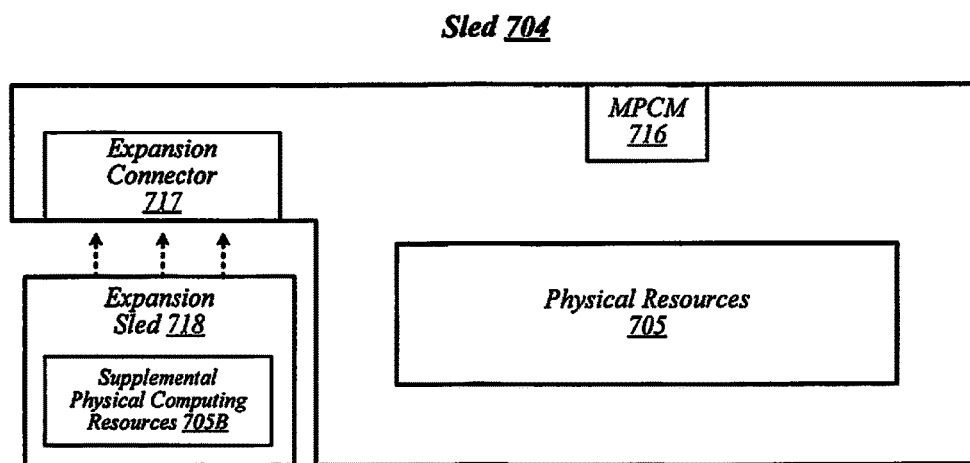
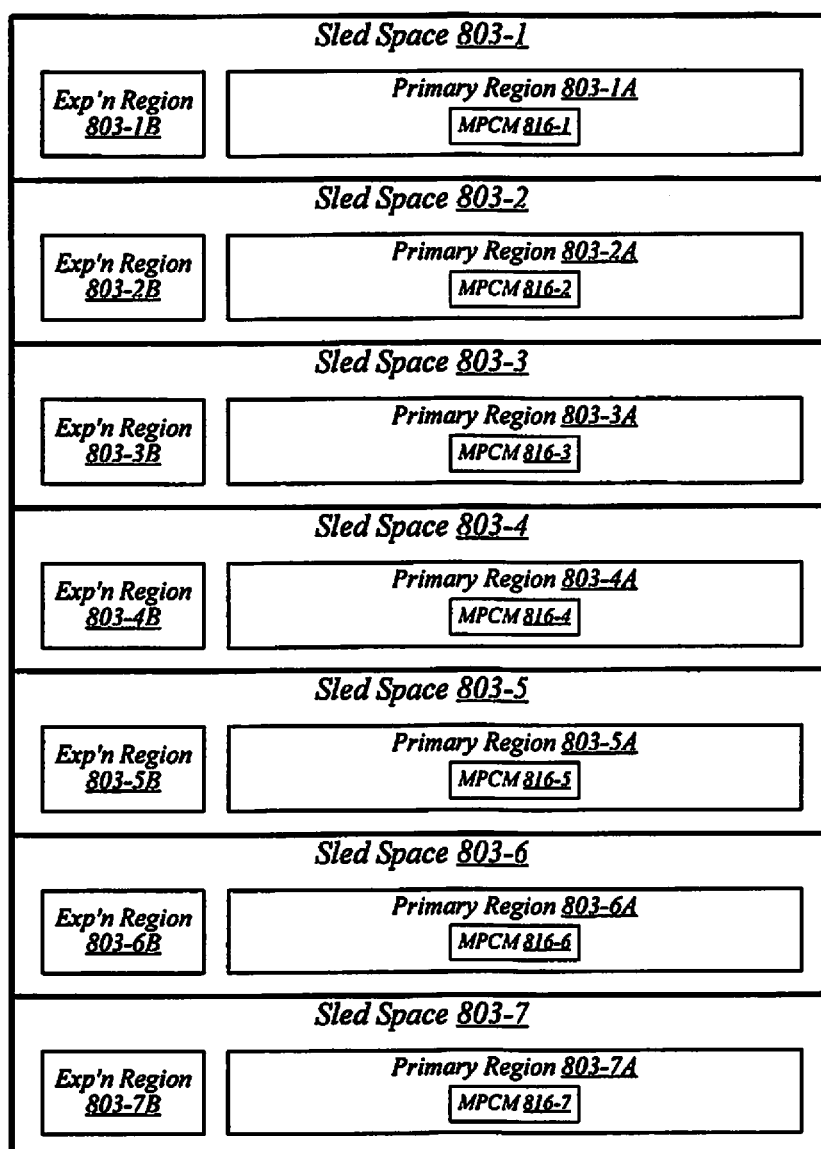


FIG. 7

**800****FIG. 8**

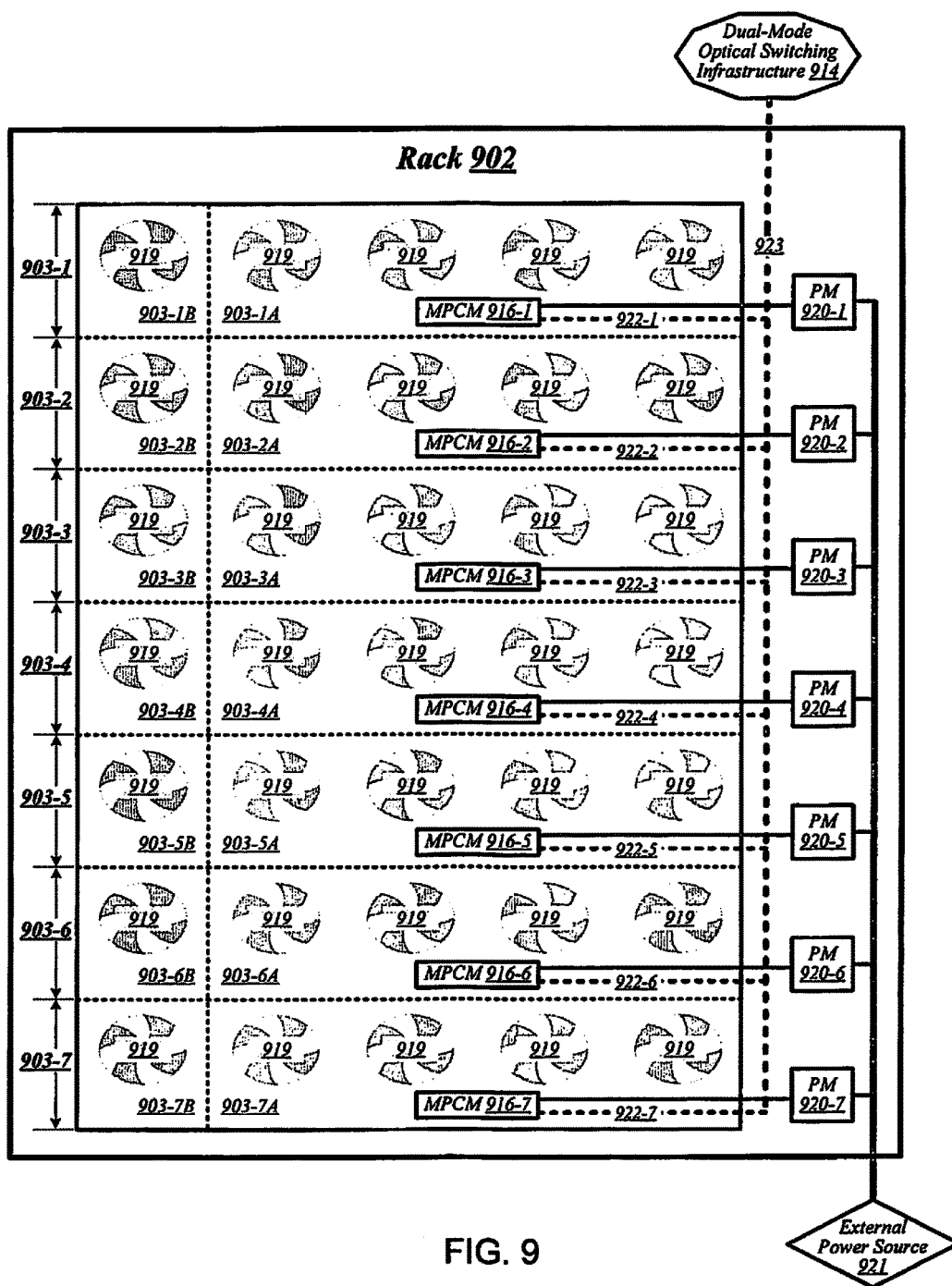


FIG. 9

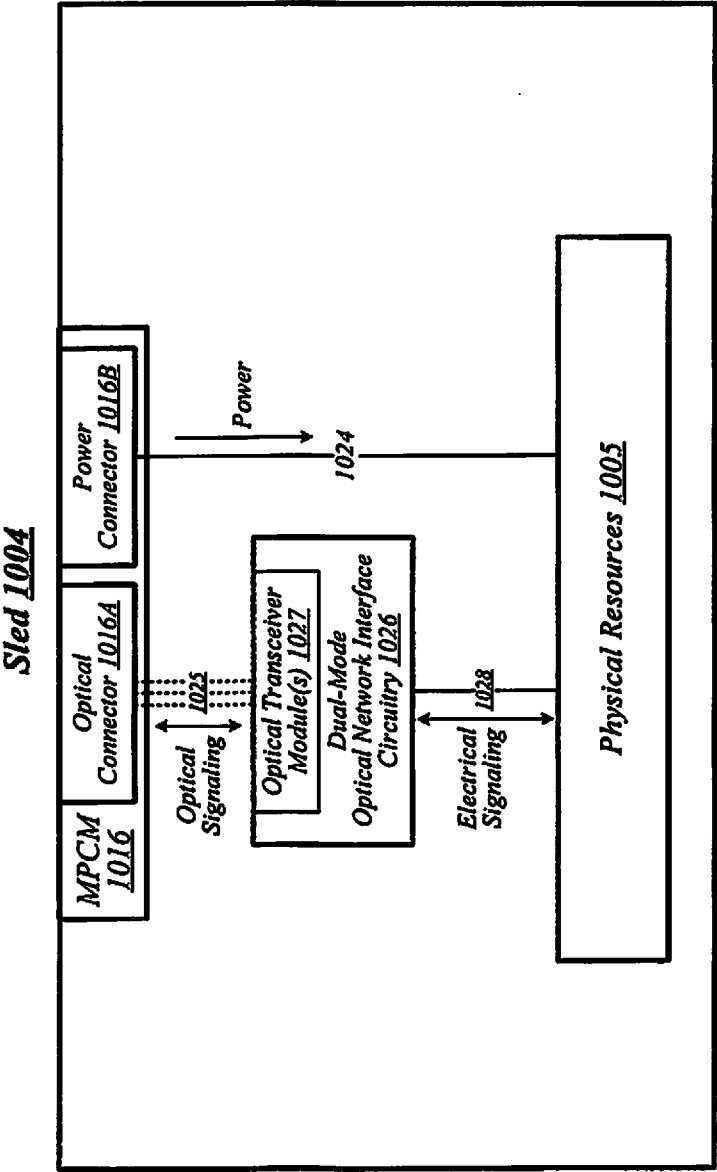


FIG. 10

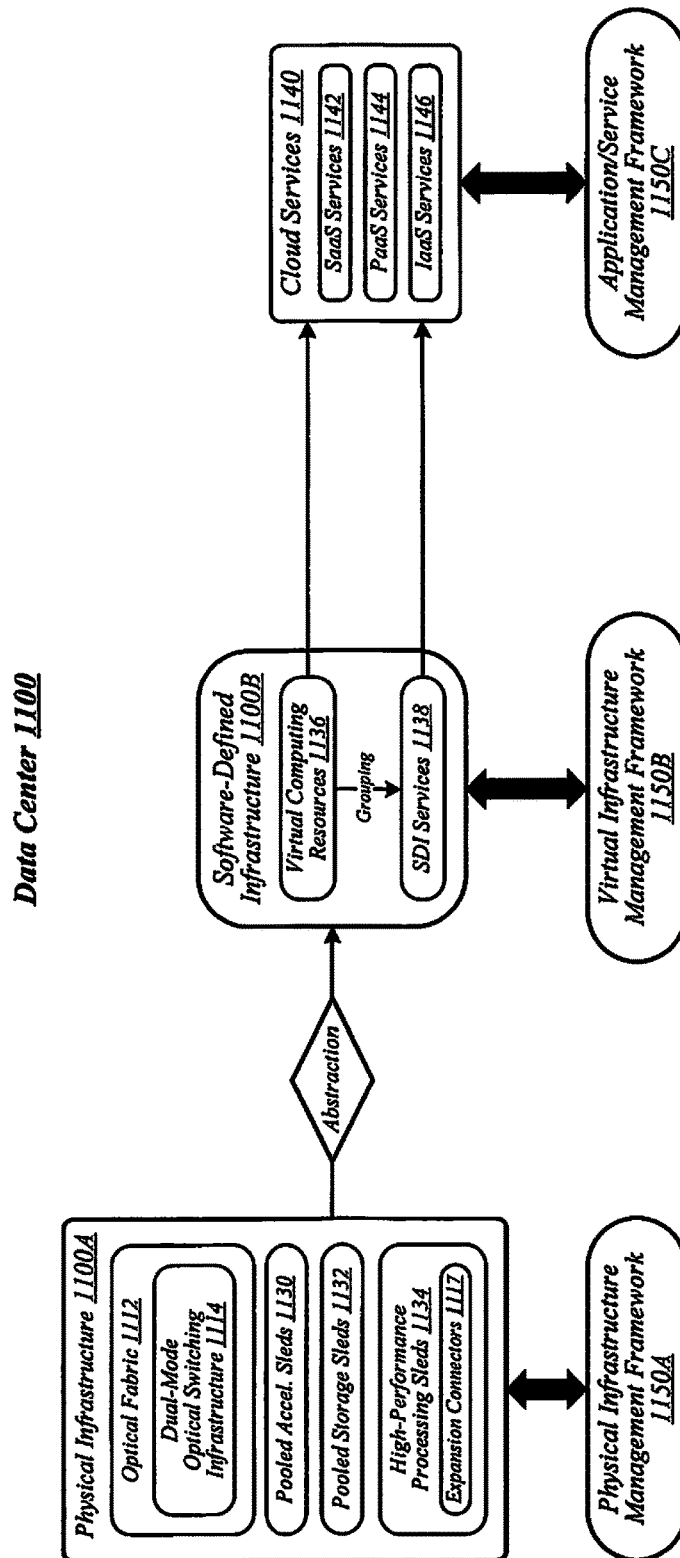


FIG. 11

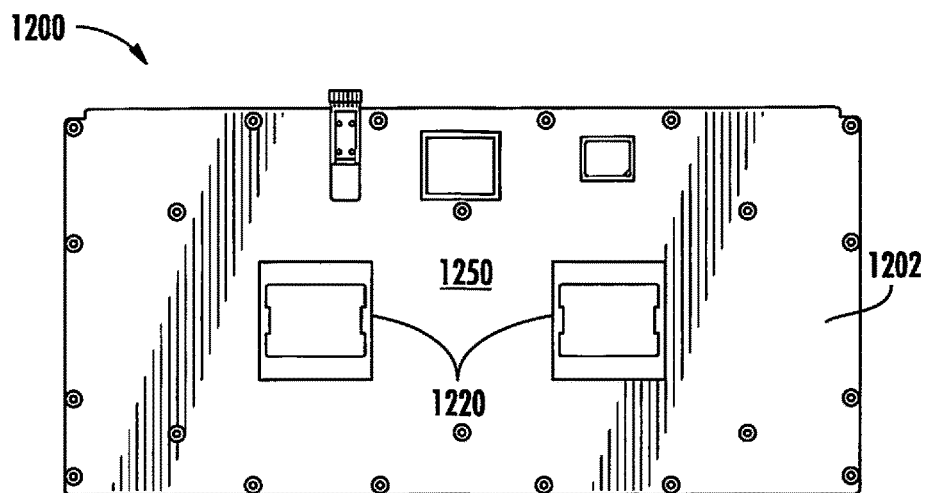


FIG. 12A

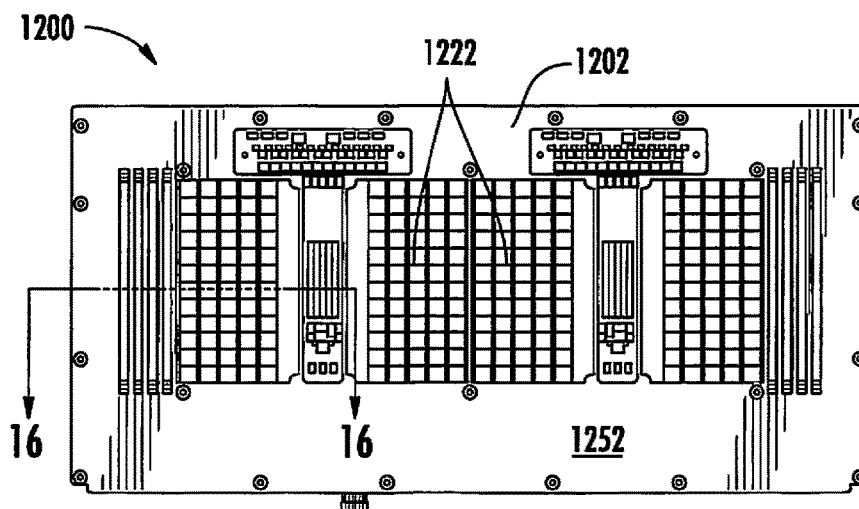
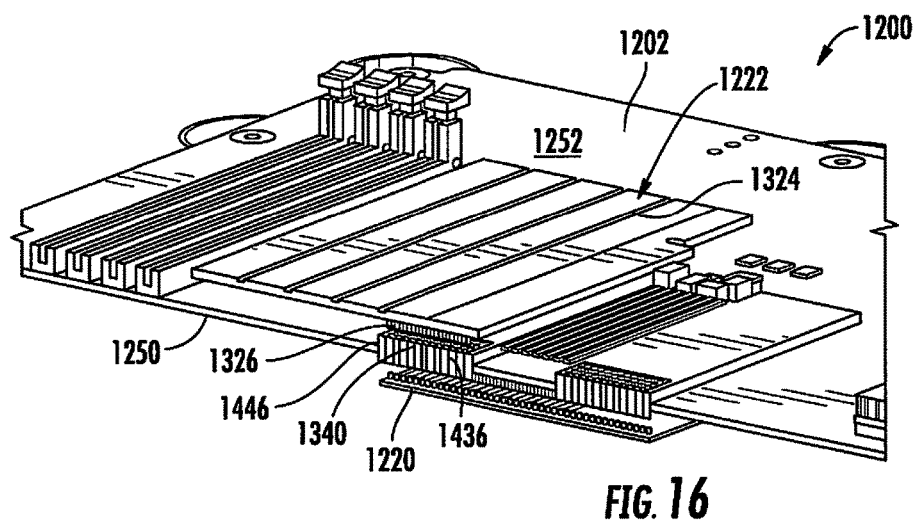
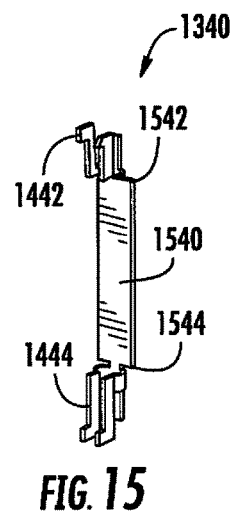
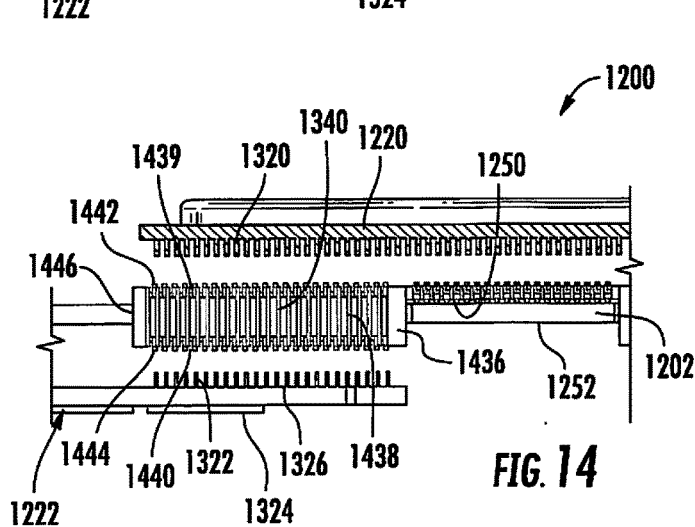
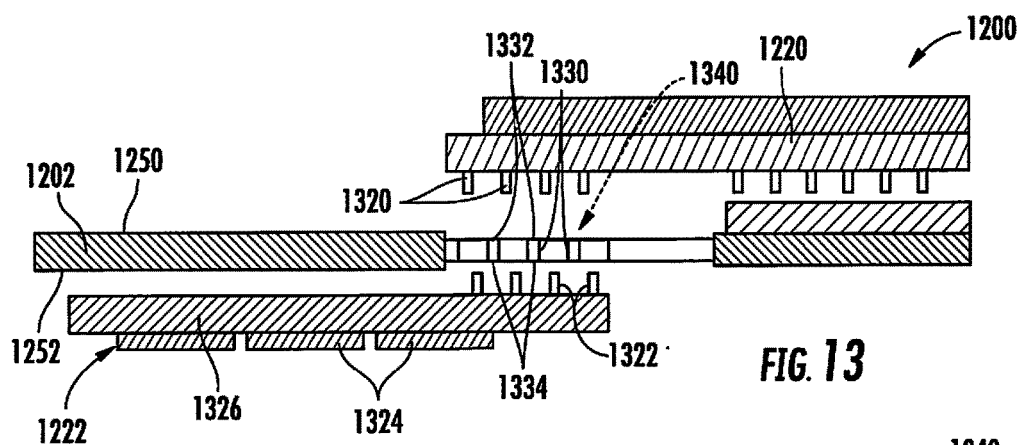
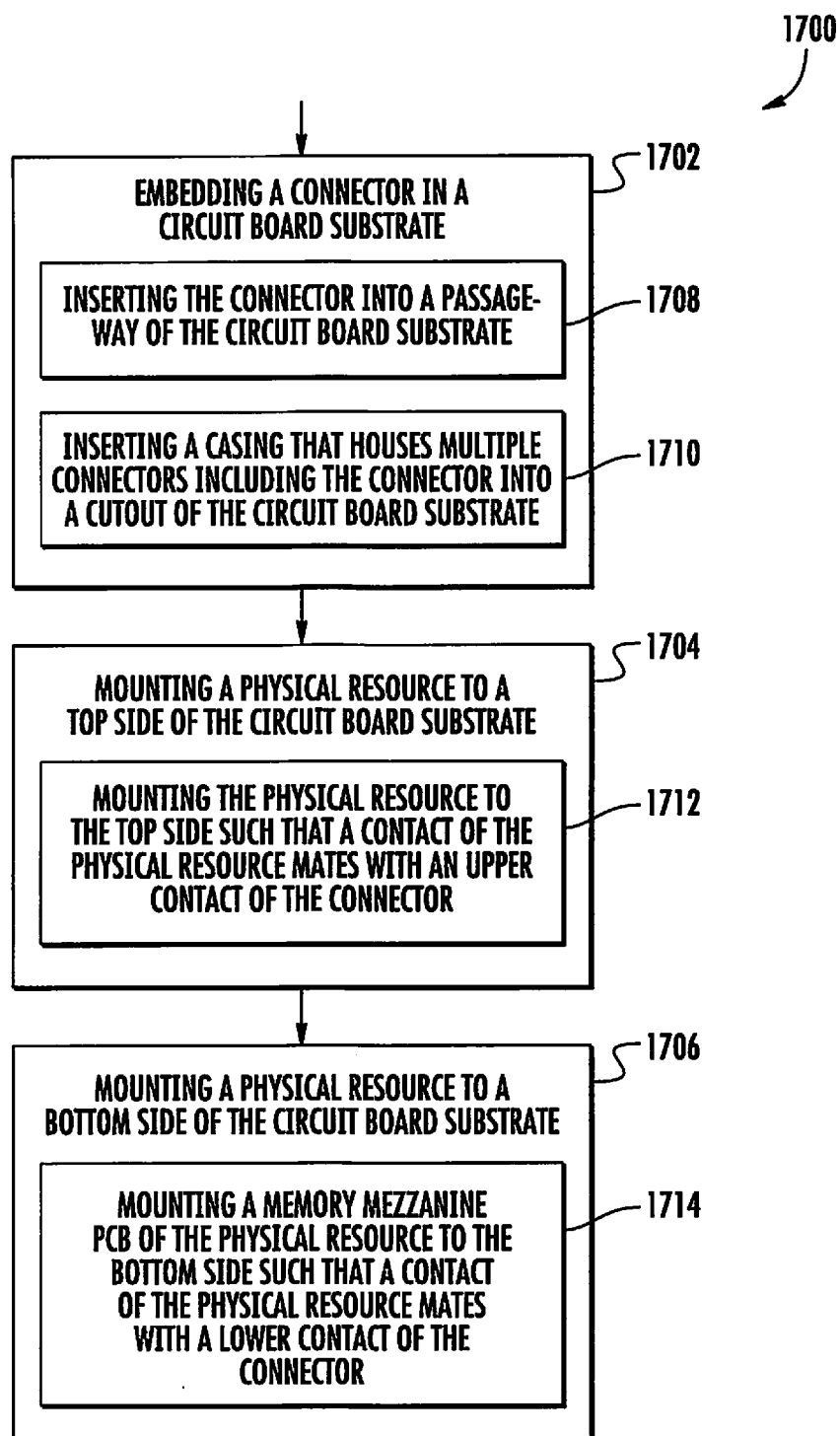
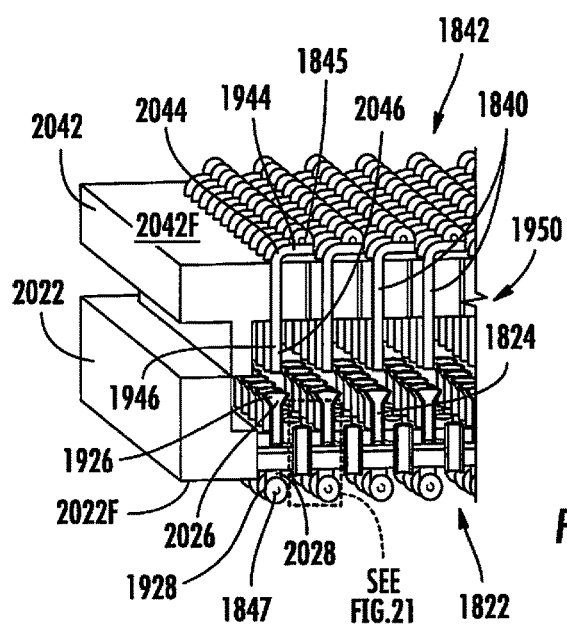
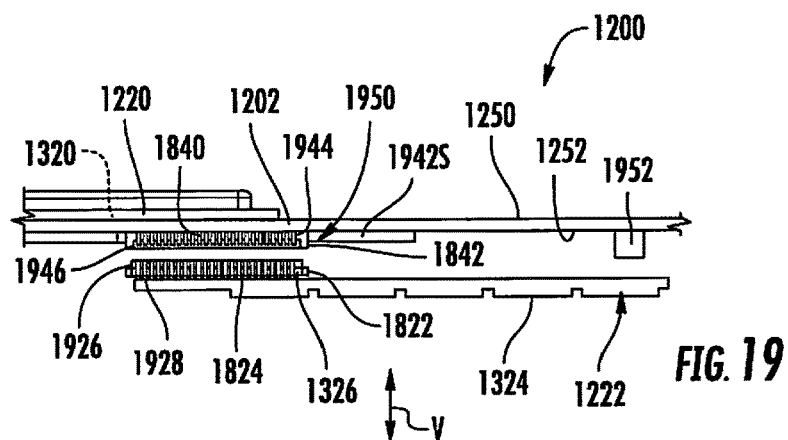
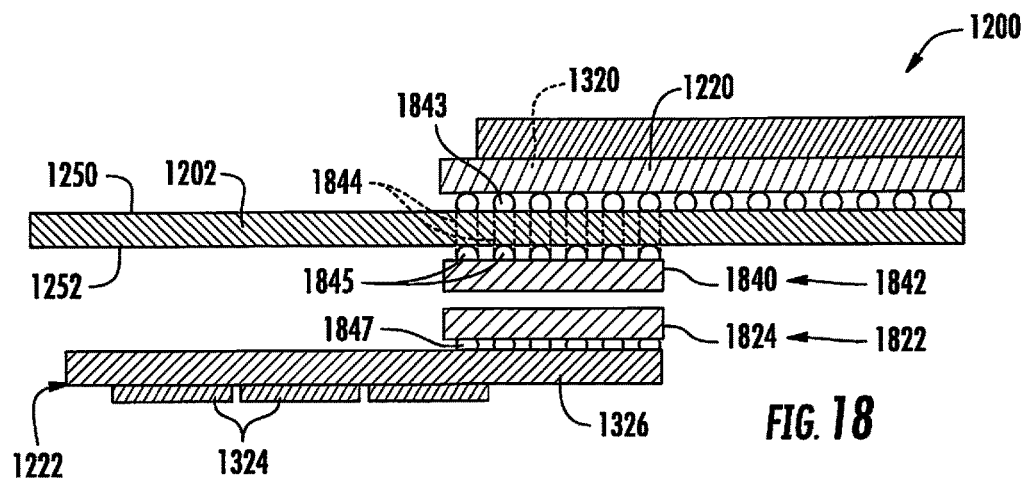


FIG. 12B





**FIG. 17**



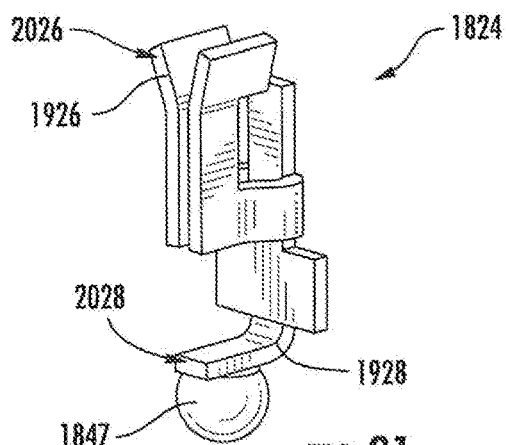


FIG. 21

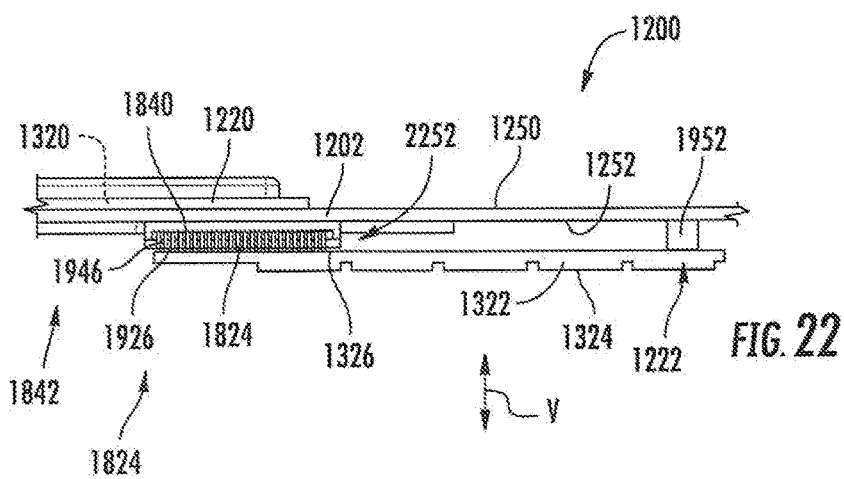


FIG. 22

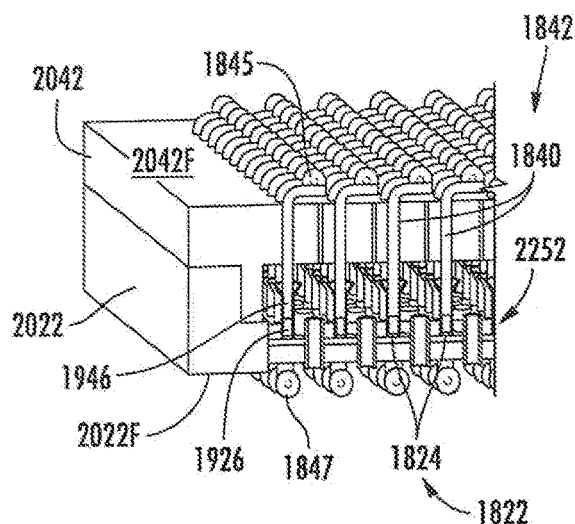


FIG. 23

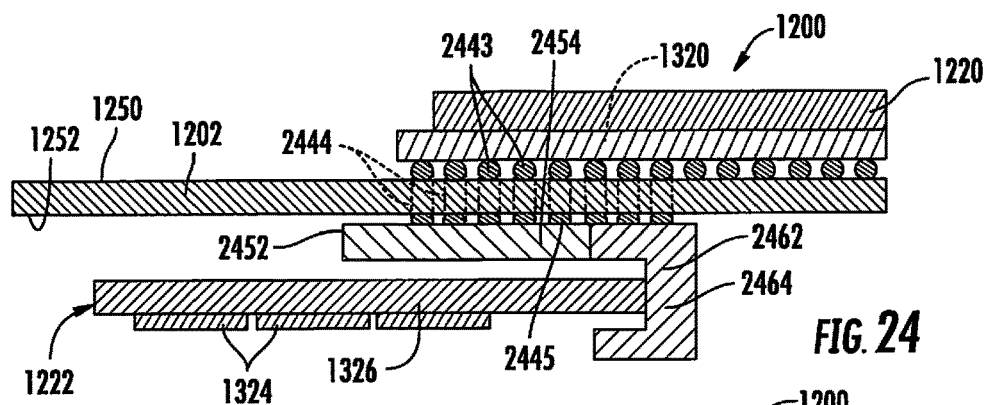


FIG. 24

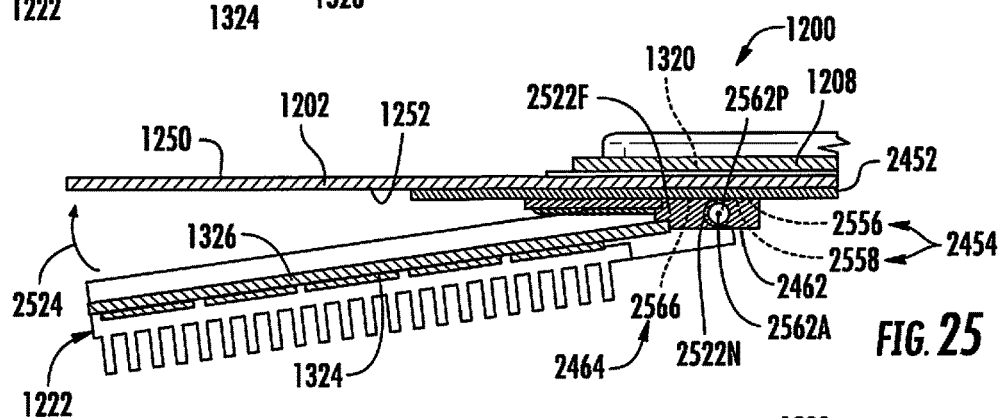


FIG. 25

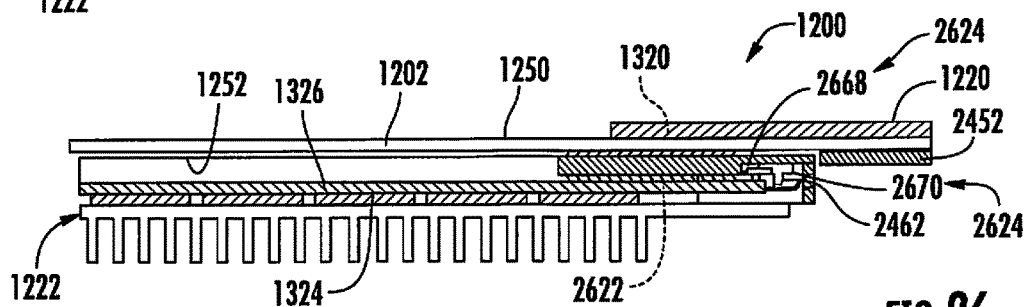


FIG. 26

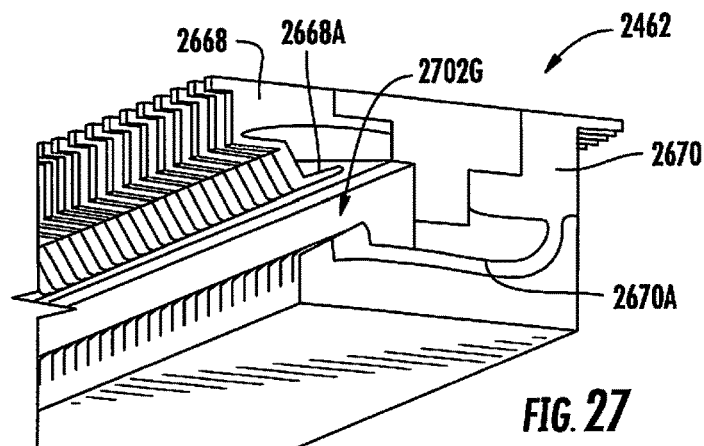


FIG. 27

## MEMORY MEZZANINE CONNECTORS

### CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefit of Indian Provisional Patent Application No. 201741030632, filed Aug. 30, 2017, and U.S. Provisional Patent Application No. 62/584,401, filed Nov. 10, 2017.

### BACKGROUND

[0002] Typical enterprise-level data centers can include several to hundreds of racks or cabinets, with each rack/cabinet housing multiple servers. Each of the various servers of a data center may be communicatively connectable to each other via one or more local networking switches, routers, and/or other interconnecting devices, cables, and/or interfaces. The number of racks and servers of a particular data center, as well as the complexity of the design of the data center, may depend on the intended use of the data center, as well as the quality of service the data center is intended to provide.

[0003] Traditional rack systems are self-contained physical support structures that include a number of pre-defined server spaces. A corresponding server may be mounted in each pre-defined server space. Each server may include physical resources and memory devices that interface with one another. Conventional interfaces between physical resources and memory devices may complicate service of the servers and be associated with undesirable maintenance and/or repair costs.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The concepts described herein are illustrated by way of example and not by way of limitation in the accompanying figures. For simplicity and clarity of illustration, elements illustrated in the figures are not necessarily drawn to scale. Where considered appropriate, reference labels have been repeated among the figures to indicate corresponding or analogous elements.

[0005] FIG. 1 is a diagram of a conceptual overview of a data center in which one or more techniques described herein may be implemented according to various embodiments;

[0006] FIG. 2 is a diagram of an example embodiment of a logical configuration of a rack of the data center of FIG. 1;

[0007] FIG. 3 is a diagram of an example embodiment of another data center in which one or more techniques described herein may be implemented according to various embodiments;

[0008] FIG. 4 is a diagram of another example embodiment of a data center in which one or more techniques described herein may be implemented according to various embodiments;

[0009] FIG. 5 is a diagram of a connectivity scheme representative of link-layer connectivity that may be established among various sleds of the data centers of FIGS. 1, 3, and 4;

[0010] FIG. 6 is a diagram of a rack architecture that may be representative of an architecture of any particular one of the racks depicted in FIGS. 1-4 according to some embodiments;

[0011] FIG. 7 is a diagram of an example embodiment of a sled that may be used with the rack architecture of FIG. 6;

[0012] FIG. 8 is a diagram of an example embodiment of a rack architecture to provide support for sleds featuring expansion capabilities;

[0013] FIG. 9 is a diagram of an example embodiment of a rack implemented according to the rack architecture of FIG. 8;

[0014] FIG. 10 is a diagram of an example embodiment of a sled designed for use in conjunction with the rack of FIG. 9;

[0015] FIG. 11 is a diagram of an example embodiment of a data center in which one or more techniques described herein may be implemented according to various embodiments;

[0016] FIG. 12A is an elevation view of a top side of a sled designed for use in conjunction with at least one of the racks depicted in FIGS. 1-4 and 9;

[0017] FIG. 12B is an elevation view of a bottom side of the sled of FIG. 12A;

[0018] FIG. 13 is a diagrammatic view of one embodiment of the sled shown in FIG. 12 with passageways formed in a circuit board substrate of the sled that are sized to receive multiple connectors;

[0019] FIG. 14 is a side elevation view of another embodiment of the sled shown in FIG. 12 with a cutout formed in a circuit board substrate of the sled that is sized to receive a casing that houses multiple connectors;

[0020] FIG. 15 is a perspective view of a connector for use with at least one of the sleds shown in FIGS. 13 and 14;

[0021] FIG. 16 is a sectional view of the sled shown in FIG. 12 taken about line 16-16 with the casing received by the cutout formed in the circuit board substrate of the sled;

[0022] FIG. 17 is a simplified flowchart of a method of mounting a plurality of physical resources to the circuit board substrate of the sled shown in FIG. 12;

[0023] FIG. 18 is a diagrammatic view of another embodiment of the sled shown in FIG. 12 that includes a connector socket for use with another connector socket of a memory device;

[0024] FIG. 19 is a side elevation view of the sled shown in FIG. 18 with the connector socket spaced from the connector socket of the memory device;

[0025] FIG. 20 is a perspective view of connectors of the respective sockets shown in FIG. 18 spaced from one another;

[0026] FIG. 21 is a detail view of one of the connectors of FIG. 20;

[0027] FIG. 22 is a side elevation view of the sled shown in FIG. 18 with the connector socket mated with the connector socket of the memory device;

[0028] FIG. 23 is a perspective view of the connectors of the respective sockets shown in FIG. 18 mated with one another;

[0029] FIG. 24 is a diagrammatic view of yet another embodiment of the sled shown in FIG. 12 that includes a pair of connector sockets;

[0030] FIG. 25 is a side elevation view of the sled shown in FIG. 24 with a memory device partially received by one of the connector sockets;

[0031] FIG. 26 is a sectional view of the sled shown in FIG. 24 taken about line 26-26 with the memory device fully received by the one of the connector sockets; and

[0032] FIG. 27 is a magnified perspective view of a portion of the connector socket shown in FIG. 26 that receives the memory device.

#### DETAILED DESCRIPTION OF THE DRAWINGS

[0033] While the concepts of the present disclosure are susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and will be described herein in detail. It should be understood, however, that there is no intent to limit the concepts of the present disclosure to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives consistent with the present disclosure and the appended claims.

[0034] References in the specification to “one embodiment,” “an embodiment,” “an illustrative embodiment,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may or may not necessarily include that particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to effect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described. Additionally, it should be appreciated that items included in a list in the form of “at least one A, B, and C” can mean (A); (B); (C); (A and B); (A and C); (B and C); or (A, B, and C). Similarly, items listed in the form of “at least one of A, B, or C” can mean (A); (B); (C); (A and B); (A and C); (B and C); or (A, B, and C).

[0035] The disclosed embodiments may be implemented, in some cases, in hardware, firmware, software, or any combination thereof. The disclosed embodiments may also be implemented as instructions carried by or stored on a transitory or non-transitory machine-readable (e.g., computer-readable) storage medium, which may be read and executed by one or more processors. A machine-readable storage medium may be embodied as any storage device, mechanism, or other physical structure for storing or transmitting information in a form readable by a machine (e.g., a volatile or non-volatile memory, a media disc, or other media device).

[0036] In the drawings, some structural or method features may be shown in specific arrangements and/or orderings. However, it should be appreciated that such specific arrangements and/or orderings may not be required. Rather, in some embodiments, such features may be arranged in a different manner and/or order than shown in the illustrative figures. Additionally, the inclusion of a structural or method feature in a particular figure is not meant to imply that such feature is required in all embodiments and, in some embodiments, may not be included or may be combined with other features.

[0037] FIG. 1 illustrates a conceptual overview of a data center 100 that may generally be representative of a data center or other type of computing network in/for which one or more techniques described herein may be implemented according to various embodiments. As shown in FIG. 1, data center 100 may generally contain a plurality of racks, each of which may house computing equipment comprising a respective set of physical resources. In the particular non-

limiting example depicted in FIG. 1, data center 100 contains four racks 102A to 102D, which house computing equipment comprising respective sets of physical resources (PCRs) 105A to 105D. According to this example, a collective set of physical resources 106 of data center 100 includes the various sets of physical resources 105A to 105D that are distributed among racks 102A to 102D. Physical resources 106 may include resources of multiple types, such as—for example—processors, co-processors, accelerators, field programmable gate arrays (FPGAs), memory, and storage. The embodiments are not limited to these examples.

[0038] The illustrative data center 100 differs from typical data centers in many ways. For example, in the illustrative embodiment, the circuit boards (“sleds”) on which components such as CPUs, memory, and other components are placed are designed for increased thermal performance. In particular, in the illustrative embodiment, the sleds are shallower than typical boards. In other words, the sleds are shorter from the front to the back, where cooling fans are located. This decreases the length of the path that air must to travel across the components on the board. Further, the components on the sled are spaced further apart than in typical circuit boards, and the components are arranged to reduce or eliminate shadowing (i.e., one component in the air flow path of another component). In the illustrative embodiment, processing components such as the processors are located on a top side of a sled while near memory, such as DIMMs, are located on a bottom side of the sled. As a result of the enhanced airflow provided by this design, the components may operate at higher frequencies and power levels than in typical systems, thereby increasing performance. Furthermore, the sleds are configured to blindly mate with power and data communication cables in each rack 102A, 102B, 102C, 102D, enhancing their ability to be quickly removed, upgraded, reinstalled, and/or replaced. Similarly, individual components located on the sleds, such as processors, accelerators, memory, and data storage drives, are configured to be easily upgraded due to their increased spacing from each other. In the illustrative embodiment, the components additionally include hardware attestation features to prove their authenticity.

[0039] Furthermore, in the illustrative embodiment, the data center 100 utilizes a single network architecture (“fabric”) that supports multiple other network architectures including Ethernet and Omni-Path. The sleds, in the illustrative embodiment, are coupled to switches via optical fibers, which provide higher bandwidth and lower latency than typical twisted pair cabling (e.g., Category 5, Category 5e, Category 6, etc.). Due to the high bandwidth, low latency interconnections and network architecture, the data center 100 may, in use, pool resources, such as memory, accelerators (e.g., graphics accelerators, FPGAs, ASICs, etc.), and data storage drives that are physically disaggregated, and provide them to compute resources (e.g., processors) on an as needed basis, enabling the compute resources to access the pooled resources as if they were local. The illustrative data center 100 additionally receives utilization information for the various resources, predicts resource utilization for different types of workloads based on past resource utilization, and dynamically reallocates the resources based on this information.

[0040] The racks 102A, 102B, 102C, 102D of the data center 100 may include physical design features that facilitate the automation of a variety of types of maintenance

tasks. For example, data center **100** may be implemented using racks that are designed to be robotically-accessed, and to accept and house robotically-manipulatable resource sleds. Furthermore, in the illustrative embodiment, the racks **102A**, **102B**, **102C**, **102D** include integrated power sources that receive a greater voltage than is typical for power sources. The increased voltage enables the power sources to provide additional power to the components on each sled, enabling the components to operate at higher than typical frequencies.

[0041] FIG. 2 illustrates an exemplary logical configuration of a rack **202** of the data center **100**. As shown in FIG. 2, rack **202** may generally house a plurality of sleds, each of which may comprise a respective set of physical resources. In the particular non-limiting example depicted in FIG. 2, rack **202** houses sleds **204-1** to **204-4** comprising respective sets of physical resources **205-1** to **205-4**, each of which constitutes a portion of the collective set of physical resources **206** comprised in rack **202**. With respect to FIG. 1, if rack **202** is representative of—for example—rack **102A**, then physical resources **206** may correspond to the physical resources **105A** comprised in rack **102A**. In the context of this example, physical resources **105A** may thus be made up of the respective sets of physical resources, including physical storage resources **205-1**, physical accelerator resources **205-2**, physical memory resources **205-3**, and physical compute resources **205-5** comprised in the sleds **204-1** to **204-4** of rack **202**. The embodiments are not limited to this example. Each sled may contain a pool of each of the various types of physical resources (e.g., compute, memory, accelerator, storage). By having robotically accessible and robotically manipulatable sleds comprising disaggregated resources, each type of resource can be upgraded independently of each other and at their own optimized refresh rate.

[0042] FIG. 3 illustrates an example of a data center **300** that may generally be representative of one in/for which one or more techniques described herein may be implemented according to various embodiments. In the particular non-limiting example depicted in FIG. 3, data center **300** comprises racks **302-1** to **302-32**. In various embodiments, the racks of data center **300** may be arranged in such fashion as to define and/or accommodate various access pathways. For example, as shown in FIG. 3, the racks of data center **300** may be arranged in such fashion as to define and/or accommodate access pathways **311A**, **311B**, **311C**, and **311D**. In some embodiments, the presence of such access pathways may generally enable automated maintenance equipment, such as robotic maintenance equipment, to physically access the computing equipment housed in the various racks of data center **300** and perform automated maintenance tasks (e.g., replace a failed sled, upgrade a sled). In various embodiments, the dimensions of access pathways **311A**, **311B**, **311C**, and **311D**, the dimensions of racks **302-1** to **302-32**, and/or one or more other aspects of the physical layout of data center **300** may be selected to facilitate such automated operations. The embodiments are not limited in this context.

[0043] FIG. 4 illustrates an example of a data center **400** that may generally be representative of one in/for which one or more techniques described herein may be implemented according to various embodiments. As shown in FIG. 4, data center **400** may feature an optical fabric **412**. Optical fabric **412** may generally comprise a combination of optical signaling media (such as optical cabling) and optical switching

infrastructure via which any particular sled in data center **400** can send signals to (and receive signals from) each of the other sleds in data center **400**. The signaling connectivity that optical fabric **412** provides to any given sled may include connectivity both to other sleds in a same rack and sleds in other racks. In the particular non-limiting example depicted in FIG. 4, data center **400** includes four racks **402A** to **402D**. Racks **402A** to **402D** house respective pairs of sleds **404A-1** and **404A-2**, **404B-1** and **404B-2**, **404C-1** and **404C-2**, and **404D-1** and **404D-2**. Thus, in this example, data center **400** comprises a total of eight sleds. Via optical fabric **412**, each such sled may possess signaling connectivity with each of the seven other sleds in data center **400**. For example, via optical fabric **412**, sled **404A-1** in rack **402A** may possess signaling connectivity with sled **404A-2** in rack **402A**, as well as the six other sleds **404B-1**, **404B-2**, **404C-1**, **404C-2**, **404D-1**, and **404D-2** that are distributed among the other racks **402B**, **402C**, and **402D** of data center **400**. The embodiments are not limited to this example.

[0044] FIG. 5 illustrates an overview of a connectivity scheme **500** that may generally be representative of link-layer connectivity that may be established in some embodiments among the various sleds of a data center, such as any of example data centers **100**, **300**, and **400** of FIGS. 1, 3, and 4. Connectivity scheme **500** may be implemented using an optical fabric that features a dual-mode optical switching infrastructure **514**. Dual-mode optical switching infrastructure **514** may generally comprise a switching infrastructure that is capable of receiving communications according to multiple link-layer protocols via a same unified set of optical signaling media, and properly switching such communications. In various embodiments, dual-mode optical switching infrastructure **514** may be implemented using one or more dual-mode optical switches **515**. In various embodiments, dual-mode optical switches **515** may generally comprise high-radix switches. In some embodiments, dual-mode optical switches **515** may comprise multi-ply switches, such as four-ply switches. In various embodiments, dual-mode optical switches **515** may feature integrated silicon photonics that enable them to switch communications with significantly reduced latency in comparison to conventional switching devices. In some embodiments, dual-mode optical switches **515** may constitute leaf switches **530** in a leaf-spine architecture additionally including one or more dual-mode optical spine switches **520**.

[0045] In various embodiments, dual-mode optical switches may be capable of receiving both Ethernet protocol communications carrying Internet Protocol (IP packets) and communications according to a second, high-performance computing (HPC) link-layer protocol (e.g., Intel's Omni-Path Architecture's, Infiniband) via optical signaling media of an optical fabric. As reflected in FIG. 5, with respect to any particular pair of sleds **504A** and **504B** possessing optical signaling connectivity to the optical fabric, connectivity scheme **500** may thus provide support for link-layer connectivity via both Ethernet links and HPC links. Thus, both Ethernet and HPC communications can be supported by a single high-bandwidth, low-latency switch fabric. The embodiments are not limited to this example.

[0046] FIG. 6 illustrates a general overview of a rack architecture **600** that may be representative of an architecture of any particular one of the racks depicted in FIGS. 1 to 4 according to some embodiments. As reflected in FIG. 6, rack architecture **600** may generally feature a plurality of

sled spaces into which sleds may be inserted, each of which may be robotically-accessible via a rack access region 601. In the particular non-limiting example depicted in FIG. 6, rack architecture 600 features five sled spaces 603-1 to 603-5. Sled spaces 603-1 to 603-5 feature respective multi-purpose connector modules (MPCMs) 616-1 to 616-5.

[0047] FIG. 7 illustrates an example of a sled 704 that may be representative of a sled of such a type. As shown in FIG. 7, sled 704 may comprise a set of physical resources 705, as well as an MPCM 716 designed to couple with a counterpart MPCM when sled 704 is inserted into a sled space such as any of sled spaces 603-1 to 603-5 of FIG. 6. Sled 704 may also feature an expansion connector 717. Expansion connector 717 may generally comprise a socket, slot, or other type of connection element that is capable of accepting one or more types of expansion modules, such as an expansion sled 718. By coupling with a counterpart connector on expansion sled 718, expansion connector 717 may provide physical resources 705 with access to supplemental computing resources 705B residing on expansion sled 718. The embodiments are not limited in this context.

[0048] FIG. 8 illustrates an example of a rack architecture 800 that may be representative of a rack architecture that may be implemented in order to provide support for sleds featuring expansion capabilities, such as sled 704 of FIG. 7. In the particular non-limiting example depicted in FIG. 8, rack architecture 800 includes seven sled spaces 803-1 to 803-7, which feature respective MPCMs 816-1 to 816-7. Sled spaces 803-1 to 803-7 include respective primary regions 803-1A to 803-7A and respective expansion regions 803-1B to 803-7B. With respect to each such sled space, when the corresponding MPCM is coupled with a counterpart MPCM of an inserted sled, the primary region may generally constitute a region of the sled space that physically accommodates the inserted sled. The expansion region may generally constitute a region of the sled space that can physically accommodate an expansion module, such as expansion sled 718 of FIG. 7, in the event that the inserted sled is configured with such a module.

[0049] FIG. 9 illustrates an example of a rack 902 that may be representative of a rack implemented according to rack architecture 800 of FIG. 8 according to some embodiments. In the particular non-limiting example depicted in FIG. 9, rack 902 features seven sled spaces 903-1 to 903-7, which include respective primary regions 903-1A to 903-7A and respective expansion regions 903-1B to 903-7B. In various embodiments, temperature control in rack 902 may be implemented using an air cooling system. For example, as reflected in FIG. 9, rack 902 may feature a plurality of fans 919 that are generally arranged to provide air cooling within the various sled spaces 903-1 to 903-7. In some embodiments, the height of the sled space is greater than the conventional "1U" server height. In such embodiments, fans 919 may generally comprise relatively slow, large diameter cooling fans as compared to fans used in conventional rack configurations. Running larger diameter cooling fans at lower speeds may increase fan lifetime relative to smaller diameter cooling fans running at higher speeds while still providing the same amount of cooling. The sleds are physically shallower than conventional rack dimensions. Further, components are arranged on each sled to reduce thermal shadowing (i.e., not arranged serially in the direction of air flow). As a result, the wider, shallower sleds allow for an increase in device performance because the devices can be

operated at a higher thermal envelope (e.g., 250 W) due to improved cooling (i.e., no thermal shadowing, more space between devices, more room for larger heat sinks, etc.).

[0050] MPCMs 916-1 to 916-7 may be configured to provide inserted sleds with access to power sourced by respective power modules 920-1 to 920-7, each of which may draw power from an external power source 921. In various embodiments, external power source 921 may deliver alternating current (AC) power to rack 902, and power modules 920-1 to 920-7 may be configured to convert such AC power to direct current (DC) power to be sourced to inserted sleds. In some embodiments, for example, power modules 920-1 to 920-7 may be configured to convert 277-volt AC power into 12-volt DC power for provision to inserted sleds via respective MPCMs 916-1 to 916-7. The embodiments are not limited to this example.

[0051] MPCMs 916-1 to 916-7 may also be arranged to provide inserted sleds with optical signaling connectivity to a dual-mode optical switching infrastructure 914, which may be the same as—or similar to—dual-mode optical switching infrastructure 514 of FIG. 5. In various embodiments, optical connectors contained in MPCMs 916-1 to 916-7 may be designed to couple with counterpart optical connectors contained in MPCMs of inserted sleds to provide such sleds with optical signaling connectivity to dual-mode optical switching infrastructure 914 via respective lengths of optical cabling 922-1 to 922-7. In some embodiments, each such length of optical cabling may extend from its corresponding MPCM to an optical interconnect loom 923 that is external to the sled spaces of rack 902. In various embodiments, optical interconnect loom 923 may be arranged to pass through a support post or other type of load-bearing element of rack 902. The embodiments are not limited in this context. Because inserted sleds connect to an optical switching infrastructure via MPCMs, the resources typically spent in manually configuring the rack cabling to accommodate a newly inserted sled can be saved.

[0052] FIG. 10 illustrates an example of a sled 1004 that may be representative of a sled designed for use in conjunction with rack 902 of FIG. 9 according to some embodiments. Sled 1004 may feature an MPCM 1016 that comprises an optical connector 1016A and a power connector 1016B, and that is designed to couple with a counterpart MPCM of a sled space in conjunction with insertion of MPCM 1016 into that sled space. Coupling MPCM 1016 with such a counterpart MPCM may cause power connector 1016 to couple with a power connector comprised in the counterpart MPCM. This may generally enable physical resources 1005 of sled 1004 to source power from an external source, via power connector 1016 and power transmission media 1024 that conductively couples power connector 1016 to physical resources 1005.

[0053] Sled 1004 may also include dual-mode optical network interface circuitry 1026. Dual-mode optical network interface circuitry 1026 may generally comprise circuitry that is capable of communicating over optical signaling media according to each of multiple link-layer protocols supported by dual-mode optical switching infrastructure 914 of FIG. 9. In some embodiments, dual-mode optical network interface circuitry 1026 may be capable both of Ethernet protocol communications and of communications according to a second, high-performance protocol. In various embodiments, dual-mode optical network interface circuitry 1026 may include one or more optical transceiver modules 1027,

each of which may be capable of transmitting and receiving optical signals over each of one or more optical channels. The embodiments are not limited in this context.

**[0054]** Coupling MPCM **1016** with a counterpart MPCM of a sled space in a given rack may cause optical connector **1016A** to couple with an optical connector comprised in the counterpart MPCM. This may generally establish optical connectivity between optical cabling of the sled and dual-mode optical network interface circuitry **1026**, via each of a set of optical channels **1025**. Dual-mode optical network interface circuitry **1026** may communicate with the physical resources **1005** of sled **1004** via electrical signaling media. **1028**. In addition to the dimensions of the sleds and arrangement of components on the sleds to provide improved cooling and enable operation at a relatively higher thermal envelope (e.g., 250 W), as described above with reference to FIG. 9, in sonic embodiments, a sled may include one or more additional features to facilitate air cooling, such as a heatpipe and/or heat sinks arranged to dissipate heat generated by physical resources **1005**. It is worthy of note that although the example sled **1004** depicted in FIG. 10 does not feature an expansion connector, any given sled that features the design elements of sled **1004** may also feature an expansion connector according to some embodiments. The embodiments are not limited in this context.

**[0055]** FIG. 11 illustrates an example of a data center **1100** that may generally be representative of one in/for which one or more techniques described herein may be implemented according to various embodiments. As reflected in FIG. 11, a physical infrastructure management framework **1150A** may be implemented to facilitate management of a physical infrastructure **1100A** of data center **1100**. In various embodiments, one function of physical infrastructure management framework **1150A** may be to manage automated maintenance functions within data center **1100**, such as the use of robotic maintenance equipment to service computing equipment within physical infrastructure **1100A**. In some embodiments, physical infrastructure **1100A** may feature an advanced telemetry system that performs telemetry reporting that is sufficiently robust to support remote automated management of physical infrastructure **1100A**. In various embodiments, telemetry information provided by such an advanced telemetry system may support features such as failure prediction/prevention capabilities and capacity planning capabilities. In some embodiments, physical infrastructure management framework **1150A** may also be configured to manage authentication of physical infrastructure components using hardware attestation techniques. For example, robots may verify the authenticity of components before installation by analyzing information collected from a radio frequency identification (RFID) tag associated with each component to be installed. The embodiments are not limited in this context.

**[0056]** As shown in FIG. 11, the physical infrastructure **1100A** of data center **1100** may comprise an optical fabric **1112**, which may include a dual-mode optical switching infrastructure **1114**. Optical fabric **1112** and dual-mode optical switching infrastructure **1114** may be the same as—or similar to—optical fabric **412** of FIG. 4 and dual-mode optical switching infrastructure **514** of FIG. 5, respectively, and may provide high-bandwidth, low-latency, multi-protocol connectivity among sleds of data center **1100**. As discussed above, with reference to FIG. 1, in various embodiments, the availability of such connectivity may

make it feasible to disaggregate and dynamically pool resources such as accelerators, memory, and storage. In some embodiments, for example, one or more pooled accelerator sleds **1130** may be included among the physical infrastructure **1100A** of data center **1100**, each of which may comprise a pool of accelerator resources—such as co-processors and/or FPGAs, for example—that is globally accessible to other sleds via optical fabric **1112** and dual-mode optical switching infrastructure **1114**.

**[0057]** In another example, in various embodiments, one or more pooled storage sleds **1132** may be included among the physical infrastructure **1100A** of data center **1100**, each of which may comprise a pool of storage resources that is globally accessible to other sleds via optical fabric **1112** and dual-mode optical switching infrastructure **1114**. In some embodiments, such pooled storage sleds **1132** may comprise pools of solid-state storage devices such as solid-state drives (SSDs). In various embodiments, one or more high-performance processing sleds **1134** may be included among the physical infrastructure **1100A** of data center **1100**. In some embodiments, high-performance processing sleds **1134** may comprise pools of high-performance processors, as well as cooling features that enhance air cooling to yield a higher thermal envelope of up to 250 W or more. In various embodiments, any given high-performance processing sled **1134** may feature an expansion connector **1117** that can accept a far memory expansion sled, such that the far memory that is locally available to that high-performance processing sled **1134** is disaggregated from the processors and near memory comprised on that sled. In some embodiments, such a high-performance processing sled **1134** may be configured with far memory using an expansion sled that comprises low-latency SSD storage. The optical infrastructure allows for compute resources on one sled to utilize remote accelerator/FPGA, memory, and/or SSD resources that are disaggregated on a sled located on the same rack or any other rack in the data center. The remote resources can be located one switch jump away or two-switch jumps away in the spine-leaf network architecture described above with reference to FIG. 5. The embodiments are not limited in this context.

**[0058]** In various embodiments, one or more layers of abstraction may be applied to the physical resources of physical infrastructure **1100A** in order to define a virtual infrastructure, such as a software-defined infrastructure **1100B**. In some embodiments, virtual computing resources **1136** of software-defined infrastructure **1100B** may be allocated to support the provision of cloud services **1140**. In various embodiments, particular sets of virtual computing resources **1136** may be grouped for provision to cloud services **1140** in the form of SDI services **1138**. Examples of cloud services **1140** may include—without limitation—software as a service (SaaS) services **1142**, platform as a service (PaaS) services **1144**, and infrastructure as a service (IaaS) services **1146**.

**[0059]** In some embodiments, management of software-defined infrastructure **1100B** may be conducted using a virtual infrastructure management framework **1150B**. In various embodiments, virtual infrastructure management framework **1150B** may be designed to implement workload fingerprinting techniques and/or machine-learning techniques in conjunction with managing allocation of virtual computing resources **1136** and/or SDI services **1138** to cloud services **1140**. In some embodiments, virtual infrastructure

management framework 1150B may use/consult telemetry data in conjunction with performing such resource allocation. In various embodiments, an application/service management framework 1150C may be implemented in order to provide QoS management capabilities for cloud services 1140. The embodiments are not limited in this context.

[0060] Referring now to FIGS. 12A and 12B, each of the sleds 204, 404, 504, 704, 1004 may be embodied as a sled 1200 in some embodiments. As discussed in more detail below, the sled 1200 is configured to be mounted in a corresponding rack 102, 202, 302, 402, 902 of the data center 100, 300, 400, 1100. In some embodiments, the sled 1200 may be optimized or otherwise configured for performing particular tasks, such as compute tasks, acceleration tasks, data storage tasks, etc. For example, in the illustrative embodiment, the sled 1200 is embodied as a compute sled that includes various physical resources on a “top side” and a “bottom side” of the sled 1200.

[0061] The illustrative sled 1200 includes a chassis-less circuit board substrate 1202, which supports various electrical components mounted thereon. It should be appreciated that the circuit board substrate 1202 is “chassis-less” in that the sled 1200 does not include a housing or enclosure. Rather, the circuit board substrate 1202 is open to the local environment. The circuit board substrate 1202 may be formed from any material capable of supporting the various electrical components mounted thereon. For example, in an illustrative embodiment, the circuit board substrate 1202 is formed from an FR-4 glass-reinforced epoxy laminate material. Of course, other materials may be used to form the circuit board substrate 1202 in other embodiments.

[0062] The illustrative sled 1200 includes one or more physical resources 1220 mounted to a “top side” 1250 of the circuit board substrate 1202. Although two physical resources 1220 are shown in FIG. 12A, it should be appreciated that the sled 1200 may include one, two, or more physical resources 1220 in other embodiments. The physical resources 1220 may be embodied as any type of processor, controller, or other compute circuit capable of performing various tasks such as compute functions and/or controlling the functions of the sled 1200 depending on, for example, the type or intended functionality of the sled 1200. For example, as discussed in more detail below, the physical resources 1220 may be embodied as high-power processors in embodiments in which the sled 1200 is embodied as a compute sled, as accelerator co-processors or circuits in embodiments in which the sled 1200 is embodied as an accelerator sled, and/or storage controllers in embodiments in which the sled 1200 is embodied as a storage sled. Again, depending on the type or intended functionality of the sled 1200, the sled 1200 may include one or more additional components, such as, but not limited to, a communication circuit having a network interface controller, physical resources in addition to those discussed above, an input/output (I/O) subsystem, a power connector, and one or more data storage drives. In any case, it should be appreciated that each of the physical resources 1220 may include, or otherwise be embodied as, a packaged device that has features capable of interfacing with another device to facilitate interconnection between the devices.

[0063] Referring now to FIG. 12B, in addition to the physical resources 1220 mounted on the top side 1250 of the circuit board substrate 1202, the sled 1200 also includes one or more physical resources 1222. The one or more physical

resources 1222 are illustratively embodied as memory devices 1222. Each memory device 1222 illustratively includes a memory package 1324 (see FIG. 13) and a memory mezzanine PCB (i.e., a printed circuit board) 1326 on which the memory package 1324 is mounted. The memory mezzanine PCB 1326 faces a “bottom side” 1252 of the circuit board substrate 1202. As such, the circuit board substrate 1202 is embodied as a double-sided circuit board.

[0064] Because the memory devices 1222 include the memory packages 1324 mounted on the memory mezzanine PCB 1326, the memory devices 1222 may be said to include, or otherwise be embodied as, one or more memory mezzanine devices, or simply memory mezzanines. The memory devices 1222 may be embodied as any type of memory device capable of storing data for the physical resources 1220 during operation of the sled 1200. For example, in the illustrative embodiments, the memory devices 1222 are embodied as dual in-line memory modules (DIMMs), which may support DDR, DDR2, DDR3, DDR4, or DDR5 random access memory (RAM). Of course, in other embodiments, the memory devices 1222 may utilize other memory technologies, including volatile and/or non-volatile memory. For example, types of volatile memory may include, but are not limited to, data rate synchronous dynamic RAM (DDR SDRAM), static random-access memory (SRAM), thyristor RAM (T-RAM) or zero-capacitor RAM (Z-RAM). Types of non-volatile memory may include byte or block addressable types of non-volatile memory. The byte or block addressable types of non-volatile memory may include, but are not limited to, 3-dimensional (3-D) cross-point memory, memory that uses chalcogenide phase change material (e.g., chalcogenide glass), multi-threshold level NAND flash memory, NOR flash memory, single or multi-level phase change memory (PCM), resistive memory, nanowire memory, ferroelectric transistor random access memory (FeTRAM), magnetoresistive random access memory (MRAM) memory that incorporates memristor technology, or spin transfer torque MRAM (STT-MRAM), or a combination of any of the above, or other non-volatile memory types. In any case, similar to the physical resources 1220, it should be appreciated that each of the physical resources 1222 may include, or otherwise be embodied as, a packaged device that has features capable of interfacing with another device to facilitate interconnection between the devices.

[0065] As discussed in more detail below, the physical resources 1220 (e.g., processors) mounted on the top side 1250 are electrically coupled to the memory packages 1324 mounted on the memory mezzanine PCB 1326. To do so, in some embodiments, one or more of the connectors 1340, 1740, 2240 may extend through the circuit board substrate 1202 and interface directly with the one or more physical resources 1220 and the memory mezzanine PCB 1326 to facilitate electrical connection between the one or more physical resources 1220 and the one or more memory devices 1222, as discussed below. In other embodiments, as further discussed below, one or more of the connectors 1340, 1740, 2240 may interface directly with the one or more memory devices 1222 without interfacing directly with the one or more physical resources 1220.

[0066] Referring now to FIG. 13, in some embodiments as discussed above, the sled 1200 includes one or more connectors 1340 to facilitate electrical coupling of the physical resources 1220 facing the top side 1250 with the memory devices 1222 facing the bottom side 1252. In the illustrative

embodiment of FIG. 13, the circuit board substrate 1202 includes multiple passageways 1330 extending there-through. Each passageway 1330 includes an opening 1332 located on the top side 1250 of the circuit board substrate 1202 and an opening 1334 located on the bottom side 1252 of the circuit board substrate 1202. A connector 1340 is inserted into each passageway 1330 such that an upper contact 1442 of the connector 1340 (see FIG. 14) is accessible from the top side 1250 and a lower contact 1444 of the connector 1340 (see FIG. 14) is accessible from the bottom side 1252. In the illustrative embodiment of FIG. 13, the connector 1340 is configured to interface directly with each of the physical resources 1220 coupled to the top side 1250 and the memory mezzanine PCB 1326 of the memory devices 1222 coupled to the bottom side 1252. That is, the upper contact 1442 of each connector 1340 is configured to mate with a corresponding feature or contact 1320 of the physical resource 1220 (e.g., a processor), and the lower contact 1444 of each connector 1340 is configured to mate with a corresponding feature or contact 1322 of the memory device 1222 (i.e., the feature 1322 may be embedded in, included in, or coupled to the memory mezzanine PCB 1326). In some embodiments, portions of the connector 1340 may extend outwardly from the openings 1332, 1334. Additionally, in the illustrative embodiment of FIG. 13, the connector 1340 is configured to interface directly with each of the physical resources 1220 and the memory devices 1222 coupled to the respective top and bottom sides 1250, 1252.

[0067] Referring now to FIG. 15, in the illustrative embodiment, the connector 1340 includes, or is otherwise embodied as, a low insertion force (LIF) connector. The illustrative connector 1340 includes a main body 1540 having a pair of contact sides 1542, 1544 located at opposite ends of the main body 1540. As shown in FIG. 15, the side 1542 includes the electrical contact 1442 that is configured to interface or mate with the corresponding feature or contact 1320 of the physical resource 1220. Similarly, the side 1544 includes the electrical contact 1444 that is configured to interface or mate with the corresponding feature or contact 1322 of the memory device 1222.

[0068] Although the illustrative connector 1340 is embodied as a LIF connector, the connector 1340 may be embodied as another suitable connector in other embodiments, such as a zero insertion force (ZIF) connector, for example. Furthermore, in some embodiments, the electrical contacts 1442, 1444 of the respective contact sides 1542, 1544 of the illustrative connector 1340 may be arranged in a pin grid array (PGA) package. In such embodiments, the corresponding features 1320 of the one or more physical resources 1220 and the corresponding features 1322 of the one or more memory devices 1222 may each be arranged in a PGA package. In other embodiments, the electrical contacts 1442, 1444 may be arranged in another suitable package.

[0069] Referring now to FIG. 14, in some embodiments, the sled 1200 may include a housing or casing 1436 that houses multiple connectors 1340. The casing 1436 may include, or otherwise be embodied as, any structure capable of housing and/or protecting the connectors 1340. The casing 1436 is illustratively formed from one or more polymeric materials. In other embodiments, however, the casing 1436 may have another suitable construction.

[0070] The casing 1436 is illustratively received by the circuit board substrate 1202 to secure the connector 1340 to the circuit board substrate 1202 between the one or more

physical resources 1220 and the memory mezzanine PCB 1326 of the one or more memory devices 1222, as shown in FIG. 14. As such, in the illustrative embodiment, the circuit board substrate 1202 includes a cutout 1446 that is sized to receive the casing 1436. When the casing 1436 is received by the cutout 1446, the connector 1340 is embedded in, or otherwise inserted into, the circuit board substrate 1202. In some embodiments, a tool (not shown) may be used to insert the casing 1436 into the cutout 1446 to attach the connector 1340 to the circuit board substrate 1202.

[0071] In the illustrative embodiment, the casing 1436 is removable from the cutout 1446 to electrically decouple the one or more physical resources 1220 from the one or more memory devices 1222. As such, the connector 1340 includes, or is otherwise embodied as, a separable or removable interconnect between the physical resources 1220 and the memory devices 1222. During service of the sled 1200, the casing 1436 and the connector 1340 may be removed to facilitate access to the physical resources 1220 and/or the memory devices 1222 for repair and/or replacement. In some instances, such as when components (e.g., one or more of the memory devices 1222) of the sled 1200 are damaged, those components may be repaired and/or replaced with little or no impact to the connector 1340, which may be removed beforehand. The illustrative connector 1340 may therefore mitigate service and/or reliability costs associated with the sled 1200 to a greater degree than other configurations.

[0072] The casing 1436 illustratively includes multiple passageways 1438 with each passageway 1438 having an opening or aperture 1439 located on, or otherwise accessible from, the top side 1250 of the circuit board substrate 1202 and an opening or aperture 1440 located on, or otherwise accessible from, the bottom side 1252 of the circuit board substrate 1202. A connector 1340 is inserted into each passageway 1438 such that the upper contact 1442 of the connector 1340 is accessible from the top side 1250 and the lower contact 1444 is accessible from the bottom side 1252 when the casing 1436 is received by the cutout 1446 of the circuit board substrate 1202. That is, when the casing 1436 is received by the cutout 1446, the electrical contacts 1442 of the contact side 1542 of each connector 1340 extend through, or are otherwise accessible through, the openings 1439 from the top side 1250 of the circuit board substrate 1202. In addition, when the casing 1436 is received by the cutout 1446, the electrical contacts 1444 of the contact side 1544 of each connector 1340 extend through, or are otherwise accessible through, the apertures 1440 from the bottom side 1252 of the circuit board substrate 1202.

[0073] Referring now to FIG. 16, a cross-sectional view of the illustrative sled 1200 is shown with the bottom side 1252 facing upward and the casing 1436 received by the cutout 1446 such that each connector 1340 is secured between a physical resource 1220 and a memory mezzanine PCB 1326 of a memory device 1222. In the illustrative embodiment, when the casing 1436 is received by the cutout 1446, the physical resource 1220 is electrically coupled to the memory device 1222 by the connectors 1340 of the casing 1436. In this way, the casing 1436 forms a connector socket for the physical resource(s) 1220 and the memory device(s) 1222. In some embodiments, the casing 1436 and associated connectors 1340 provide the electrical coupling between the physical resources 1220 and the memory devices 1222 without provision of heat sink to dissipate heat associated

with operation of the connector 1340. Because a heat sink need not be provided to dissipate heat associated with operation of the connectors 1340 in some embodiments, the sled 1200 may include fewer components in the illustrative configuration than in other configurations.

[0074] Referring now to FIG. 17, an illustrative method 1700 of mounting the physical resources 1220, 1222 to the circuit board substrate 1202 is shown. The method 1700 may be performed by a robot or installer to mount a physical resource 1220 and a physical resource 1222 to the circuit board substrate 1202. Of course, it should be appreciated that the method 1700 may be performed to mount multiple physical resources 1220 and multiple physical resources 1222 to the circuit board substrate 1202. Additionally, it should be appreciated that the method 1700 may be performed in a number of sequences other than the sequence described below.

[0075] The method 1700 begins with block 1702, in which the connector 1340 is embedded in the circuit board substrate 1202. In some embodiments (e.g., as described above with reference to FIG. 13), block 1702 may be performed by inserting the connector 1340 into one of the passageways 1330 formed in the circuit board substrate 1202, as indicated by sub-block 1708. In such embodiments, the connector 1340 may be inserted into the passageway 1330 such that the upper contact 1442 of the connector 1340 is accessible from the top side 1250 of the circuit board substrate 1202 and the lower contact 1444 of the connector 1340 is accessible from the bottom side 1252 of the circuit board substrate 1202. In other embodiments (e.g., as described above with reference to FIG. 14), block 1702 may be performed by inserting the casing 1436 into the cutout 1446 formed in the circuit board substrate 1202, as indicated by sub-block 1710. In those embodiments, the casing 1436 may be inserted into the cutout 1446 such that the upper contacts 1442 of the connectors 1340 housed by the casing 1436 are accessible from the top side 1250 of the circuit board substrate 1202 and the lower contacts 1444 of the connectors 1340 housed by the casing 1436 are accessible from the bottom side 1252 of the circuit board substrate 1202.

[0076] It should be appreciated that subsequent to embedding the connector 1340 in the circuit board substrate 1202, the connector 1340 may be removed by a robot or installer for servicing, repair, and/or replacement. That is, the connector 1340 may be removed from the passageway 1330 in some embodiments, and the casing 1436 that houses multiple connectors 1340 may be removed from the cutout 1446 in other embodiments, for example.

[0077] From the block 1702, the method 1700 subsequently proceeds to the block 1704. In the block 1704, the physical resource 1220 is mounted to the top side 1250 of the circuit board substrate 1202. To do so, the physical resource 1220 may be mounted to the top side 1250 such that a contact 1320 of the physical resource 1220 mates with the upper contact 1442 of the connector 1340, as indicated by sub-block 1712.

[0078] It should be appreciated that subsequent to mounting the physical resource 1220 to the top side 1250 of the circuit board substrate 1202, the physical resource 1220 may be removed by a robot or installer for servicing, repair, and/or replacement. That is, the physical resource 1220 may be removed from the top side 1250 such that the contact 1320 of the physical resource 1220 is de-coupled from the contact 1442 of the connector 1340.

[0079] From the block 1704, the method 1700 subsequently proceeds to the block 1706. In the block 1706, the physical resource 1222 is mounted to the bottom side 1252 of the circuit board substrate 1202. To do so, the memory mezzanine PCB 1326 of the memory device 1222 may be mounted to the bottom side 1252 such that a contact 1322 of the physical resource 1222 mates with the lower contact 1444 of the connector 1340, as indicated by sub-block 1714.

[0080] It should be appreciated that subsequent to mounting the physical resource 1222 to the bottom side 1252 of the circuit board substrate 1202, the physical resource 1222 may be removed by a robot or installer for servicing, repair, and/or replacement. That is, the physical resource 1222 may be removed from the bottom side 1252 such that the contact 1322 of the physical resource 1222 is de-coupled from the contact 1444 of the connector 1340.

[0081] Referring now to FIG. 18, in some embodiments as discussed above, the sled 1200 includes one or more connectors 1840 to facilitate electrical coupling of a physical resource 1220 coupled to the top side 1250 with a memory device 1222 coupled to the bottom side 1252. Of course, in some embodiments, the one or more connectors 1840 may facilitate electrical coupling of one or more physical resources 1220 with one or more memory devices 1222. In the illustrative embodiment of FIG. 18, the connectors 1840 are grouped together or housed in a connector socket 1842, which is electrically coupled to the bottom side 1252 of the circuit board substrate 1202 and coupled to the memory mezzanine PCB 1326 of the memory device 1222.

[0082] Each of the illustrative connectors 1840 may include, or otherwise be embodied as, any device capable of interfacing with the physical resource 1220 and the memory mezzanine PCB 1326 of the memory device 1222 to electrically couple the physical resource 1220 to the memory device 1222. In the illustrative embodiment, the connector socket 1842 does not extend through, and is not embedded in, the circuit board substrate 1202. Rather, as will be apparent from the discussion below, the connector socket 1842 is arranged beneath the bottom side 1252 of the circuit board substrate 1202 and electrically coupled (e.g., soldered) thereto.

[0083] In the illustrative embodiment, the circuit board substrate 1202 is arranged between the physical resource 1220 and the connector socket 1842. Moreover, the connector socket 1842 is illustratively arranged between the bottom side 1252 of the circuit board substrate 1202 and the memory mezzanine PCB 1326 of the memory device 1222.

[0084] It should be appreciated that, as shown in FIG. 18, the physical resource 1220 does not directly interface with, and is not affixed or attached to, the connector socket 1842. Rather, the physical resource 1220 interfaces with vias 1844 included in the circuit board substrate 1202 along the top side 1250 of the circuit board substrate 1202. The vias 1844 extend from the top side 1250 to the bottom side 1252 of the circuit board substrate 1202 to electrically couple the top side 1250 to the bottom side 1252. As such, in the illustrative embodiment, the vias 1844 include, or are otherwise embodied as, through-hole vias. In other embodiments, however, the vias 1844, or a portion thereof, may include, or otherwise be embodied as, other suitable vias, such as blind vias or buried vias, for example.

[0085] Each of the vias 1844 is electrically coupled to a corresponding electrical contact 1320 (shown in phantom) of the physical resource 1220, such as a processor pin or a

contact of another connector socket located on the top side 1250 of the circuit board substrate 1202. Specifically, each of the vias 1844 is electrically coupled to a corresponding electrical contact 1320 of the physical resource 1220 (or of another connector socket) by a soldering ball 1843. The soldering balls 1843 are illustratively arranged between the physical resource 1220 and the top side 1250 of the circuit board substrate 1202 to affix and electrically connect the physical resource 1220 to the top side 1250. Soldering balls 1845 are also illustratively arranged between the bottom side 1252 of the circuit board substrate 1202 and the connector socket 1842 to affix and electrically connect the connector socket 1842 to the bottom side 1252.

[0086] In the illustrative embodiment of FIG. 18, the memory device 1222 includes a corresponding connector socket 1822 that includes connectors 1824. The connector socket 1822 and the connectors 1824 may be mounted to, embedded in, or otherwise inserted into the memory mezzanine PCB 1326. The connector socket 1822 is configured to interface or mate with the connector socket 1842 to electrically couple the physical resource 1220 to the memory device 1222, as further discussed below.

[0087] Referring now to FIG. 20, each of the connectors 1840 of the connector socket 1842 illustratively includes, or is otherwise embodied as, a low insertion force (LIF) connector. In other embodiments, however, each of the connectors 1840 of the connector socket 1842 may include, or otherwise be embodied as, another suitable connector, such as a zero insertion force (ZIF) connector, pins, or the like.

[0088] The connectors 1824 are illustratively grouped together or housed in the connector socket 1822 of the memory device 1222, as shown in FIG. 20. Each of the connectors 1824 of the connector socket 1822 illustratively includes, or is otherwise embodied as, a low insertion force (LIF) connector. In other embodiments, however, each of the connectors 1824 of the connector socket 1822 may include, or otherwise be embodied as, another suitable connector, such as a zero insertion force (ZIF) connector, for example.

[0089] Each of the illustrative connectors 1840 of the connector socket 1842 includes a contact side 2044 and a contact side 2046 arranged opposite the contact side 2044. The contact side 2044 includes an electrical contact 1944 (see FIG. 19) that is electrically coupled to a corresponding via 1844 of the circuit board substrate 1202 through a corresponding soldering ball 1845. In some embodiments, each electrical contact 1944 may be electrically coupled to a corresponding via 1844 through a corresponding solder ball 1845 and a connector socket substrate 1942S. The contact side 2046 includes an electrical contact 1946 (see FIG. 19) that extends away from the bottom side 1252 of the circuit board substrate 1202 and is configured to mate with an electrical contact 1926 of a corresponding connector 1824 of the connector socket 1822.

[0090] Each of the illustrative connectors 1824 of the connector socket 1822 includes a contact side 2026 and a contact side 2028 arranged opposite the contact side 2026, as best seen in FIG. 21. The contact side 2026 includes the electrical contact 1926 and the contact side 2028 includes an electrical contact 1928. A solder ball 1847 may be coupled to the contact side 2028 of each of the connectors 1824.

[0091] The connectors 1840 of the connector socket 1842 are illustratively supported by a connector carrier 2042 that may be housed by, or otherwise included in, a housing (not

shown). The contact sides 2044 of the connectors 1840 extend outwardly from a top face 2042F of the contact carrier 2042 such that the electrical contacts 1944 are arranged outwardly of the top face 2042F. The soldering balls 1845 are coupled to the electrical contacts 1944 and arranged outwardly of the top face 2042F.

[0092] The connectors 1824 of the connector socket 1822 are illustratively supported by a connector carrier 2022 that may be housed by, or otherwise included in, a housing. The contact sides 2028 of the connectors 1824 extend outwardly from a bottom face 2022F of the contact carrier 2022 such that the electrical contacts 1928 are arranged outwardly of the bottom face 2022F. The soldering balls 1847 are coupled to the electrical contacts 1928 and arranged outwardly of the bottom face 2022F.

[0093] Referring now to FIG. 19, each of the electrical contacts 1944 of the connectors 1840 of the connector socket 1842 is electrically coupled to a corresponding electrical contact 1320 of the physical resource 1220. In an illustrative de-coupled state 1950 of the sled 1200, the electrical contacts 1946 of the connectors 1840 of the connector socket 1842 are spaced from the electrical contacts 1926 of the connectors 1824 of the connector socket 1822 in a vertical direction V. The connector sockets 1842, 1822 are therefore electrically de-coupled from one another in the state 1950, as shown in FIGS. 19 and 20. As such, the physical resource 1220 is electrically de-coupled from the memory device 1222 in the de-coupled state 1950.

[0094] A standoff 1952 is illustratively affixed to the bottom side 1252 of the circuit board substrate 1202. In some embodiments, the standoff 1952 may constrain movement of the connector socket 1842 in the vertical direction V relative to the connector socket 1822, or vice versa. In such embodiments, the standoff 1952 may facilitate mating of the electrical contacts 1946 with the electrical contacts 1926. In other embodiments, the standoff 1952 may elevate the circuit board substrate 1202 above a support surface (not shown) to facilitate mounting of one or more components to the circuit board substrate 1202, among other things.

[0095] Referring now to FIGS. 22 and 23, in an illustrative coupled state 2252 of the sled 1200, the electrical contacts 1946 of the connectors 1840 of the connector socket 1842 are mated with the electrical contacts 1926 of the connectors 1824 of the connector socket 1822. Accordingly, the physical resource 1220 is electrically coupled to the memory device 1222 in the coupled state 2252. The standoff 1952 contacts the memory device 1222 in the coupled state 2252. Contact between the standoff 1952 and the memory device 1222 may secure the position of the electrical contacts 1946 in the vertical direction V relative to the electrical contacts 1926 or vice versa, to facilitate mating between the connector sockets 1842, 1822. Additionally, when the sled 1200 is in the coupled state 2252, the connector carrier 2042 contacts the connector carrier 2022.

[0096] In some embodiments, the electrical contacts 1944, 1946 of the connectors 1840 of the connector socket 1842 may be arranged in a pin grid array (PGA) package. Similarly, in some embodiments, the electrical contacts 1926, 1928 of the connectors 1824 of the connector socket 1822 may be arranged in a pin grid array (PGA) package. In other embodiments, however, the electrical contacts 1944, 1946, as well as the electrical contacts 1926, 1928, may be arranged in another suitable package.

[0097] In the illustrative embodiment, the physical resource 1220 may be electrically coupled to the memory device 1222 by the connector socket 1842 without provision of heat sink to dissipate heat associated with operation of the connector socket 1842. Because a heat sink need not be provided to dissipate heat associated with operation of the connector 1842, the sled 1200 may include fewer components in the illustrative configuration than in other configurations.

[0098] Referring now to FIG. 24, connector sockets 2452, 2462 may be included in the sled 1200 in yet another embodiment thereof. The connector sockets 2452, 2462 may include respective connectors 2454, 2464 that may include, or otherwise be embodied as, any devices capable of cooperatively interfacing with the physical resource 1220 and the memory mezzanine PCB 1326 of the memory device 1222 to electrically couple the physical resource 1220 to the memory device 1222. Of course, in some embodiments, the connectors 2454, 2464 may cooperatively electrically couple one or more physical resources 1220 to one or more memory devices 1222. In the illustrative embodiment, the connector sockets 2452, 2462 do not extend through, and are not embedded in, the circuit board substrate 1202. Rather, as will be apparent from the discussion below, the connector sockets 2452, 2462 are arranged beneath the bottom side 1252 of the circuit board substrate 1202.

[0099] In the illustrative embodiment, the circuit board substrate 1202 is arranged between the physical resource 1220 and the connector sockets 2452, 2462. Moreover, the connector sockets 2452, 2462 illustratively extend between the bottom side 1252 of the circuit board substrate 1202 and the memory mezzanine PCB 1326 of the memory device 1222.

[0100] The physical resource 1220 does not directly interface with, and is not affixed or attached to, the connector sockets 2452, 2462, as shown in FIG. 24. Rather, the physical resource 1220 interfaces with vias 2444 included in the circuit board substrate 1202 along the top side 1250 of the circuit board substrate 1202. The vias 2444 extend from the top side 1250 to the bottom side 1252 of the circuit board substrate 1202 to electrically couple the top side 1250 to the bottom side 1252. As such, in the illustrative embodiment, the vias 2444 include, or are otherwise embodied as, through hole vias. In other embodiments, however, the vias 2444 may include, or otherwise be embodied as, other suitable vias, such as blind vias or buried vias, for example.

[0101] Each of the vias 2444 is electrically coupled to a corresponding electrical contact 1320 (shown in phantom) of the physical resource 1220. Specifically, each of the vias 2444 is electrically coupled to a corresponding electrical contact 1320 of the physical resource 1220 by a soldering ball 2443. The soldering balls 2443 are illustratively arranged between the physical resource 1220 and the top side 1250 of the circuit board substrate 1202 to affix the physical resource 1220 to the top side 1250. Soldering balls 2445 are also illustratively arranged between the bottom side 1252 of the circuit board substrate 1202 and the connector sockets 2452, 2462 to affix the connector sockets 2452, 2462 to the bottom side 1252. The connector sockets 2452, 2462 are affixed to the bottom side 1252 of the circuit board substrate 1202 adjacent to one another.

[0102] The illustrative connector socket 2452 may include, or otherwise be embodied as, any device or physical interface capable of interfacing with the physical resource

1220 and the connector socket 2462 to electrically couple the physical resource 1220 to the connector socket 2462. The illustrative connector socket 2462 may include, or otherwise be embodied as, any device or physical interface capable of interfacing with the connector socket 2452 and the memory mezzanine PCB 1326 of the memory device 1222 to electrically couple the connector socket 2452 to the memory device 1222.

[0103] Referring now to FIG. 25, each connector 2454 of the illustrative connector socket 2452 includes an electrical contact 2556 (shown in phantom) and an electrical contact 2558 (shown in phantom) arranged opposite the electrical contact 2556. In some embodiments, each electrical contact 2556 may be a pin or solder pad electrically coupled to a corresponding soldering ball 2445 and via 2444. Each electrical contact 2558 may extend away from each electrical contact 2556 and the bottom side 1252 of the circuit board substrate 1202. When the memory device 1222 is received by the connector socket 2462, each electrical contact 2558 may be configured to mate or interface with a corresponding contact 2622 (see FIG. 26) of the memory device 1222 that may be mounted to the memory mezzanine PCB 1326.

[0104] In the illustrative embodiment, the electrical contacts 2556, 2558 of the connectors 2454 of the connector socket 2452 are arranged in a land grid array (LGA) package. As such, the illustrative connector socket 2452 may include, or otherwise be embodied as, an LGA connector socket. In other embodiments, the electrical contacts 2556, 2558 may be arranged in another suitable package, and the connector socket 2452 may include, or otherwise be embodied as, another suitable connector socket.

[0105] In the illustrative embodiment, the connector socket 2462 is sized to receive the memory mezzanine PCB 1326 of the memory device 1222, as shown in FIG. 25. Each connector 2464 of the connector socket 2462 includes an electrical contact 2566 (shown in phantom) that is electrically coupled to a corresponding via 2444 and soldering ball 2445.

[0106] In the illustrative embodiment, the connector socket 2462 defines a gap 2702G (see FIG. 27) that is sized to receive the memory mezzanine PCB 1326 of the memory device 1222. The connector socket 2462 includes a pair of cylindrical pivot posts 2562P, only one of which is shown in FIG. 25. The illustrative memory device 1222 (e.g., the memory mezzanine PCB 1326) includes a pair of flanges 2522F each having a notch 2522N formed therein (only one of the flanges 2522F is shown) that is sized to receive one of the pivot posts 2562P. When the notches 2522N receive the pivot posts 2562P, the memory device 1222 (e.g., the memory mezzanine PCB 1326) may be pivoted on the pivot posts 2562P about an axis 2562A that extends into the page toward the bottom side 1252 of the circuit board substrate 1202, as indicated by arrow 2524.

[0107] Referring now to FIGS. 26 and 27, the memory device 1222 is pivoted on the pivot posts 2562P about the axis 2562A toward the bottom side 1252 of the circuit board substrate 1202 until the memory mezzanine PCB 1326 of the memory device 1222 is fully received by the gap 2702G. In the illustrative embodiment, the gap 2702G is defined between electrical contacts 2668, 2670 of the connector socket 2462 that are vertically spaced from one another, as best seen in FIG. 27. The electrical contacts 2668 and 2670 provide the illustrative features 2624 of the memory inter-

face **2624**. One of the electrical contacts **2566**, **2668**, **2670** of the connector socket **2462** may be configured to mate or interface with the electrical contact **2558** of the connector socket **2452**.

**[0108]** When the memory device **1222** is fully received by the gap **2702G**, the memory mezzanine PCB **1326** of the memory device **1222** contacts each of the electrical contacts **2668**, **2670** of the connector socket **2462**, as shown in FIG. **26**. Specifically, the memory mezzanine PCB **1326** contacts respective cantilevered contact arms **2668A**, **2670A** of the electrical contacts **2668**, **2670**. The contact arms **2668A**, **2670A** may cooperate to hold the memory device **1222** in place when the memory mezzanine PCB **1326** is fully received by the gap **2702G**.

**[0109]** In the illustrative embodiment, the connector socket **2462** includes, or is otherwise embodied as, a small outline dual in-line memory module (SODIMM) connector. In other embodiments, however, the connector socket **2462** may include, or otherwise be embodied as, another suitable connector.

#### EXAMPLES

**[0110]** Illustrative examples of the technologies disclosed herein are provided below. An embodiment of the technologies may include any one or more, and any combination of, the examples described below.

**[0111]** Example 1 includes a sled for operation in a rack of a data center, the sled comprising a circuit board substrate having a top side and a bottom side opposite the top side; a physical resource coupled to the top side of the circuit board substrate; a memory device coupled to the bottom side of the circuit board substrate; and a connector to electrically couple the physical resource to the memory device, wherein the connector extends through the circuit board substrate to the top and bottom sides thereof, and wherein the connector comprises (i) a first contact accessible from the top side of the circuit board substrate and electrically mated with a corresponding contact of the physical resource and (ii) a second contact, opposite the first contact, accessible from the bottom side of the circuit board substrate and electrically mated with a corresponding contact of the memory device.

**[0112]** Example 2 includes the subject matter of Example 1, and wherein the connector comprises a low insertion force connector.

**[0113]** Example 3 includes the subject matter of any of Examples 1 and 2, and wherein the circuit board substrate comprises a passageway extending through the circuit board substrate and having a first opening located on the top side and a second opening, opposite the first opening, located on the bottom side, wherein the connector is inserted into the passageway of the circuit board substrate.

**[0114]** Example 4 includes the subject matter of any of Examples 1-3, and wherein the first contact of the connector extends outwardly from the first opening and the second contact of the connector extends outwardly from the second opening.

**[0115]** Example 5 includes the subject matter of any of Examples 1-4, and wherein the connector is coupled directly to the circuit board substrate.

**[0116]** Example 6 includes the subject matter of any of Examples 1-5, and further including a casing that houses a plurality of connectors that includes the connector.

**[0117]** Example 7 includes the subject matter of any of Examples 1-6, and wherein the casing is formed from a polymeric material.

**[0118]** Example 8 includes the subject matter of any of Examples 1-7, and wherein the circuit board substrate includes a cutout sized to receive the casing to secure the casing and connector to the circuit board substrate between the physical resource and the memory device.

**[0119]** Example 9 includes the subject matter of any of Examples 1-8, and wherein the casing is secured to the circuit board substrate to electrically couple the one or more physical resources to the one or more memory devices by the connector without provision of a heat sink to dissipate heat associated with operation of the connector.

**[0120]** Example 10 includes the subject matter of any of Examples 1-9, and wherein the casing is removable from the cutout to electrically decouple the one or more physical resources from the one or more memory devices.

**[0121]** Example 11 includes the subject matter of any of Examples 1-10, and wherein the casing comprises a plurality of passageways and each of the plurality of connectors is inserted into a corresponding passageway.

**[0122]** Example 12 includes the subject matter of any of Examples 1-11, and wherein each passageway includes a first opening located on the top side of the circuit board substrate and a second opening, opposite the first opening, located on the bottom side of the circuit board substrate, and wherein each first contact of each connector extends from the first opening of the corresponding passageway and each second contact of each connector extends from the second opening of the corresponding passageway.

**[0123]** Example 13 includes the subject matter of any of Examples 1-12, and wherein the physical resource comprises a processor.

**[0124]** Example 14 includes a sled for operation in a rack of a data center, the sled comprising a circuit board substrate having a top side and a bottom side opposite the top side, wherein the circuit board substrate comprises a plurality of vias extending therethrough; a physical resource coupled to the top side of the circuit board substrate and comprising a plurality of contacts, wherein each contact of the plurality of contacts of the physical resource is electrically coupled to a corresponding via of the circuit board substrate; a memory mezzanine comprising a plurality of contacts; and a connector socket coupled to the bottom side of the circuit board substrate, wherein the connector socket comprises a plurality of connectors and each connector comprises (i) a first contact electrically coupled to a corresponding via of the circuit board substrate and (ii) a second contact, opposite the first contact, extending away from the bottom side of the circuit board substrate, wherein each second contact is to mate with a corresponding contact of the memory mezzanine.

**[0125]** Example 15 includes the subject matter of Example 14, and wherein the connector socket is arranged between the bottom side of the circuit board substrate and the memory mezzanine.

**[0126]** Example 16 includes the subject matter of any of Examples 14 and 15, and wherein the physical resource is electrically coupled to the memory mezzanine by the connector socket without provision of a heat sink to dissipate heat associated with operation of the connector socket.

[0127] Example 17 includes the subject matter of any of Examples 14-16, and wherein each connector of the connector socket comprises a low insertion force connector.

[0128] Example 18 includes the subject matter of any of Examples 14-17, and wherein the memory mezzanine comprises connector socket having a plurality of connectors, wherein each connector of the connector socket of the memory mezzanine comprises a corresponding contact of the plurality of contacts of the memory mezzanine, wherein the connector socket of the memory mezzanine is to mate with the connector socket coupled to the bottom side of the circuit board substrate.

[0129] Example 19 includes the subject matter of any of Examples 14-18, and wherein each of the connectors of the connector socket of the memory mezzanine comprises a low insertion force connector.

[0130] Example 20 includes the subject matter of any of Examples 14-19, and wherein the connector socket comprises a land grid array socket.

[0131] Example 21 includes the subject matter of any of Examples 14-20, and wherein the connector socket comprises a first connector socket and wherein the sled further comprises a second connector socket coupled to the bottom side of the circuit board substrate adjacent to the first connector socket, wherein the second connector socket is to receive a circuit board substrate of the memory mezzanine and comprises a plurality of connectors and each connector of the second connector socket includes a first contact electrically coupled to a corresponding via of the circuit board substrate.

[0132] Example 22 includes the subject matter of any of Examples 14-21, and wherein the second connector socket comprises second electrical contacts and third electrical contacts vertically spaced from the second electrical contacts to define a gap therebetween.

[0133] Example 23 includes the subject matter of any of Examples 14-22, and wherein each of the second electrical contacts and the third electrical contacts comprise a cantilevered contact arm.

[0134] Example 24 includes the subject matter of any of Examples 14-23, and wherein the second connector socket comprises a small outline dual in-line memory module connector.

[0135] Example 25 includes the subject matter of any of Examples 14-24, and wherein the physical resource comprises a processor.

[0136] Example 26 includes a sled for operation in a rack of a data center, the sled comprising a circuit board substrate having a top side and a bottom side opposite the top side; and a connector to electrically couple a first physical resource located on the top side of the circuit board substrate with a second physical resource located on the bottom side of the circuit board substrate, wherein the connector comprises (i) a first contact accessible from the top side of the circuit board substrate to electrically mate with a corresponding contact of the first physical resource and (ii) a second contact, opposite the first contact, accessible from the bottom side of the circuit board substrate to electrically mate with a corresponding contact of the second physical resource.

[0137] Example 27 includes the subject matter of Example 26, and wherein the connector comprises a low insertion force connector.

[0138] Example 28 includes the subject matter of any of Examples 26 and 27, and wherein the circuit board substrate comprises a passageway extending through the circuit board substrate and having a first opening located on the top side and a second opening, opposite the first opening, located on the bottom side, wherein the connector is inserted into the passageway of the circuit board substrate.

[0139] Example 29 includes the subject matter of any of Examples 26-28, and further including a casing that houses a plurality of connectors that includes the connector.

[0140] Example 30 includes the subject matter of any of Examples 26-29, and wherein the circuit board substrate includes a cutout sized to receive the casing to secure the casing and connector to the circuit board substrate between the first physical resource and the second physical resource.

[0141] Example 31 includes the subject matter of any of Examples 26-30, and wherein the casing is removable from the cutout to electrically decouple the first physical resource from the second physical resource.

[0142] Example 32 includes the subject matter of any of Examples 26-31, and wherein the casing comprises a plurality of passageways and each of the plurality of connectors is inserted into a corresponding passageway.

[0143] Example 33 includes the subject matter of any of Examples 26-32, and wherein the first physical resource comprises a processor and the second physical resource comprises a memory device.

[0144] Example 34 includes a sled for operation in a rack of a data center, the sled comprising a circuit board substrate having a top side and a bottom side opposite the top side, wherein the circuit board substrate comprises a plurality of vias extending therethrough, wherein each via is to electrically couple a first physical resource positioned on the top side of the circuit board substrate to one or more other physical resources positioned on the bottom side of the circuit board substrate; a connector socket coupled to the bottom side of the circuit board substrate, wherein the connector socket comprises a plurality of connectors and each connector comprises (i) a first contact electrically coupled to a corresponding via of the circuit board substrate and (ii) a second contact, opposite the first contact, extending away from the bottom side of the circuit board substrate, wherein each second contact is to mate with a corresponding contact of a second physical resource to electrically couple the second physical resource to the first physical resource.

[0145] Example 35 includes the subject matter of Example 34, and wherein the connector socket is arranged between the bottom side of the circuit board substrate and the second physical resource.

[0146] Example 36 includes the subject matter of any of Examples 34 and 35, and wherein each connector of the connector socket comprises a low insertion force connector.

[0147] Example 37 includes the subject matter of any of Examples 34-36, and wherein the connector socket is to mate with a corresponding connector socket of the second physical resource.

[0148] Example 38 includes the subject matter of any of Examples 34-37, and wherein the connector socket comprises a land grid array socket.

[0149] Example 39 includes the subject matter of any of Examples 34-38, and wherein the connector socket comprises a first connector socket and wherein the sled further comprises a second connector socket coupled to the bottom side of the circuit board substrate adjacent to the first

connector socket, wherein the second connector socket is to receive a circuit board substrate of the second physical resource and comprises a plurality of connectors and each connector of the second connector socket includes a first contact electrically coupled to a corresponding via of the circuit board substrate.

**[0150]** Example 40 includes the subject matter of any of Examples 34-39, and wherein the second connector socket comprises second electrical contacts and third electrical contacts vertically spaced from the second electrical contacts to define a gap therebetween.

**[0151]** Example 41 includes the subject matter of any of Examples 34-40, and wherein each of the second electrical contacts and the third electrical contacts comprise a cantilevered contact arm.

**[0152]** Example 42 includes the subject matter of any of Examples 34-41, and wherein the second connector socket comprises a small outline dual in-line memory module connector.

**[0153]** Example 43 includes the subject matter of any of Examples 34-42, and wherein the first physical resource comprises a processor and the second physical resource comprises a memory device.

**[0154]** Example 44 includes a method of mounting a plurality of physical resources to a circuit board substrate, the method comprising embedding a connector in the circuit board substrate, mounting a first physical resource of the plurality of physical resources to a top side of the circuit board substrate, and mounting a second physical resource of the plurality of physical resources to a bottom side of the circuit board substrate opposite the top side of the circuit board substrate.

**[0155]** Example 45 includes the subject matter of Example 44, wherein embedding the connector in the circuit board substrate comprises inserting the connector into a passageway of the circuit board substrate.

**[0156]** Example 46 includes the subject matter of any of Examples 44 and 45, wherein inserting the connector into the passageway comprises inserting the connector into the passageway such that a first contact of the connector is accessible from the top side of the circuit board substrate and a second contact of the connector, spaced from the first contact, is accessible from the bottom side of the circuit board substrate.

**[0157]** Example 47 includes the subject matter of any of Examples 44-46, wherein embedding the connector in the circuit board substrate comprises inserting a casing that houses multiple connectors, including the connector, into a cutout of the circuit board substrate.

**[0158]** Example 48 includes the subject matter of any of Examples 44-47, wherein inserting the casing into the cutout comprises inserting the casing into the cutout such that a first contact of the connector is accessible from the top side of the circuit board substrate and a second contact of the connector, spaced from the first contact, is accessible from the bottom side of the circuit board substrate.

**[0159]** Example 49 includes the subject matter of any of Examples 44-48, wherein mounting the first physical resource to the top side comprises mounting the first physical resource to the top side such that an electrical contact of the first physical resource mates with a corresponding feature of the connector.

**[0160]** Example 50 includes the subject matter of any of Examples 44-49, wherein the first physical resource is a processor.

**[0161]** Example 51 includes the subject matter of any of Examples 44-50, wherein mounting the second physical resource to the bottom side comprises mounting a memory mezzanine printed circuit board of the second physical resource to the bottom side such that an electrical contact of the second physical resource mates with a corresponding feature of the connector.

**[0162]** Example 52 includes the subject matter of any of Examples 44-51, wherein the second physical resource is a memory device.

**[0163]** Example 53 includes a physical resource comprising a processor and a connector socket, wherein the connector socket includes a first connector, and wherein the first connector includes a first electrical contact mated with the processor and a second electrical contact, spaced from the first electrical contact, to mate with a corresponding feature of a second connector separate from the first connector.

**[0164]** Example 54 includes the subject matter of Example 53, wherein the connector socket includes a plurality of first connectors.

**[0165]** Example 55 includes the subject matter of any of Examples 53 and 54, further comprising a casing that houses the processor and the connector socket.

**[0166]** Example 56 includes the subject matter of any of Examples 53-55, wherein the physical resource is mountable to a circuit board substrate.

**[0167]** Example 57 includes a physical resource comprising a memory package and a memory mezzanine printed circuit board, wherein the memory mezzanine printed circuit board includes a connector socket having a first connector, and wherein the first connector includes a first electrical contact mated with the memory package and a second electrical contact, spaced from the first electrical contact, to mate with a corresponding feature of a second connector separate from the first connector.

**[0168]** Example 58 includes the subject matter of Example 57, wherein the connector socket includes a plurality of first connectors.

**[0169]** Example 59 includes the subject matter of any of Examples 57 and 58, further comprising a casing that houses the memory package and the memory mezzanine printed circuit board.

**[0170]** Example 60 includes the subject matter of any of Examples 57-59, wherein the physical resource is mountable to a circuit board substrate.

1. A sled comprising:

- a circuit board substrate having a top side and a bottom side opposite the top side;
- a physical resource coupled to the top side of the circuit board substrate;
- a memory device coupled to the bottom side of the circuit board substrate; and
- a connector to electrically couple the physical resource to the memory device, wherein the connector extends through the circuit board substrate to the top and bottom sides thereof, and wherein the connector comprises (i) a first contact accessible from the top side of the circuit board substrate and mated with a corresponding contact of the physical resource and (ii) a second contact, opposite the first contact, accessible

from the bottom side of the circuit board substrate and electrically mated with a corresponding contact of the memory device.

2. The sled of claim 1, wherein the circuit board substrate comprises a passageway extending through the circuit board substrate and having a first opening located on the top side and a second opening, opposite the first opening, located on the bottom side,

wherein the connector is located in the passageway of the circuit board substrate, the first contact of the connector extends outwardly from the first opening, and the second contact of the connector extends outwardly from the second opening.

3. The sled of claim 1, wherein the connector is coupled directly to the circuit board substrate, wherein the connector comprises a low insertion force connector.

4. The sled of claim 1, further comprising a casing that houses a plurality of connectors that includes the connector.

5. The sled of claim 4, wherein the circuit board substrate includes a cutout sized to receive the casing to secure the casing and connector to the circuit board substrate between the physical resource and the memory device,

wherein the casing is removable from the cutout to electrically decouple the one or more physical resources from the one or more memory devices.

6. The sled of claim 5, wherein the casing is secured to the circuit board substrate to electrically couple the one or more physical resources to the one or more memory devices by the connector without provision of a heat sink to dissipate heat associated with operation of the connector.

7. The sled of claim 4, wherein the casing comprises a plurality of passageways and each of the plurality of connectors is located in a corresponding passageway.

8. The sled of claim 7, wherein each passageway includes a first opening located on the top side of the circuit board substrate and a second opening, opposite the first opening, located on the bottom side of the circuit board substrate, and

wherein each first contact of each connector extends from the first opening of the corresponding passageway and each second contact of each connector extends from the second opening of the corresponding passageway.

9. A sled comprising:

a circuit board substrate having a top side and a bottom side opposite the top side, wherein the circuit board substrate comprises a plurality of vias extending there-through;

a physical resource coupled to the top side of the circuit board substrate and comprising a plurality of contacts, wherein each contact of the plurality of contacts of the physical resource is electrically coupled to a corresponding via of the circuit board substrate;

a memory mezzanine comprising a plurality of contacts; and

a connector socket coupled to the bottom side of the circuit board substrate, wherein the connector socket comprises a plurality of connectors and each connector comprises (i) a first contact electrically coupled to a corresponding via of the circuit board substrate and (ii) a second contact, opposite the first contact, extending away from the bottom side of the circuit board substrate, wherein each second contact is to mate with a corresponding contact of the memory mezzanine.

10. The sled of claim 9, wherein the connector socket is arranged between the bottom side of the circuit board substrate and the memory mezzanine.

11. The sled of claim 9, wherein the memory mezzanine comprises connector socket having a plurality of connectors, wherein each connector of the connector socket of the memory mezzanine comprises a corresponding contact of the plurality of contacts of the memory mezzanine, wherein the connector socket of the memory mezzanine is to mate with the connector socket coupled to the bottom side of the circuit board substrate, wherein each of the connectors of the connector socket of the memory mezzanine comprises a low insertion force connector, wherein the connector socket comprises a land grid array socket.

12. The sled of claim 9, wherein the connector socket comprises a first connector socket and wherein the sled further comprises a second connector socket coupled to the bottom side of the circuit board substrate adjacent to the first connector socket, wherein the second connector socket is to receive a circuit board substrate of the memory mezzanine and comprises a plurality of connectors and each connector of the second connector socket includes a first contact electrically coupled to a corresponding via of the circuit board substrate.

13. The sled of claim 12, wherein the second connector socket comprises second electrical contacts and third electrical contacts vertically spaced from the second electrical contacts to define a gap therebetween, wherein each of the second electrical contacts and the third electrical contacts comprise a cantilevered contact arm.

14. The sled of claim 12, wherein the second connector socket comprises a small outline dual in-line memory module connector.

15. A sled comprising:

a circuit board substrate having a top side and a bottom side opposite the top side; and

a connector to electrically couple a first physical resource located on the top side of the circuit board substrate with a second physical resource located on the bottom side of the circuit board substrate, wherein the connector comprises (i) a first contact accessible from the top side of the circuit board substrate to electrically mate with a corresponding contact of the first physical resource and (ii) a second contact, opposite the first contact, accessible from the bottom side of the circuit board substrate to electrically mate with a corresponding contact of the second physical resource.

16. The sled of claim 15, wherein the circuit board substrate comprises a passageway extending through the circuit board substrate and having a first opening located on the top side and a second opening, opposite the first opening, located on the bottom side,

wherein the connector is located in the passageway of the circuit board substrate.

17. The sled of claim 15, further comprising a casing that houses a plurality of connectors that includes the connector.

18. The sled of claim 17, wherein the circuit board substrate includes a cutout sized to receive the casing to secure the casing and connector to the circuit board substrate between the first physical resource and the second physical resource,

wherein the casing is removable from the cutout to electrically decouple the first physical resource from the second physical resource.

**19.** The sled of claim **17**, wherein the casing comprises a plurality of passageways and each of the plurality of connectors is located in a corresponding passageway.

**20.** The sled of claim **15**, wherein the first physical resource comprises a processor and the second physical resource comprises a memory device.

**21.** A sled comprising:

a circuit board substrate having a top side and a bottom side opposite the top side, wherein the circuit board substrate comprises a plurality of vias extending there-through, wherein each via is to electrically couple a first physical resource positioned on the top side of the circuit board substrate to one or more other physical resources positioned on the bottom side of the circuit board substrate;

a connector socket coupled to the bottom side of the circuit board substrate, wherein the connector socket comprises a plurality of connectors and each connector comprises (i) a first contact electrically coupled to a corresponding via of the circuit board substrate and (ii) a second contact, opposite the first contact, extending away from the bottom side of the circuit board substrate, wherein each second contact is to mate with a corresponding contact of a second physical resource to electrically couple the second physical resource to the first physical resource.

**22.** The sled of claim **21**, wherein the connector socket is arranged between the bottom side of the circuit board substrate and the second physical resource.

**23.** The sled of claim **21**, wherein the connector socket is to mate with a corresponding connector socket of the second physical resource, wherein the connector socket comprises a land grid array socket.

**24.** The sled of claim **21**, wherein the connector socket comprises a first connector socket and wherein the sled further comprises a second connector socket coupled to the bottom side of the circuit board substrate adjacent to the first connector socket, wherein the second connector socket is to receive a circuit board substrate of the second physical resource and comprises a plurality of connectors and each connector of the second connector socket includes a first contact electrically coupled to a corresponding via of the circuit board substrate, wherein the second connector socket comprises a small outline dual in-line memory module connector.

**25.** The sled of claim **24**, wherein the second connector socket comprises second electrical contacts and third electrical contacts vertically spaced from the second electrical contacts to define a gap therebetween,

wherein each of the second electrical contacts and the third electrical contacts comprise a cantilevered contact arm.

**26.** A method of mounting a plurality of physical resources to a circuit board substrate, the method comprising:

embedding a connector in the circuit board substrate;

mounting a first physical resource of the plurality of physical resources to a top side of the circuit board substrate; and

mounting a second physical resource of the plurality of physical resources to a bottom side of the circuit board substrate opposite the top side of the circuit board substrate.

**27.** The method of claim **26**, wherein embedding the connector in the circuit board substrate comprises inserting the connector into the passageway such that a first contact of the connector is accessible from the top side of the circuit board substrate and a second contact of the connector, spaced from the first contact, is accessible from the bottom side of the circuit board substrate.

**28.** The method of claim **26**, wherein embedding the connector in the circuit board substrate comprises inserting a casing that houses multiple connectors, including the connector, into a cutout of the circuit board substrate.

**29.** The method of claim **28**, wherein inserting the casing into the cutout comprises inserting the casing into the cutout such that a first contact of the connector is accessible from the top side of the circuit board substrate and a second contact of the connector, spaced from the first contact, is accessible from the bottom side of the circuit board substrate.

**30.** The method of claim **26**, wherein mounting the second physical resource to the bottom side comprises mounting a memory mezzanine printed circuit board of the second physical resource to the bottom side such that an electrical contact of the second physical resource mates with a corresponding feature of the connector.

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