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(54) **WAFER ENCAPSULATED MICROELECTROMECHANICAL STRUCTURE AND METHOD OF MANUFACTURING SAME**

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Related U.S. Application Data

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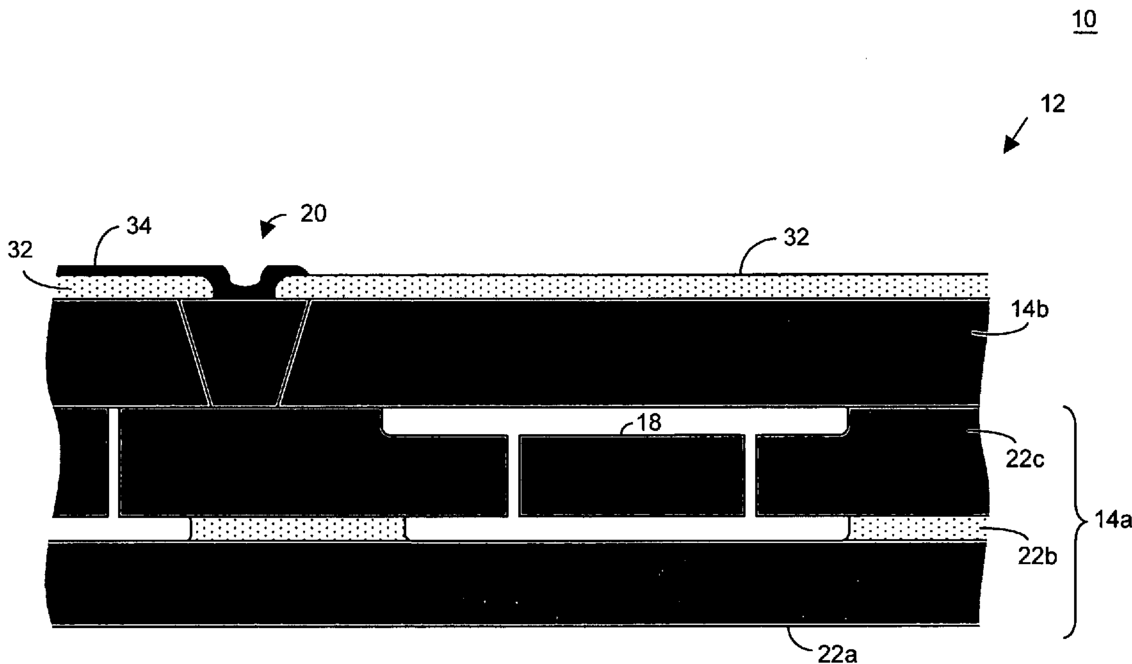
Publication Classification

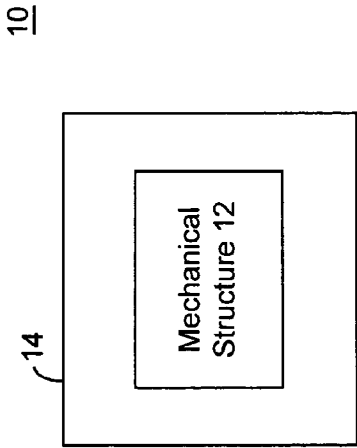
(51) **Int. Cl.**
H01L 31/0312 (2006.01)

(52) **U.S. Cl.** **257/77**

(57) **ABSTRACT**

There are many inventions described and illustrated herein. In one aspect, the present inventions relate to devices, systems and/or methods of encapsulating and fabricating electromechanical structures or elements, for example, accelerometer, gyroscope or other transducer (for example, pressure sensor, strain sensor, tactile sensor, magnetic sensor and/or temperature sensor), filter or resonator. The fabricating or manufacturing microelectromechanical systems of the present invention, and the systems manufactured thereby, employ wafer bonding encapsulation techniques.





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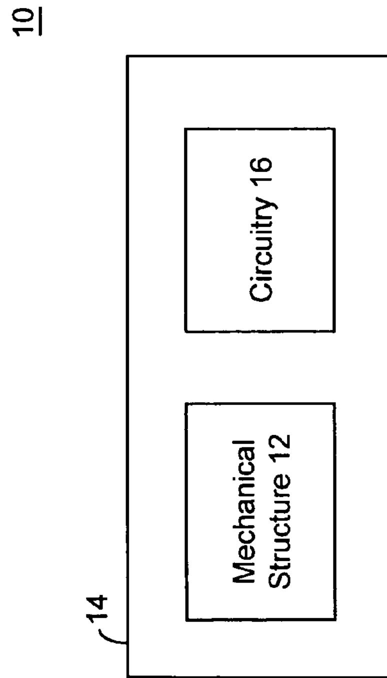


FIGURE 1B

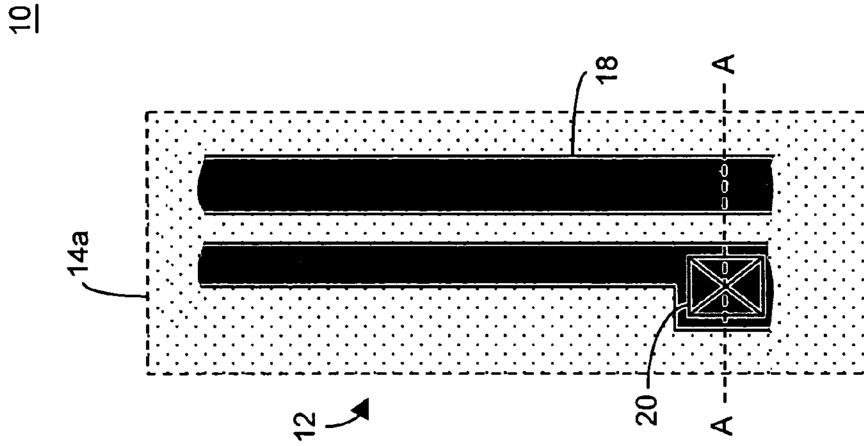
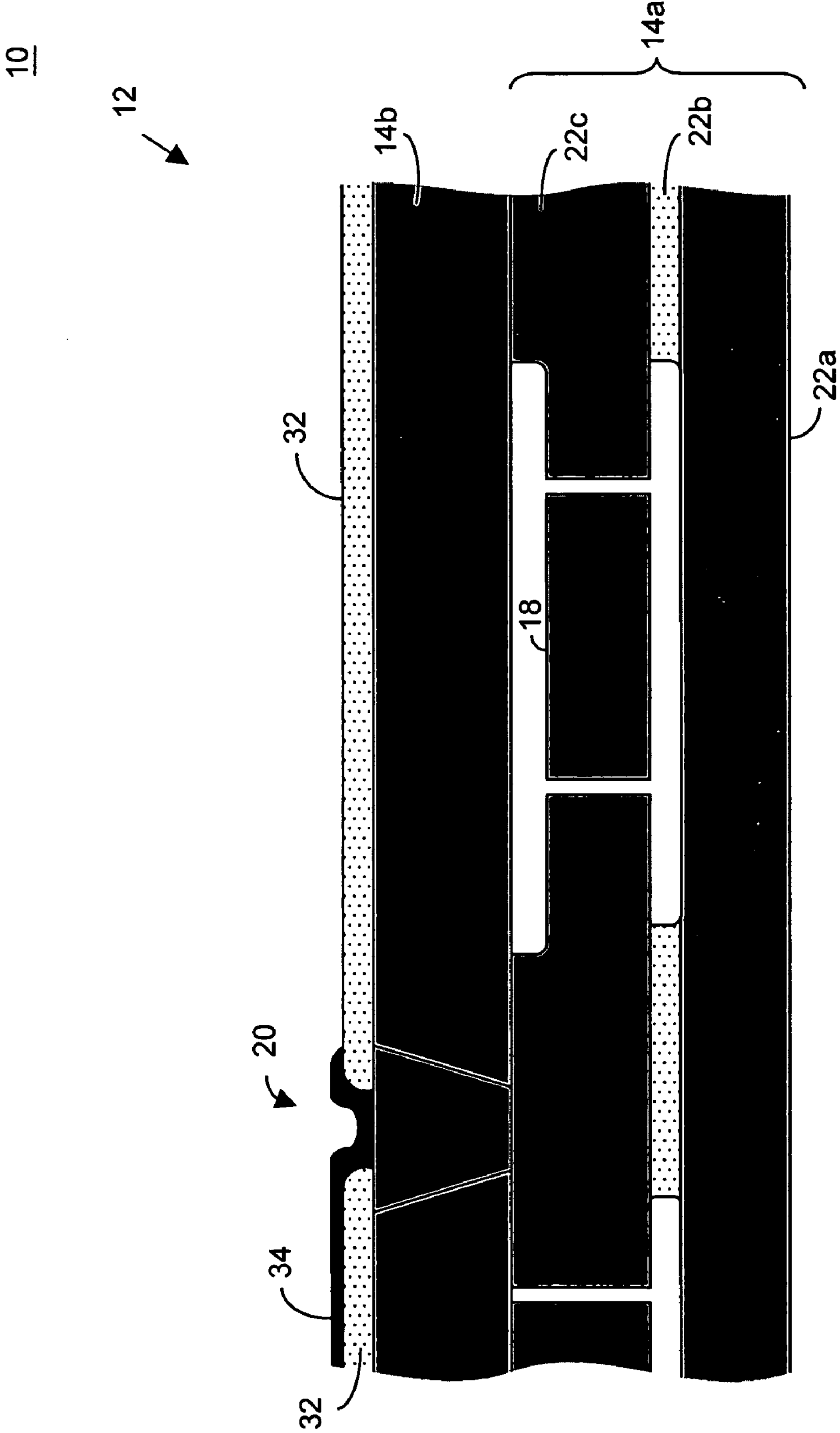


FIGURE 2



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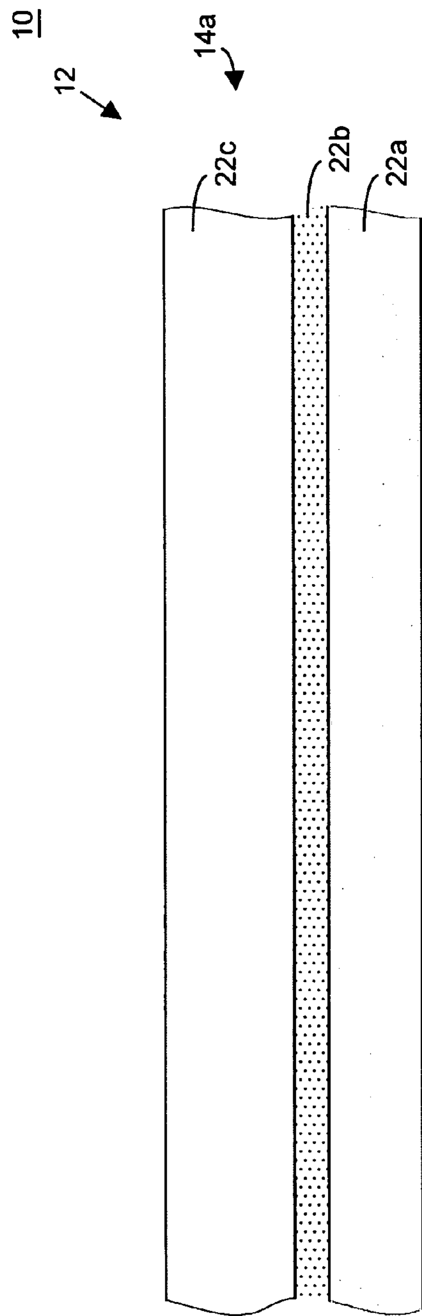

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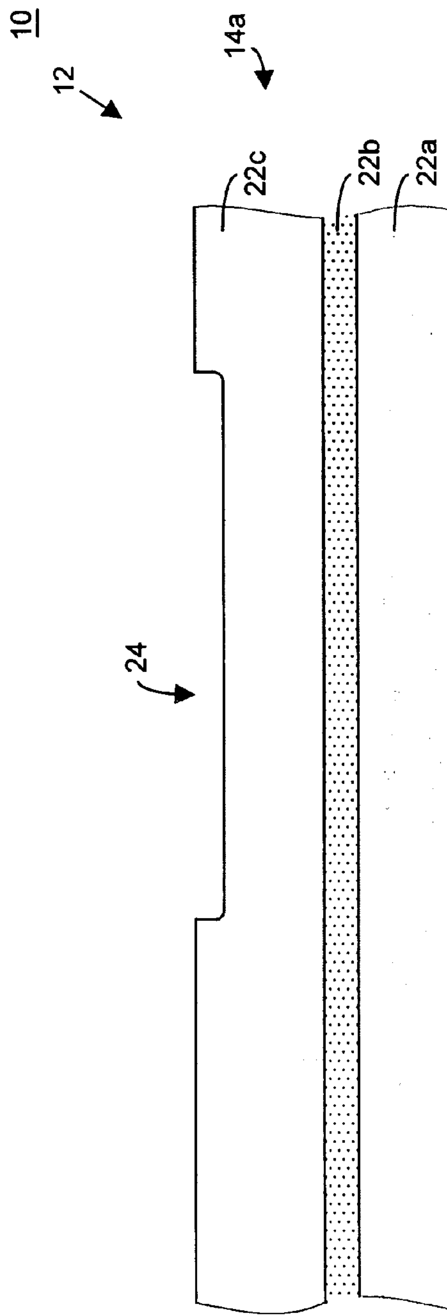

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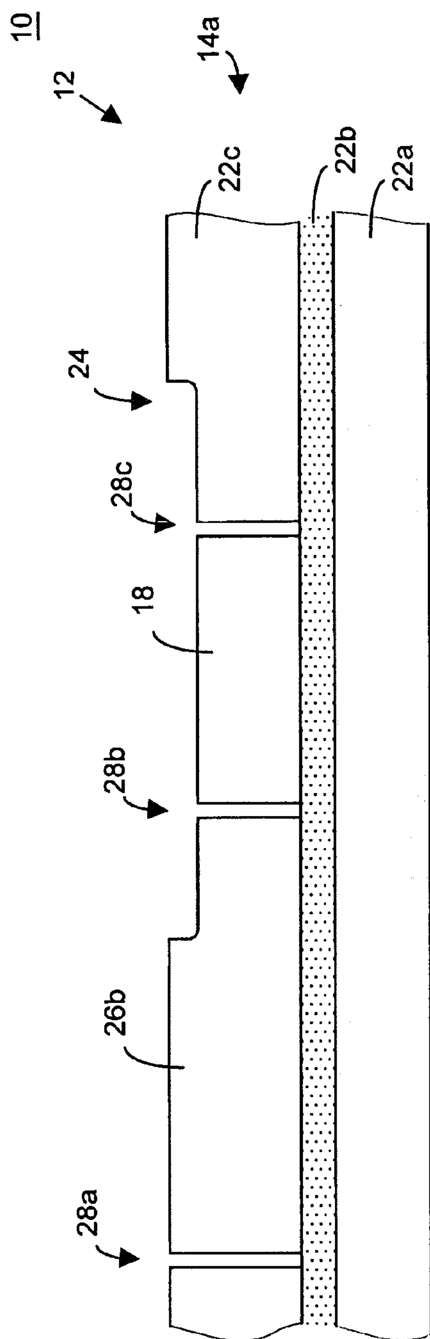


FIGURE 4C

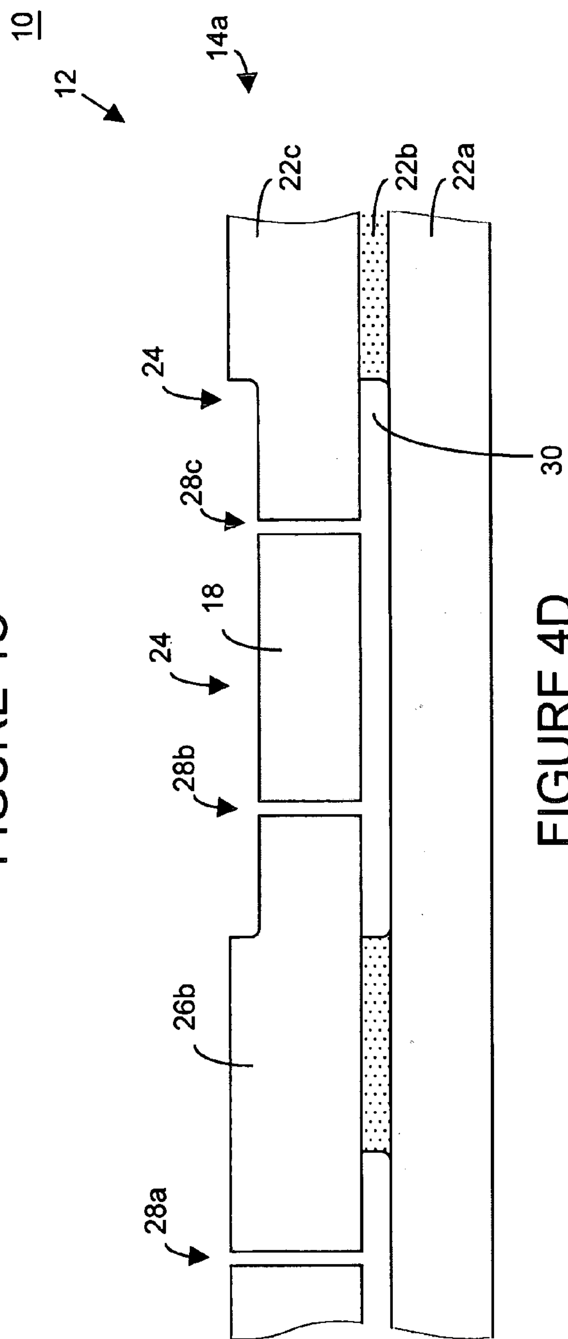
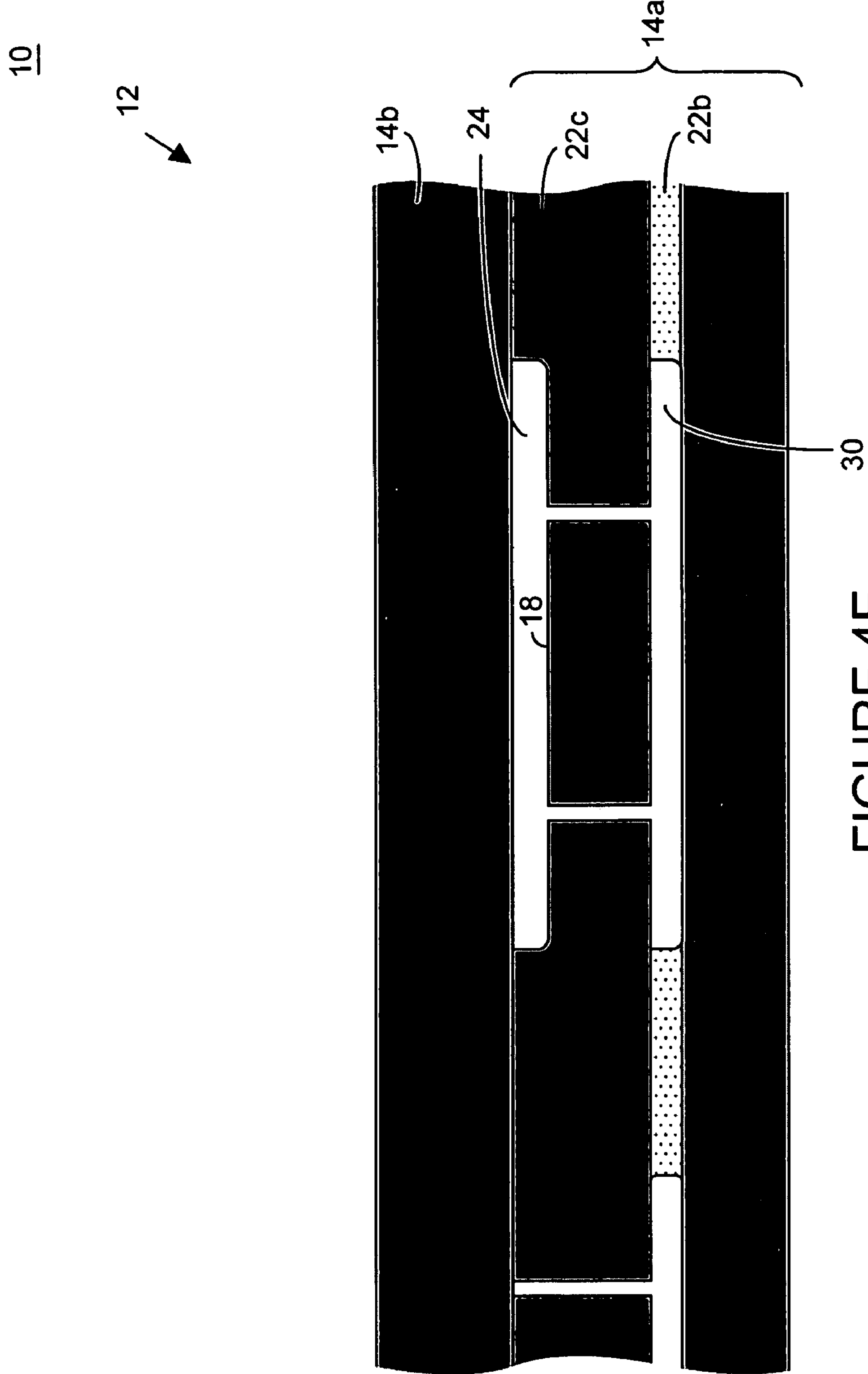


FIGURE 4D



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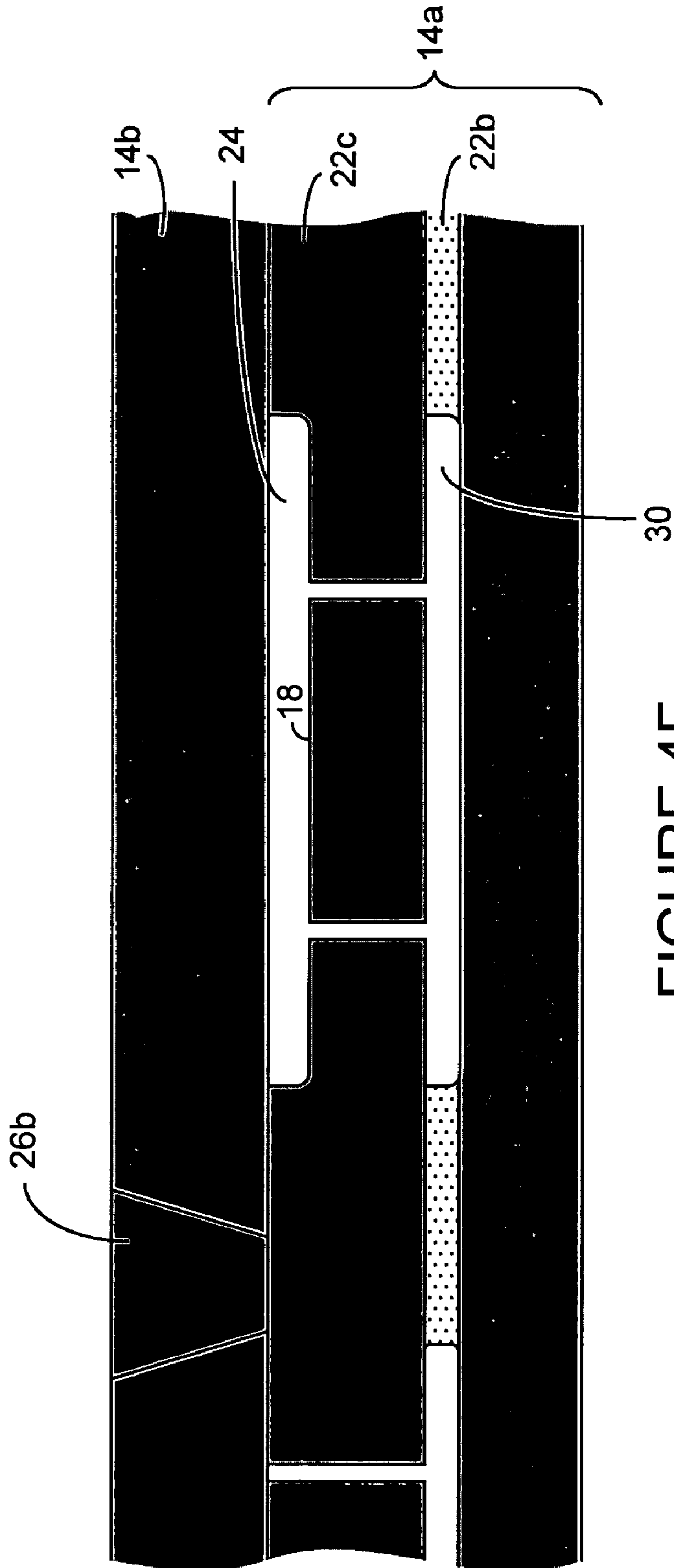


FIGURE 4F

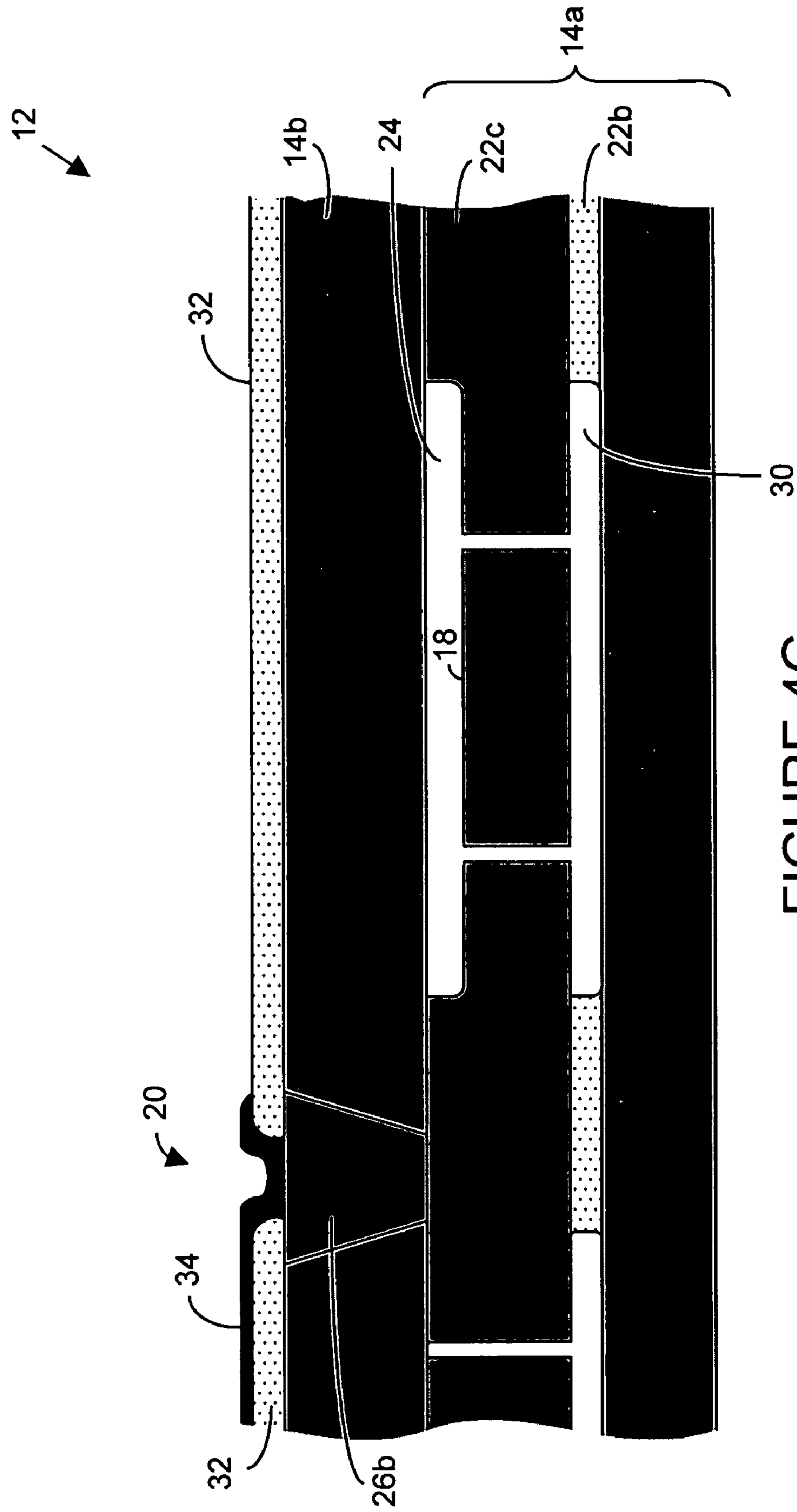
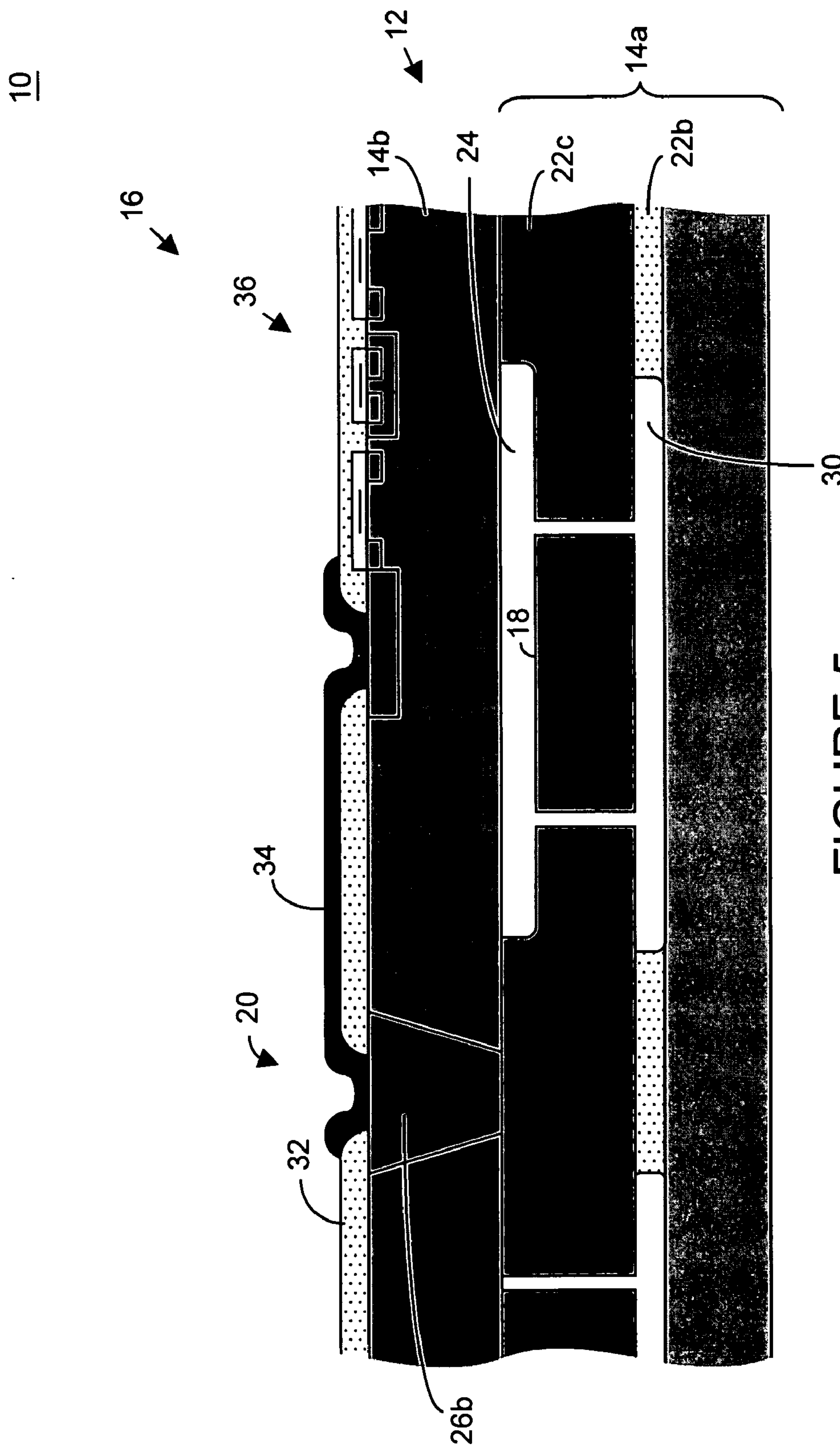


FIGURE 4G



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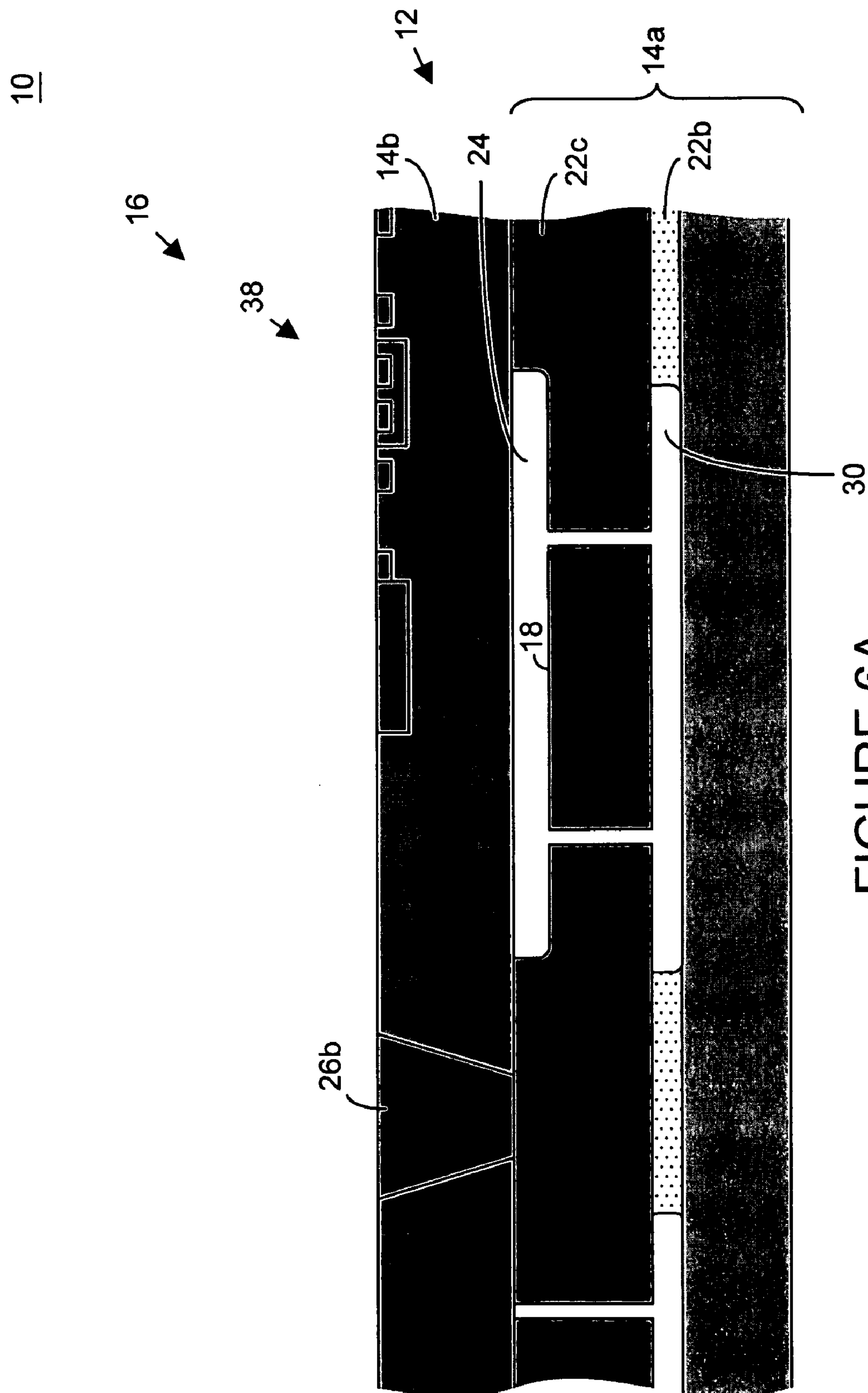
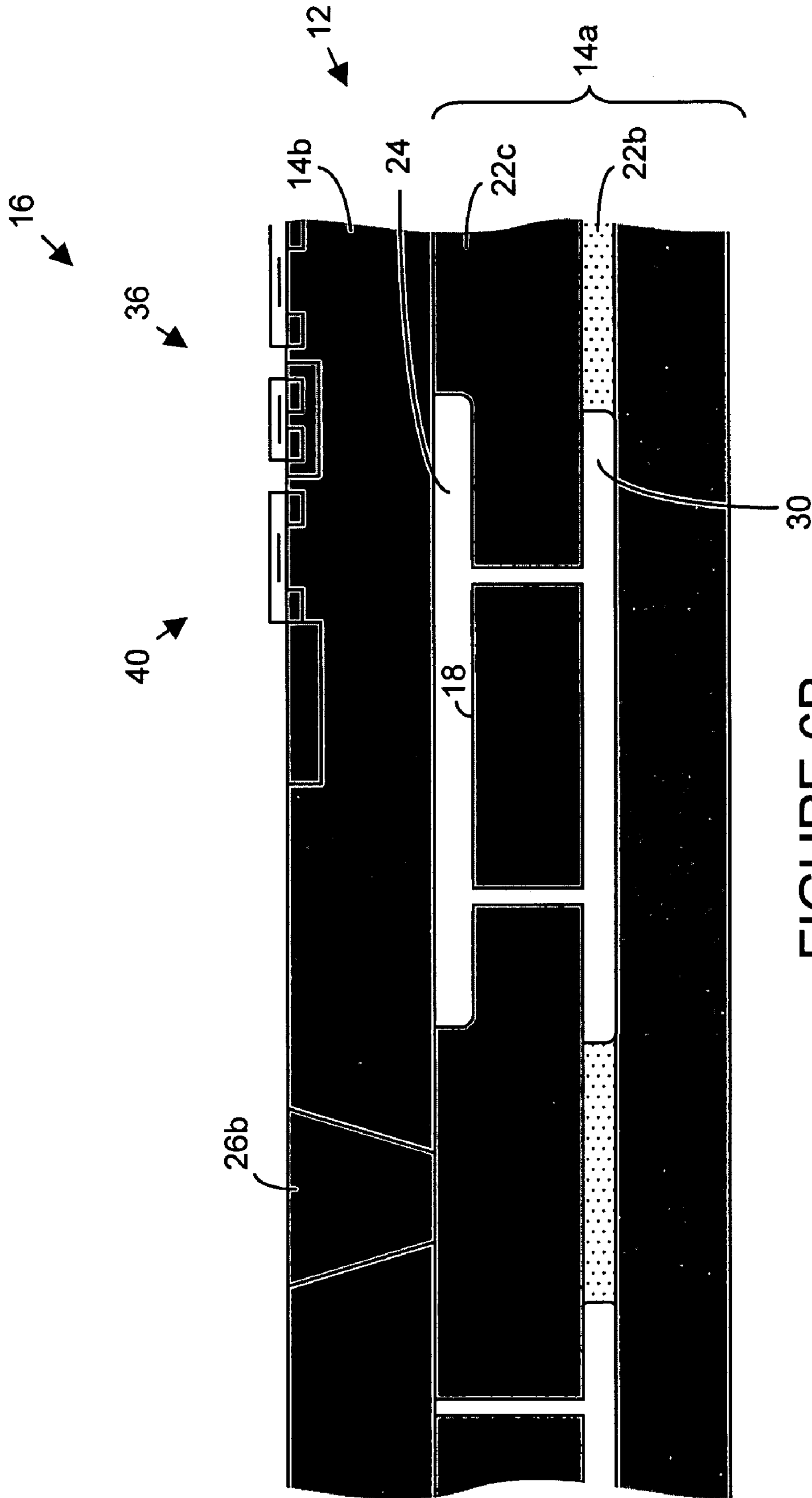


FIGURE 6A



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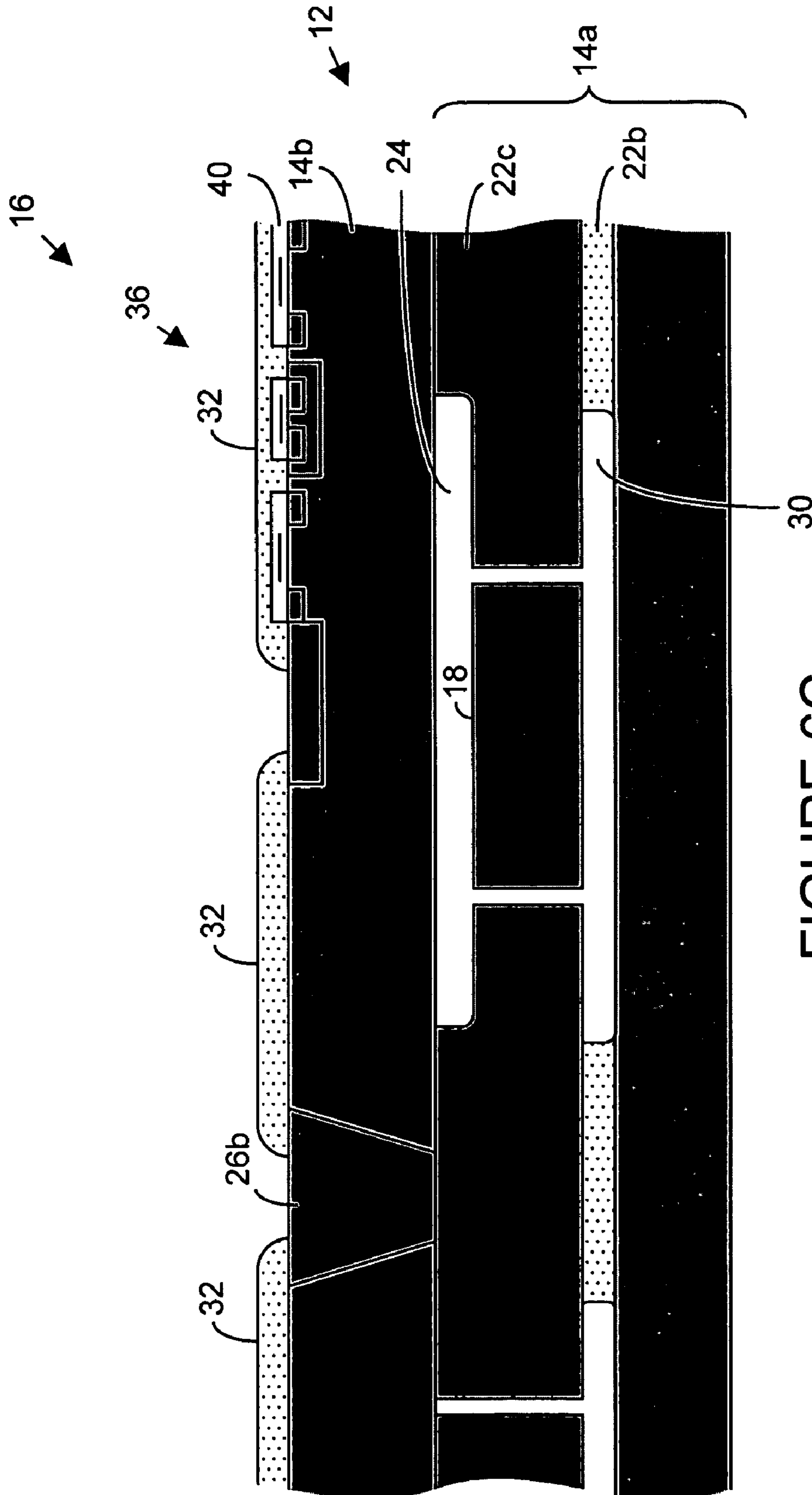

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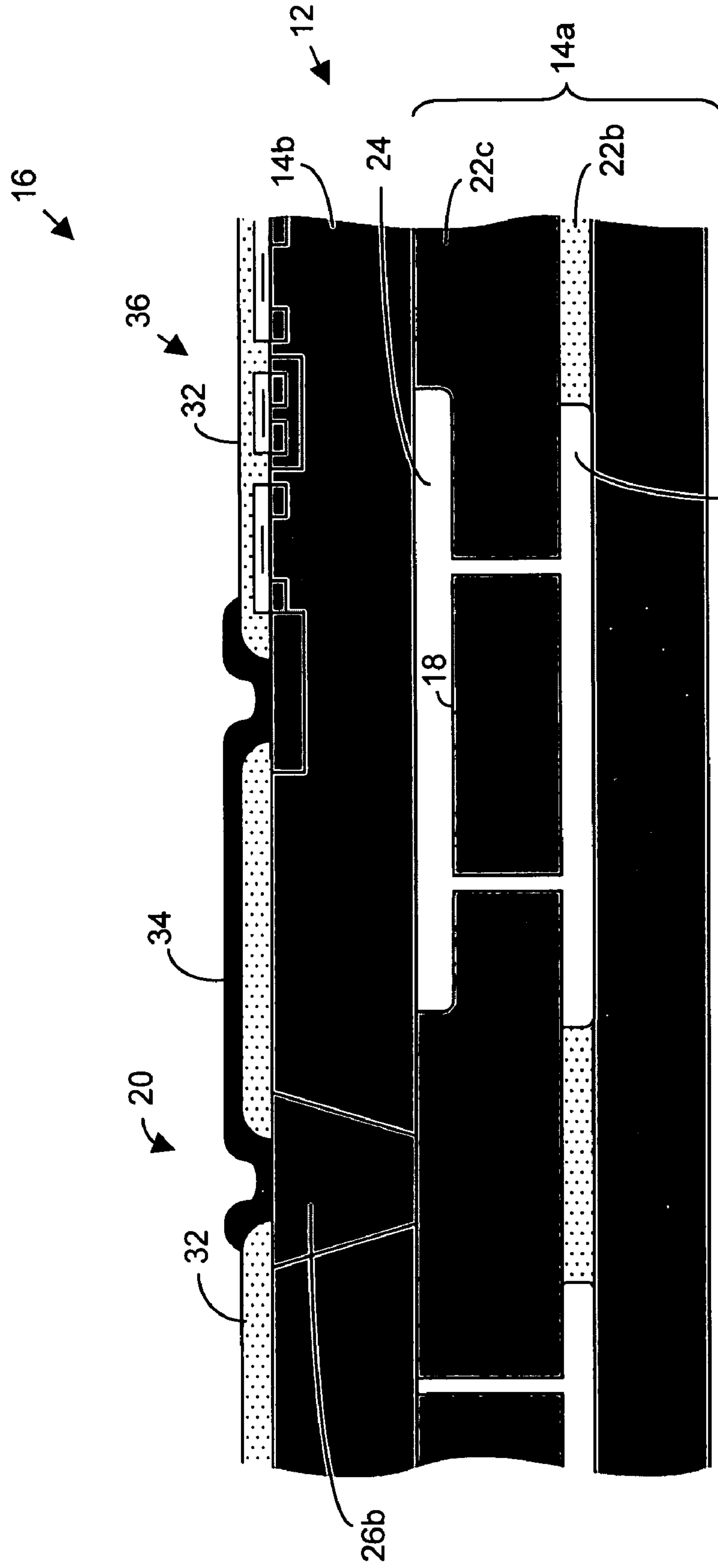

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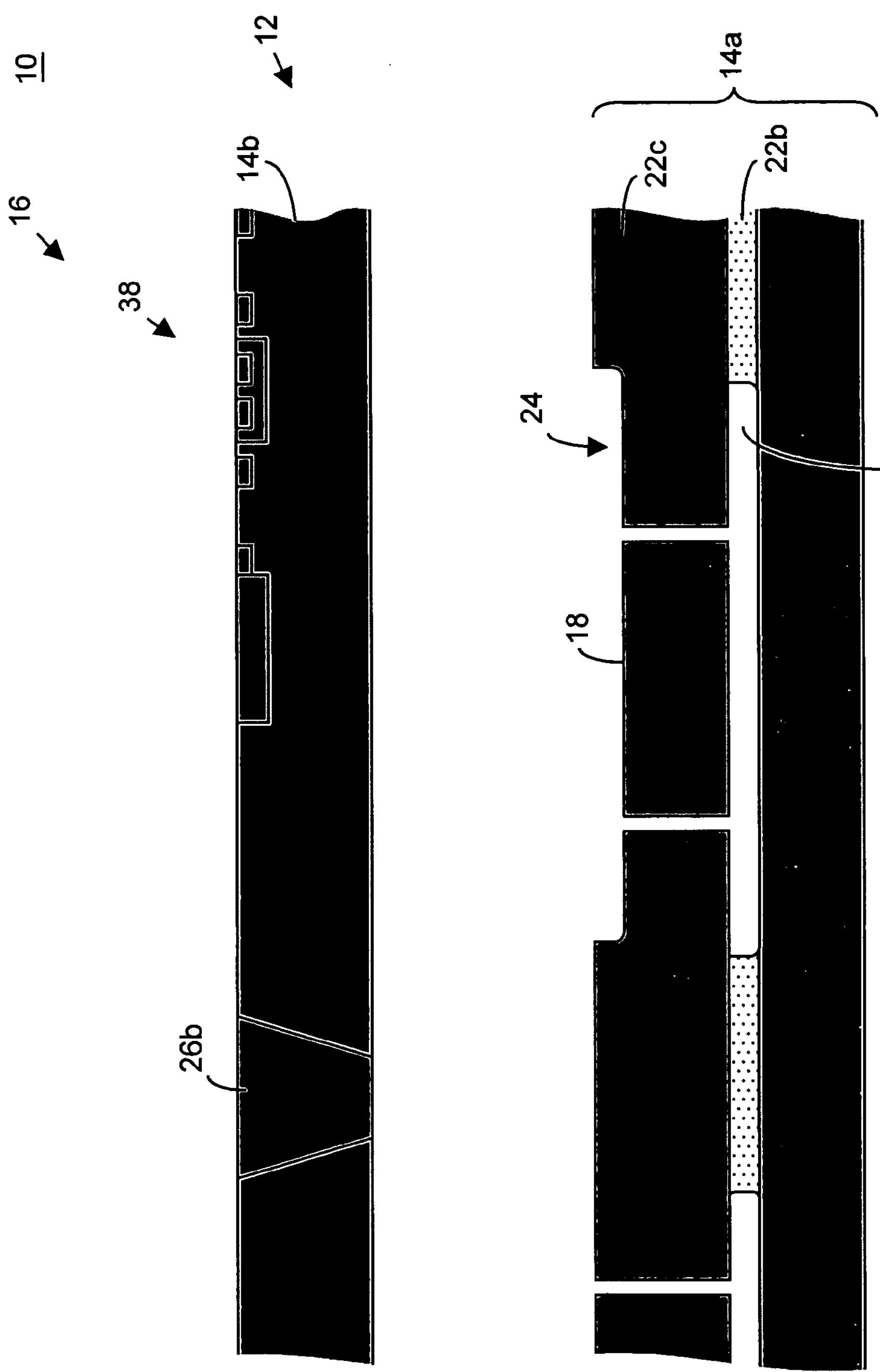

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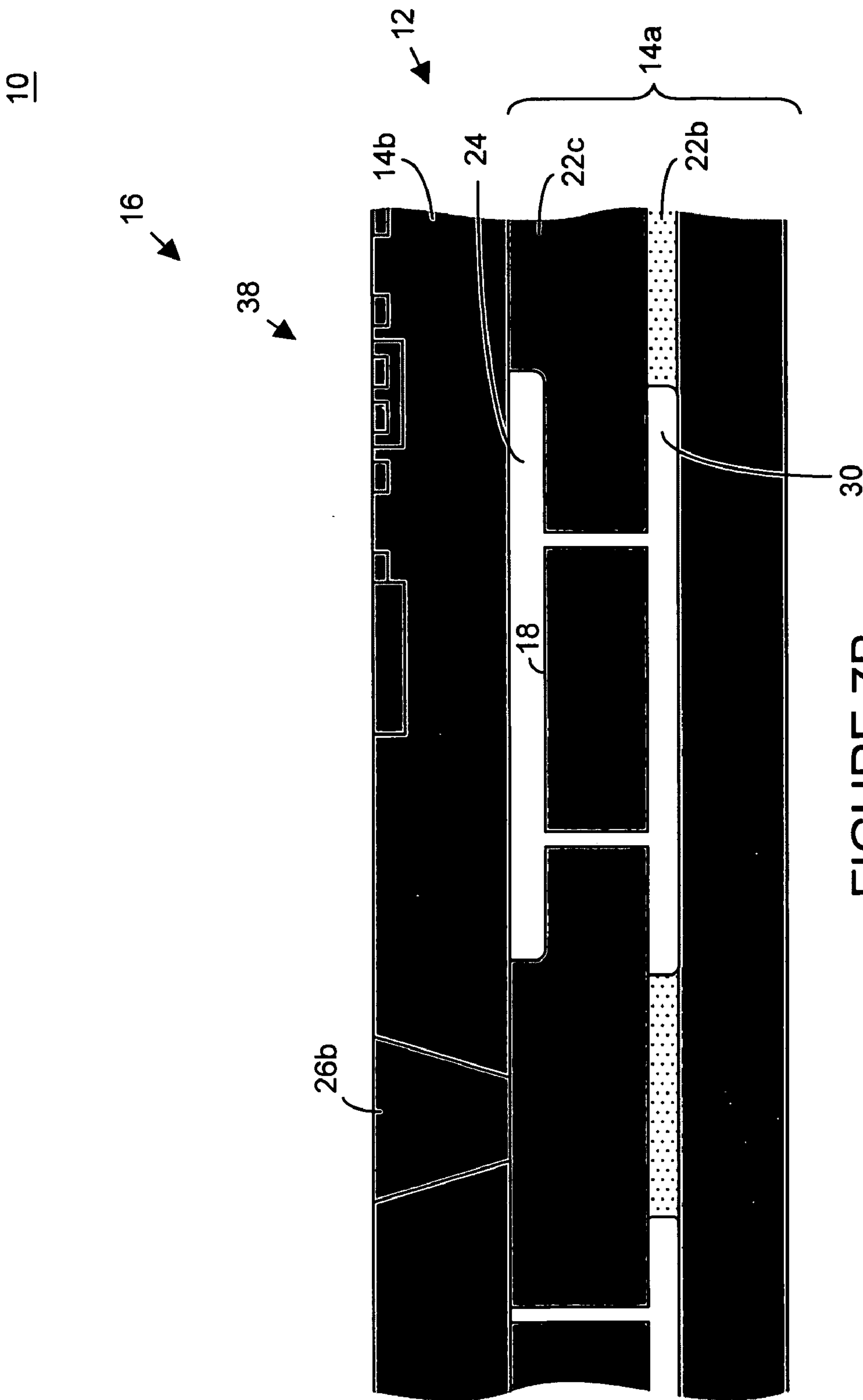
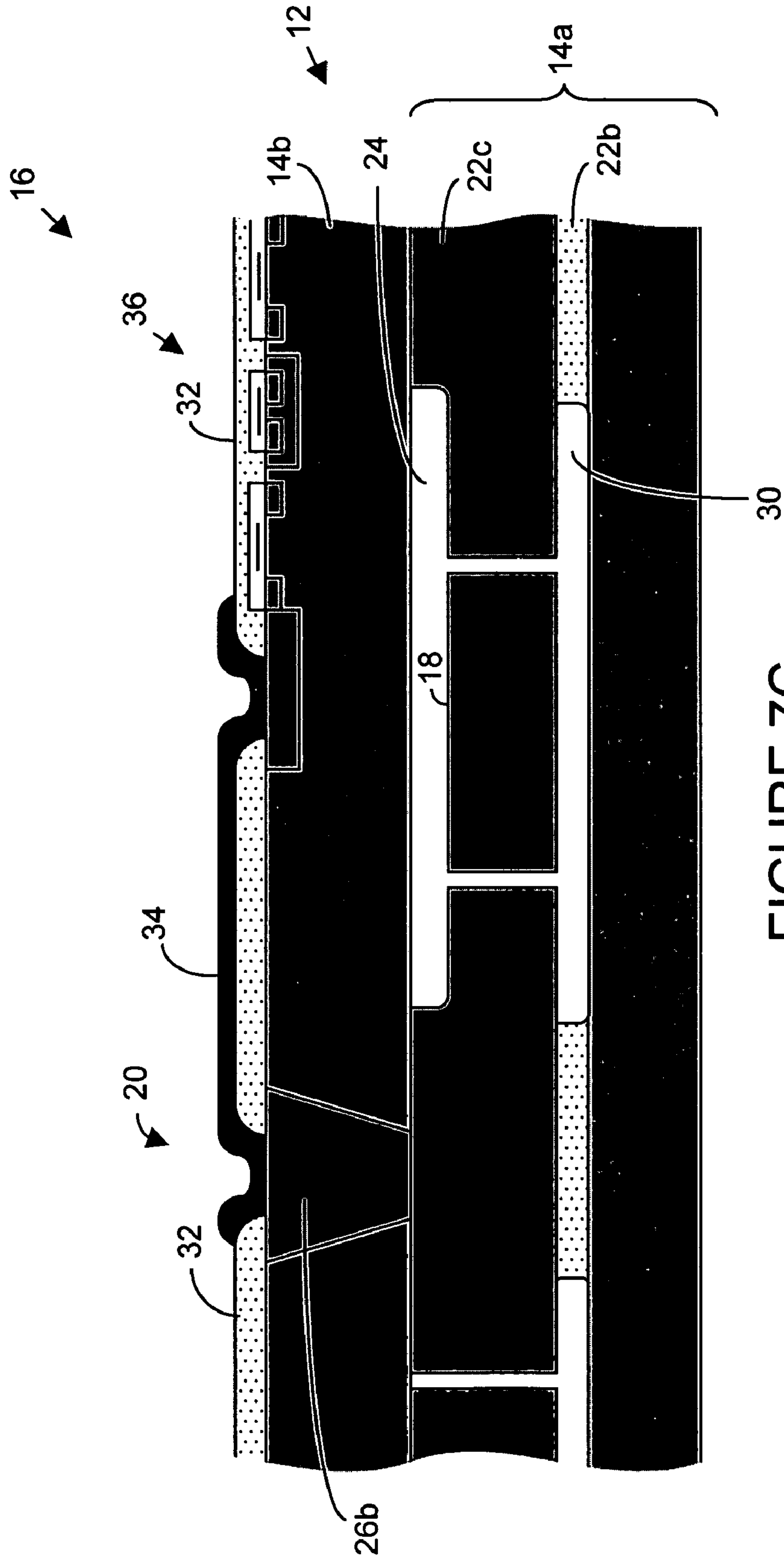


FIGURE 7B



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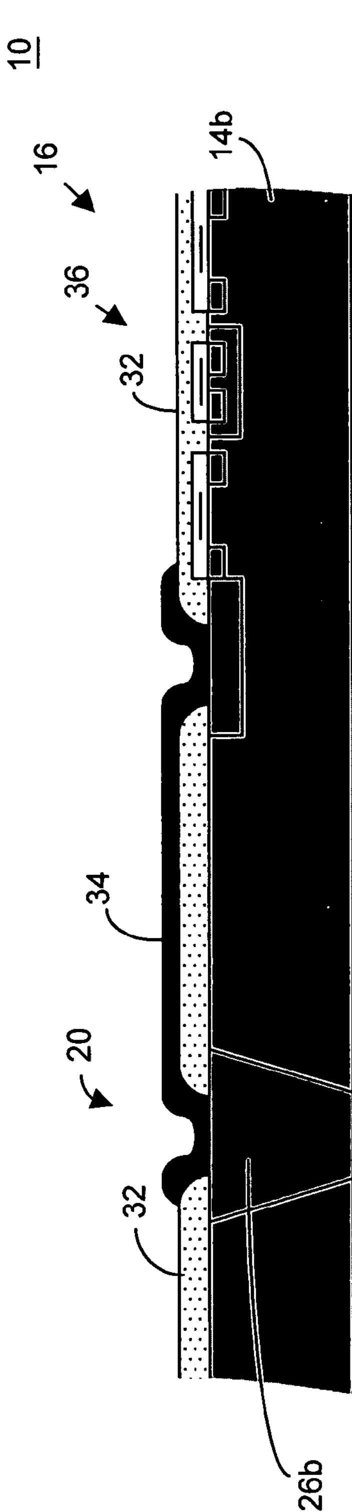


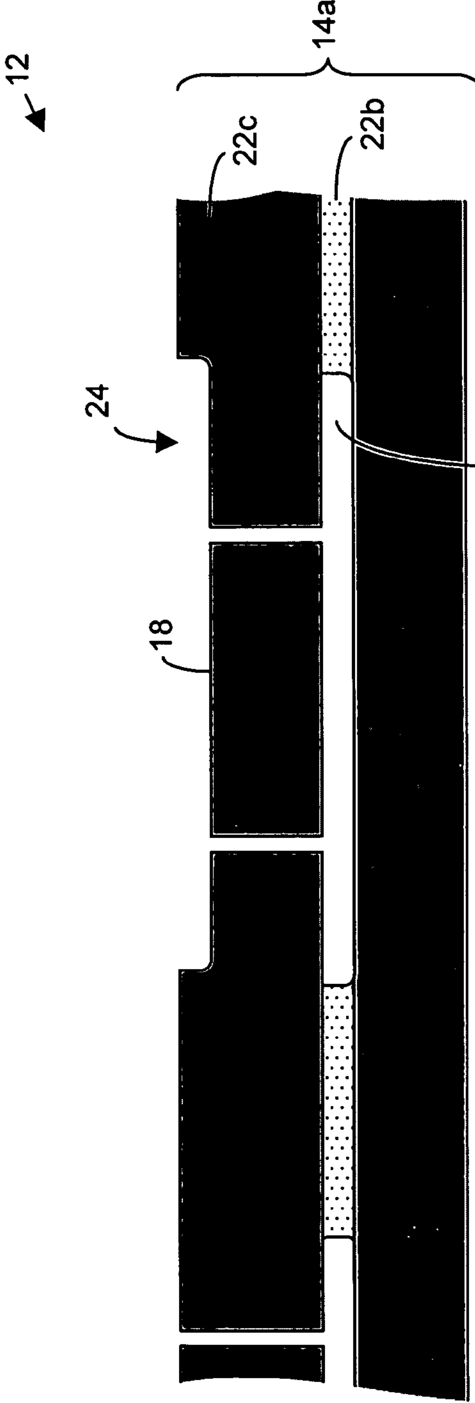


FIGURE 8A

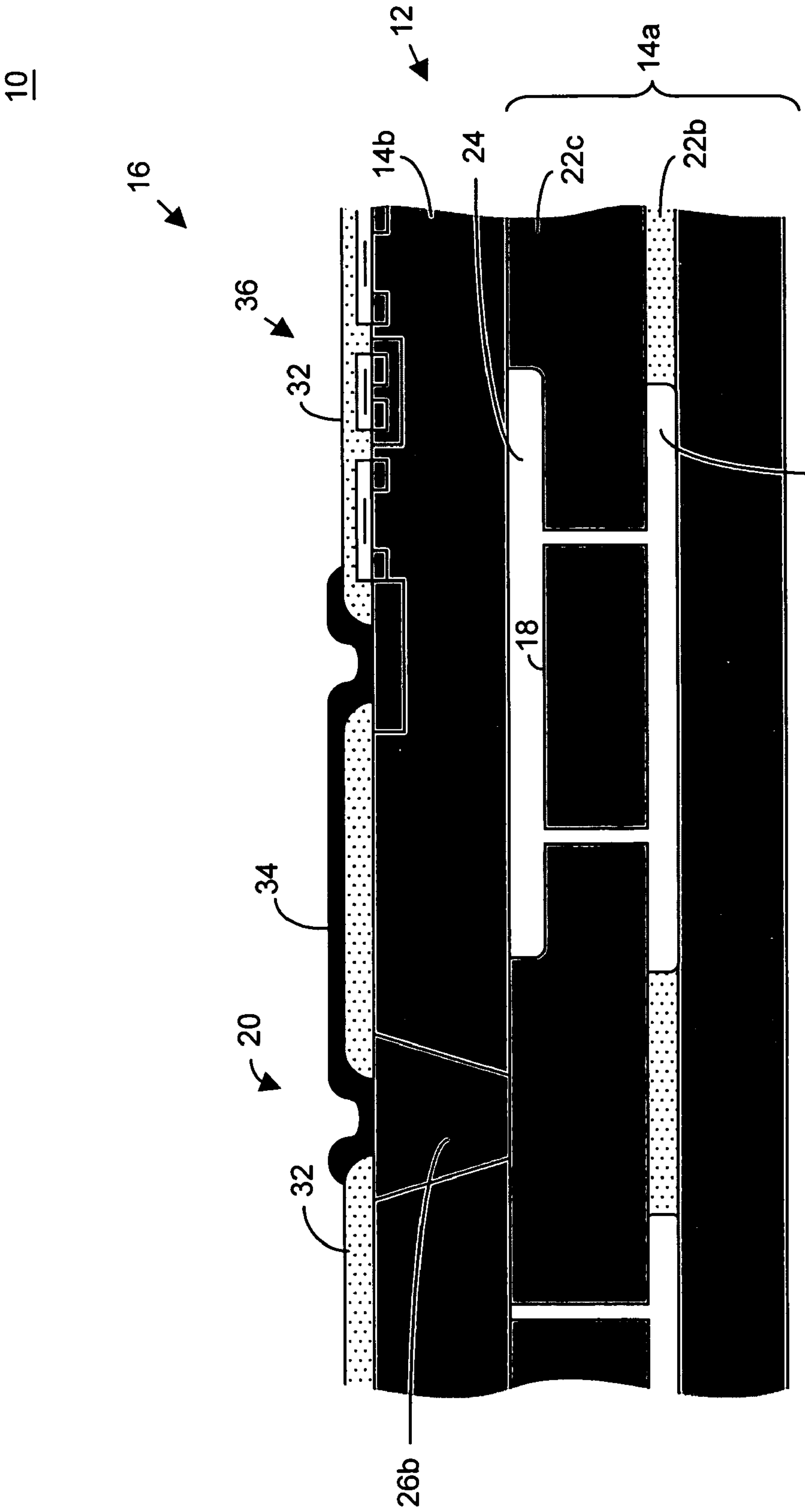
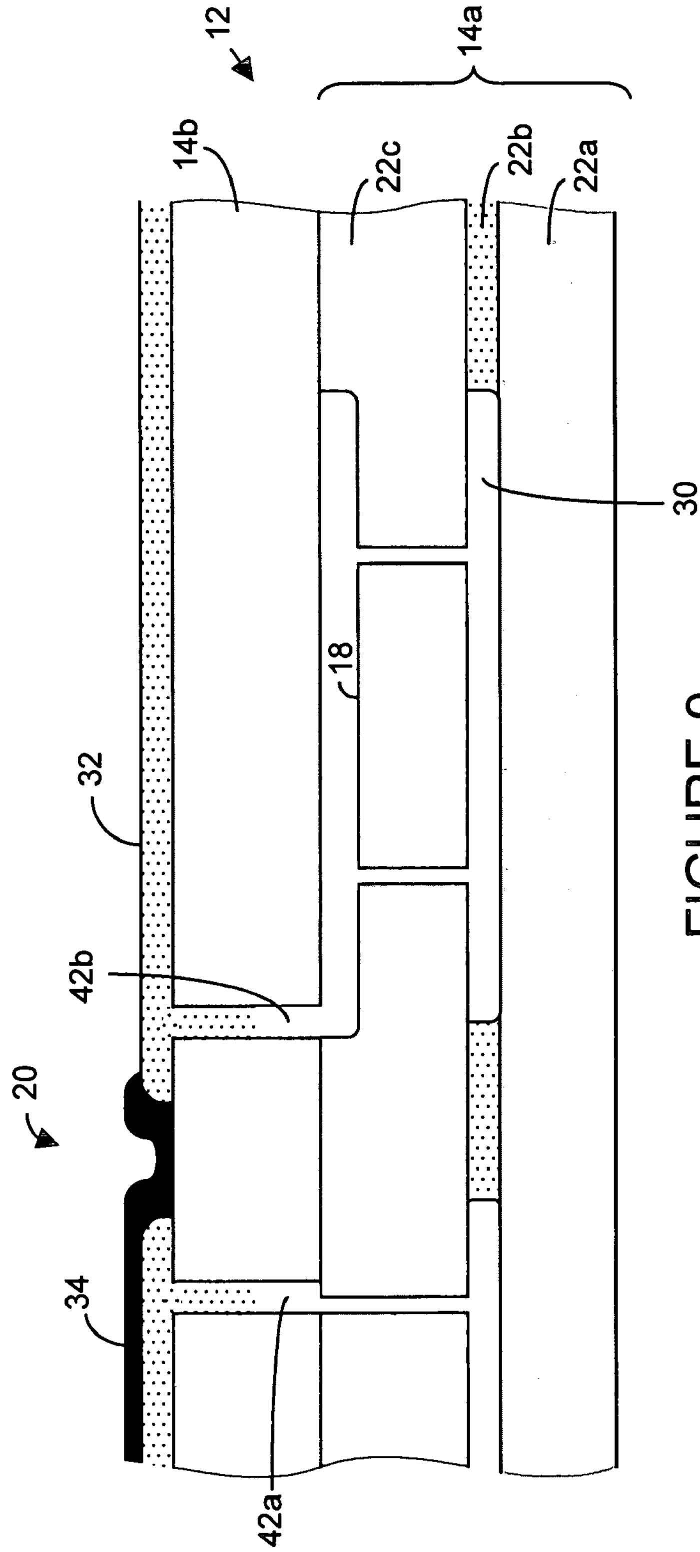


FIGURE 8B



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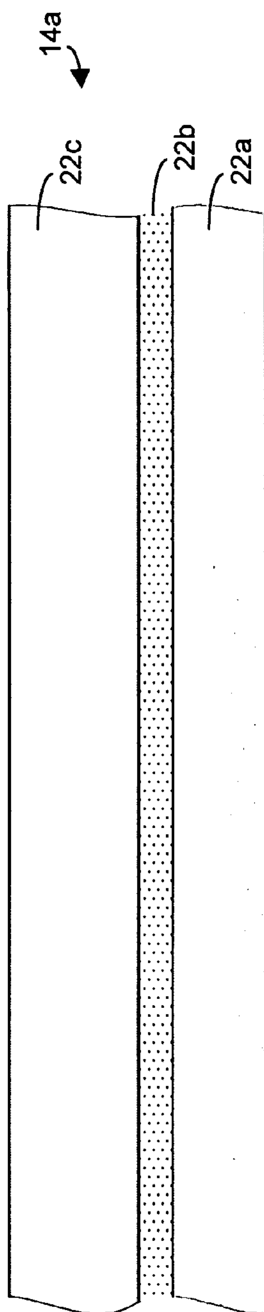
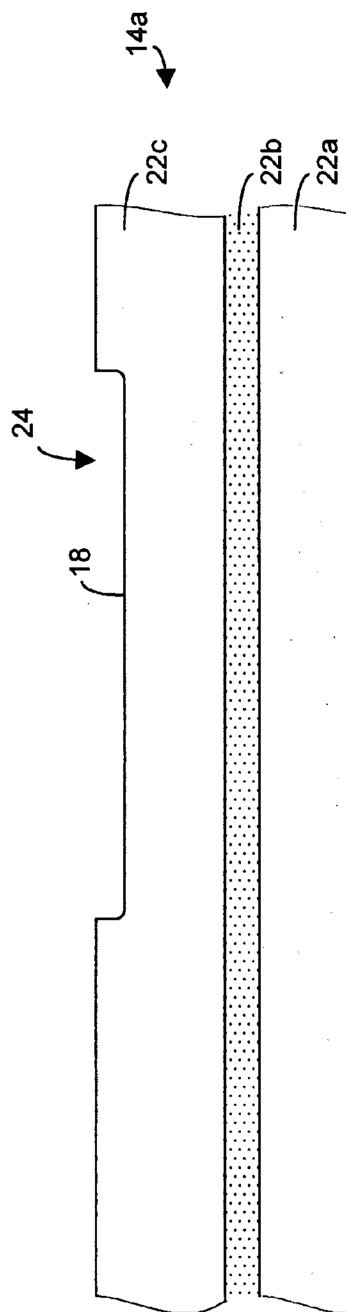


FIGURE 10A



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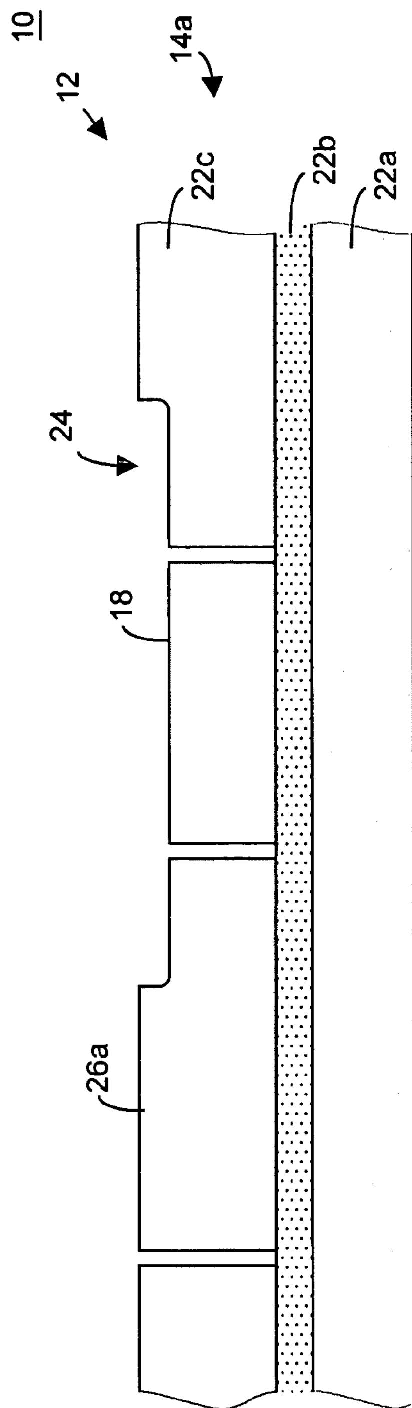

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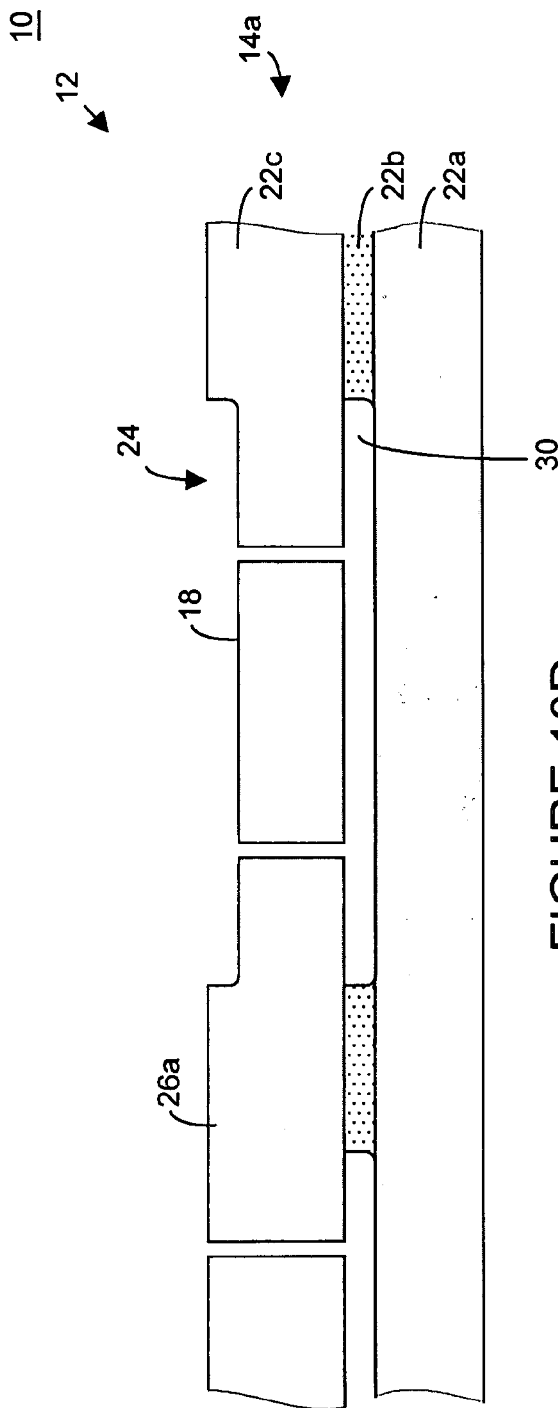

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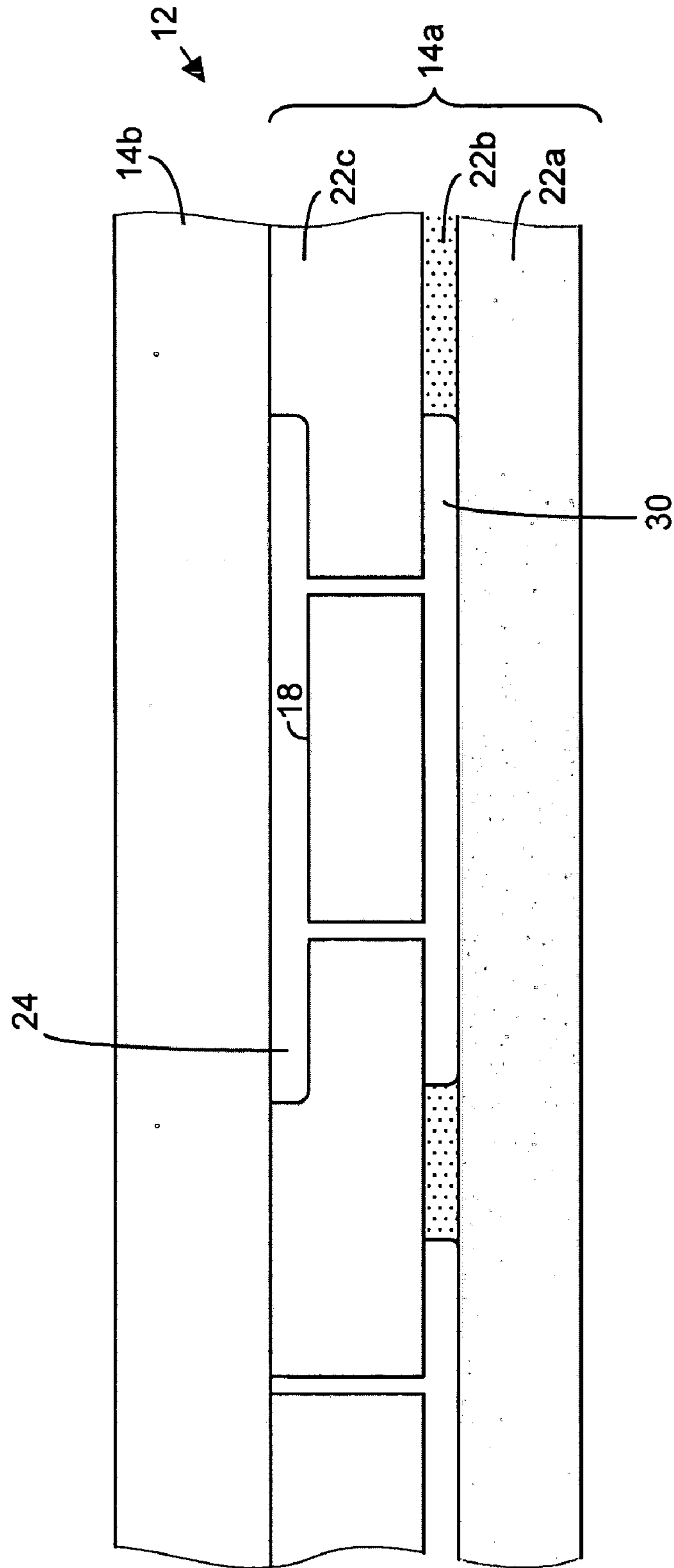


FIGURE 10E

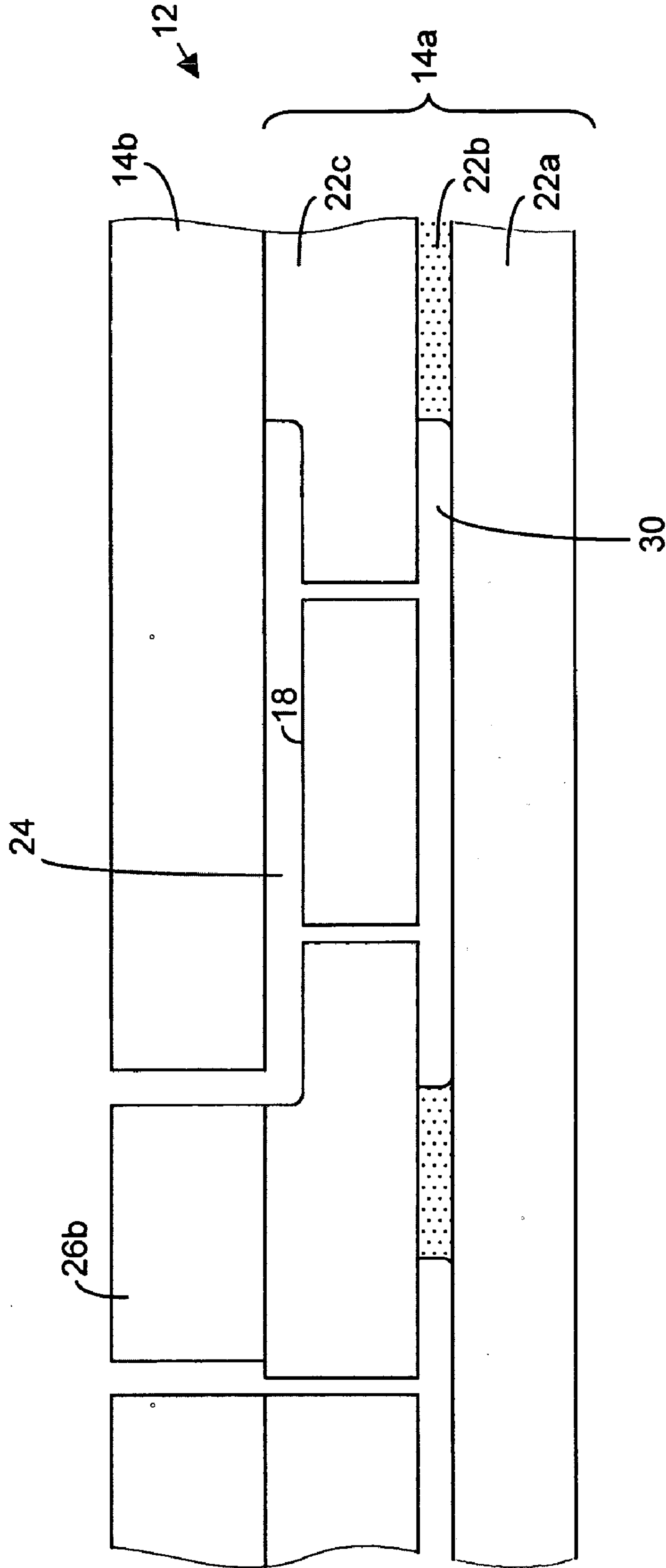


FIGURE 10F

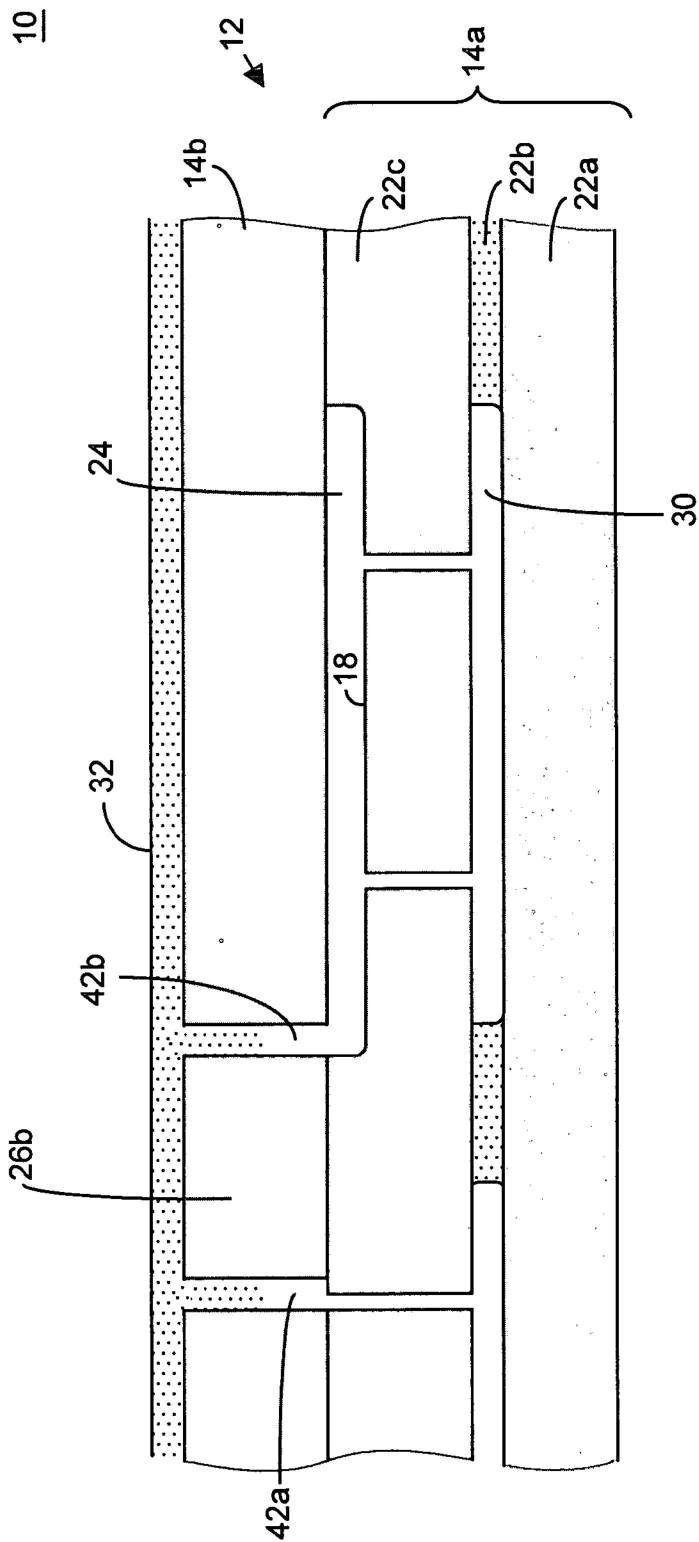


FIGURE 10G

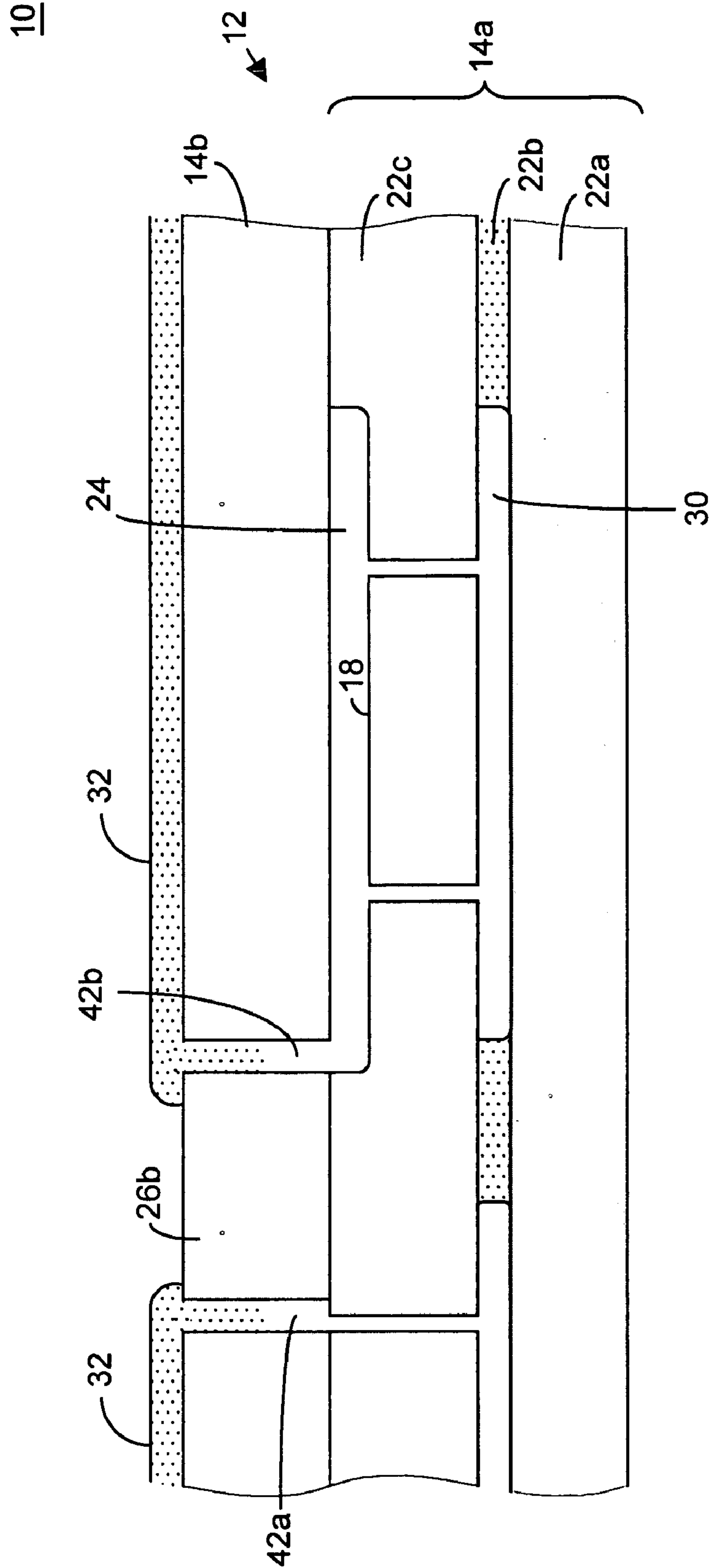


FIGURE 10H

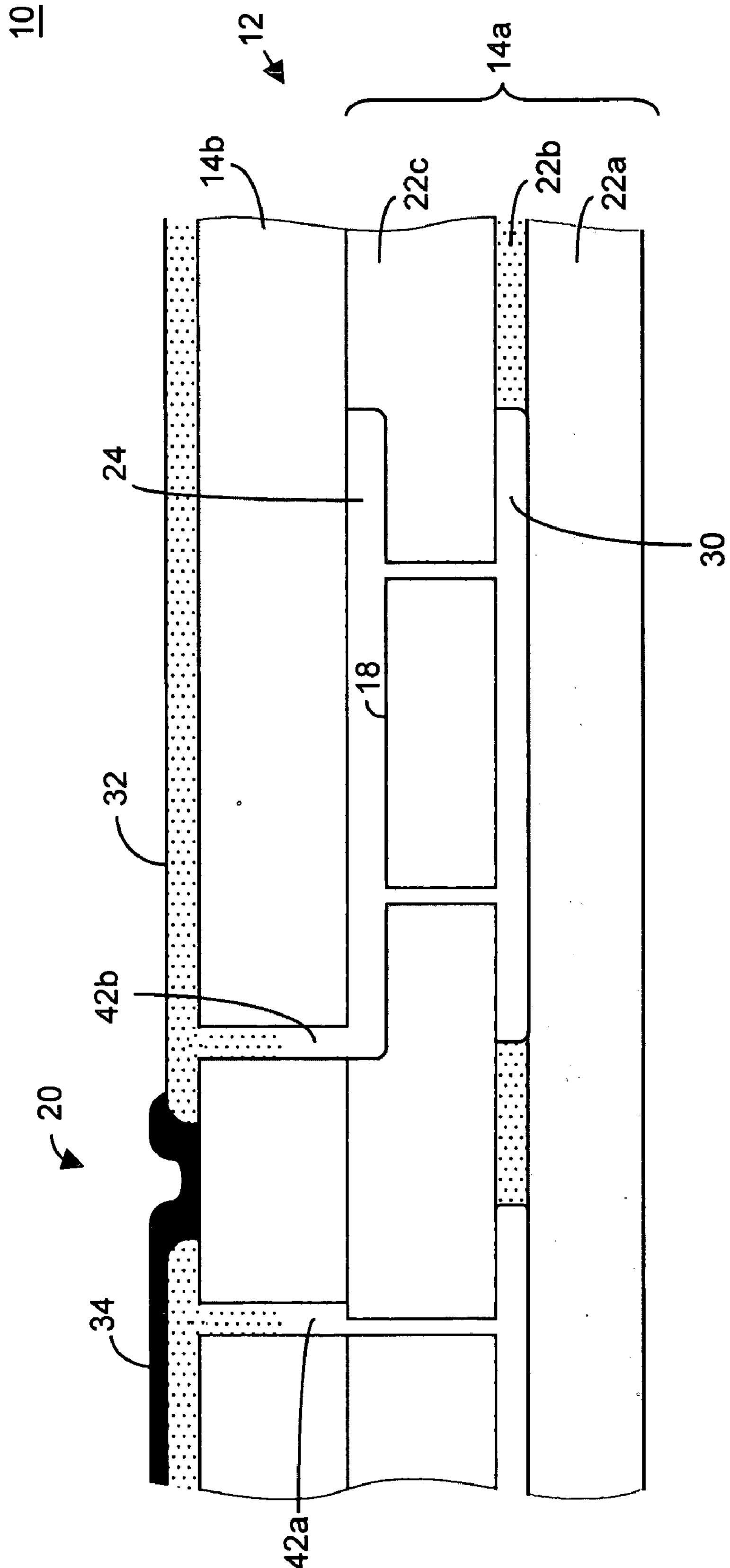
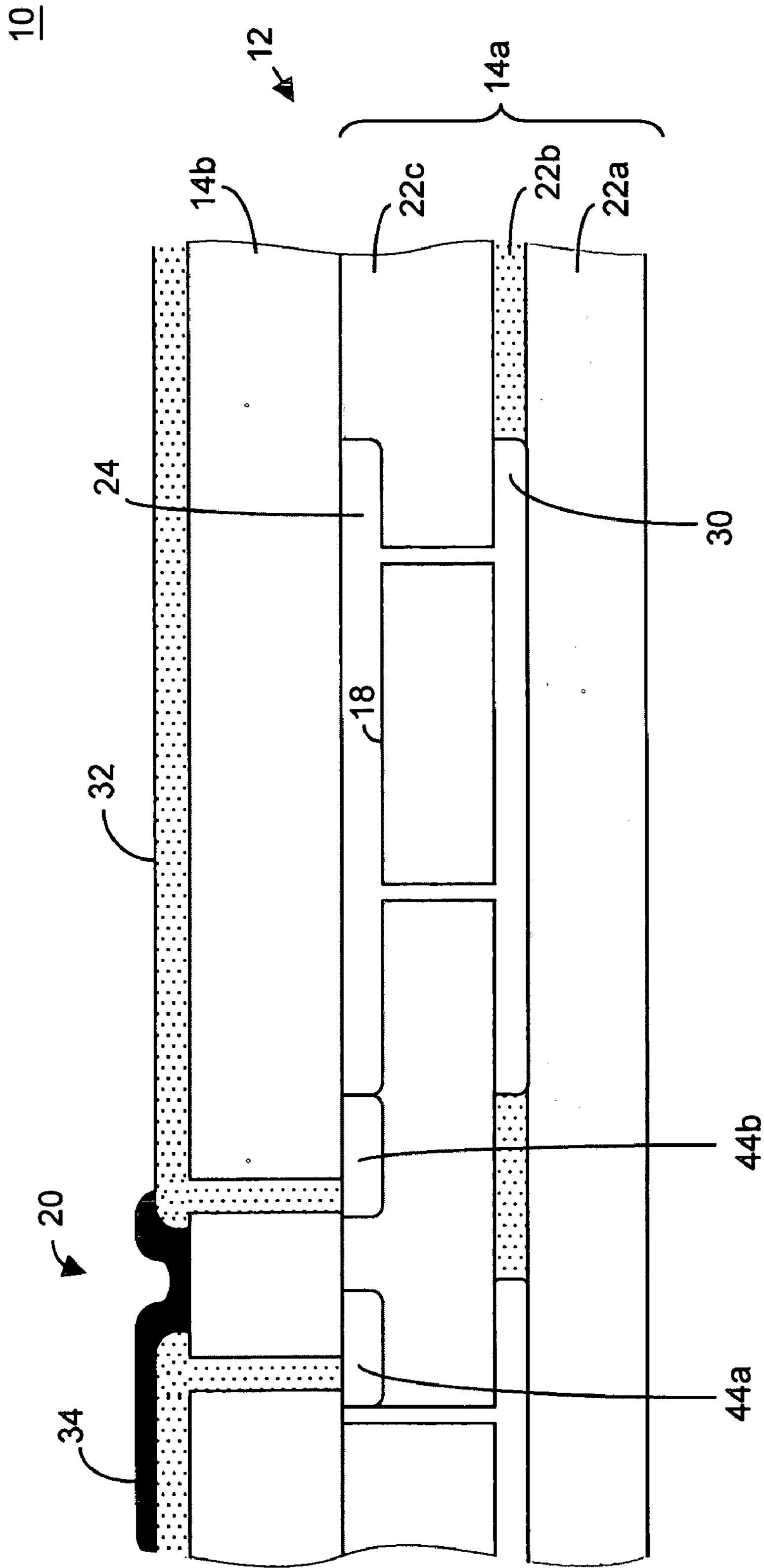


FIGURE 10I



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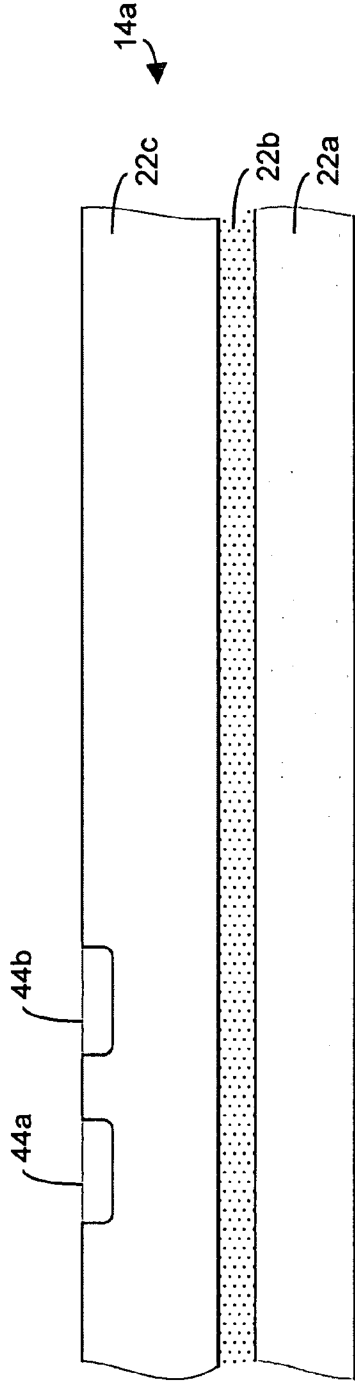
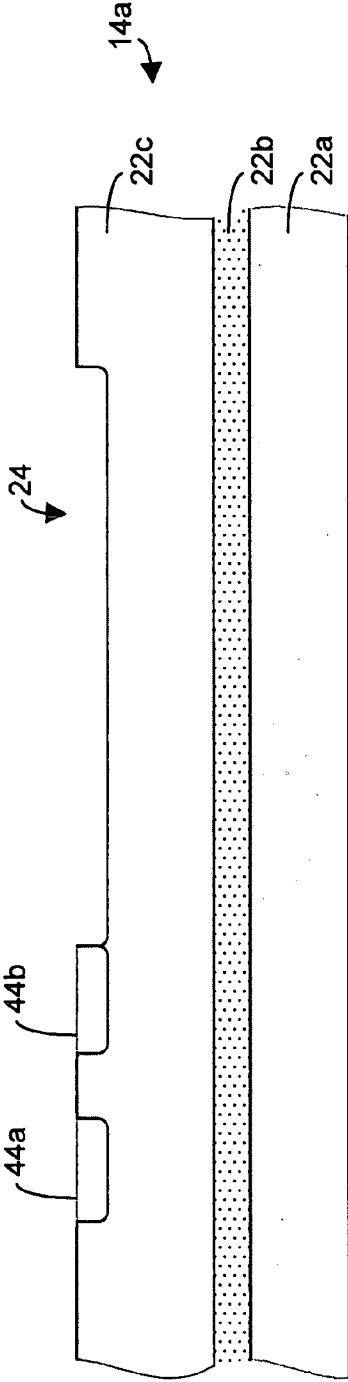


FIGURE 12A



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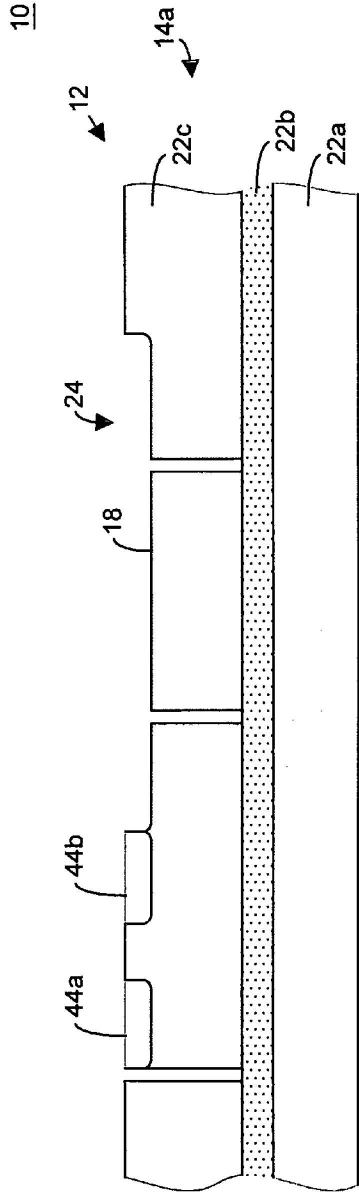


FIGURE 12C

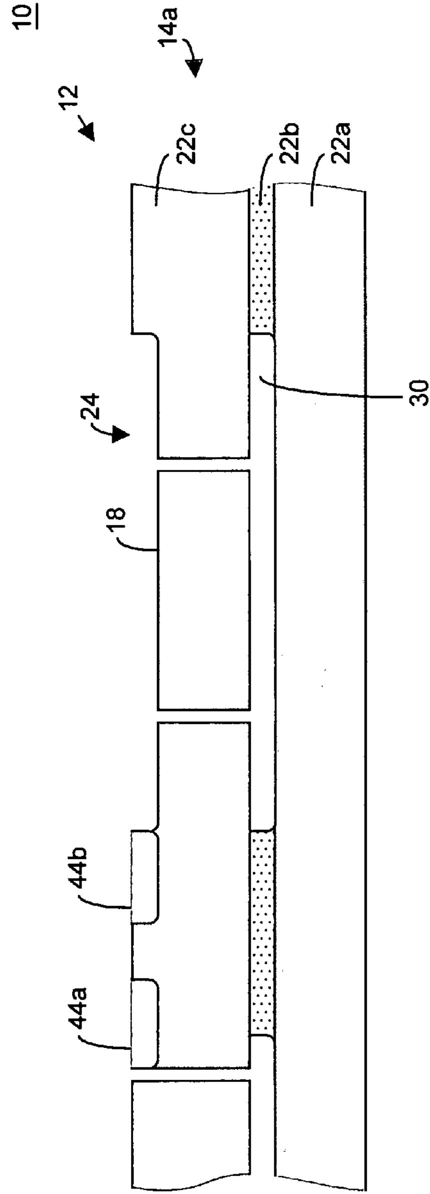


FIGURE 12D

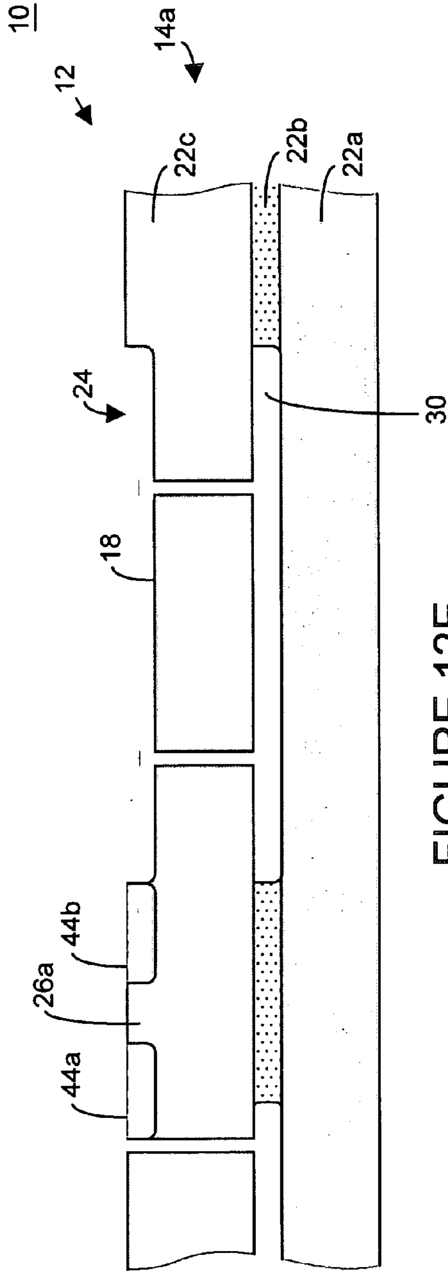
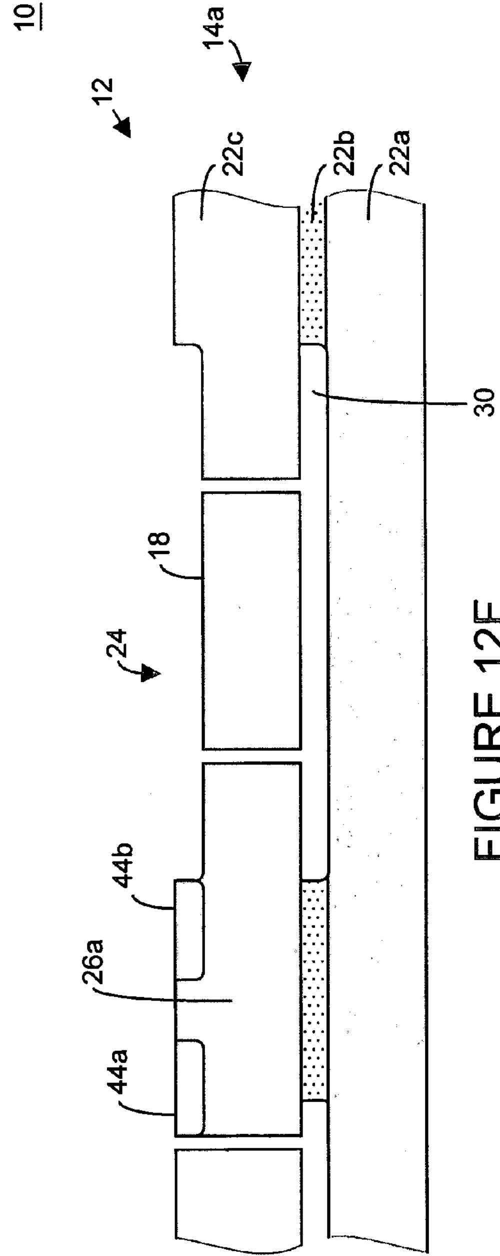


FIGURE 12E



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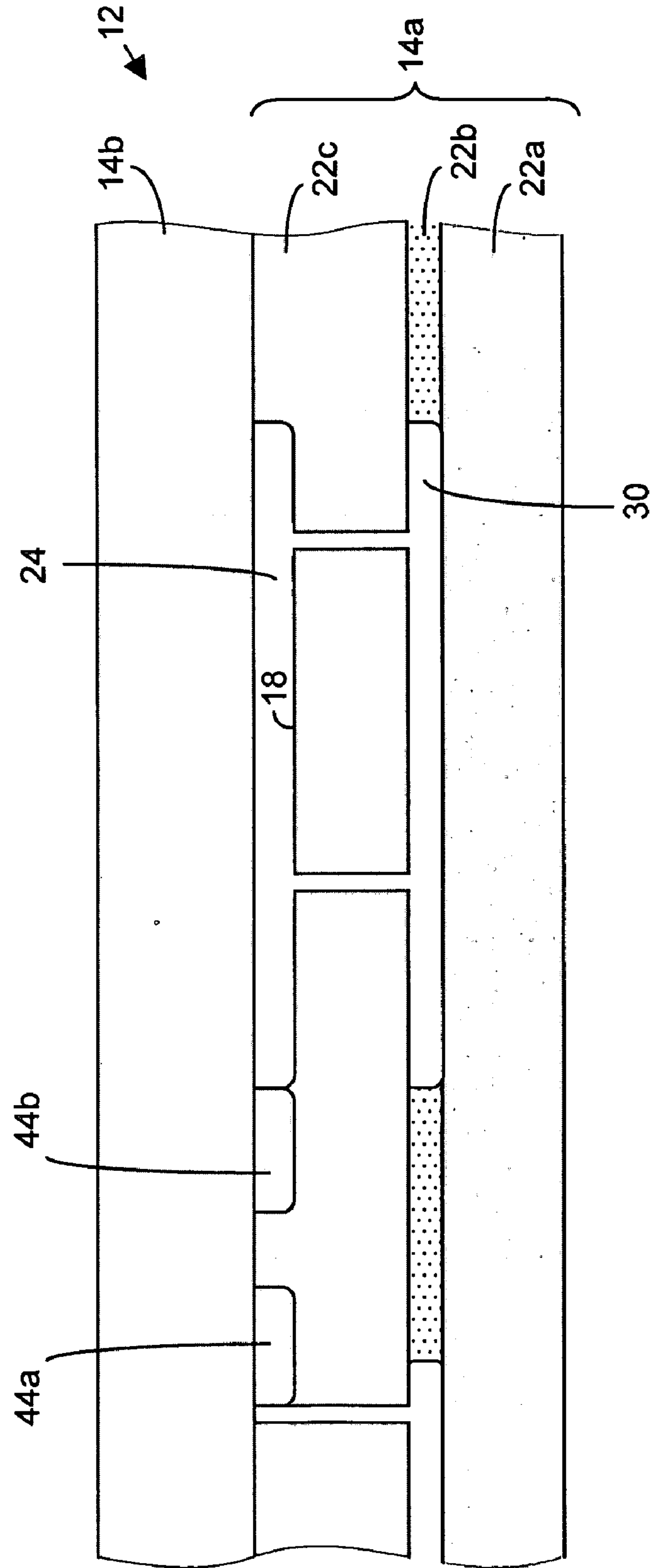


FIGURE 12G

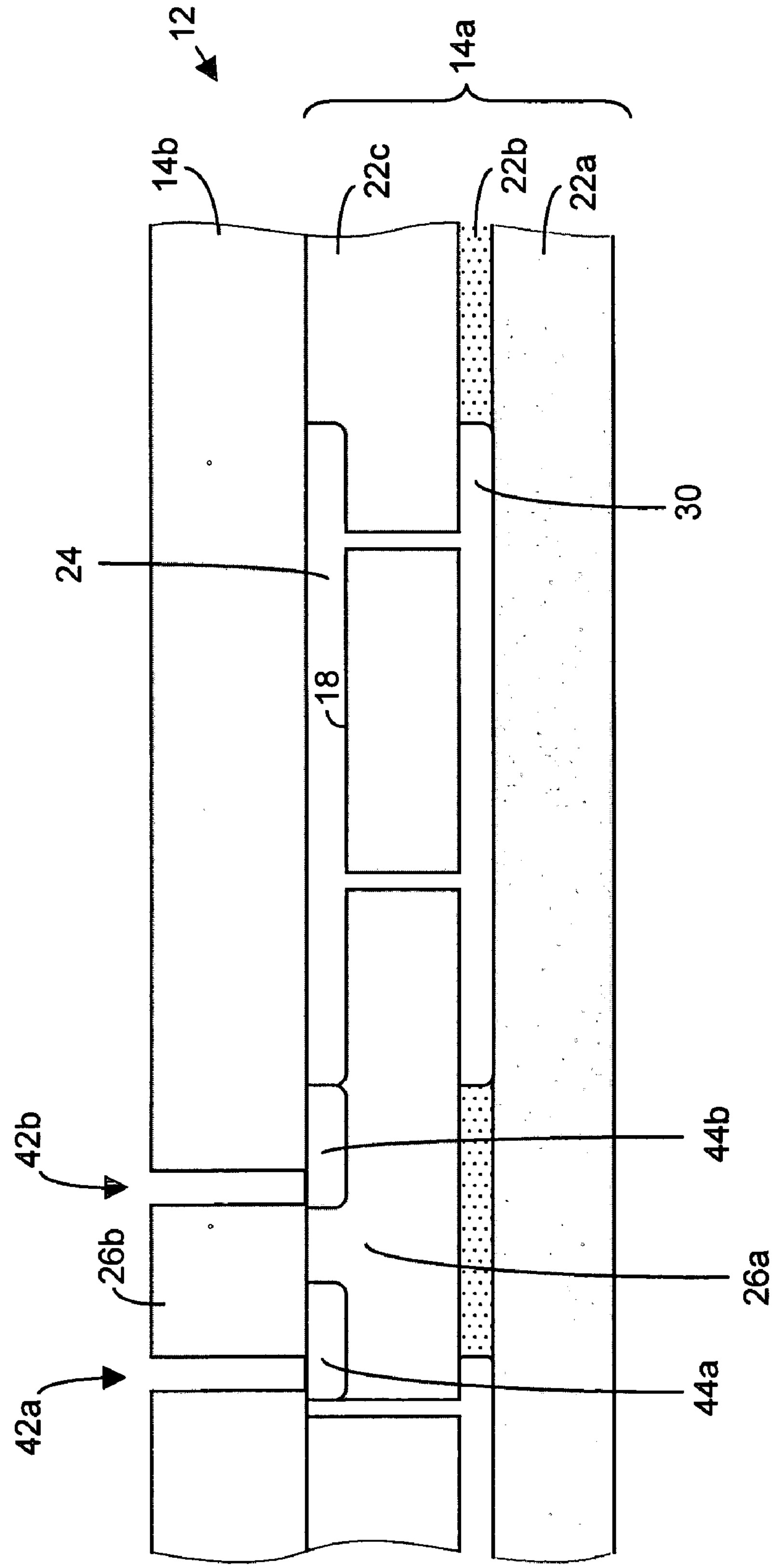


FIGURE 12H

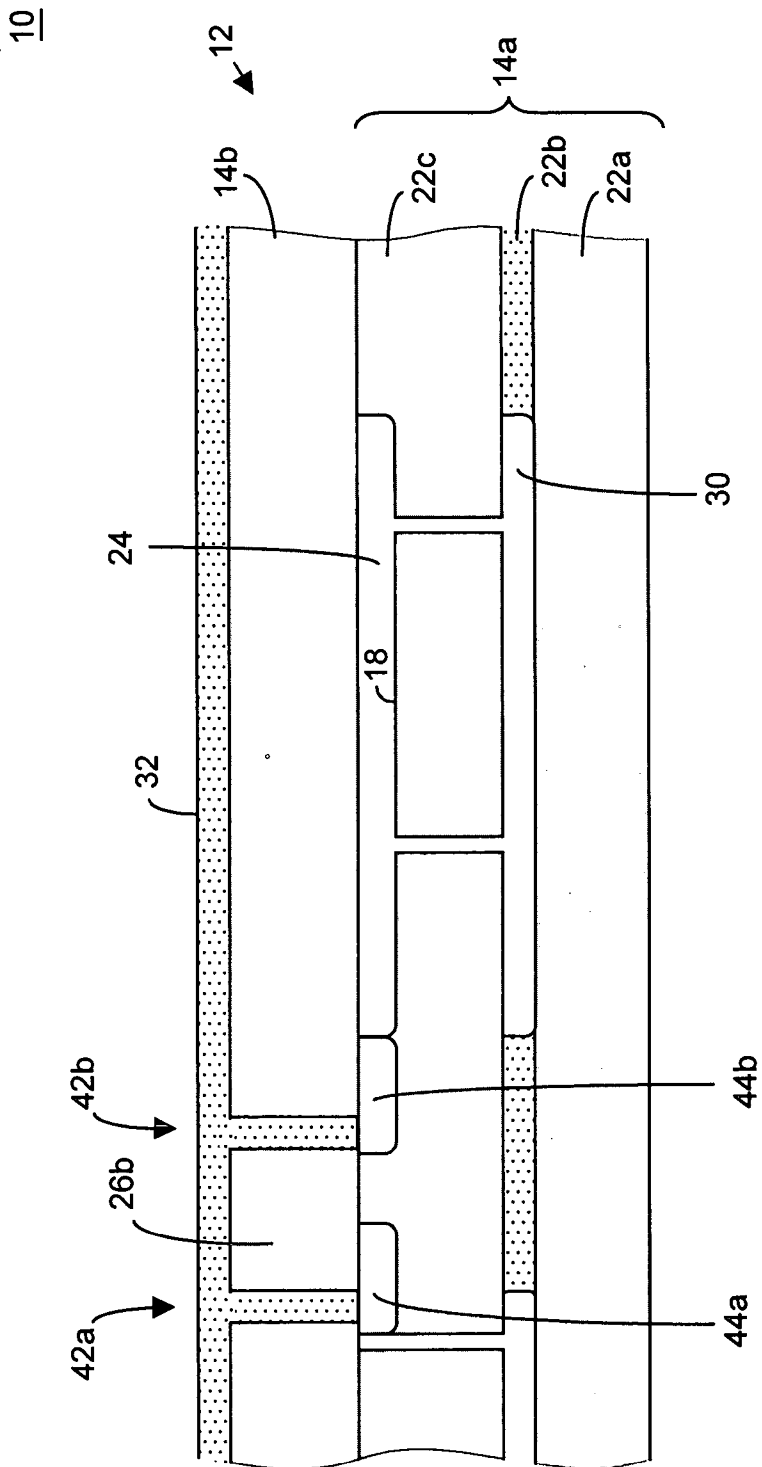


FIGURE 12I

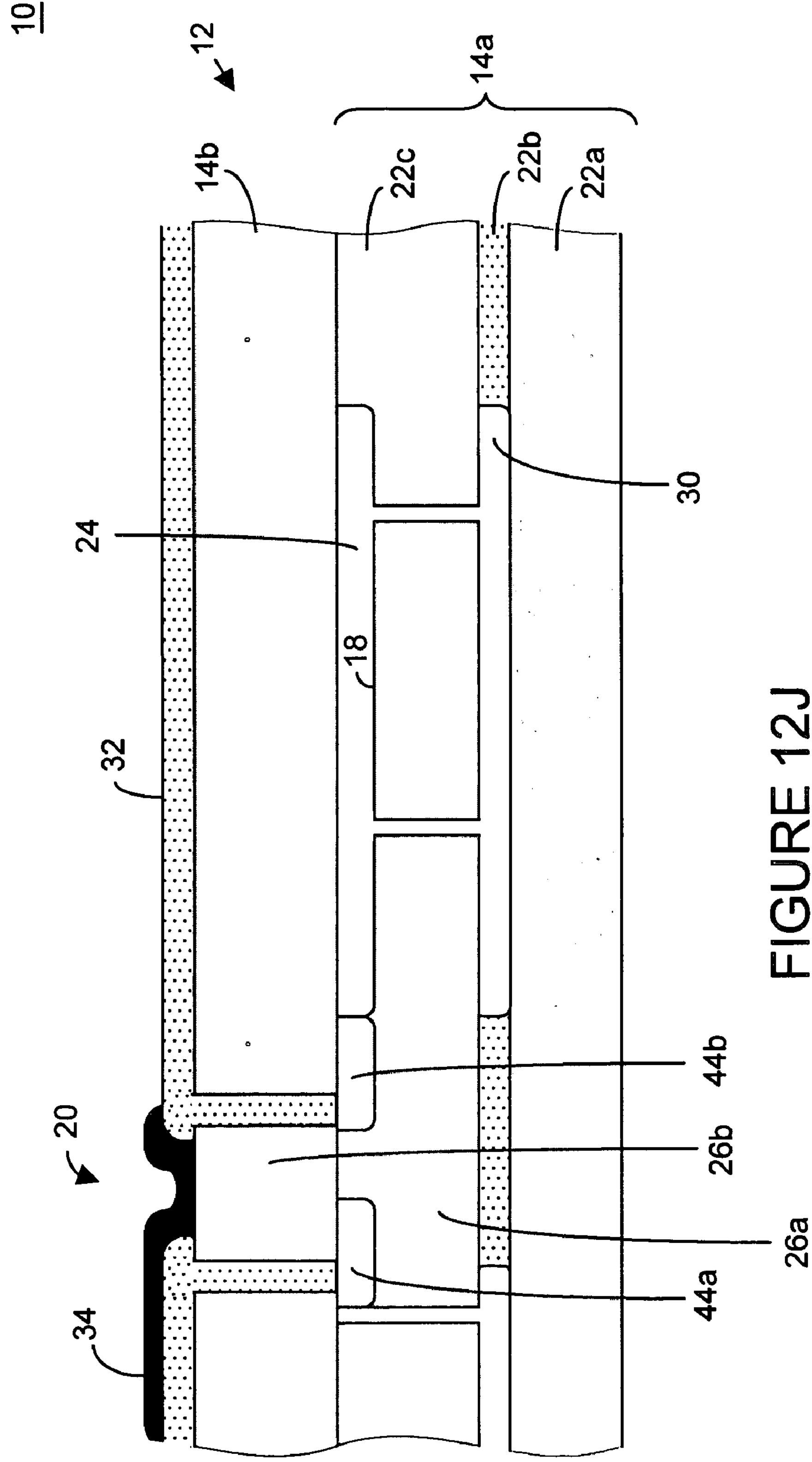


FIGURE 12J

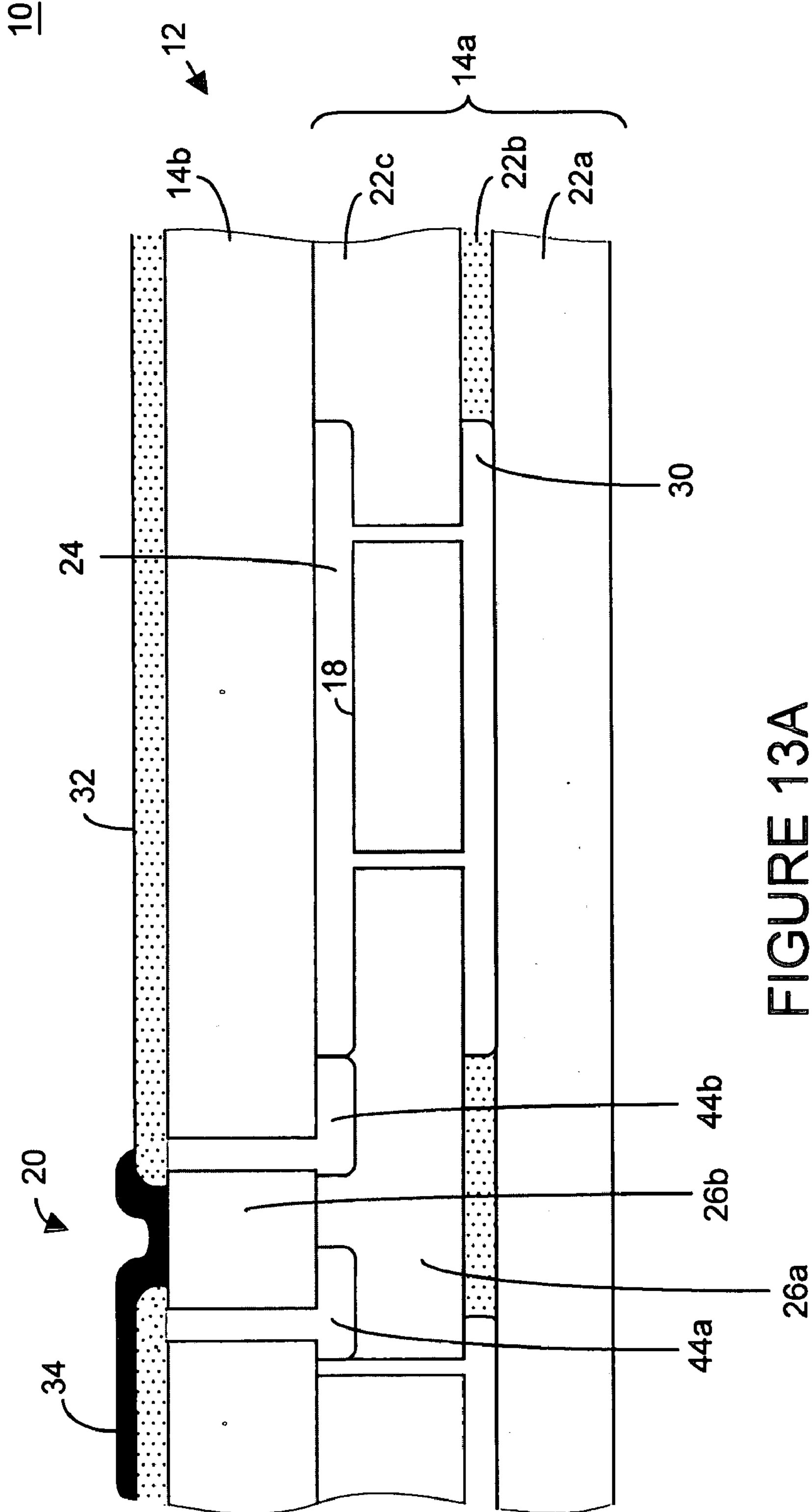
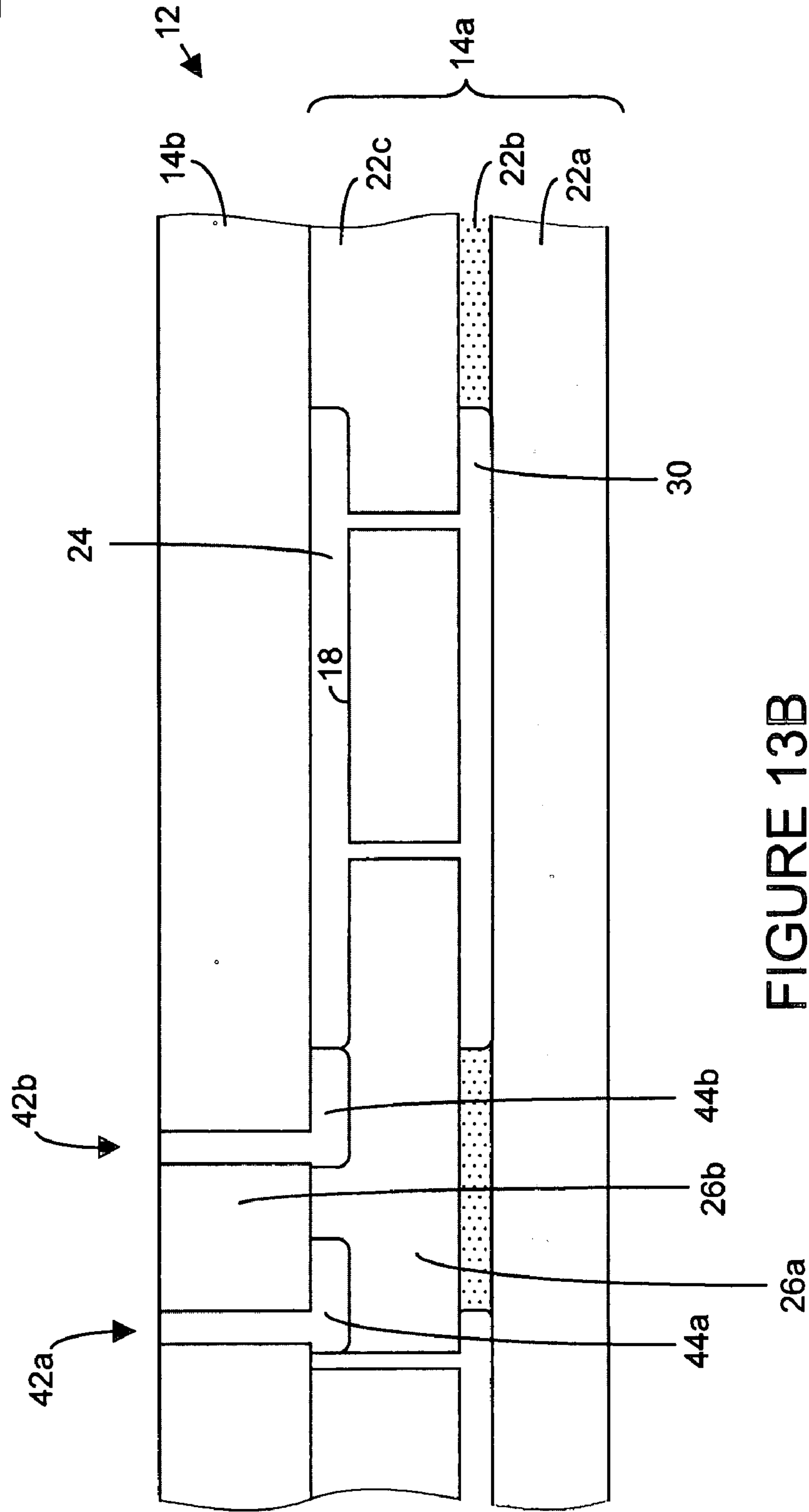


FIGURE 13A



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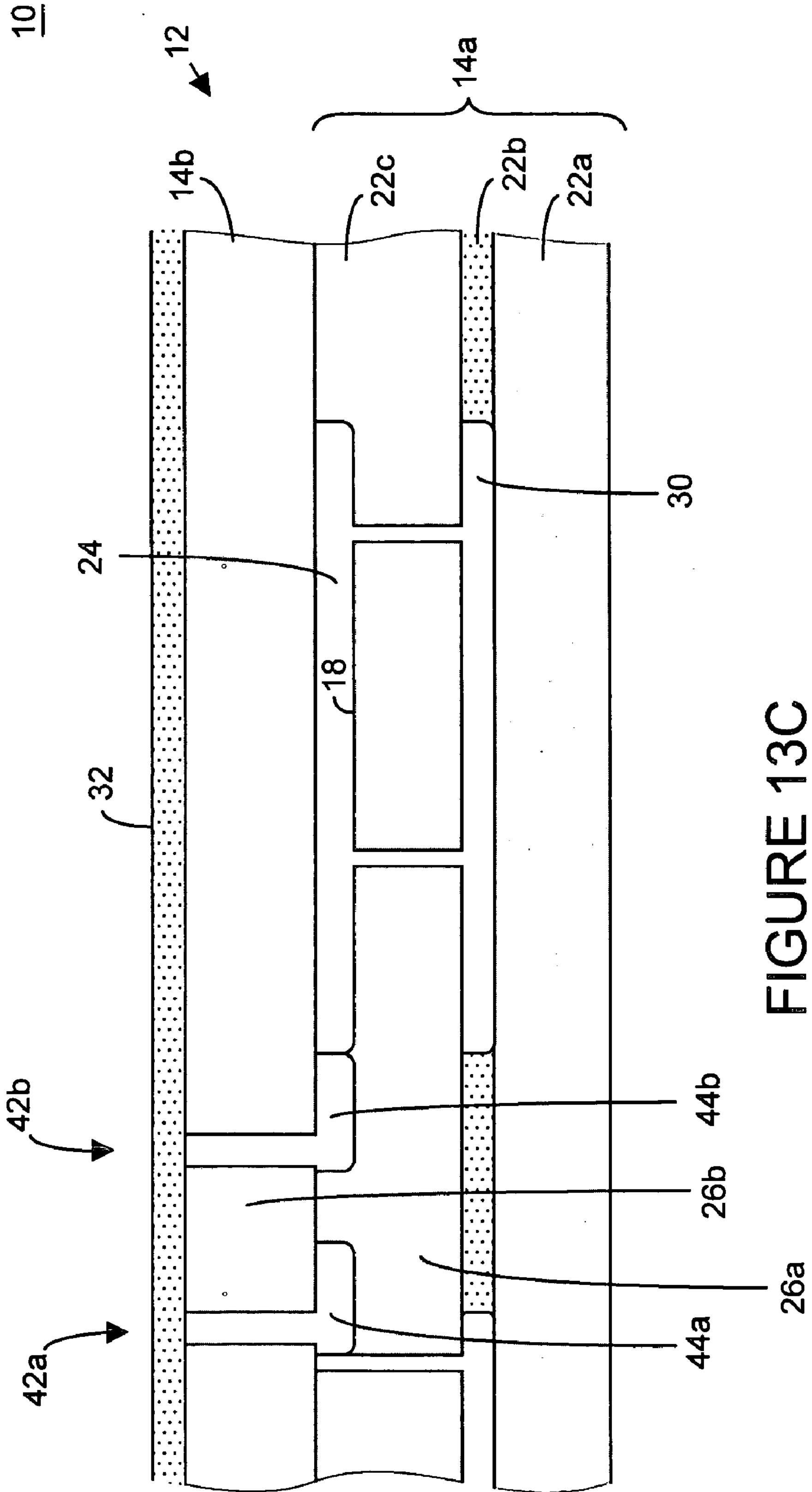

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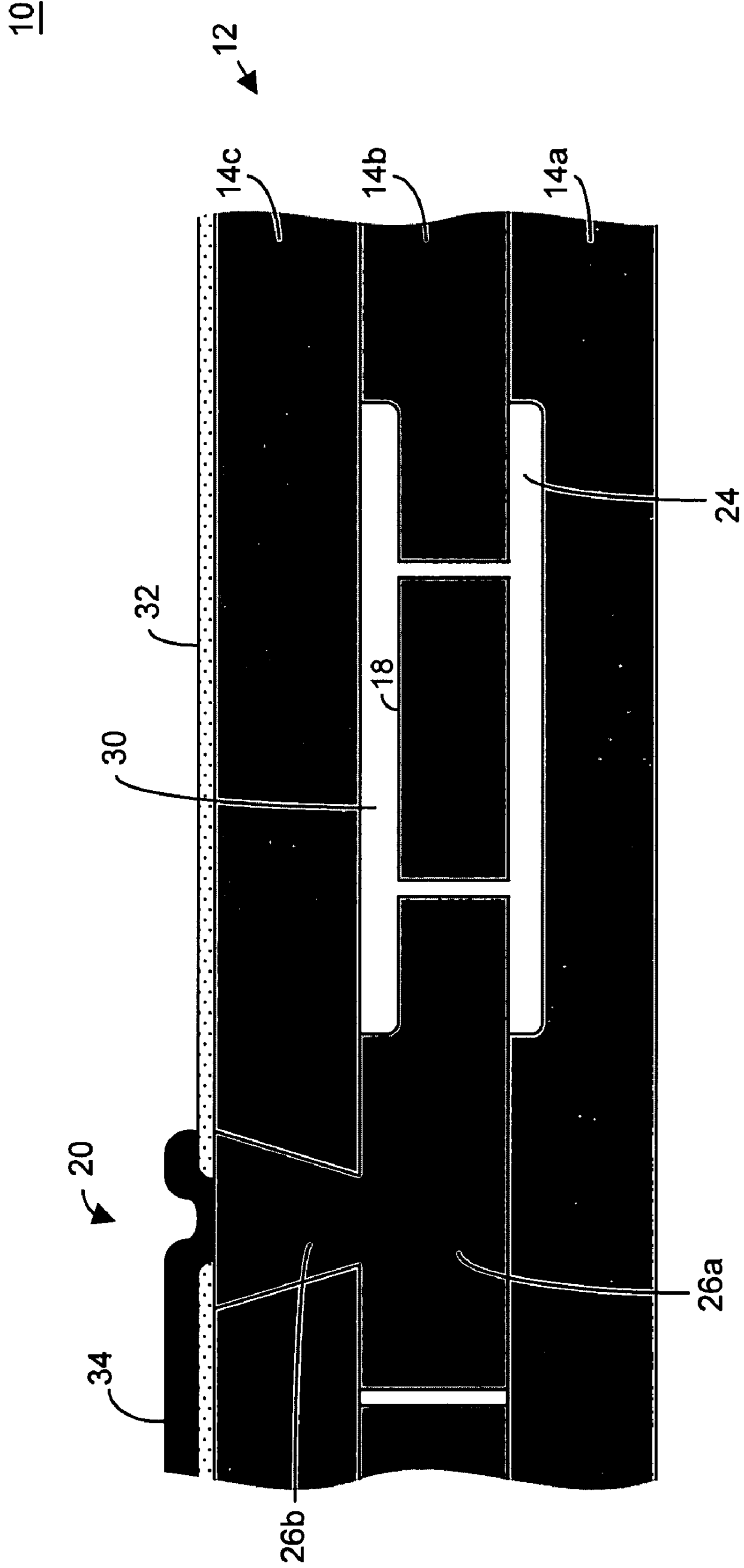

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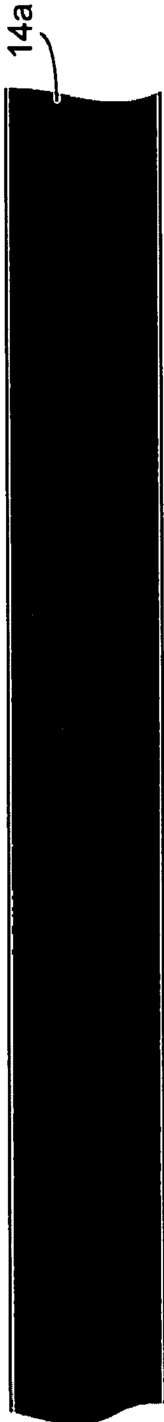


FIGURE 15A

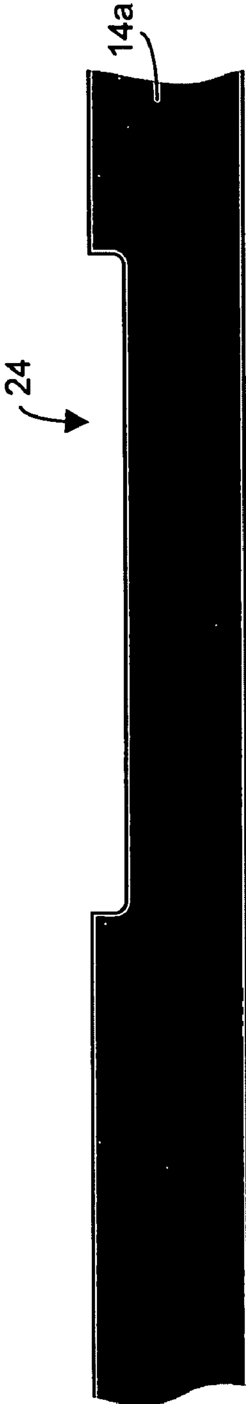
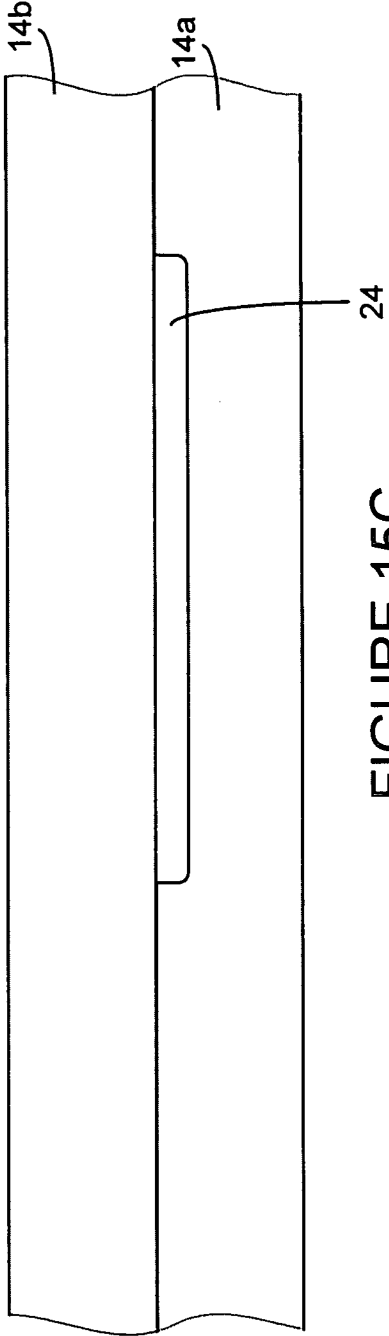


FIGURE 15B



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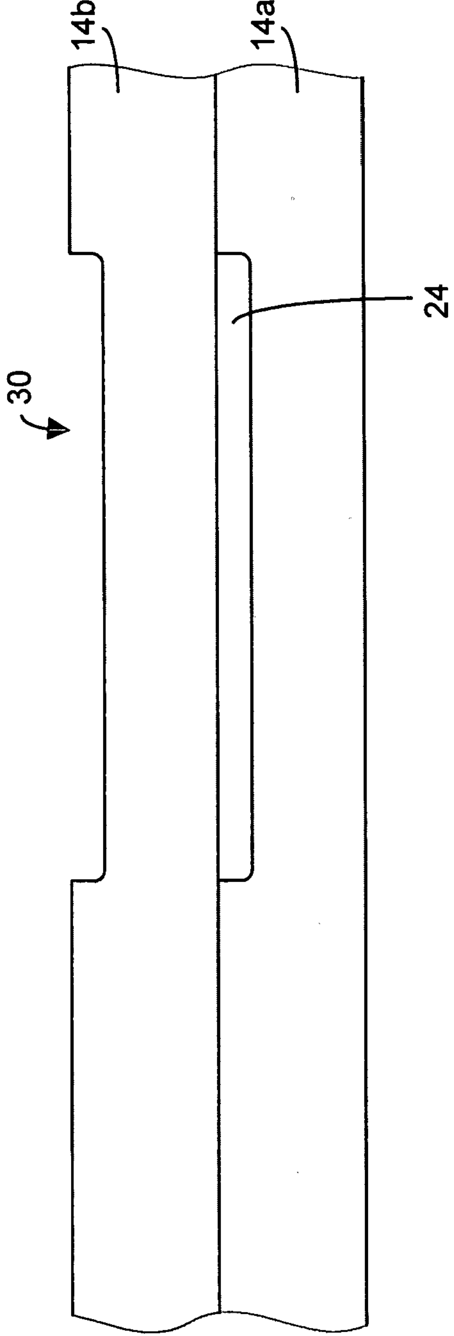
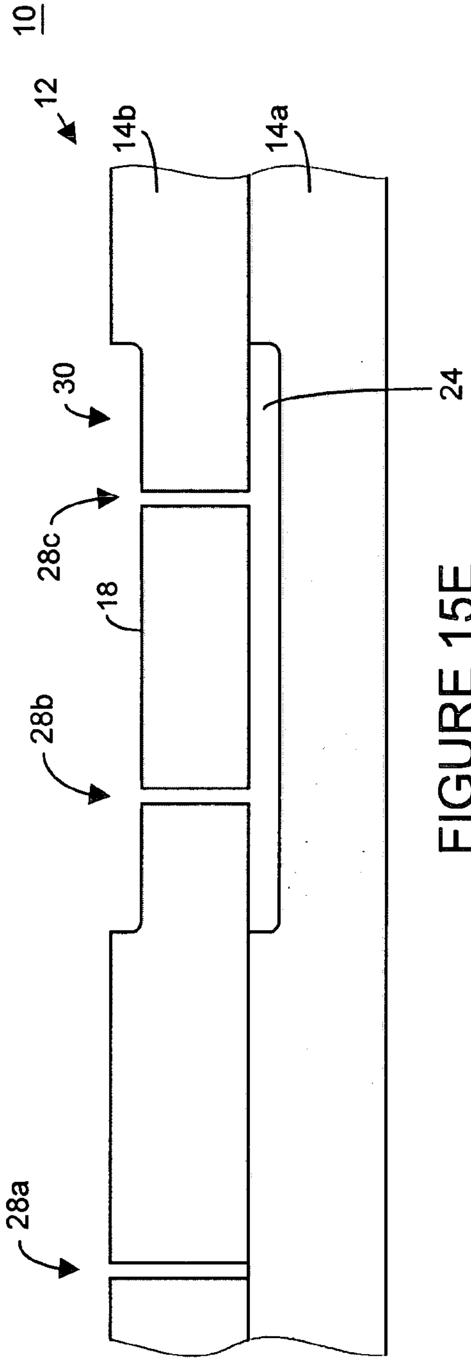


FIGURE 15D



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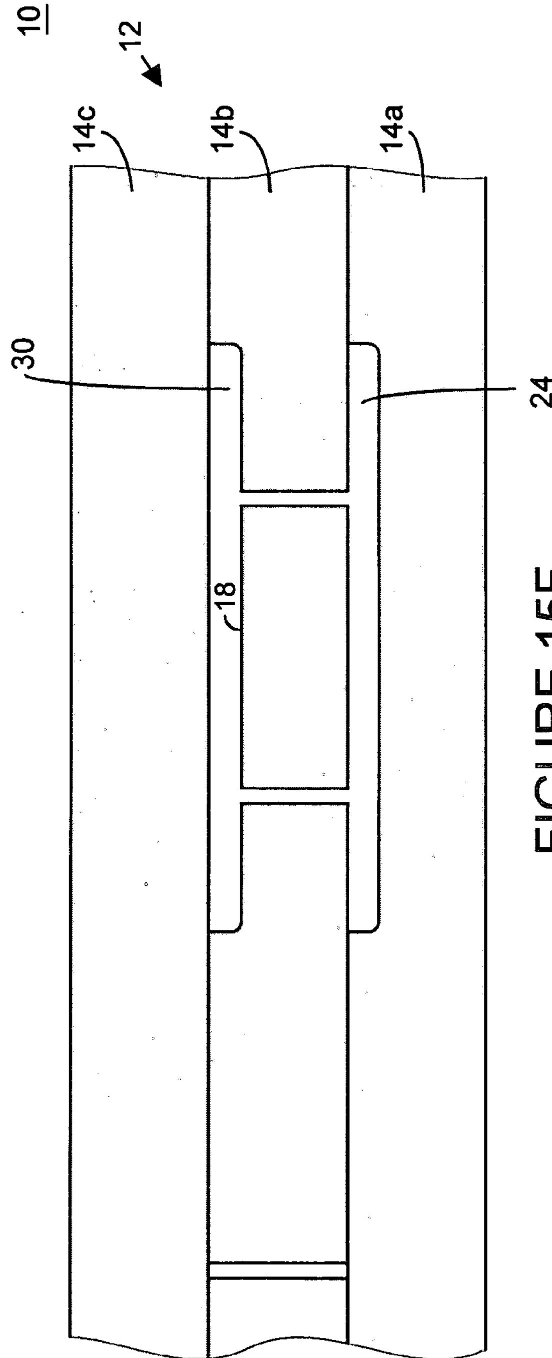

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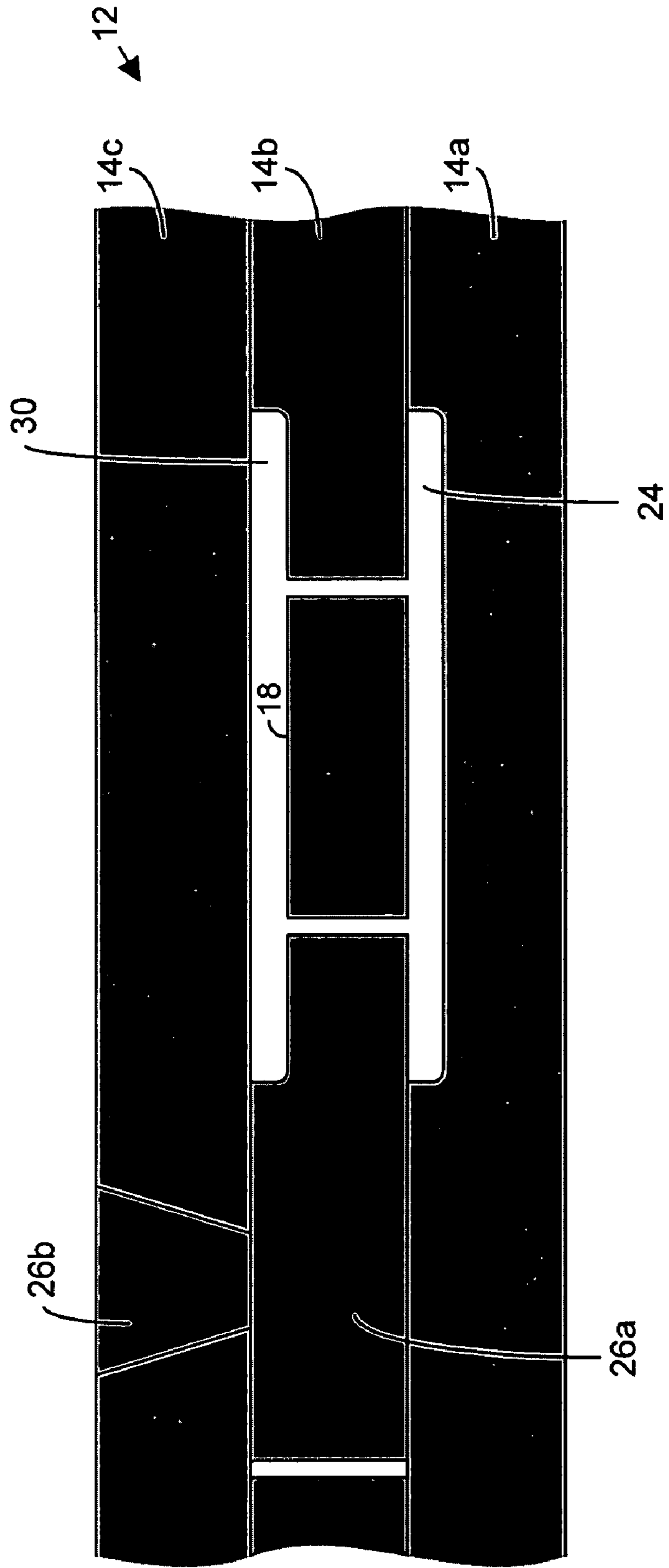

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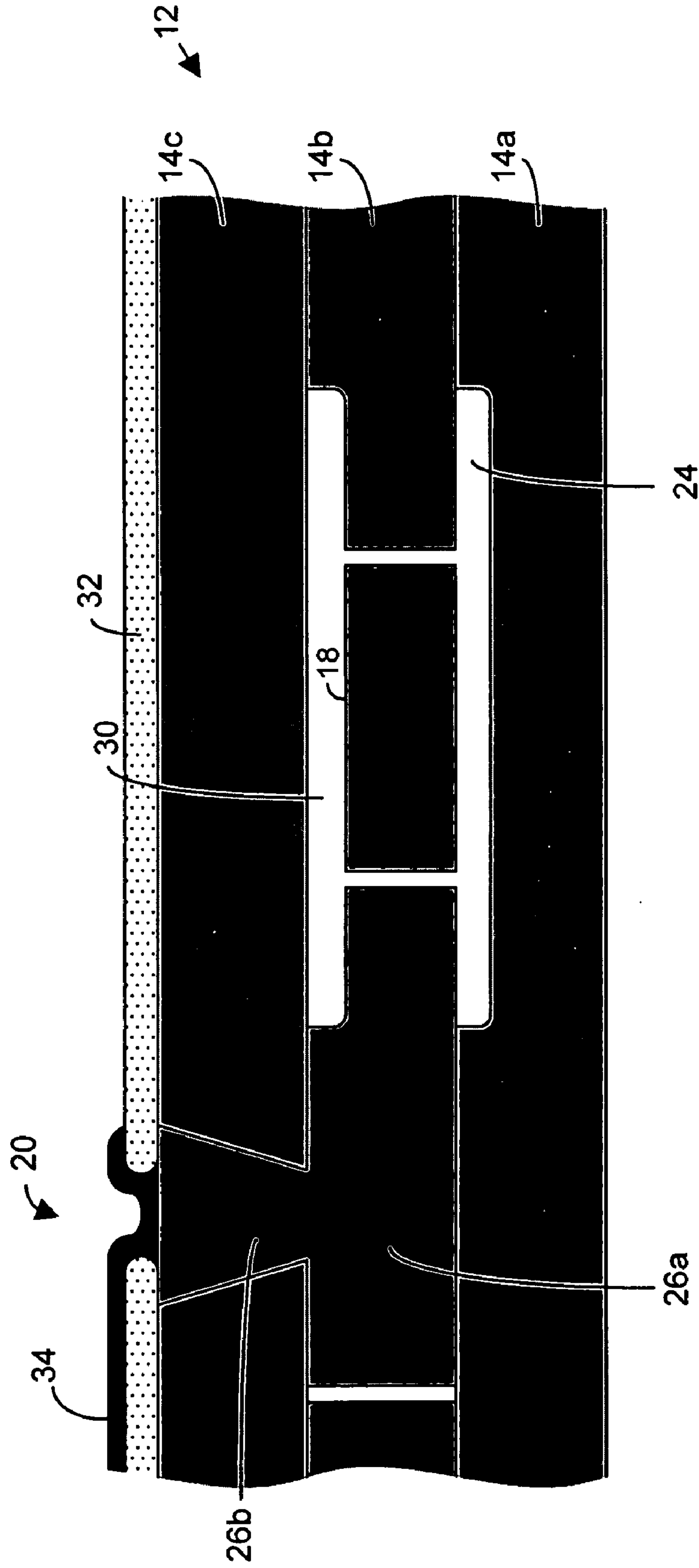
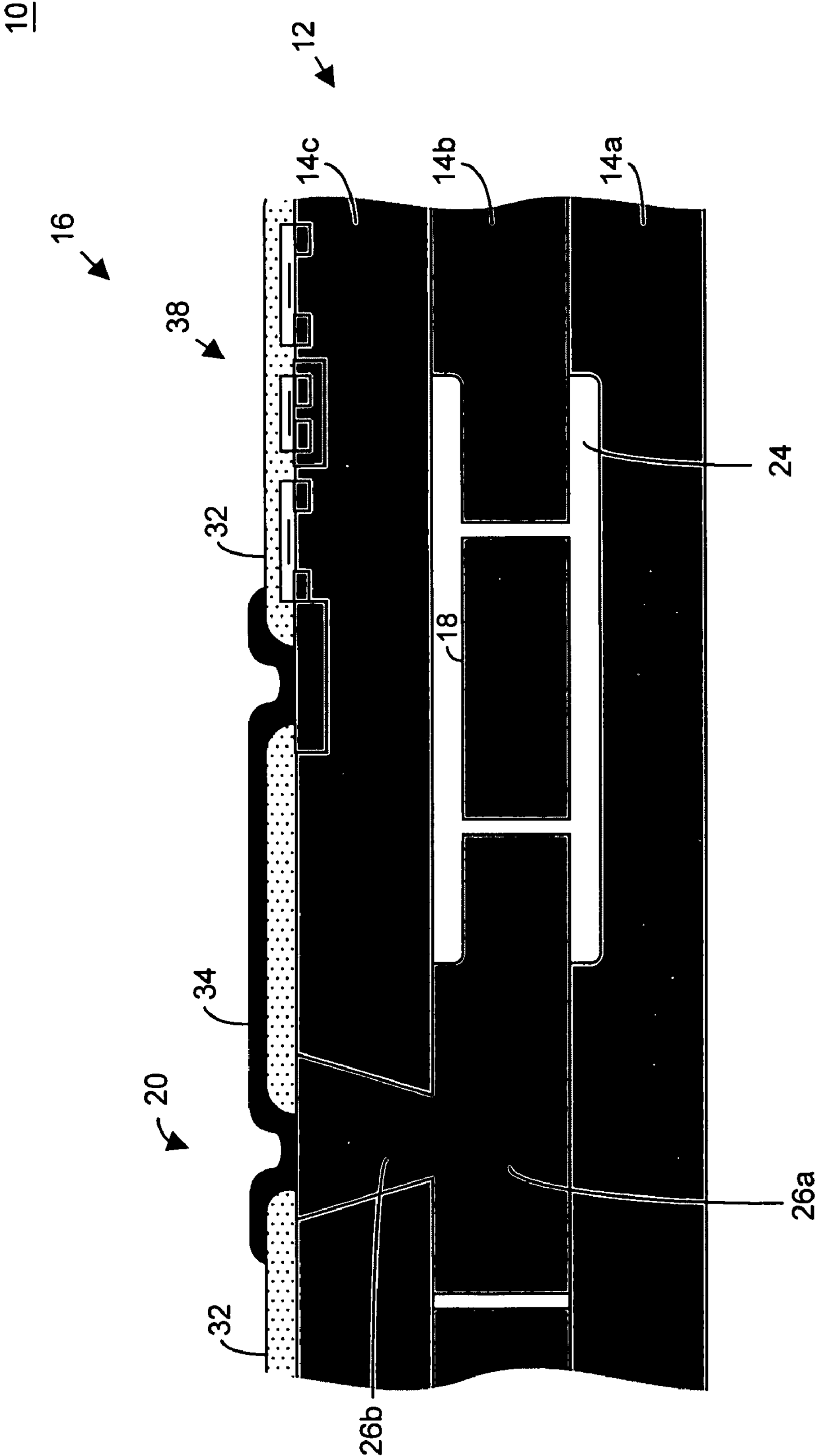


FIGURE 15H



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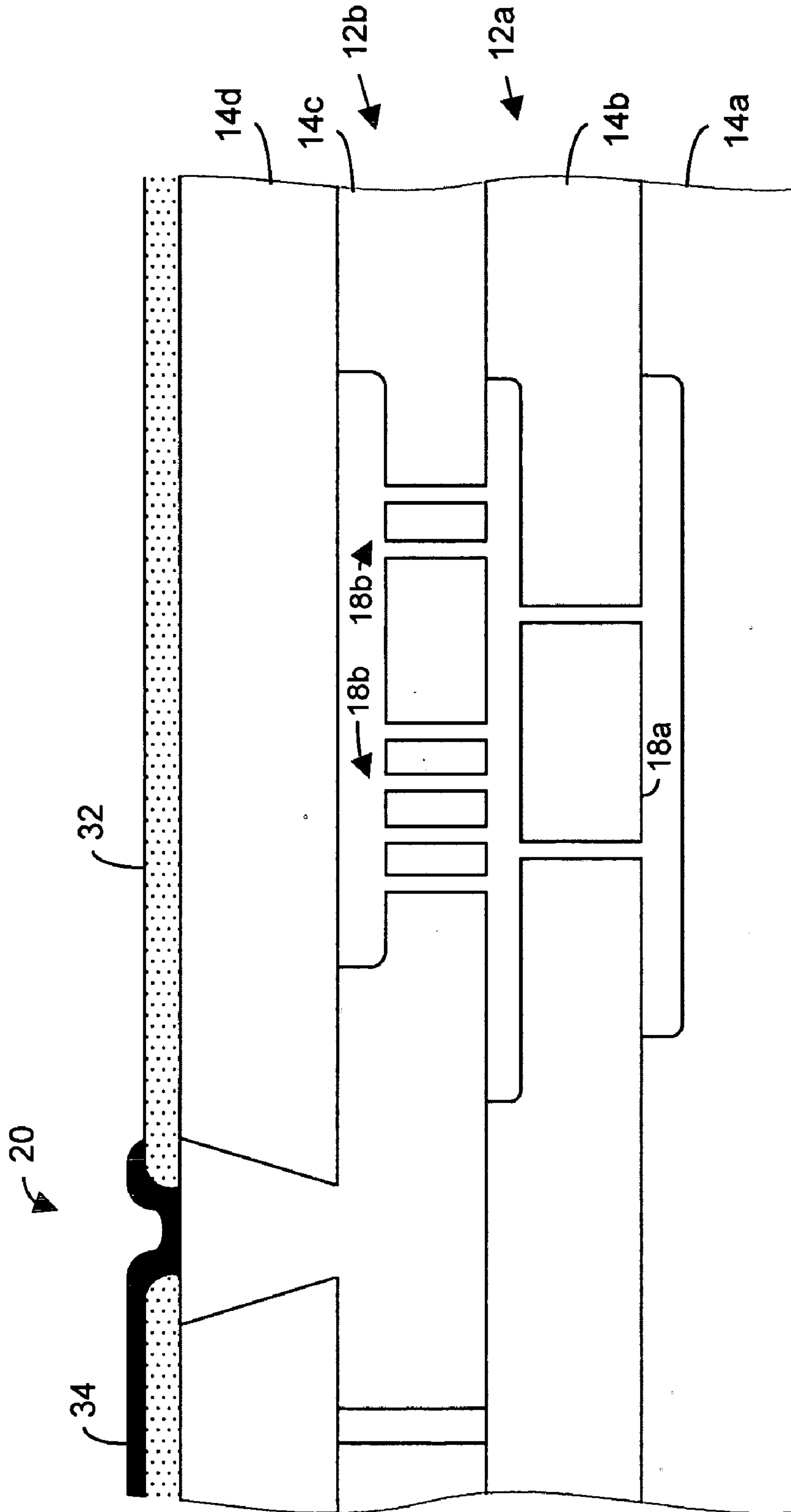
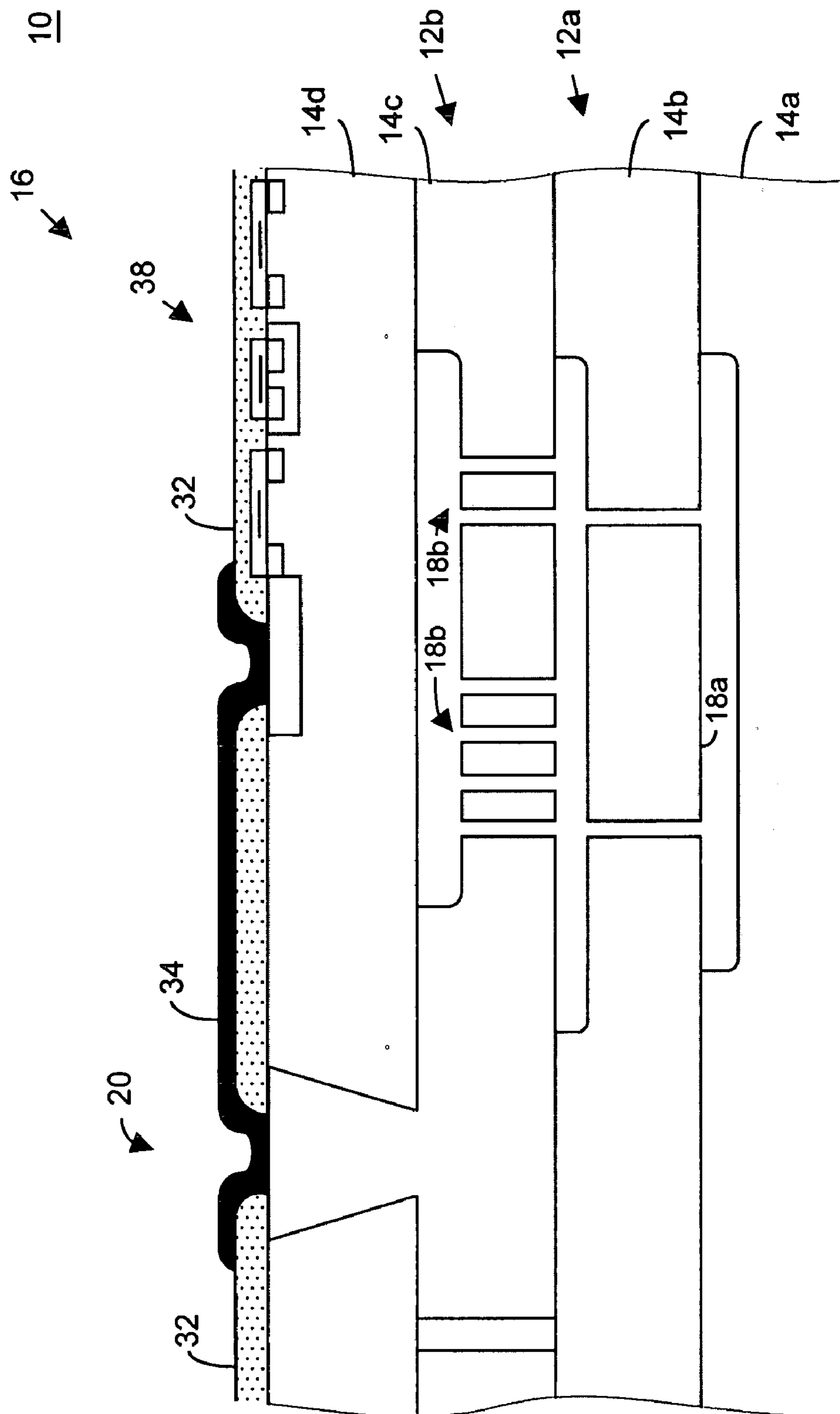


FIGURE 17



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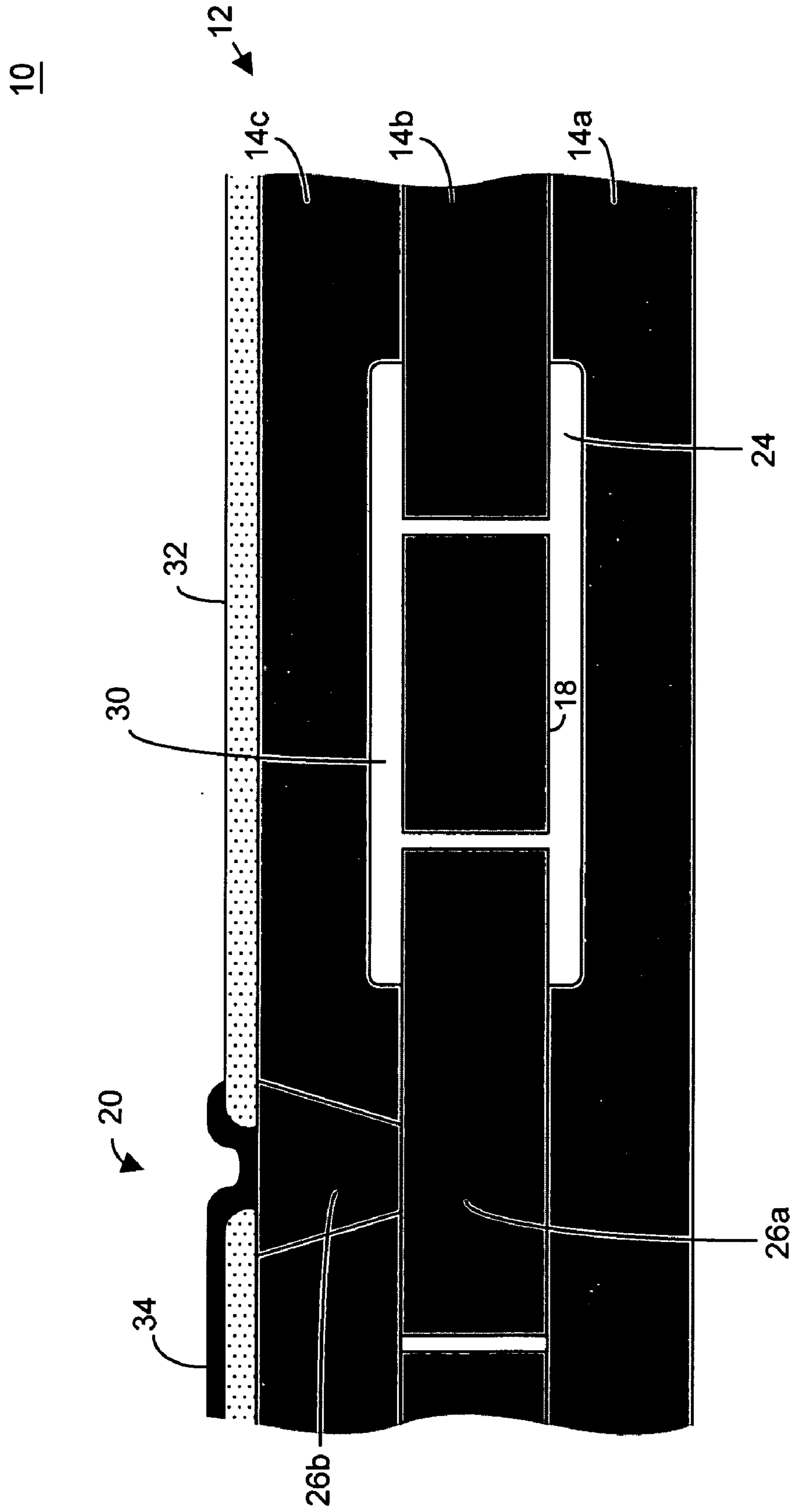


FIGURE 19

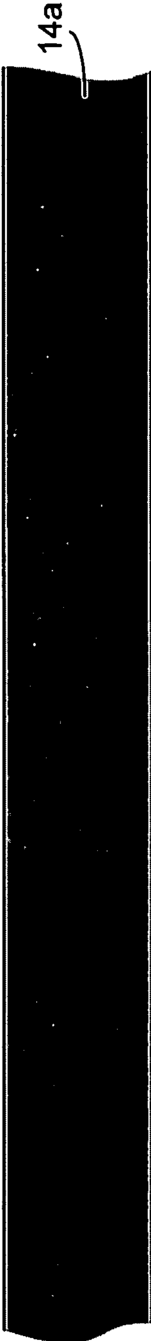


FIGURE 20A

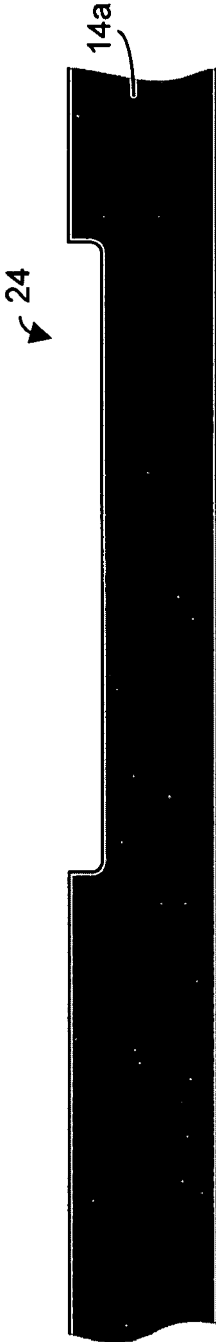


FIGURE 20B

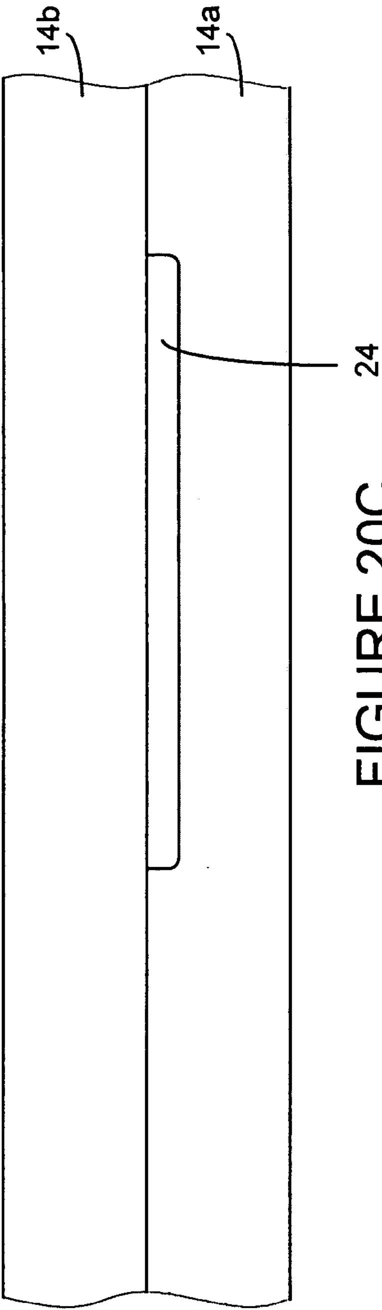


FIGURE 20C

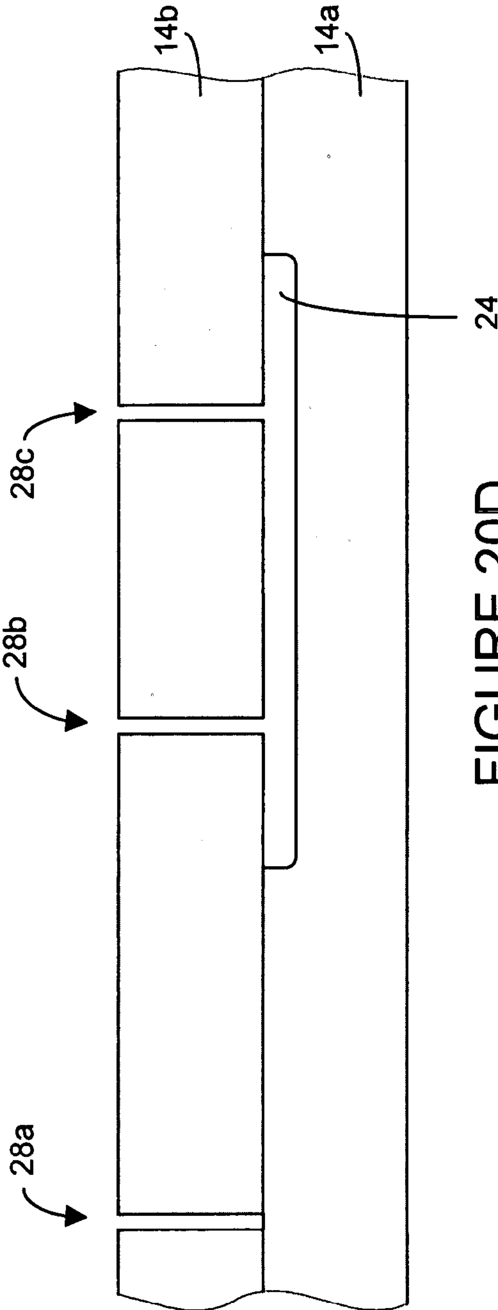


FIGURE 20D

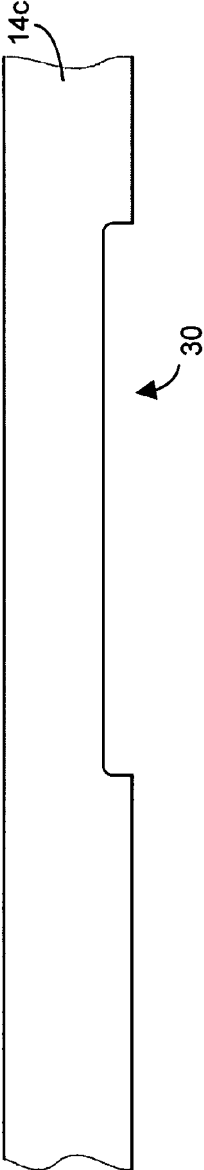


FIGURE 20E

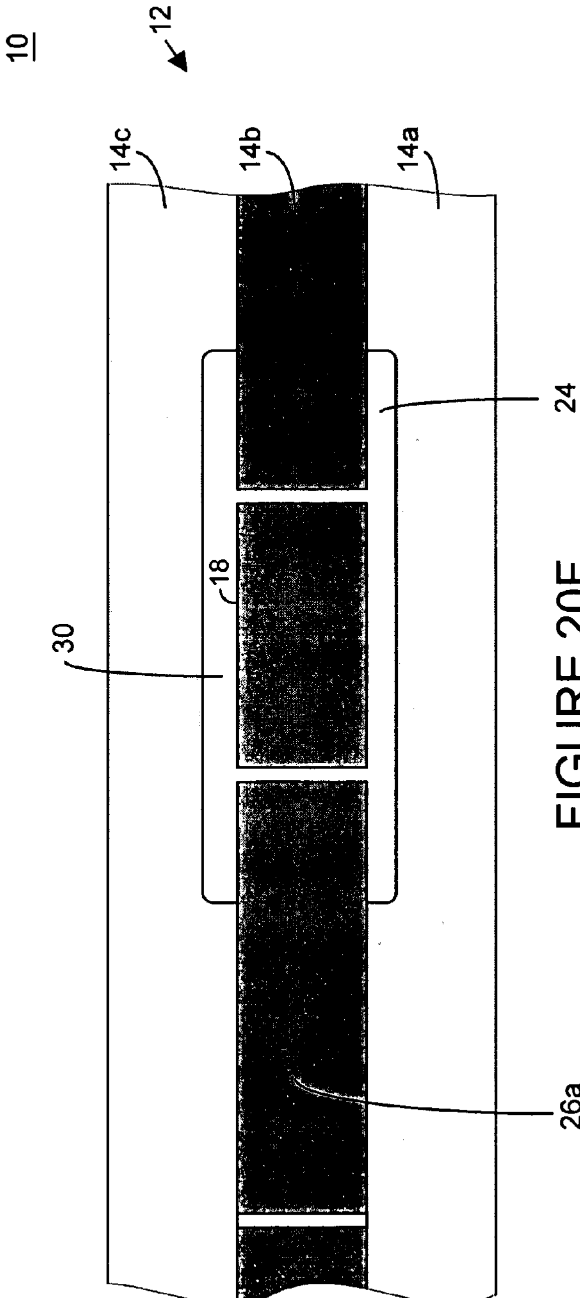


FIGURE 20F

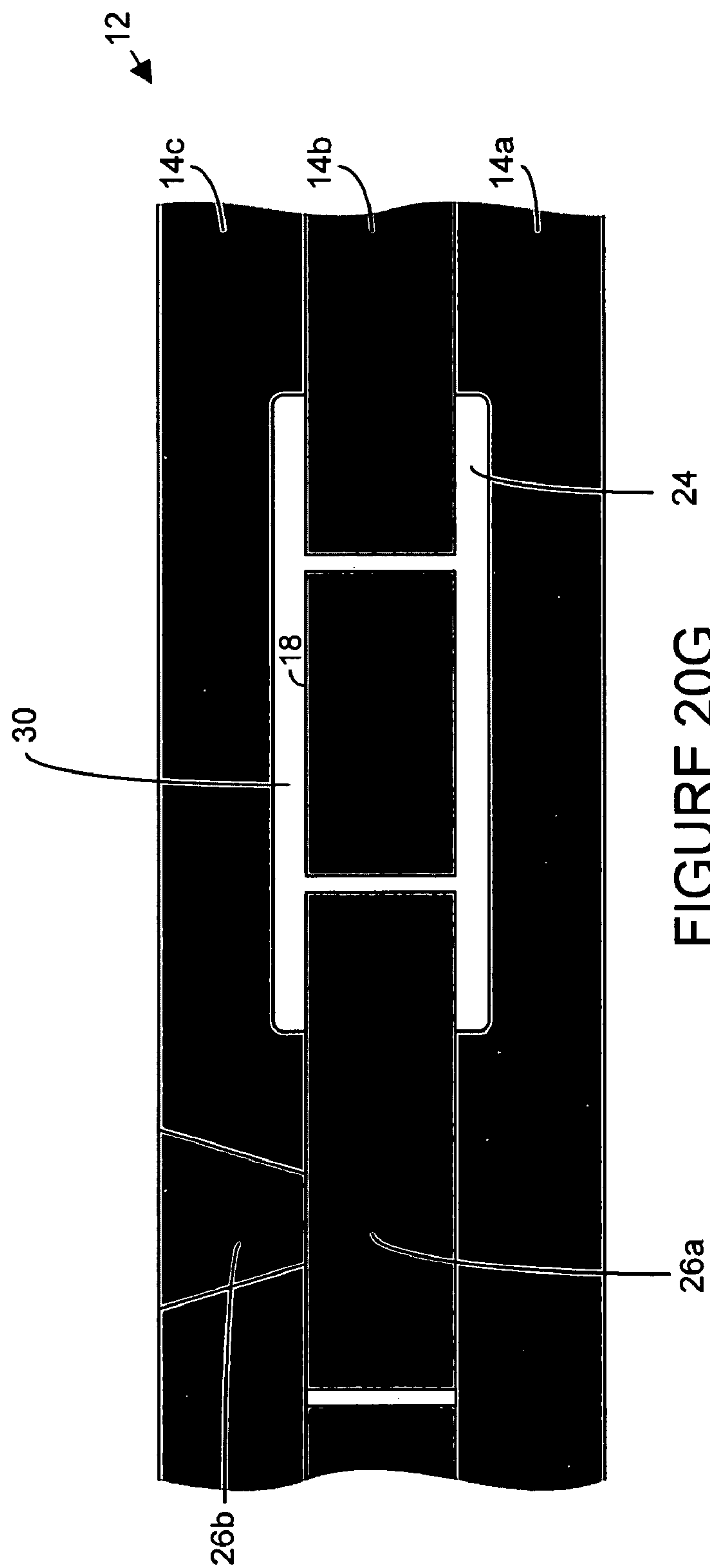


FIGURE 20G

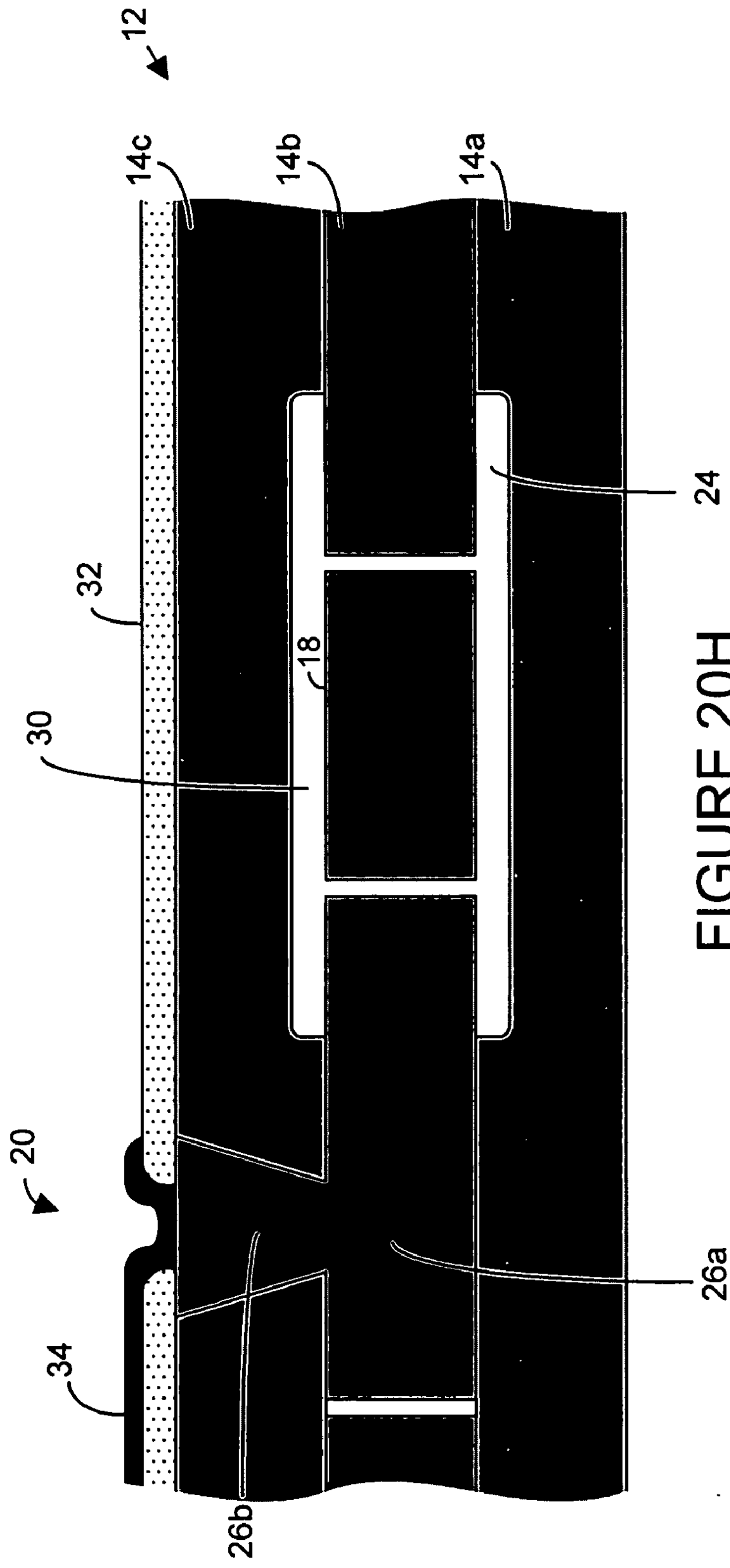


FIGURE 20H

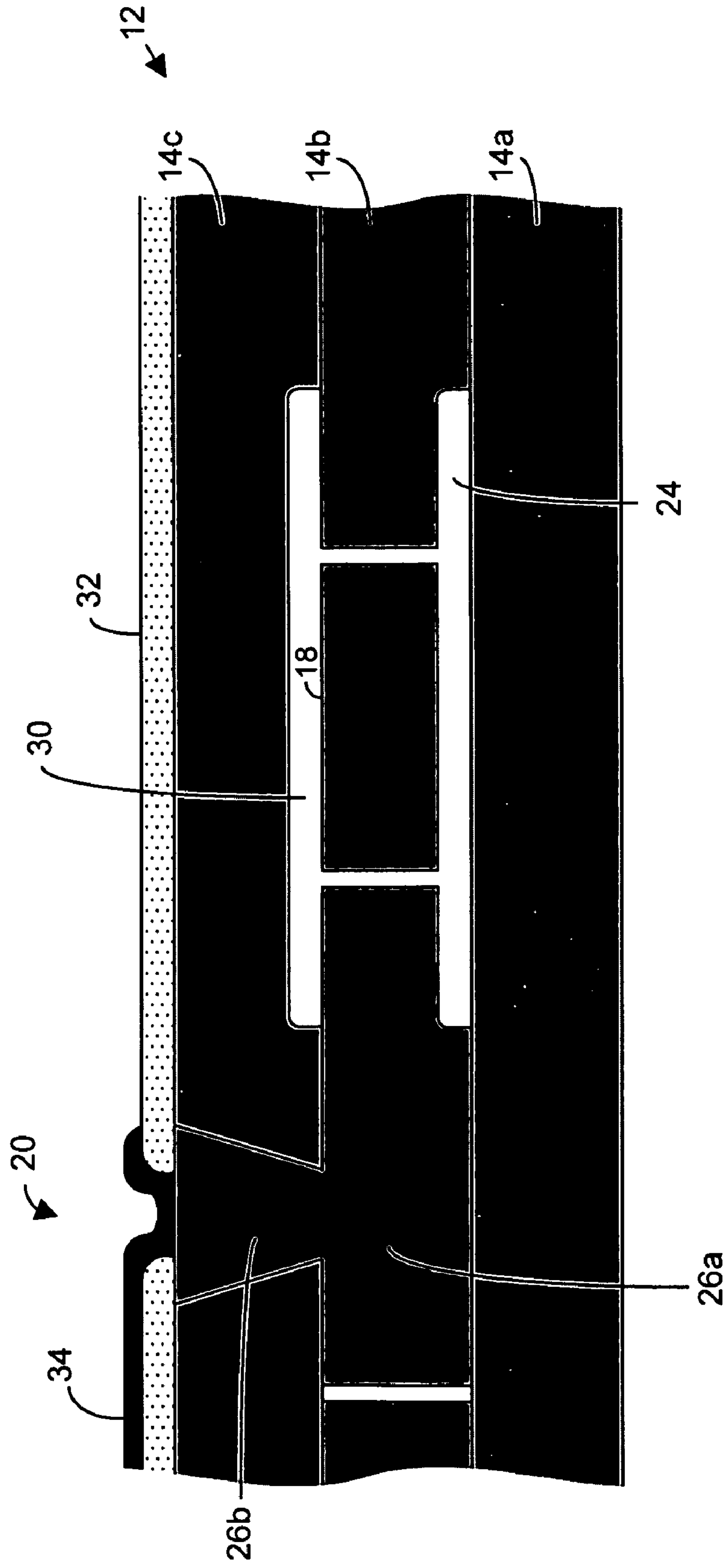


FIGURE 21

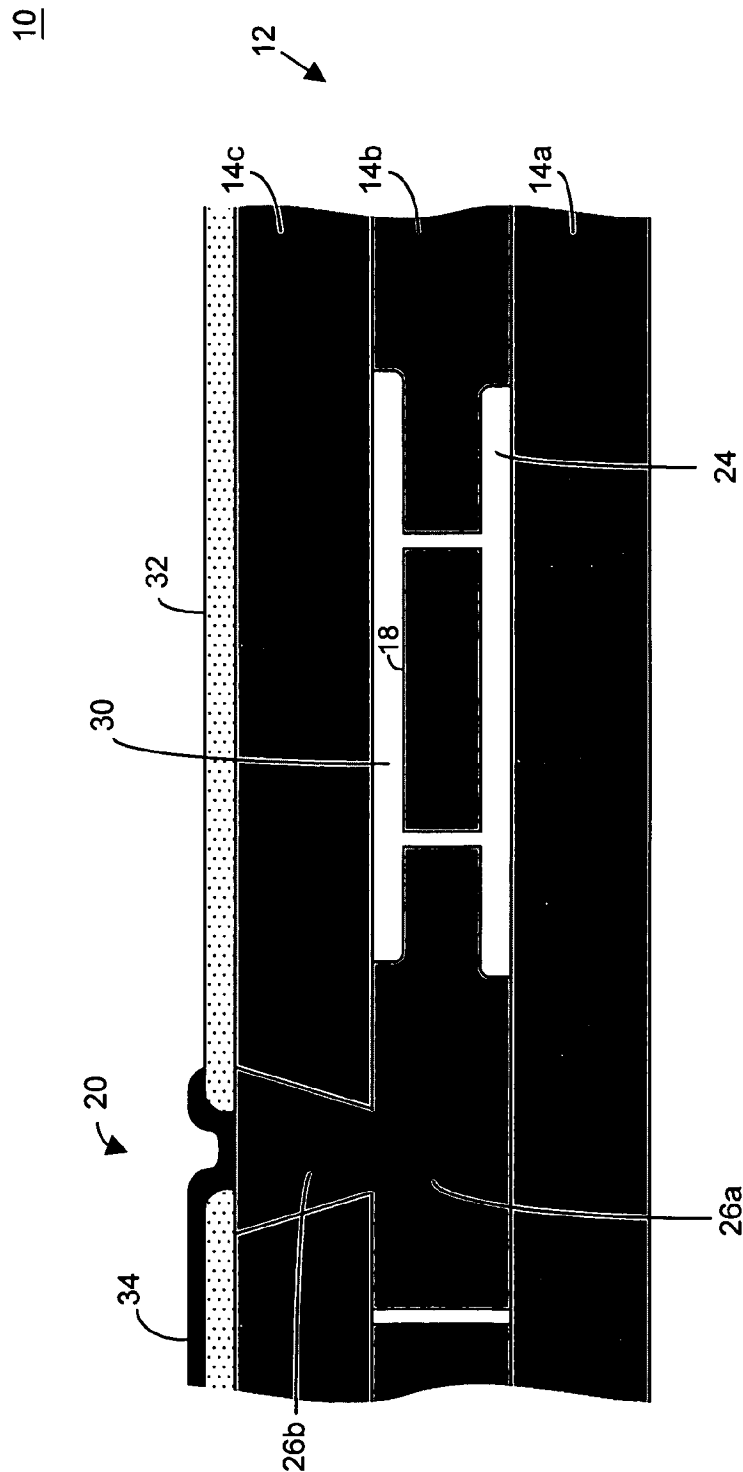


FIGURE 22

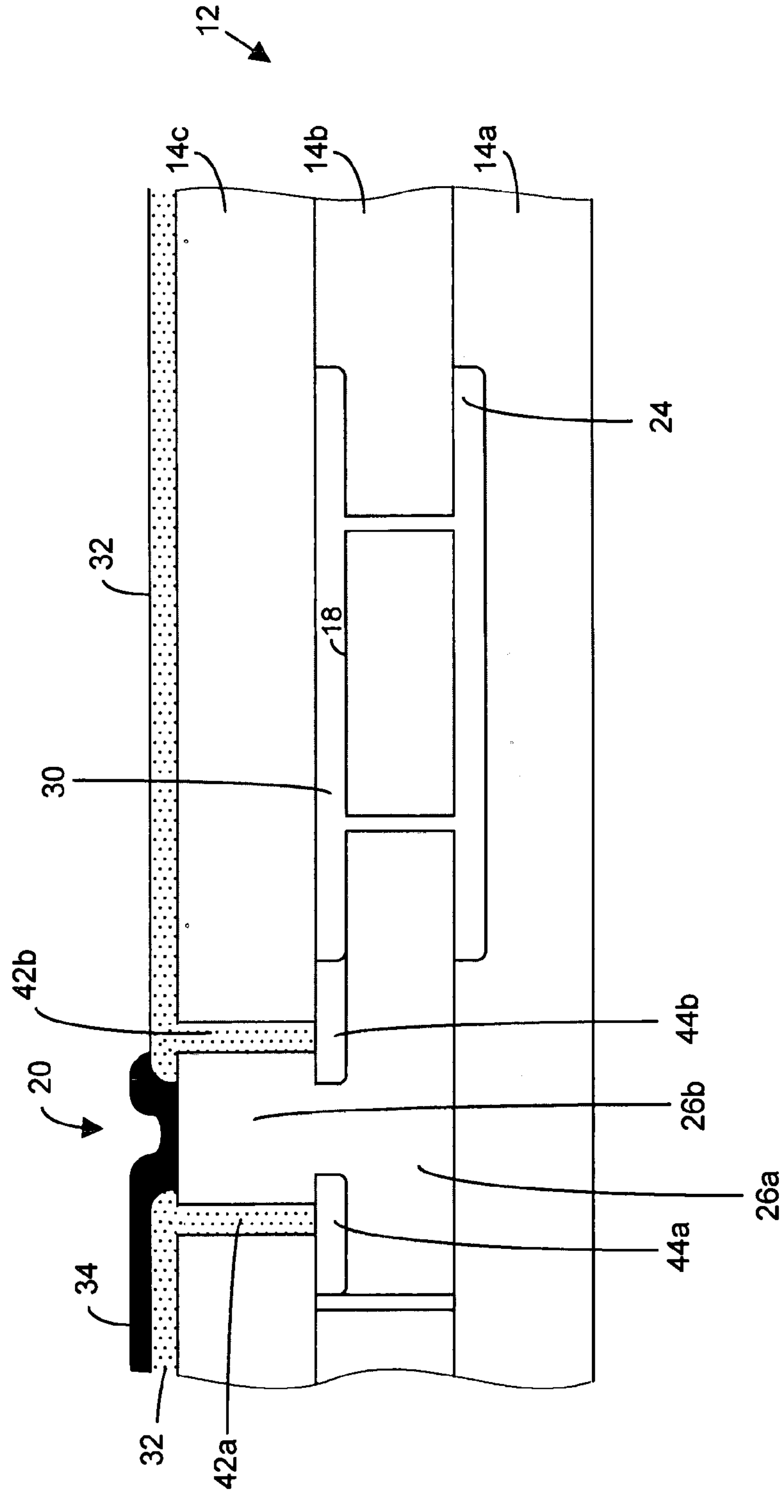


FIGURE 23

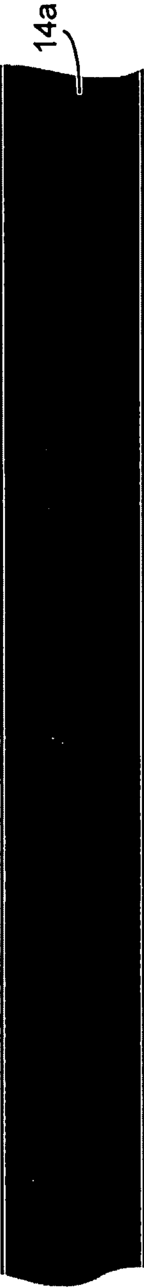


FIGURE 24A

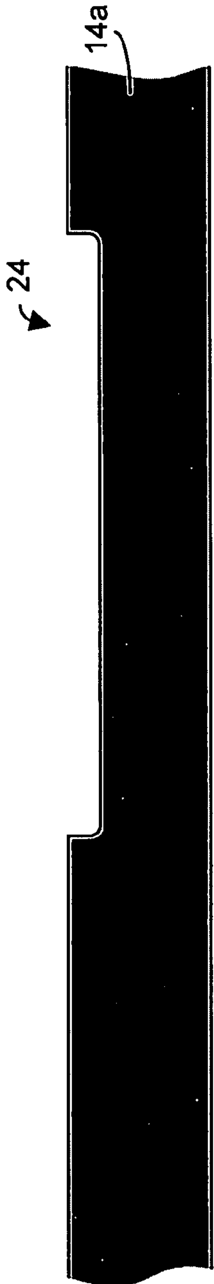


FIGURE 24B

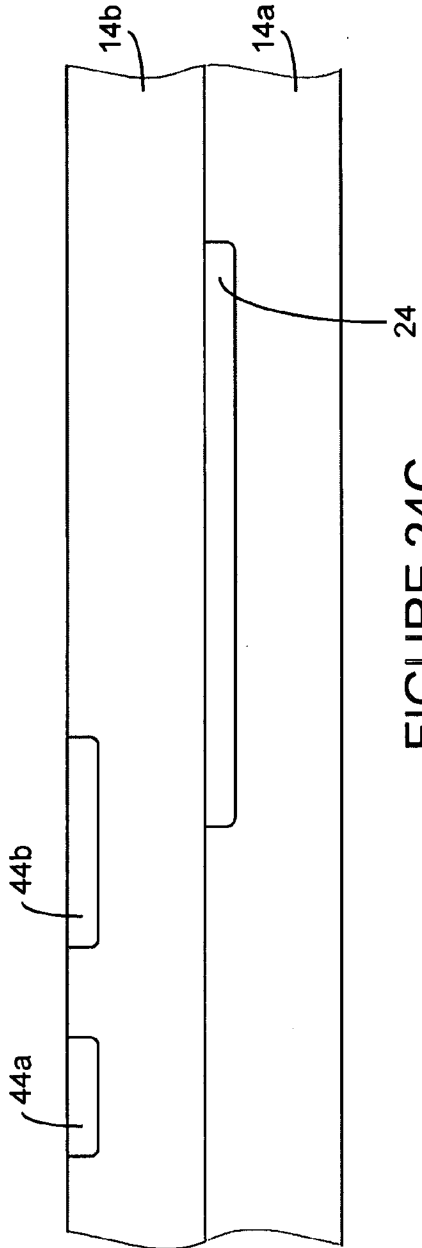


FIGURE 24C

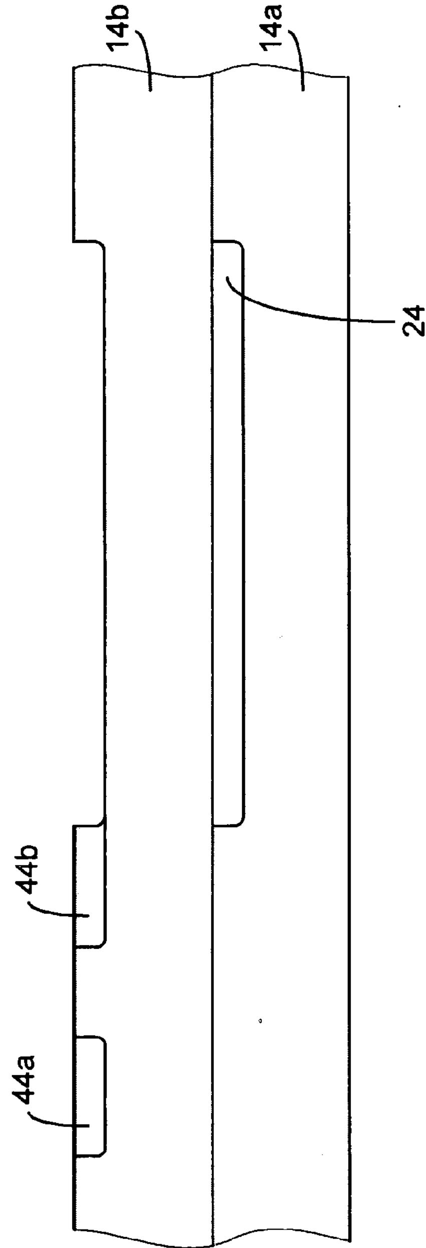


FIGURE 24D

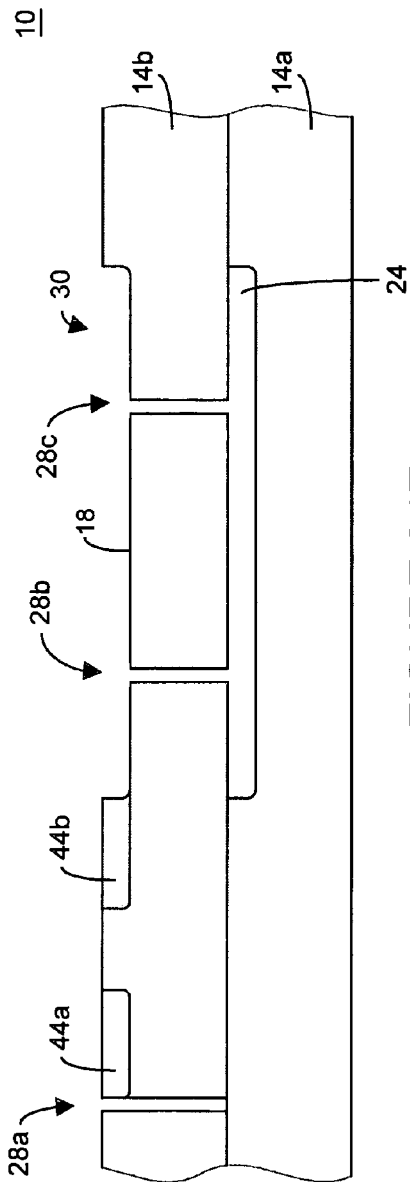


FIGURE 24E

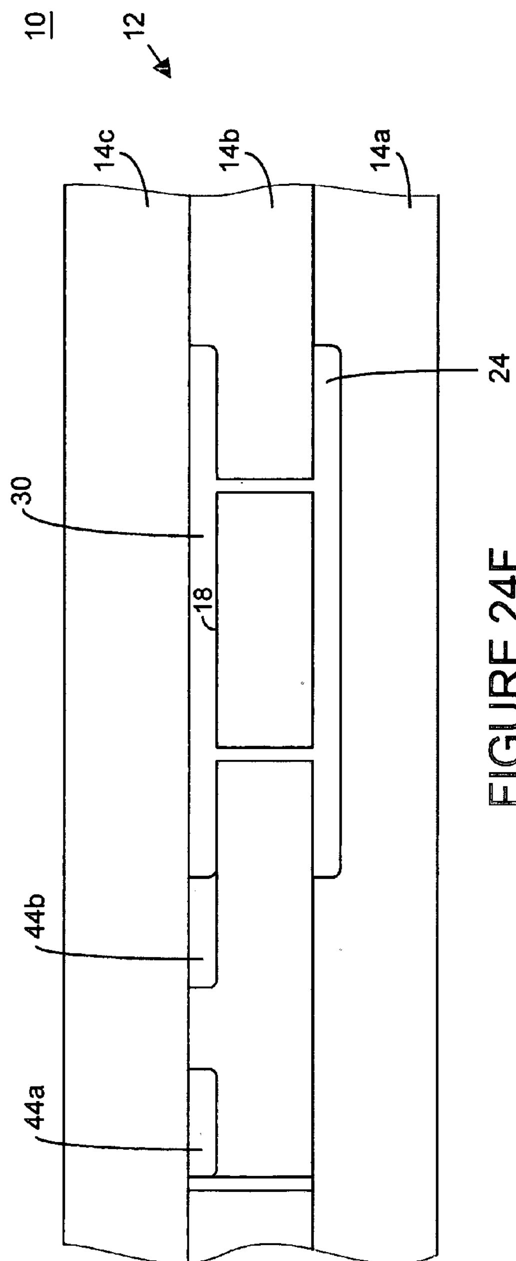
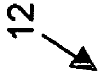


FIGURE 24F



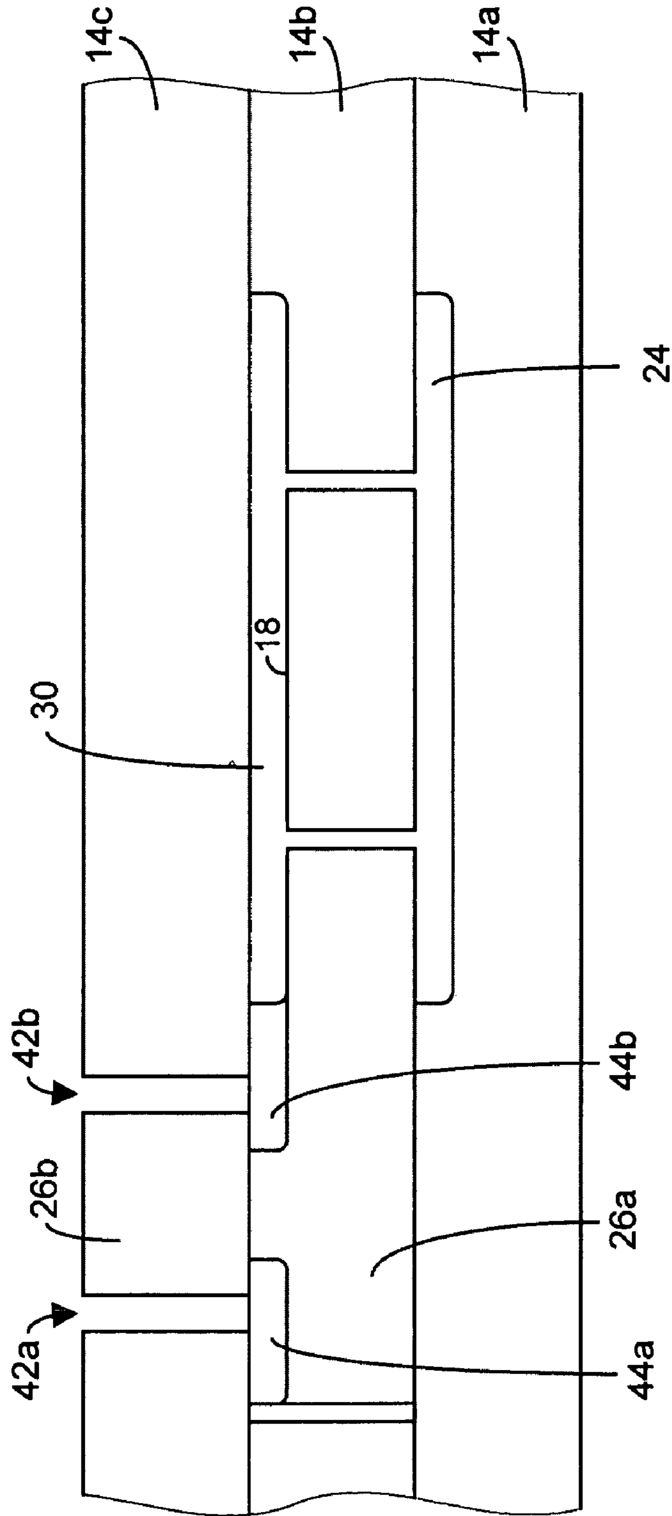


FIGURE 24G

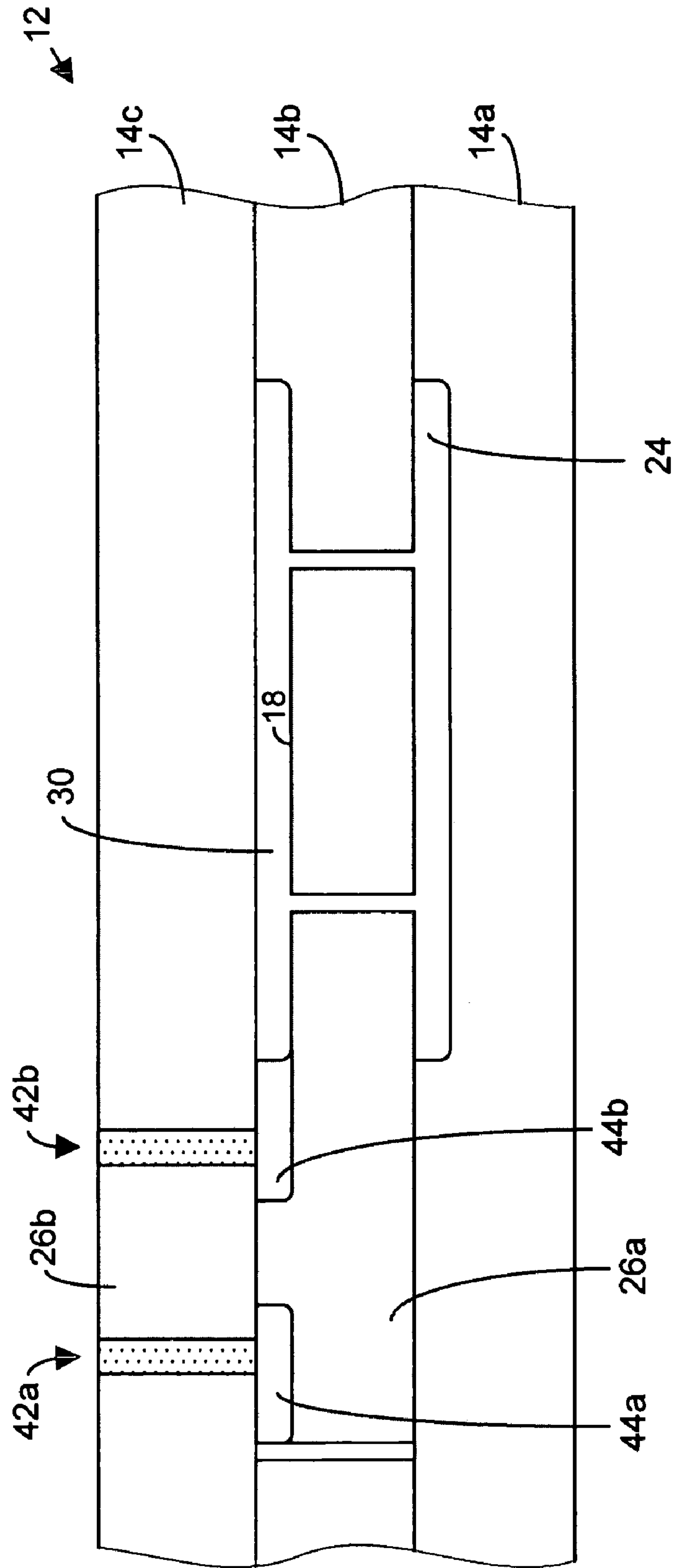


FIGURE 24H

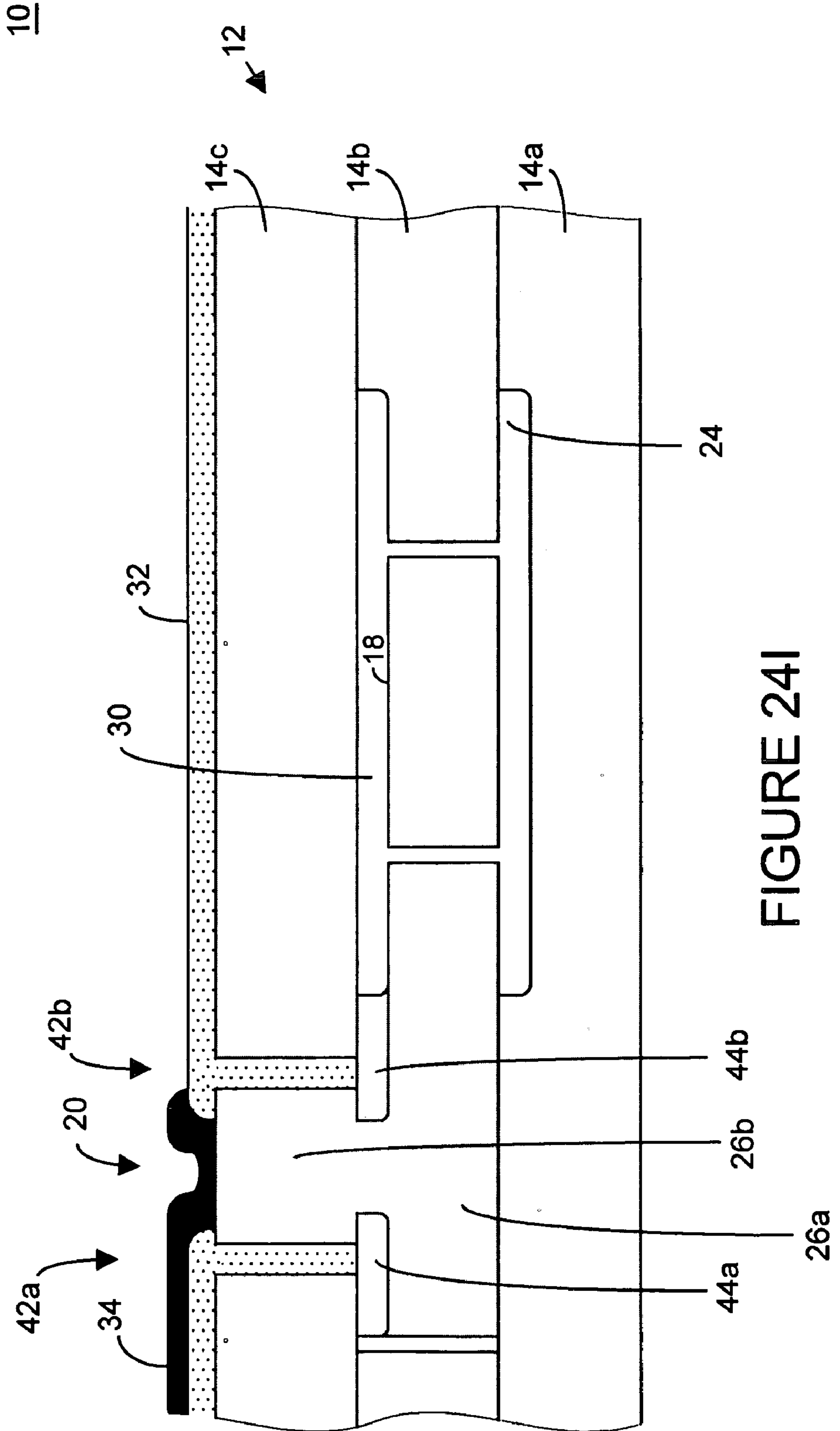


FIGURE 24I

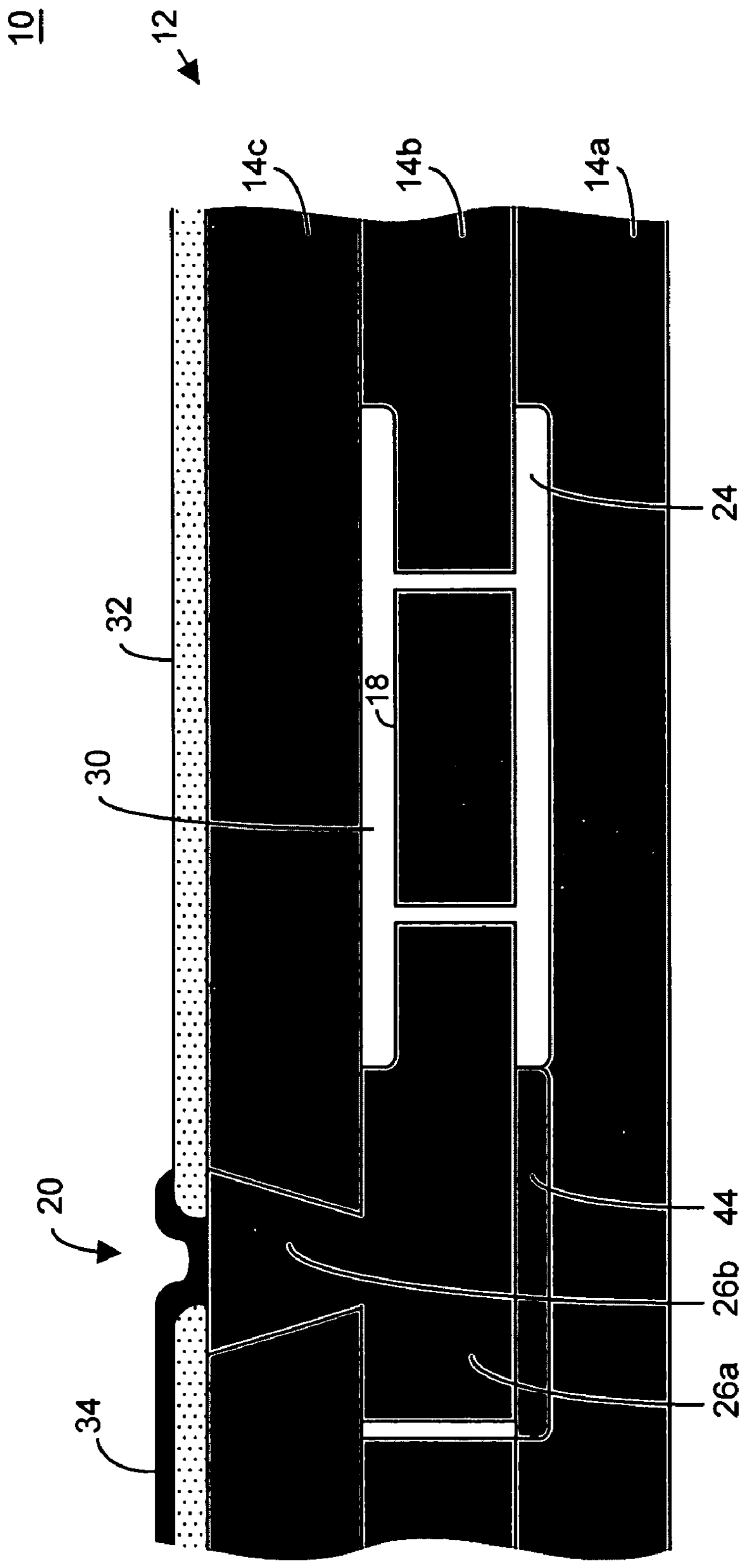


FIGURE 25

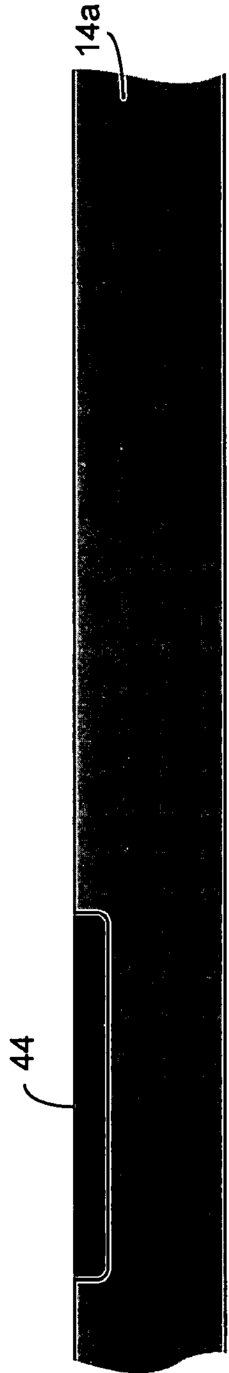


FIGURE 26A

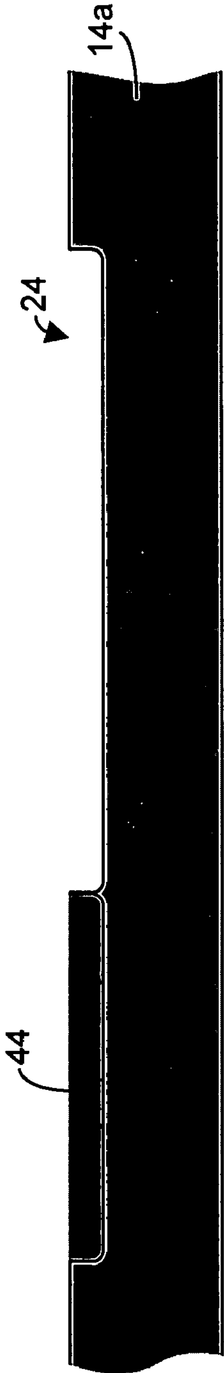


FIGURE 26B

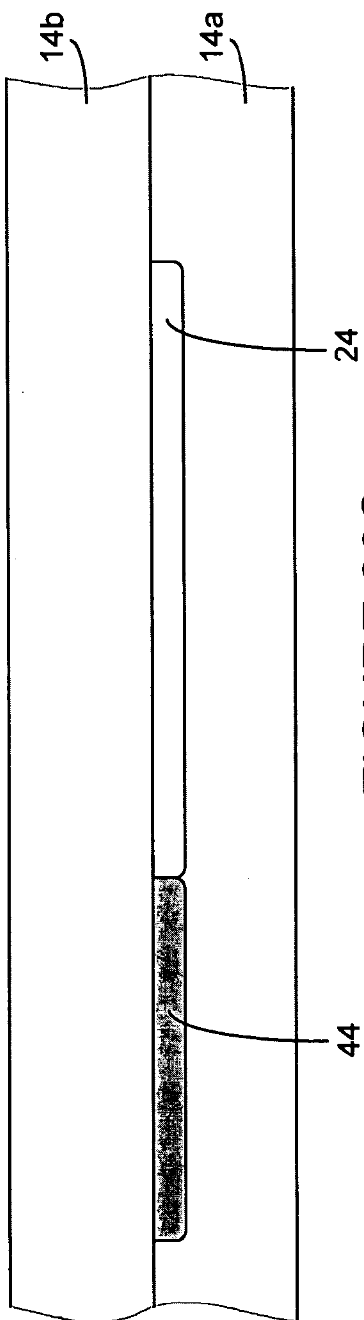


FIGURE 26C

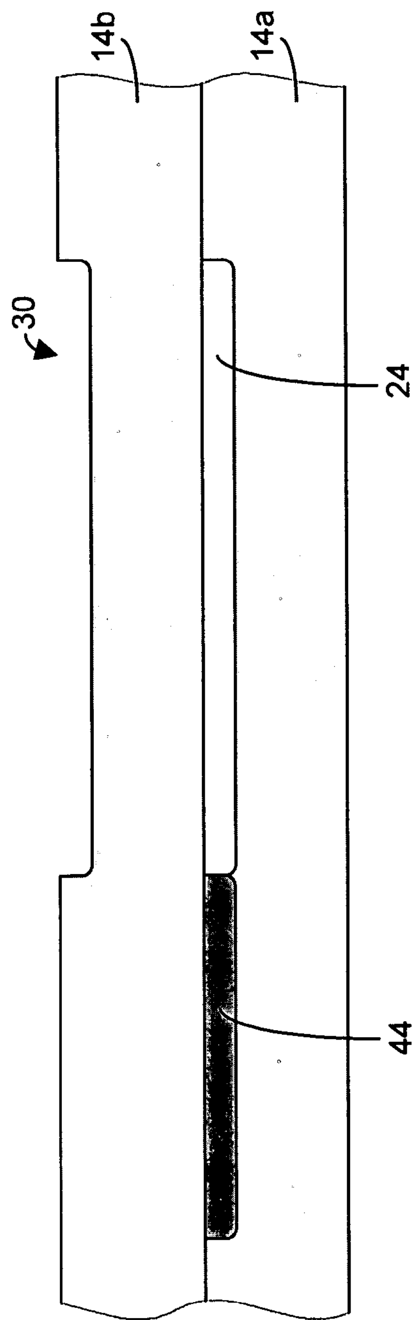


FIGURE 26D

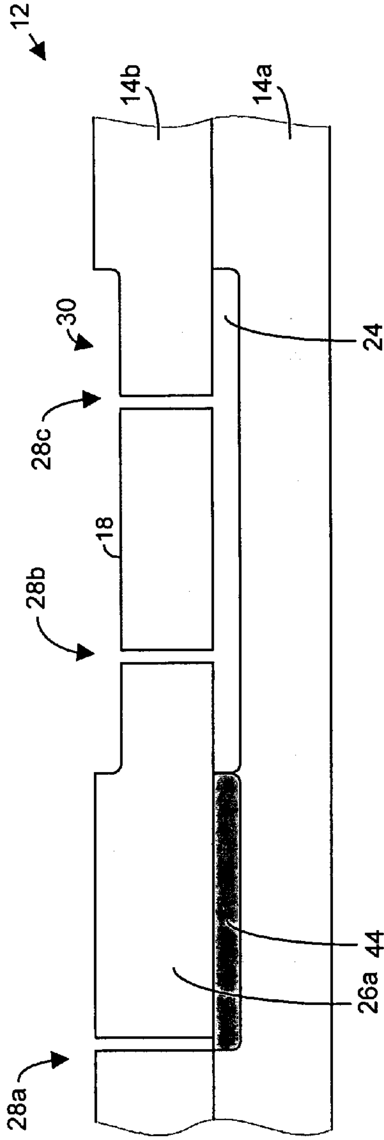


FIGURE 26E

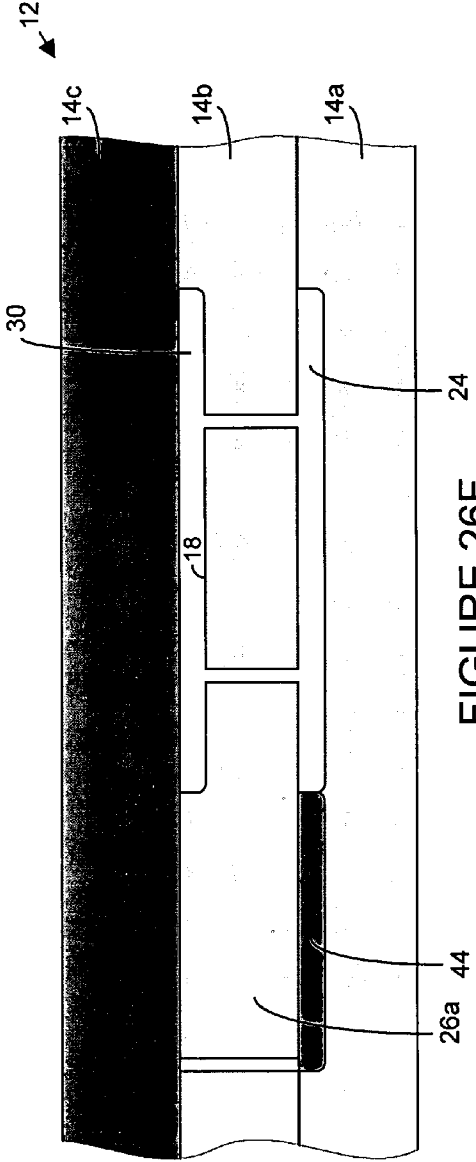


FIGURE 26F

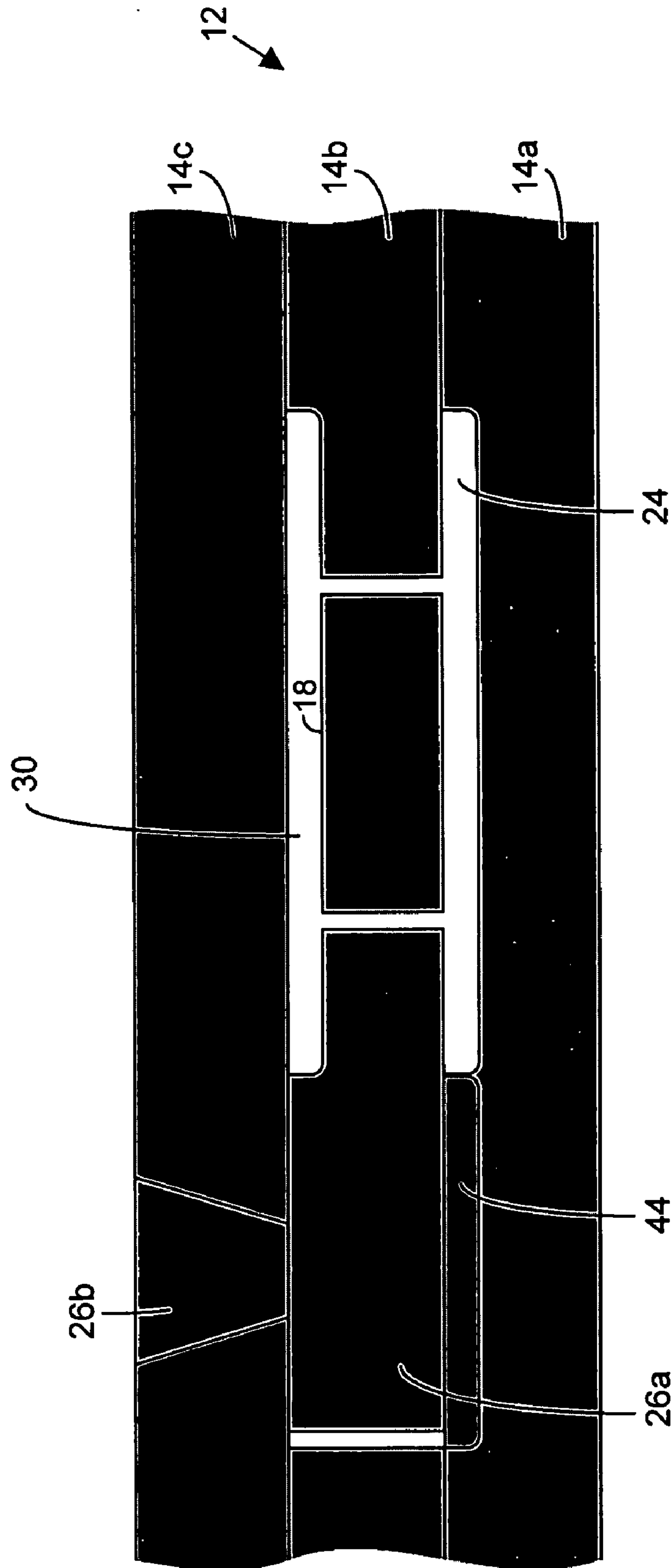


FIGURE 26G

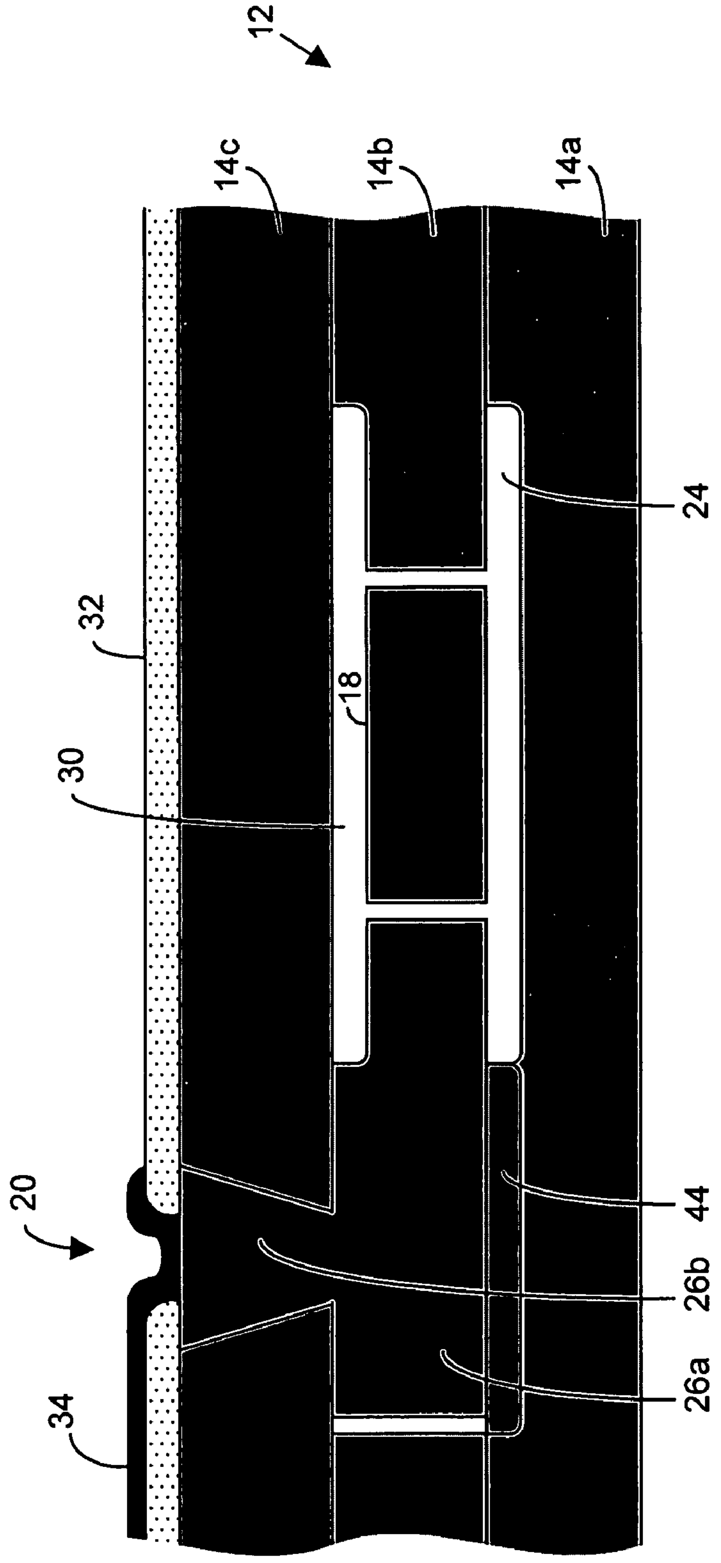


FIGURE 26H

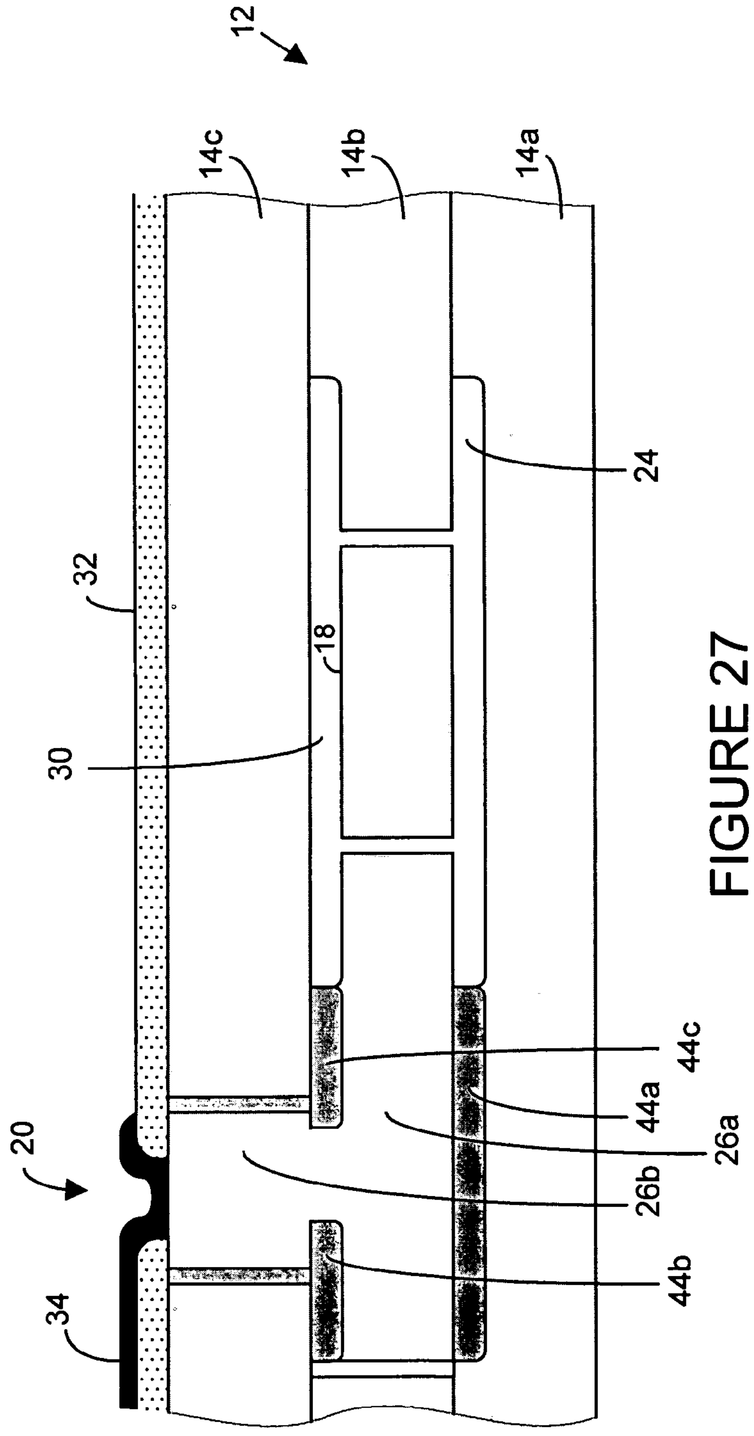


FIGURE 27

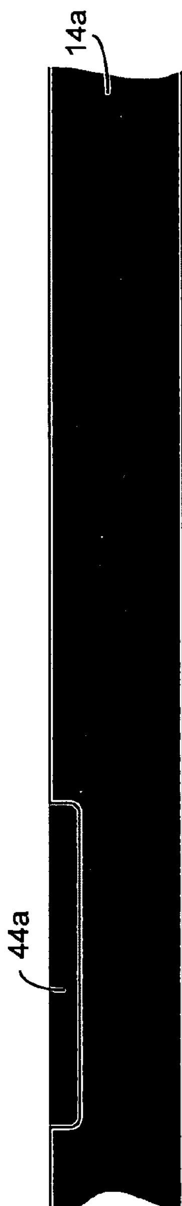


FIGURE 28A

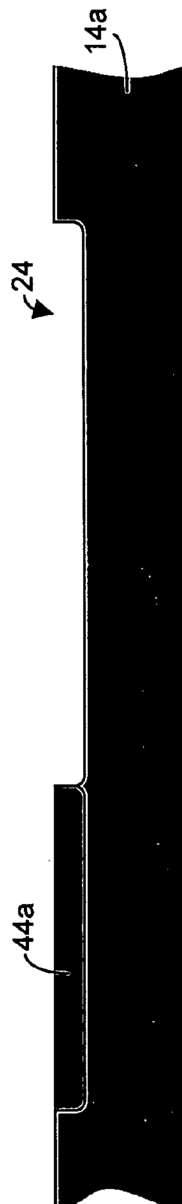


FIGURE 28B

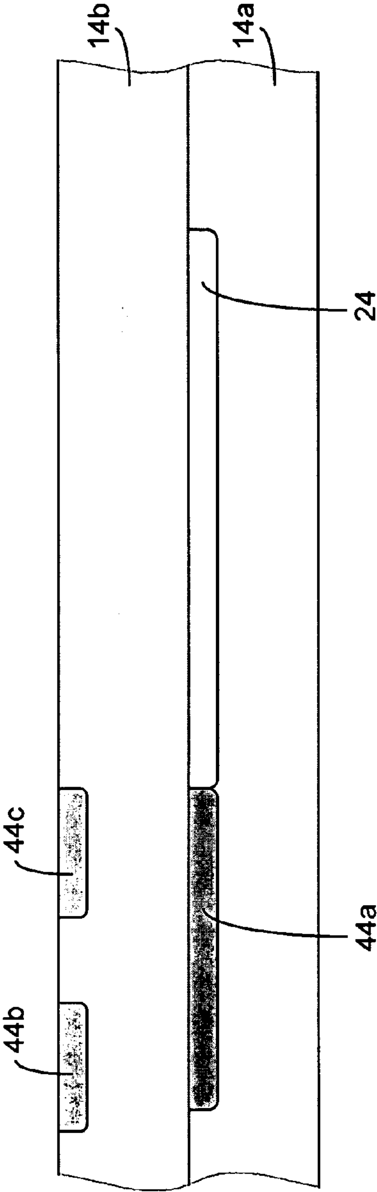


FIGURE 28C

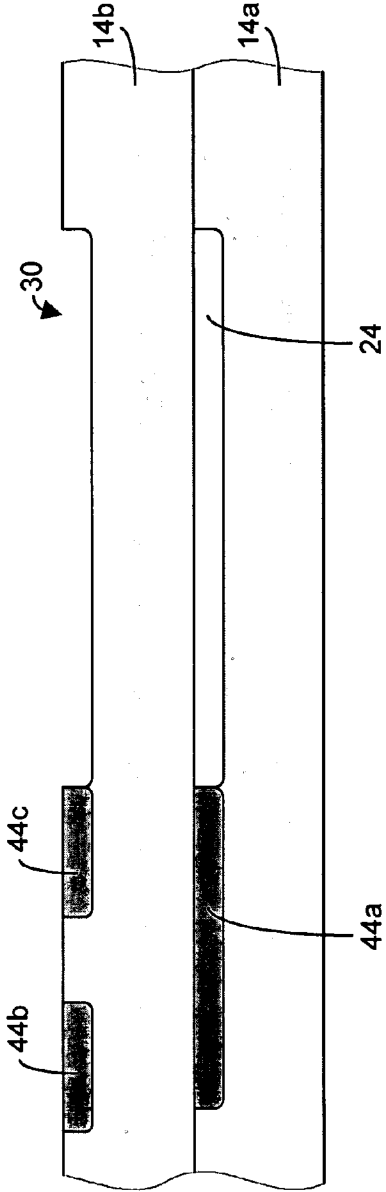


FIGURE 28D

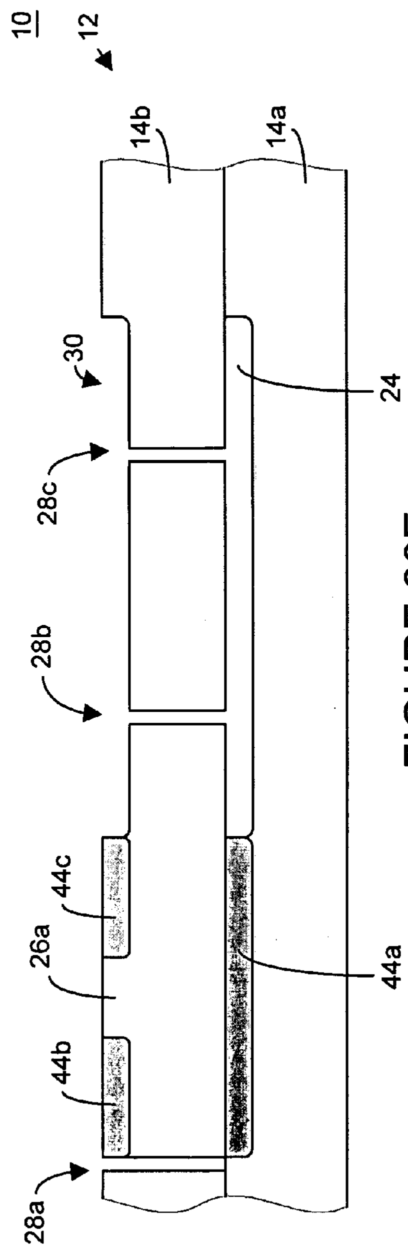


FIGURE 28E

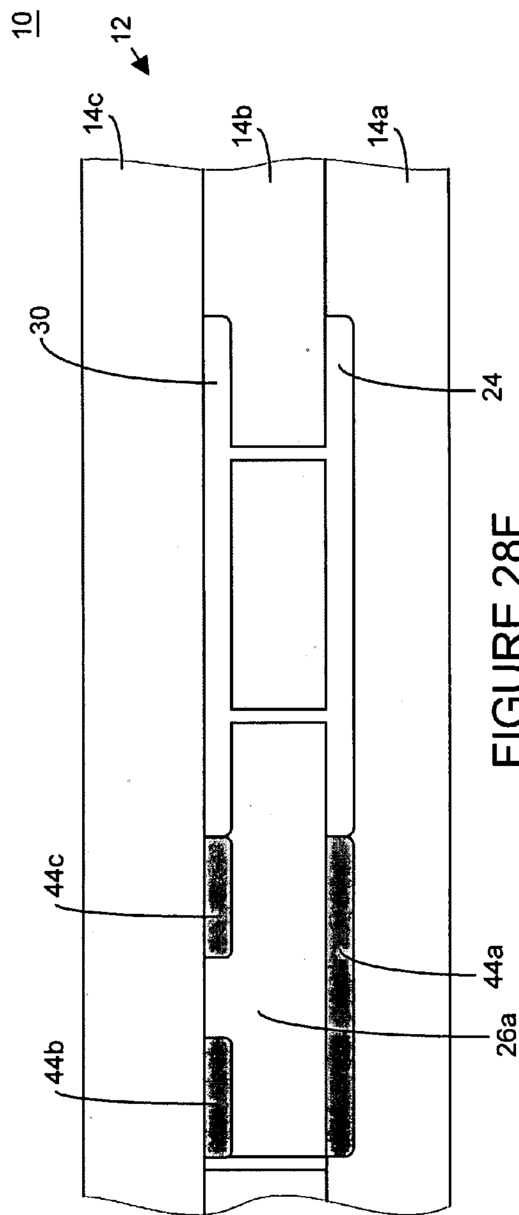


FIGURE 28F

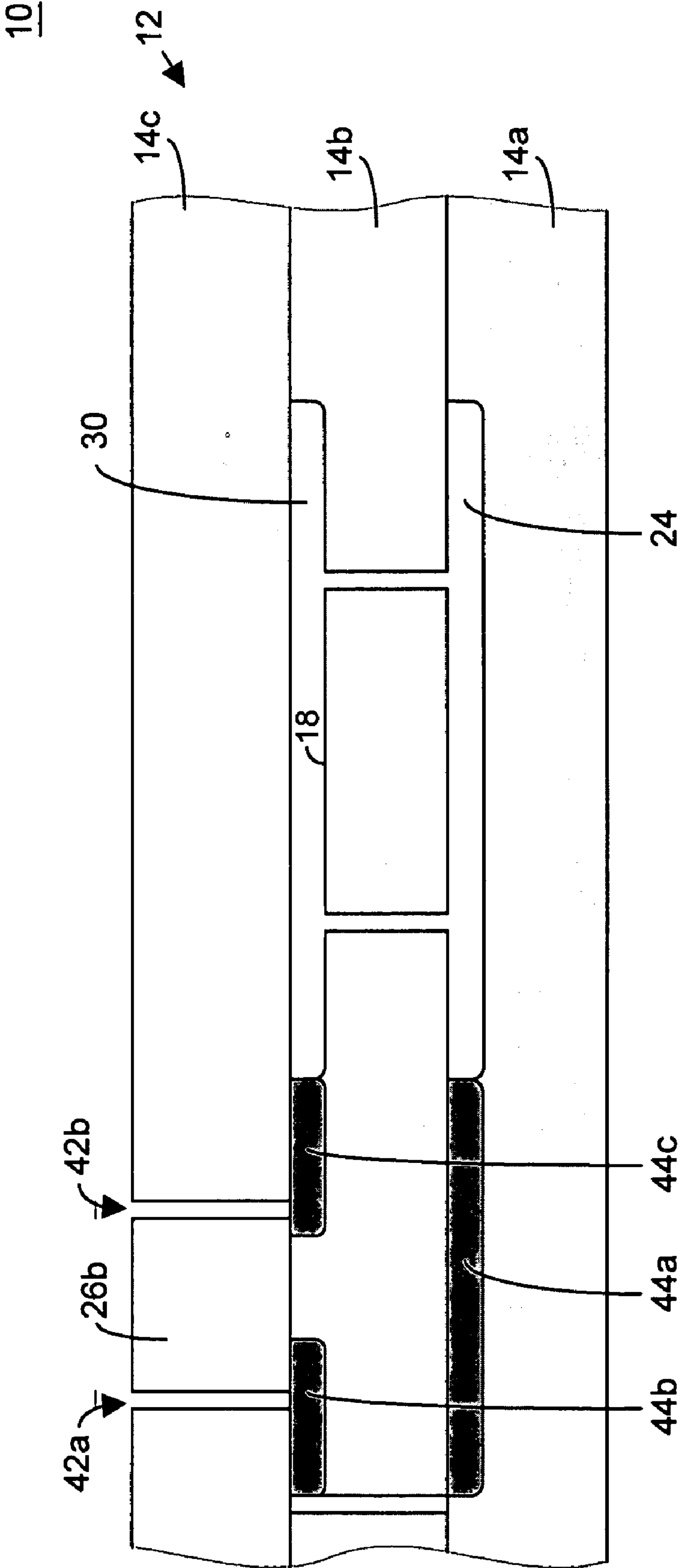


FIGURE 28G

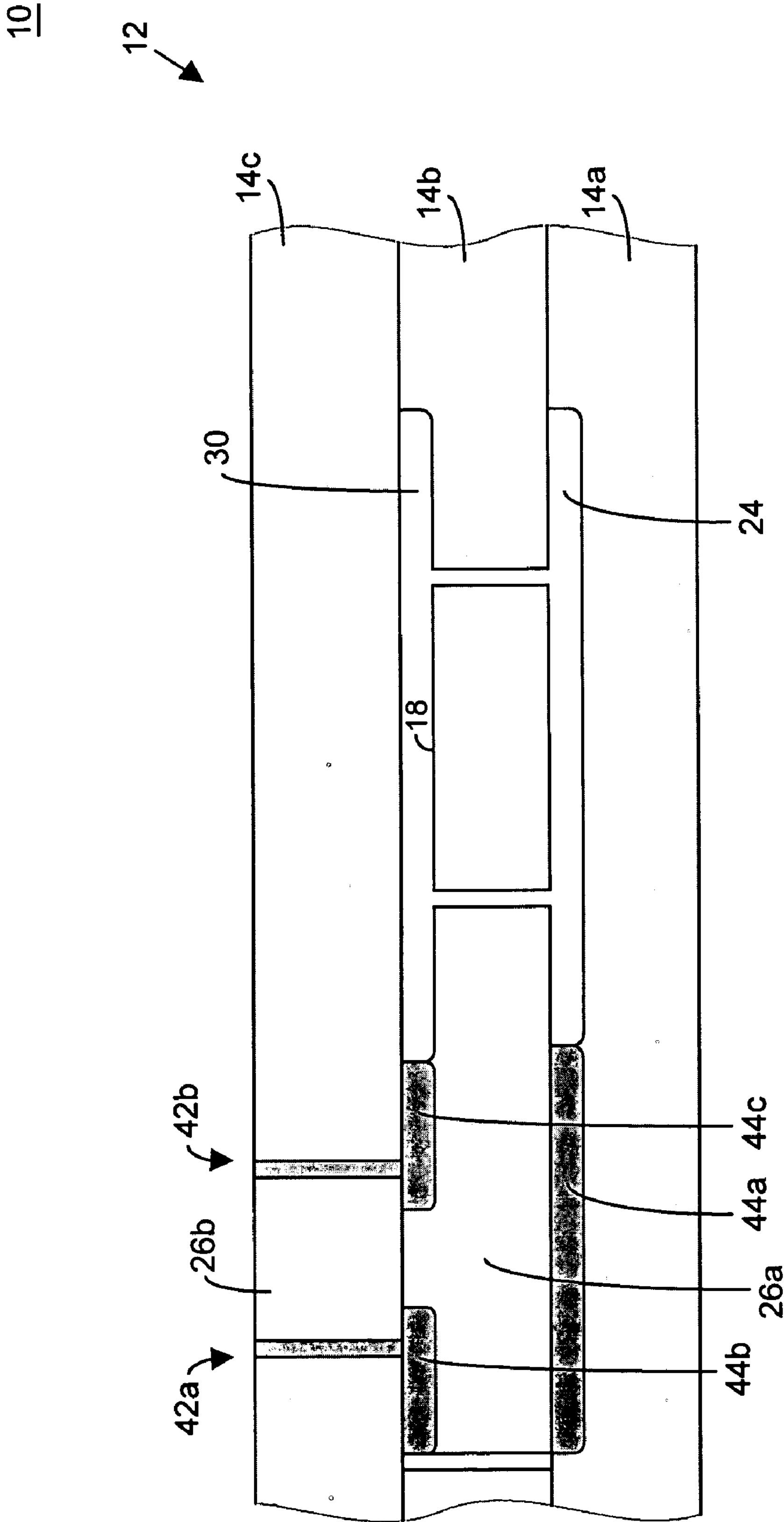


FIGURE 28H

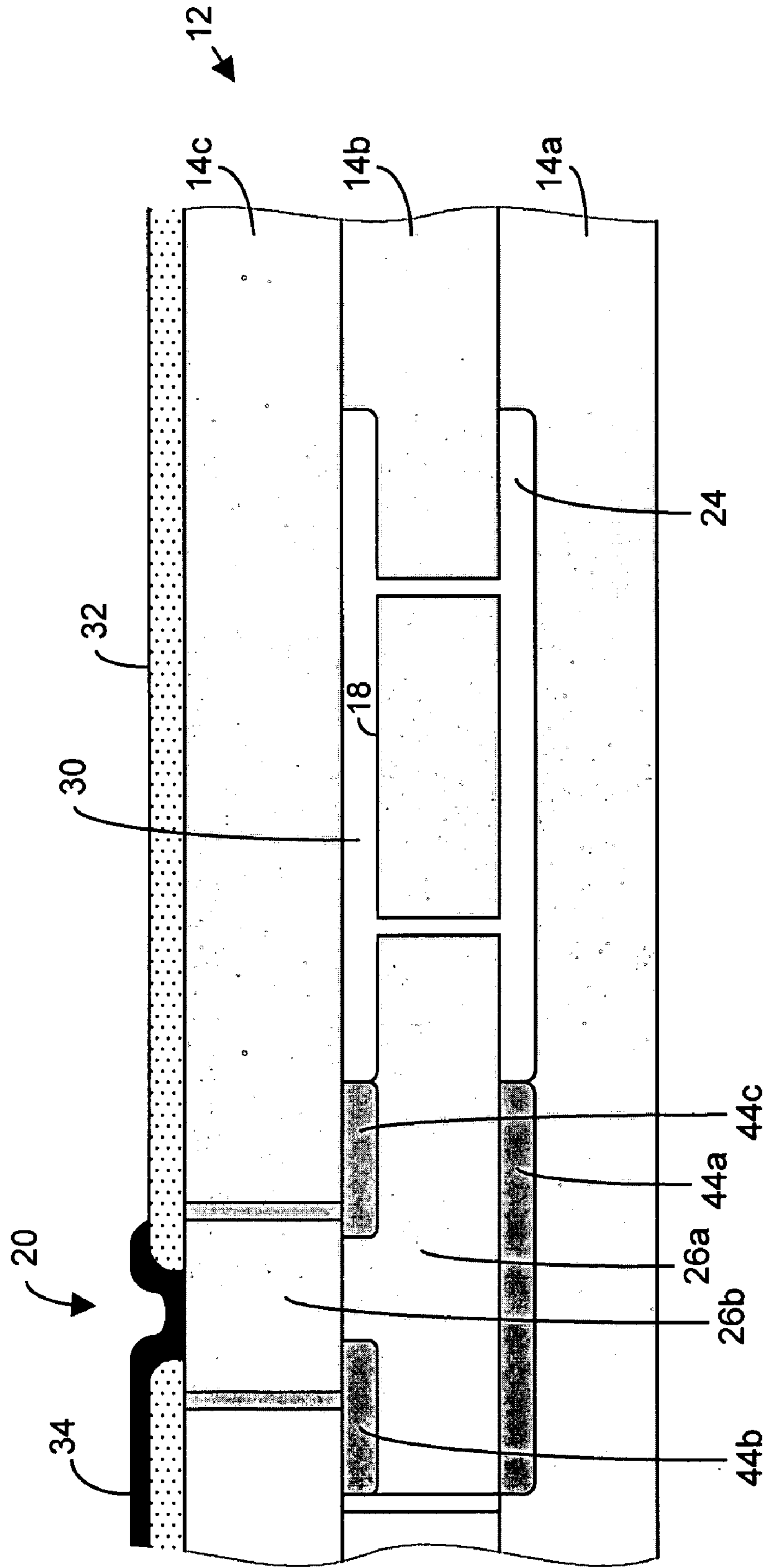


FIGURE 28I

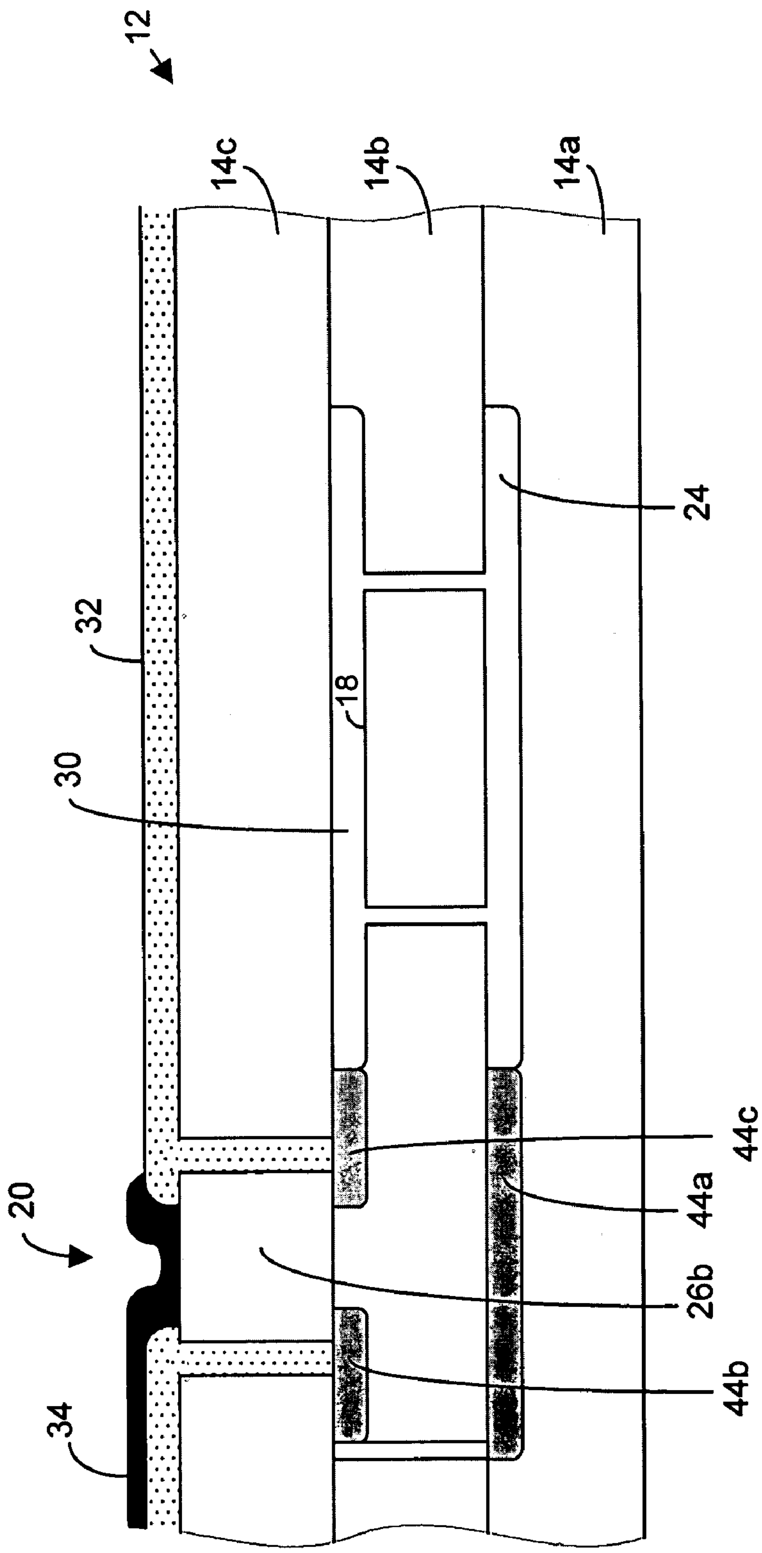


FIGURE 29

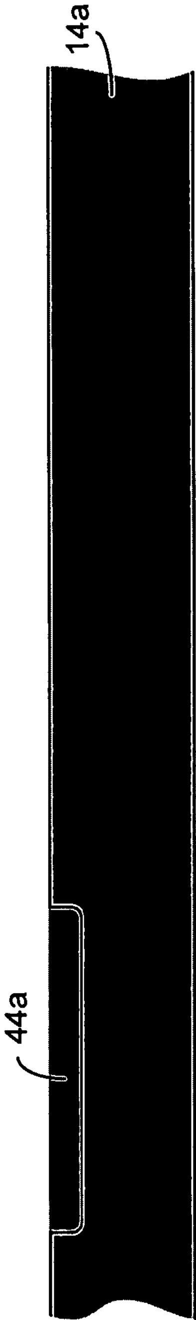


FIGURE 30A

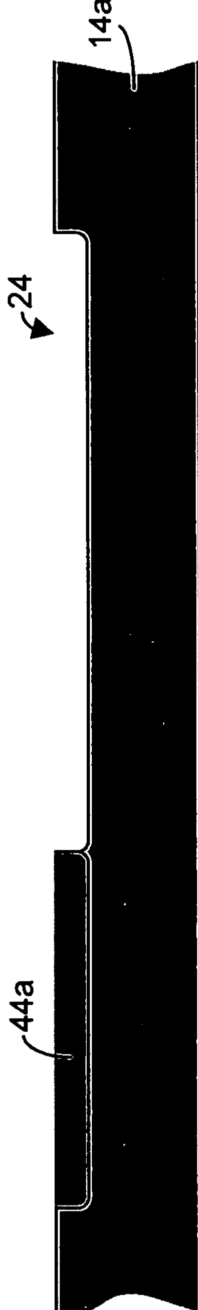


FIGURE 30B

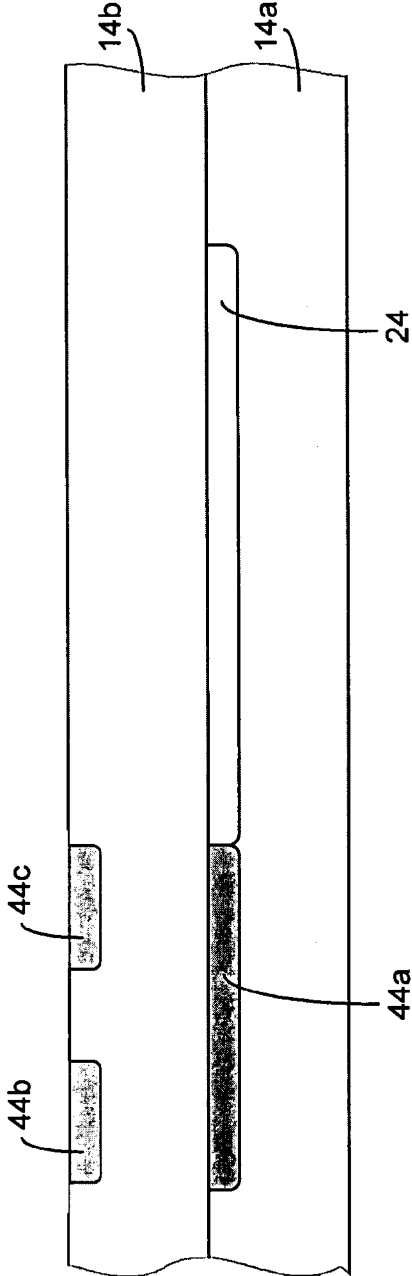


FIGURE 30C

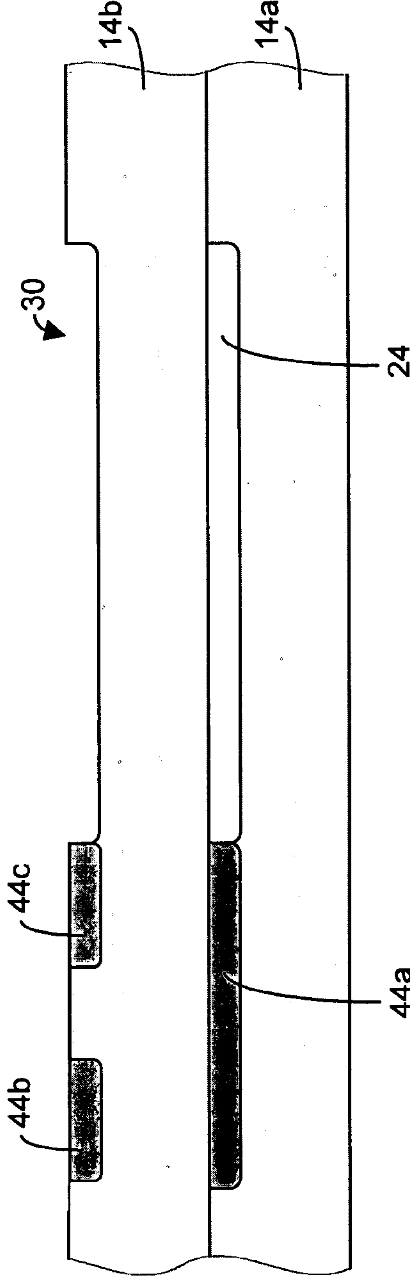


FIGURE 30D

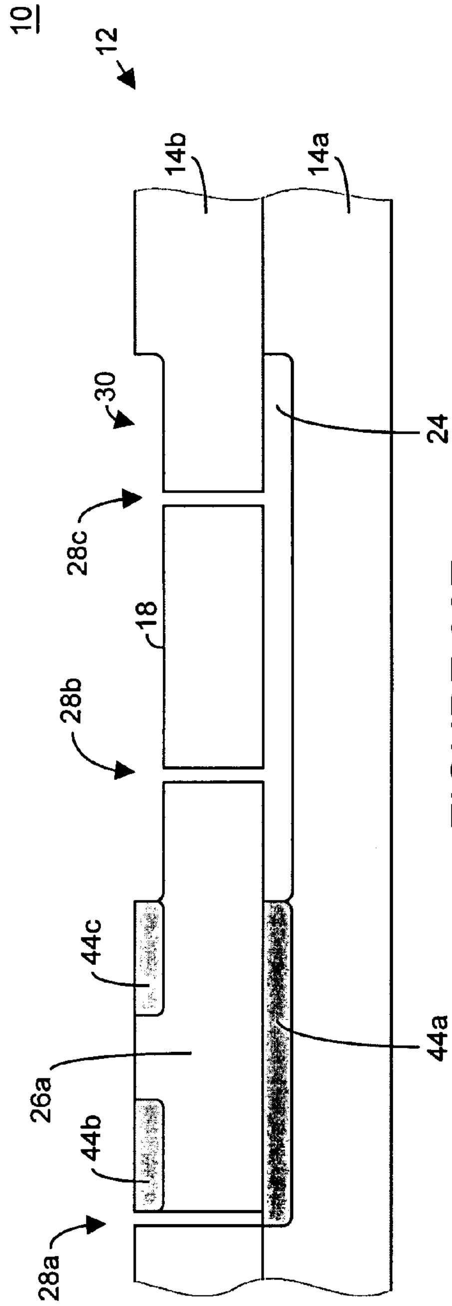


FIGURE 30E

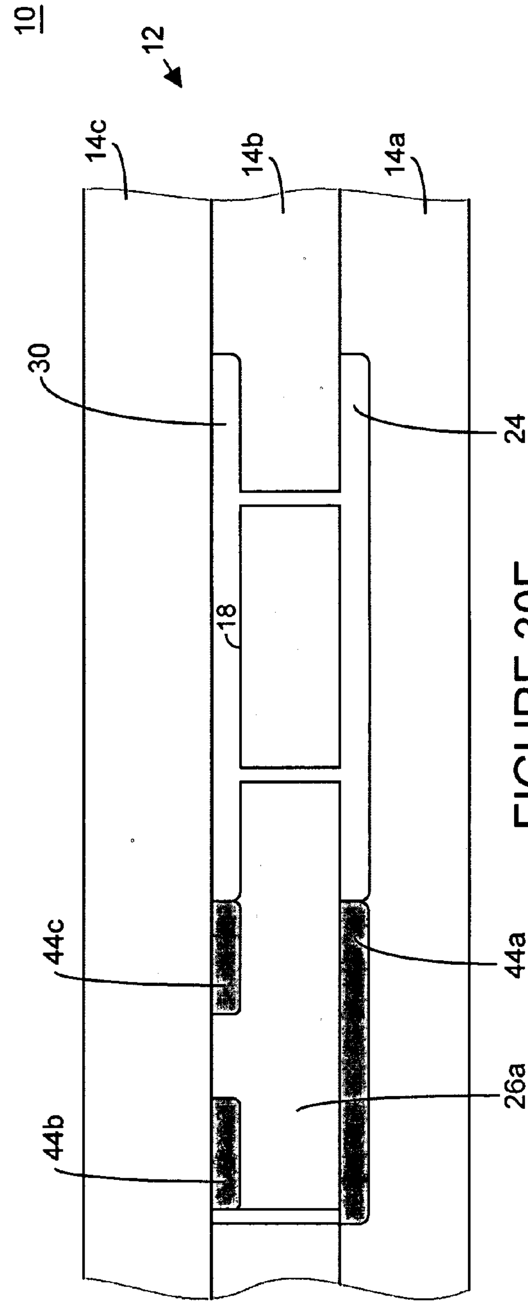


FIGURE 30F

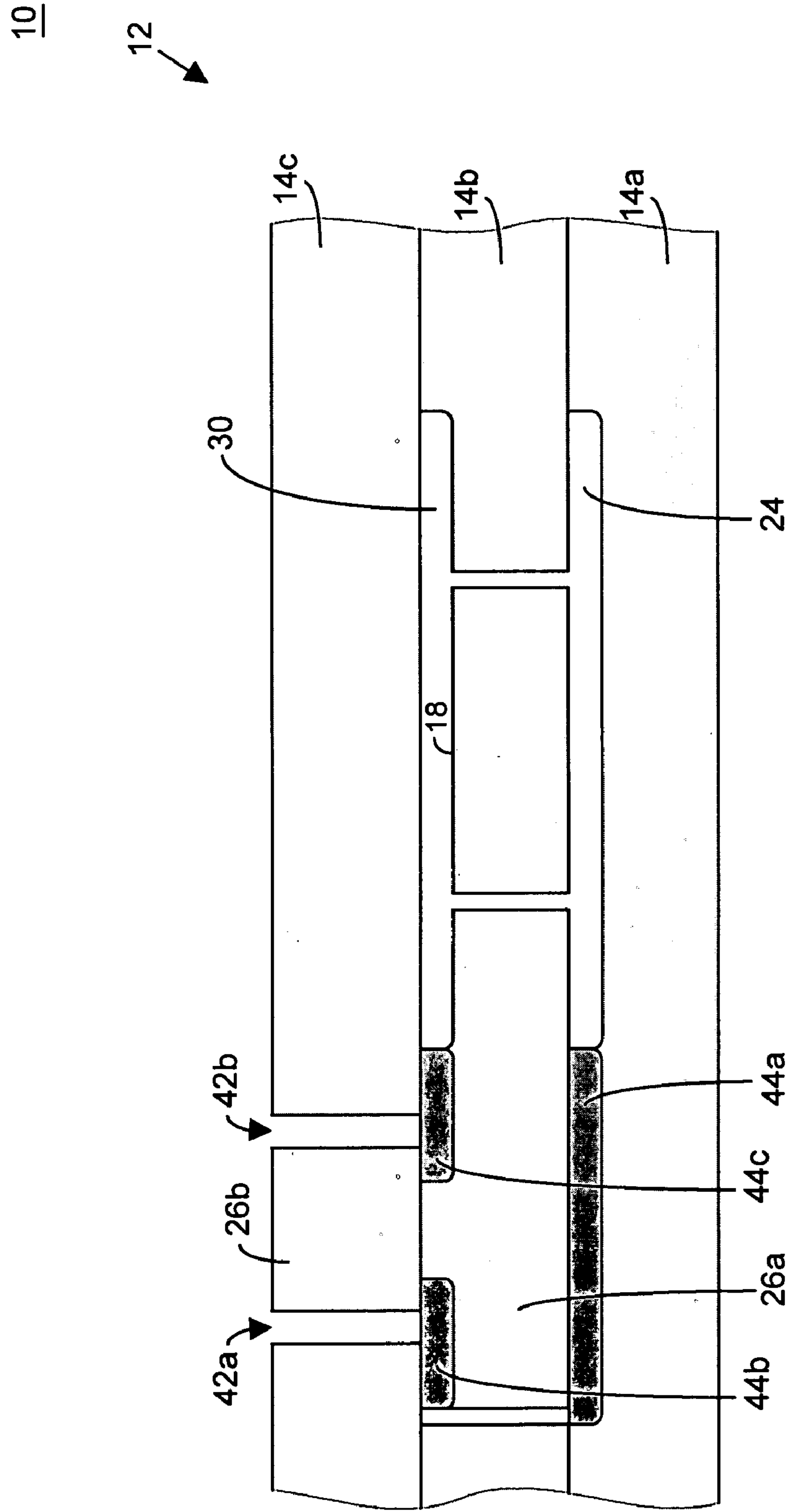


FIGURE 30G

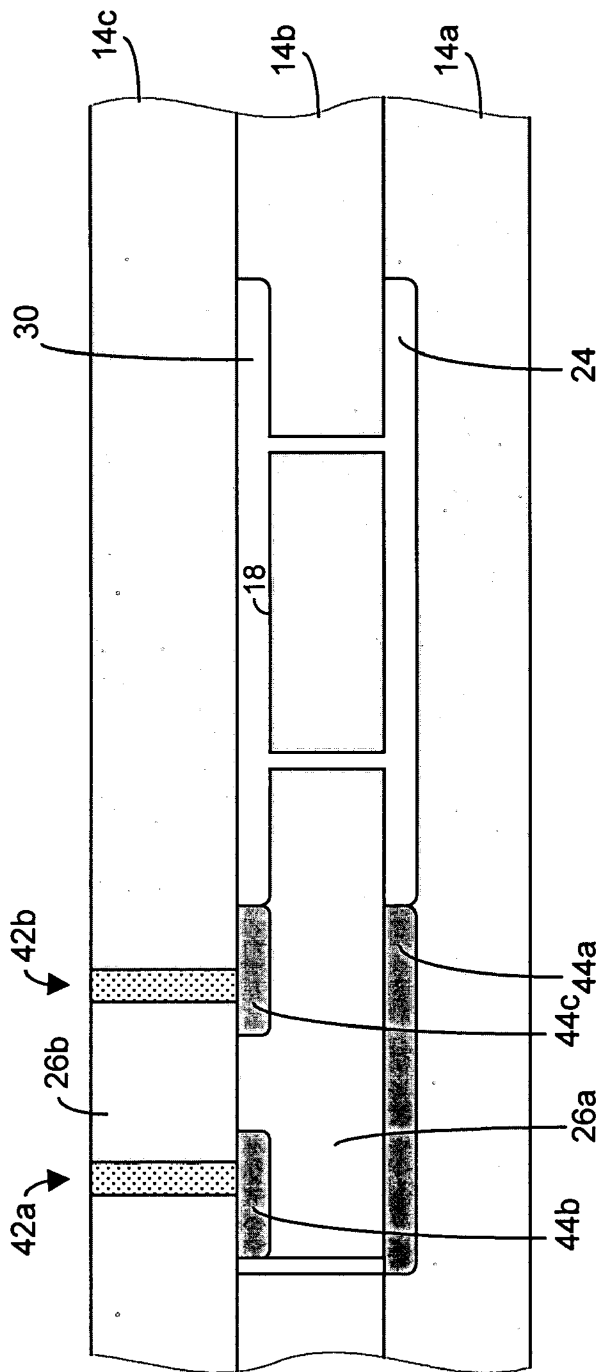


FIGURE 30H

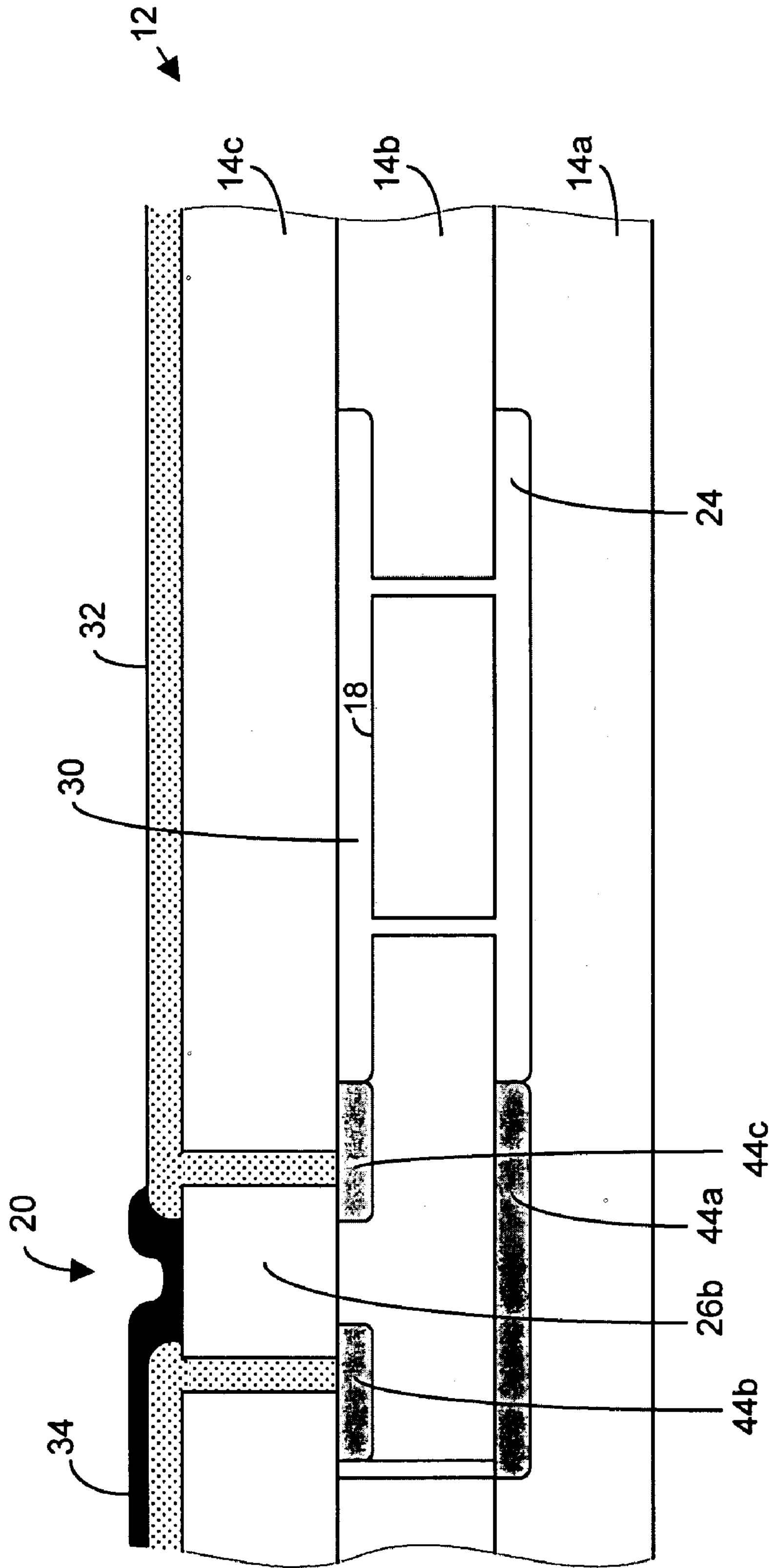


FIGURE 30I

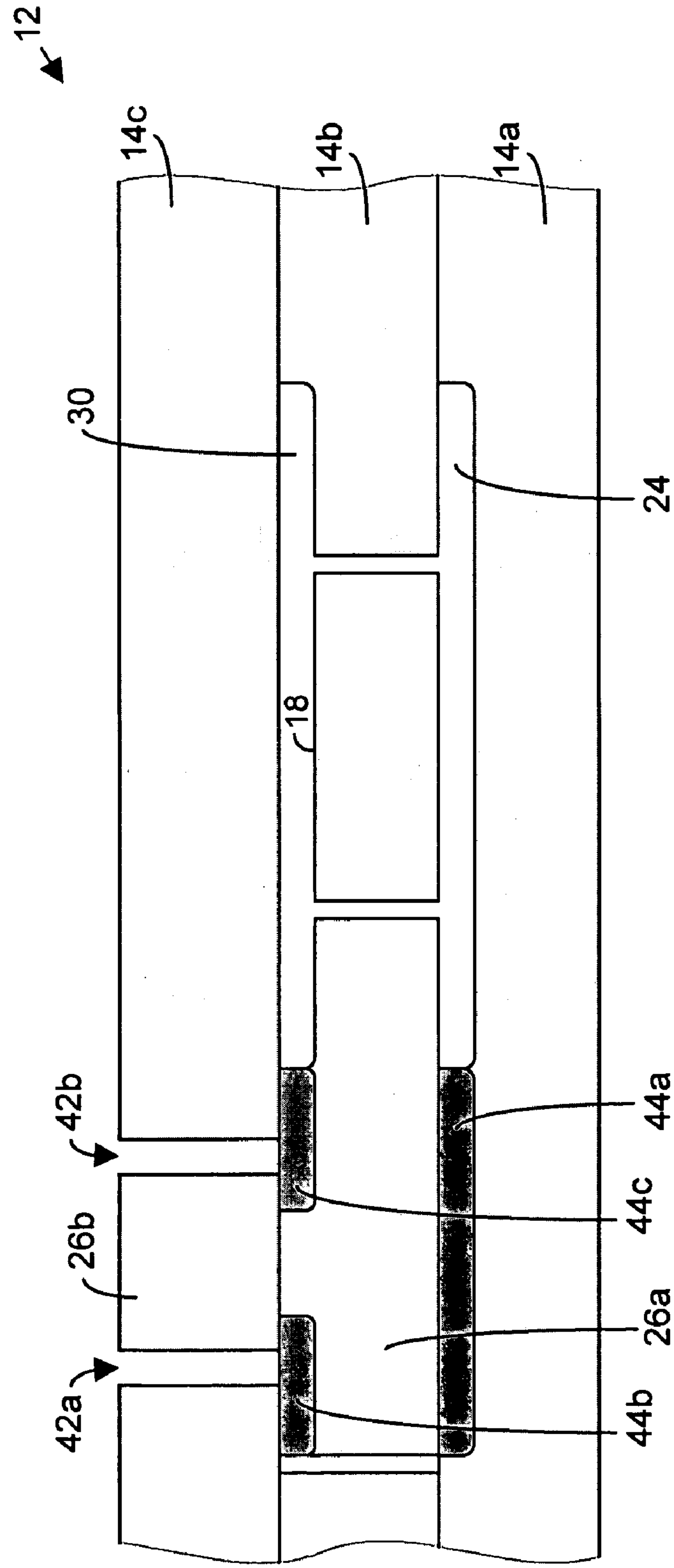


FIGURE 31A

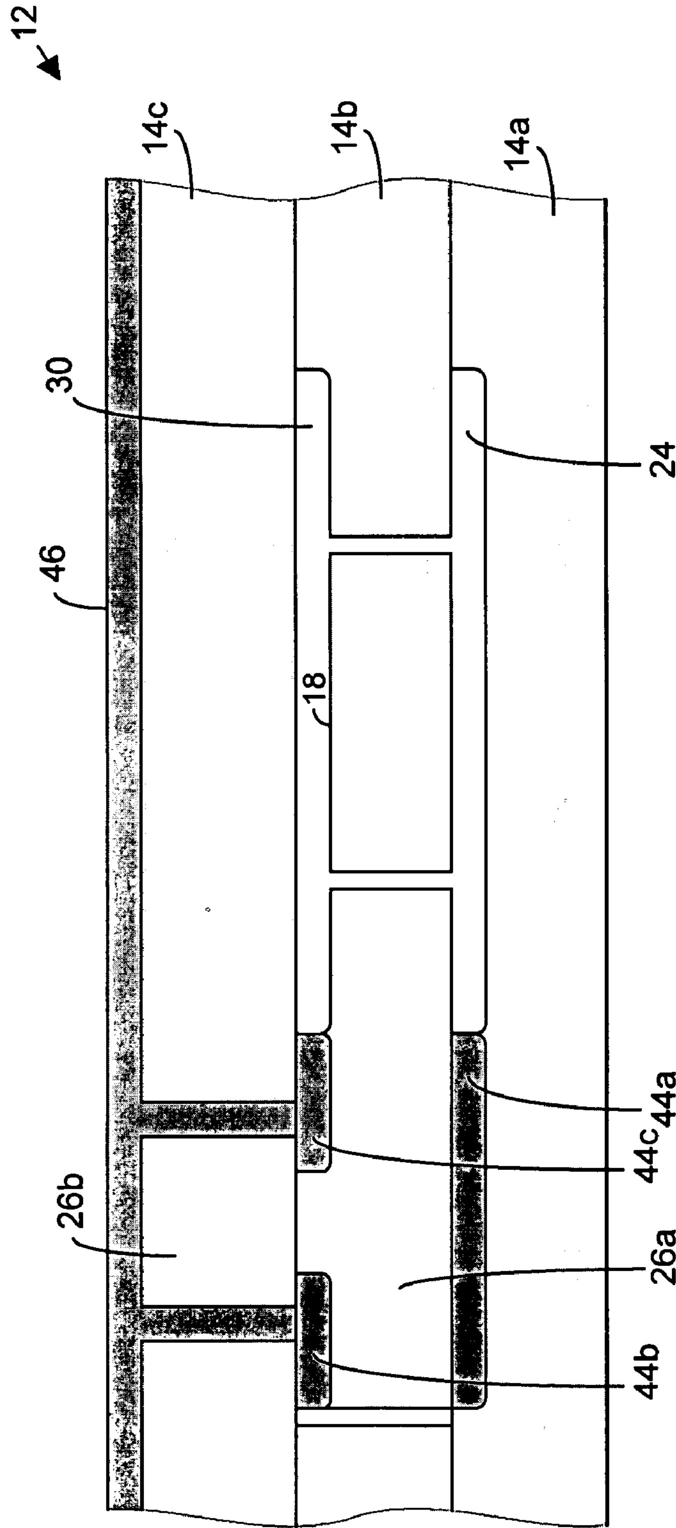


FIGURE 31B

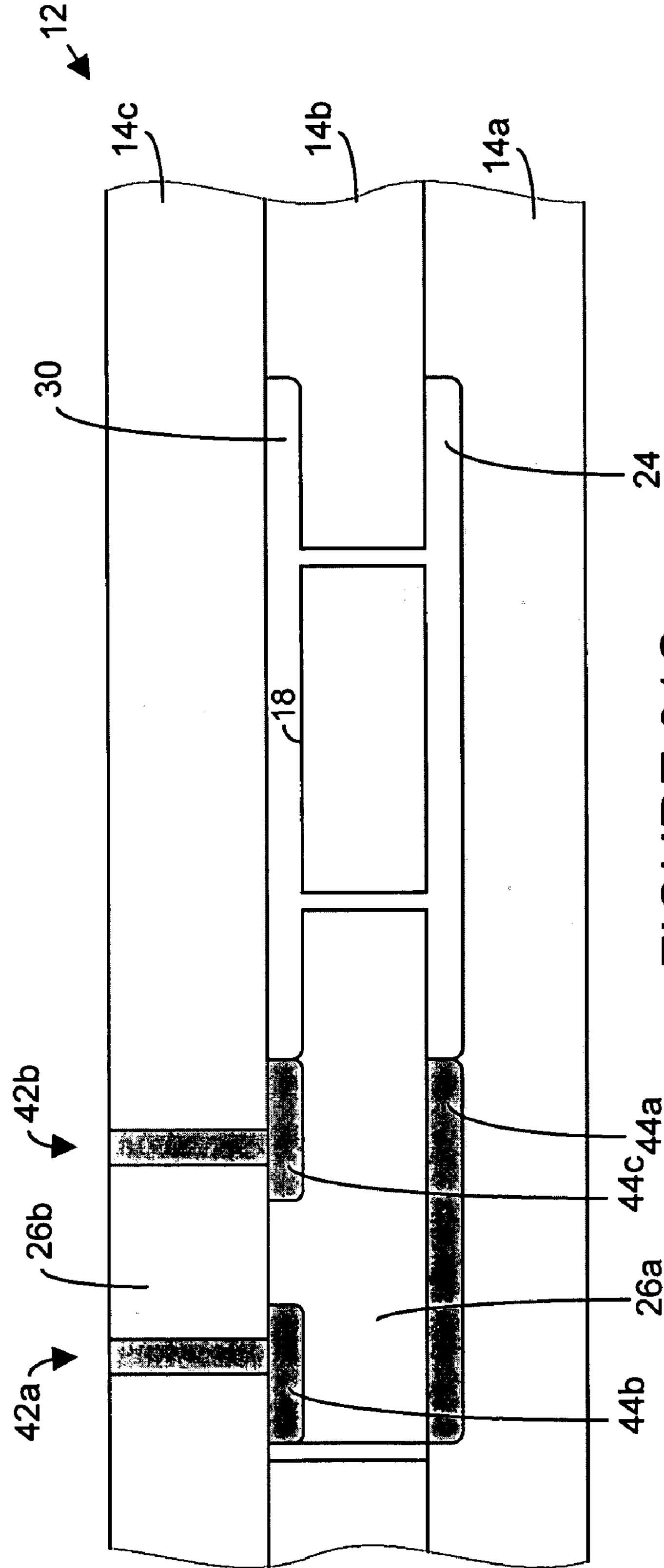


FIGURE 31C

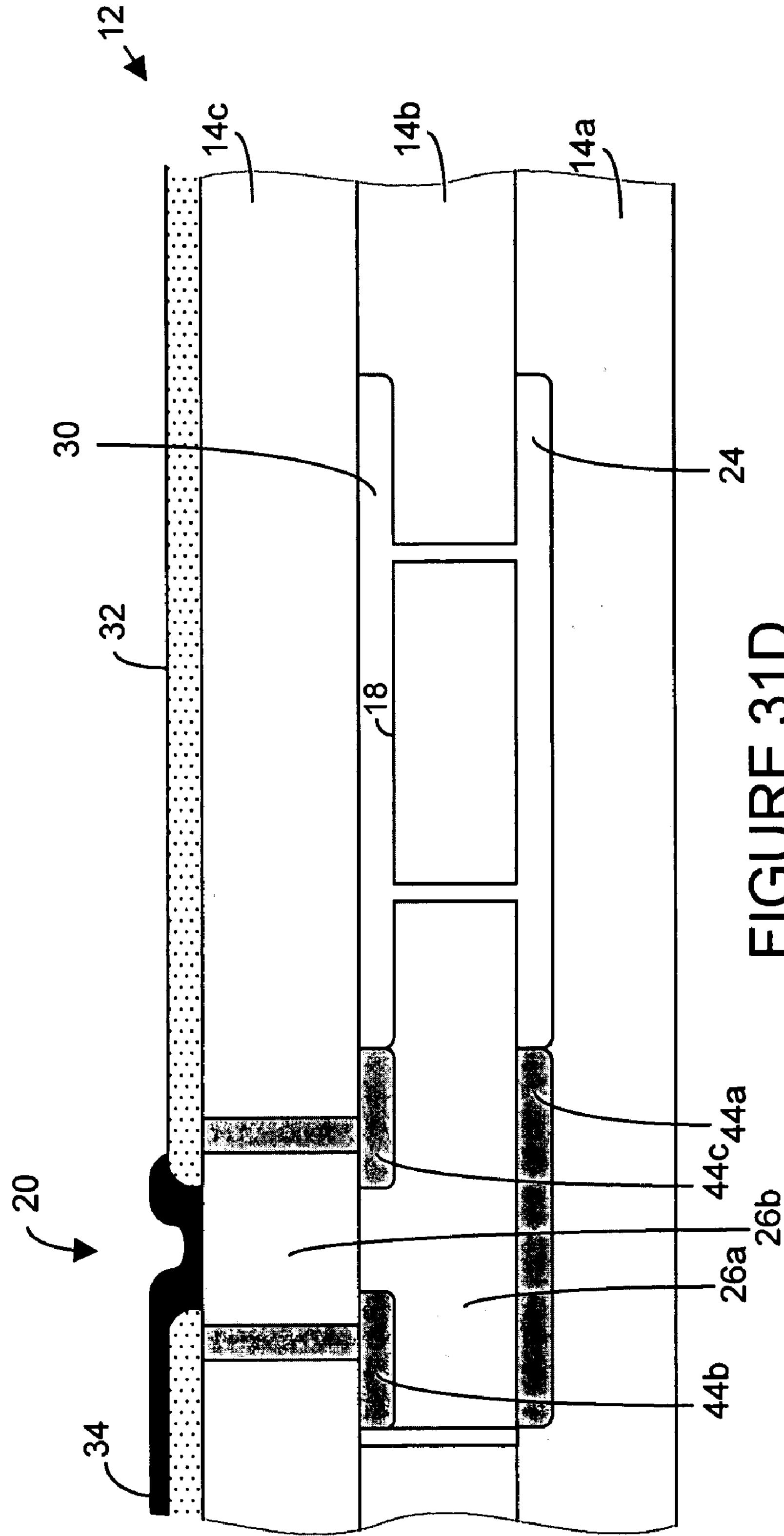


FIGURE 31D

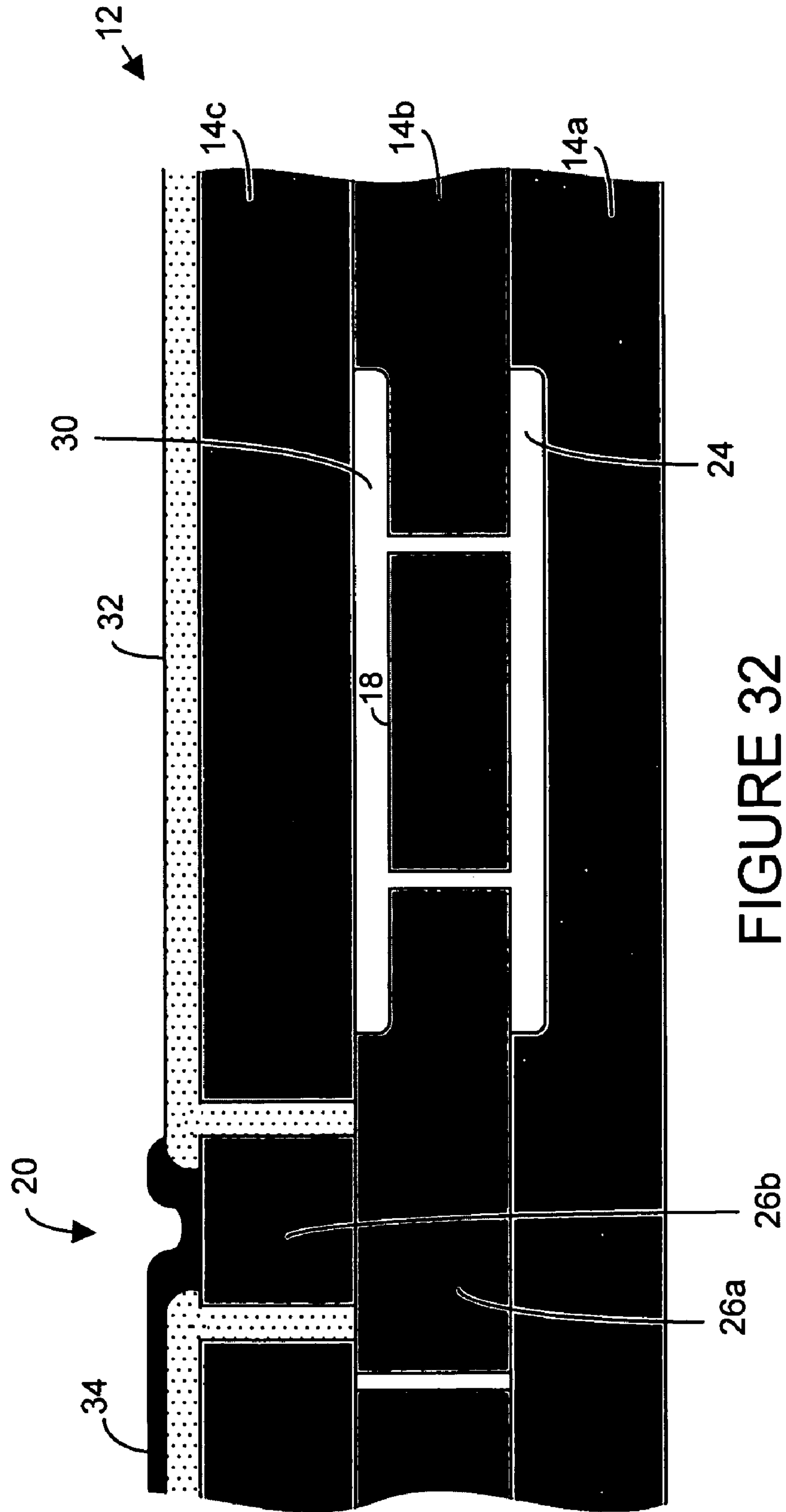


FIGURE 32

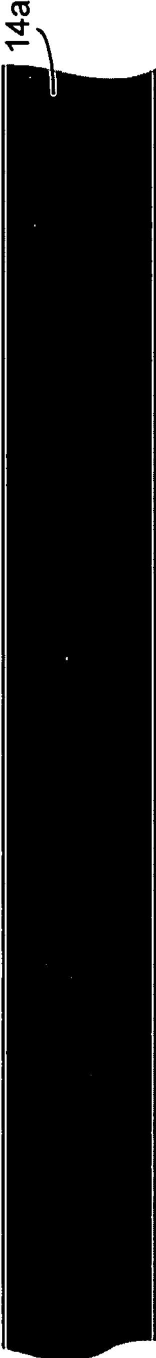


FIGURE 33A

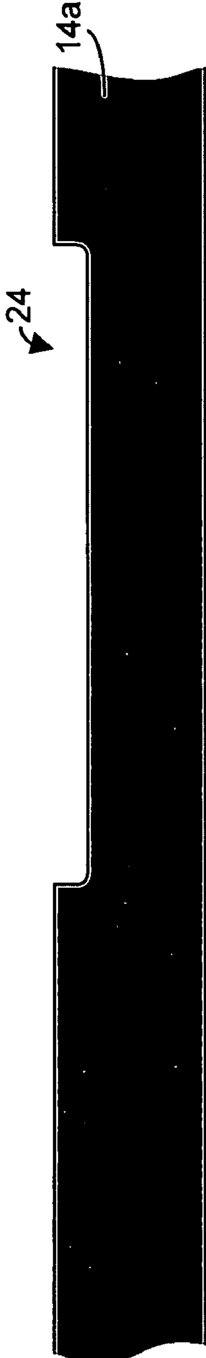


FIGURE 33B

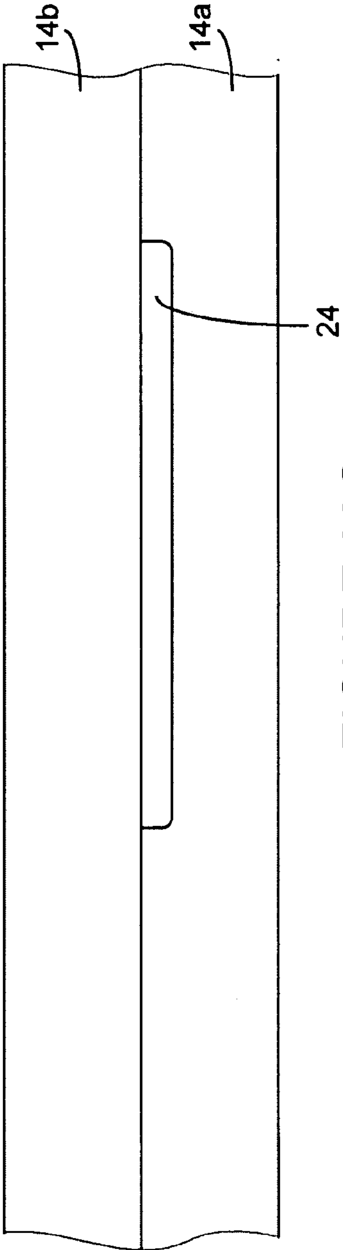


FIGURE 33C

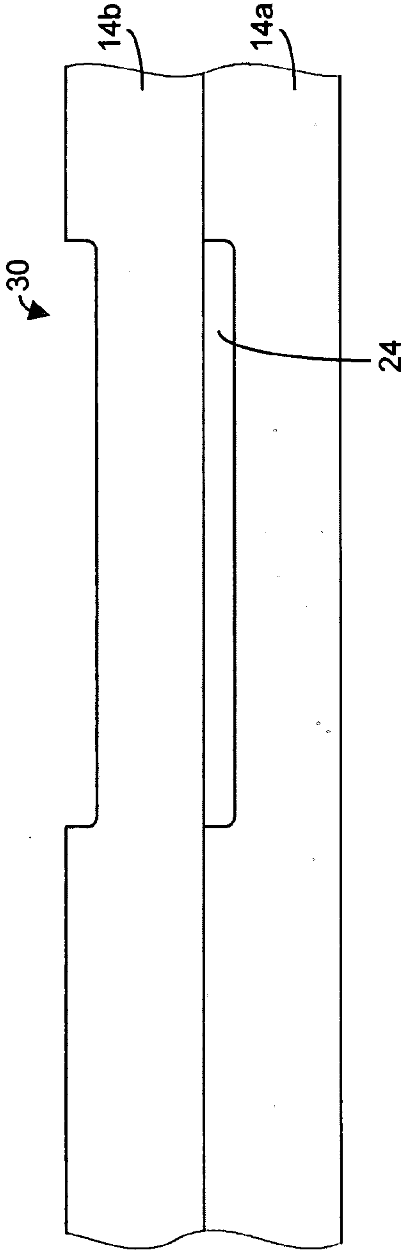


FIGURE 33D

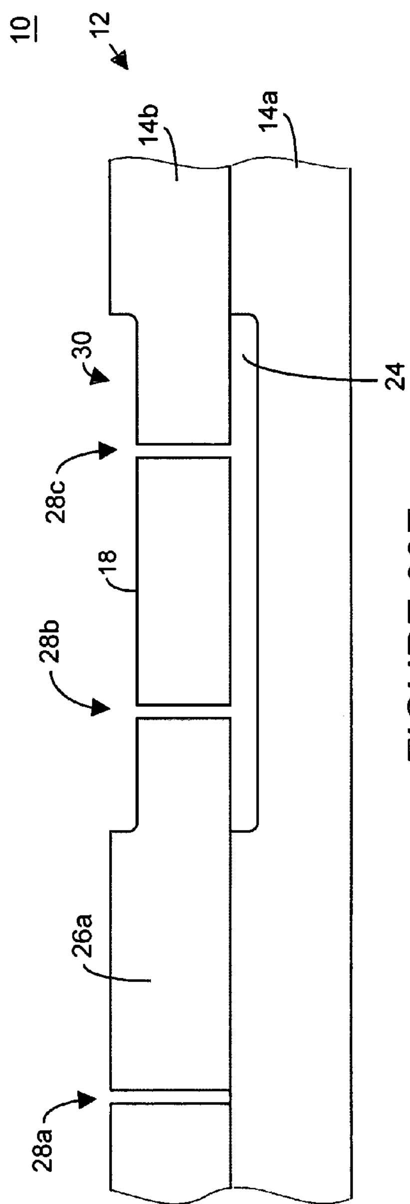


FIGURE 33E

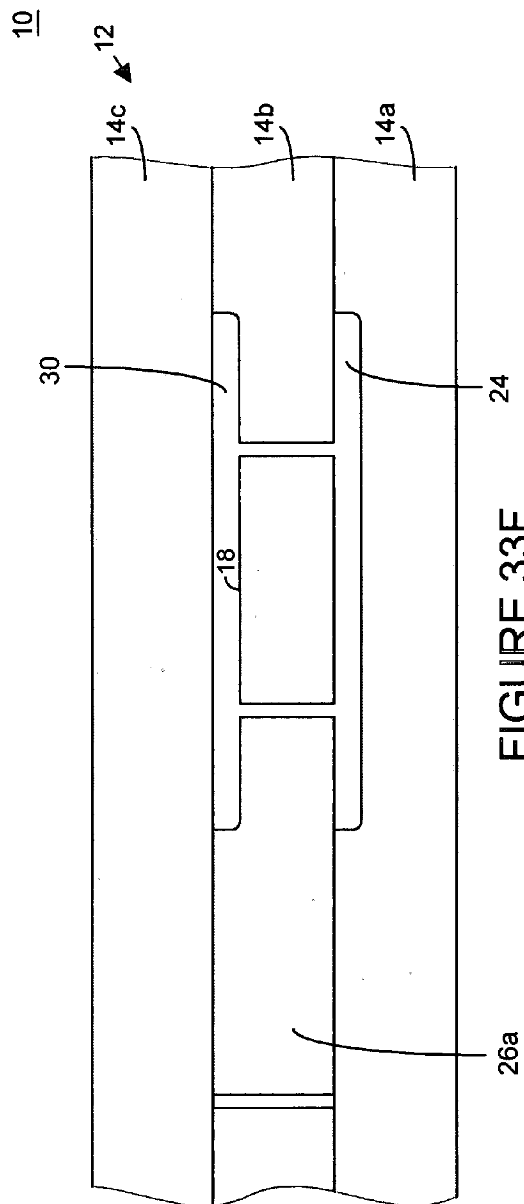


FIGURE 33F

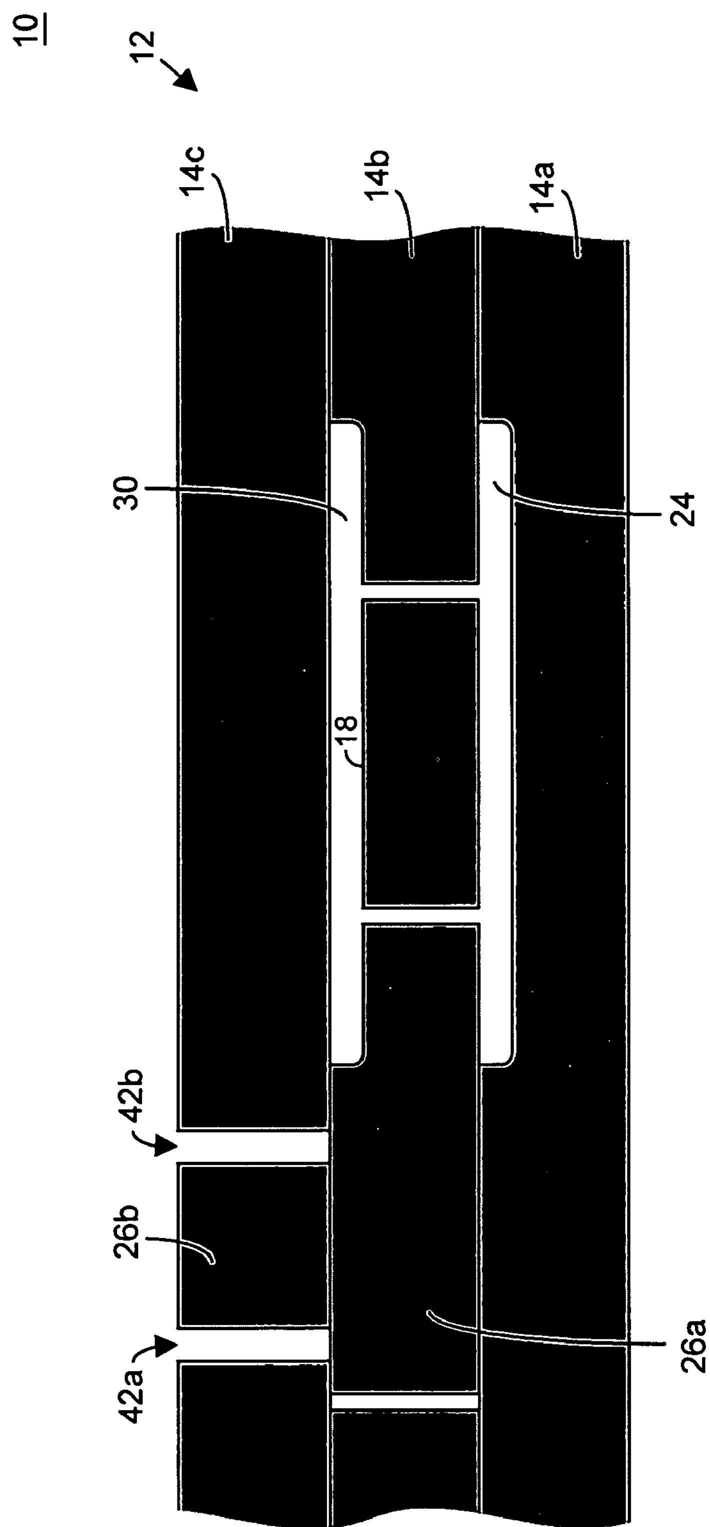


FIGURE 33G

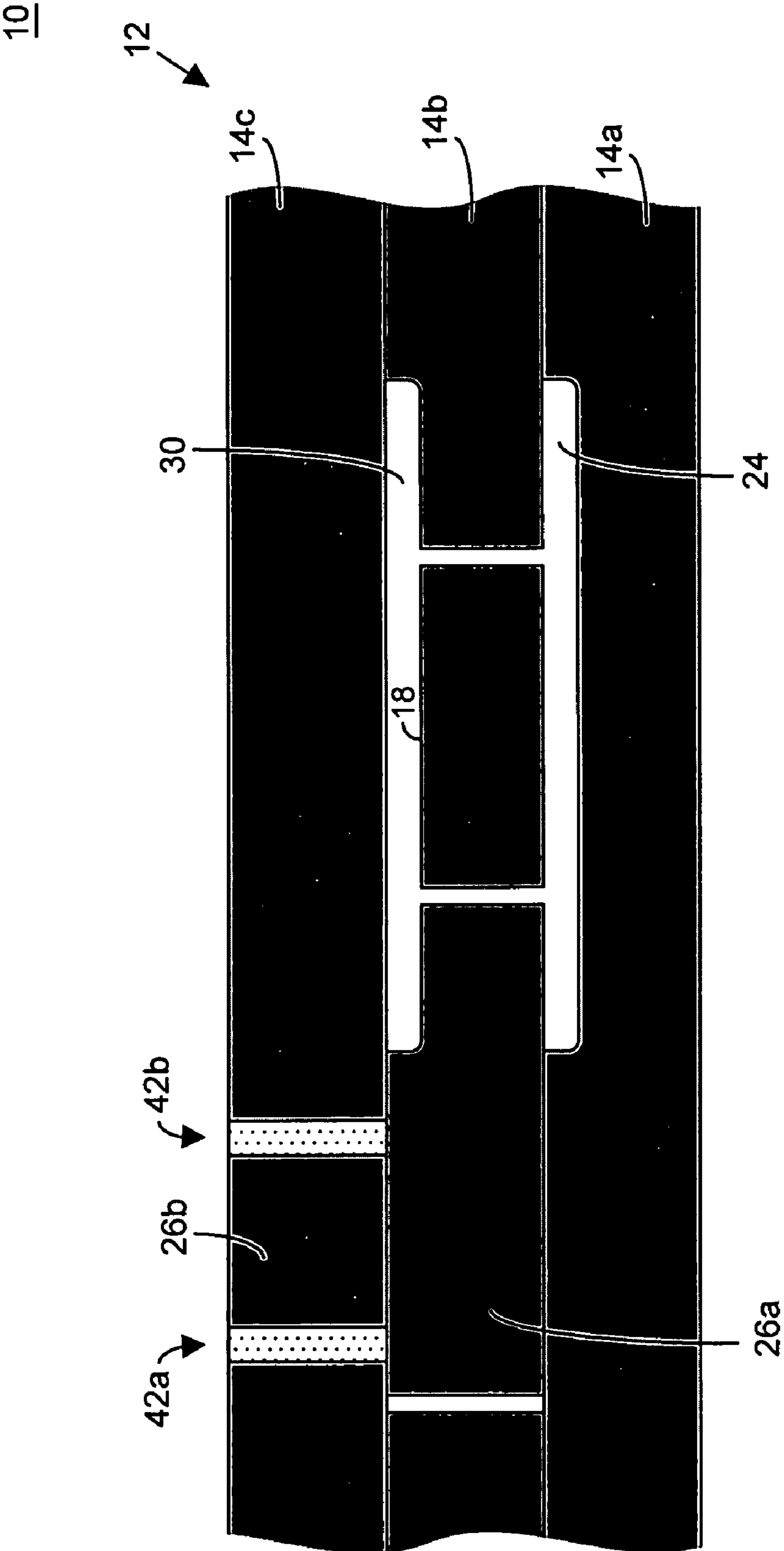


FIGURE 33H

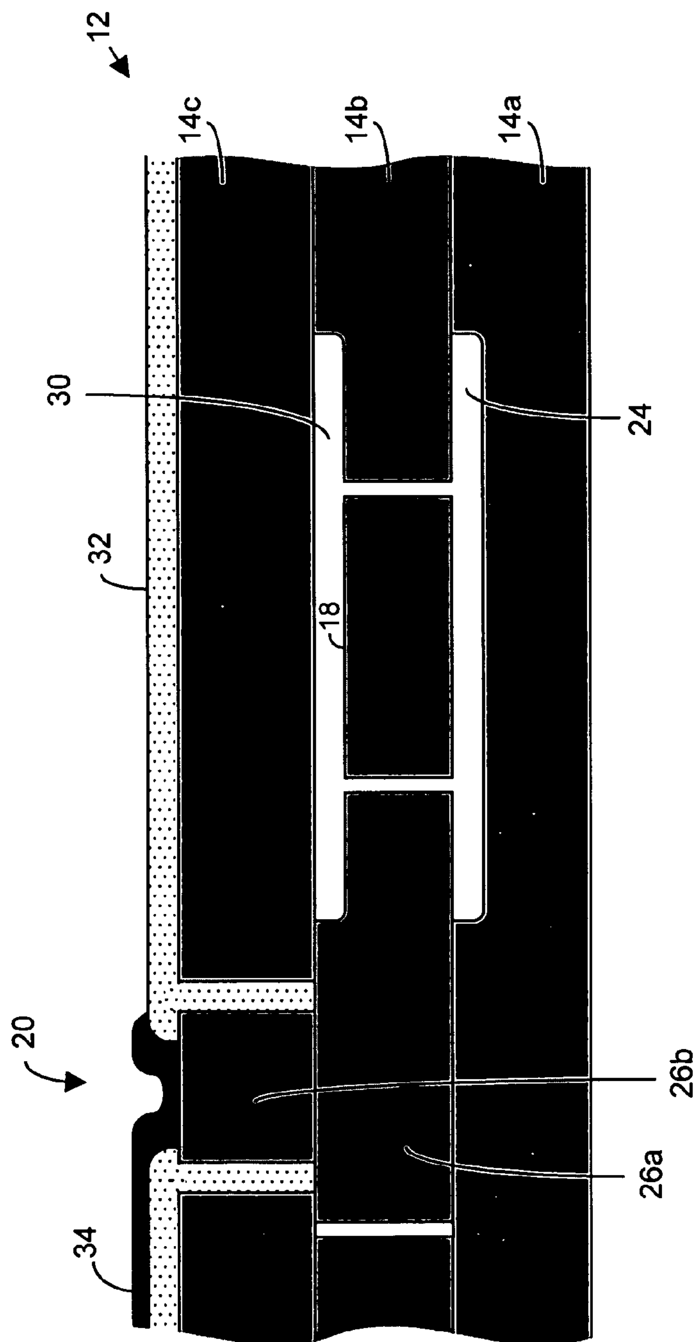


FIGURE 33I

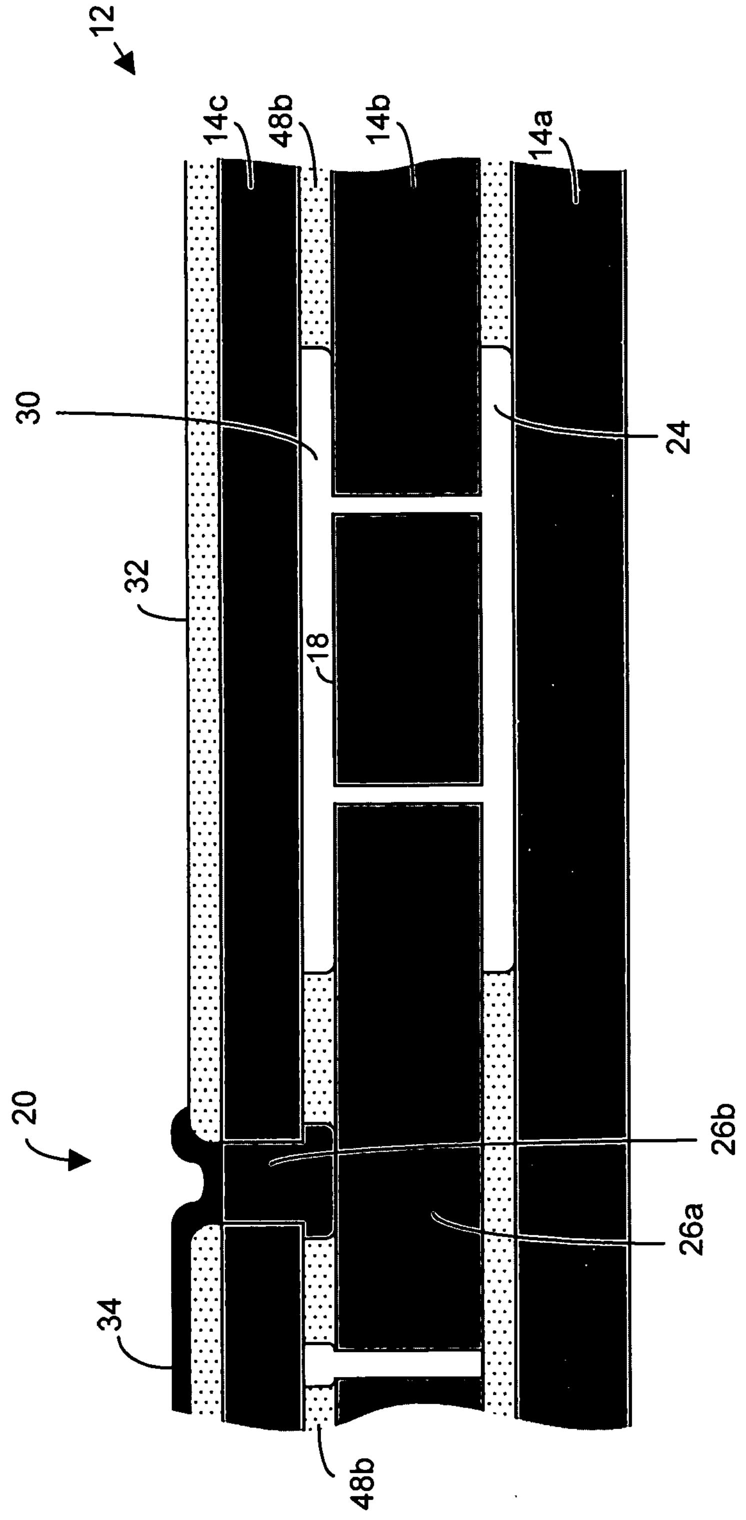


FIGURE 34

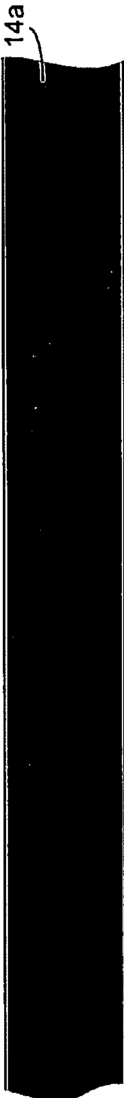


FIGURE 35A

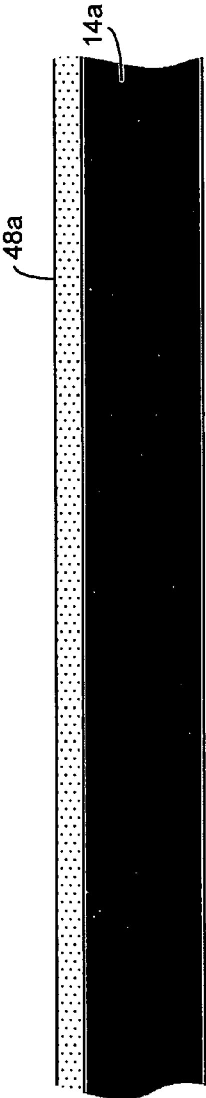


FIGURE 35B

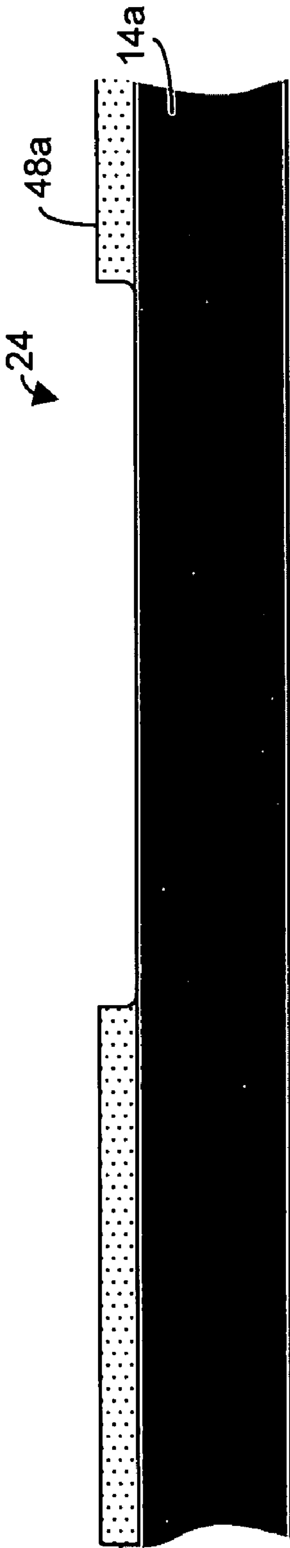


FIGURE 35C

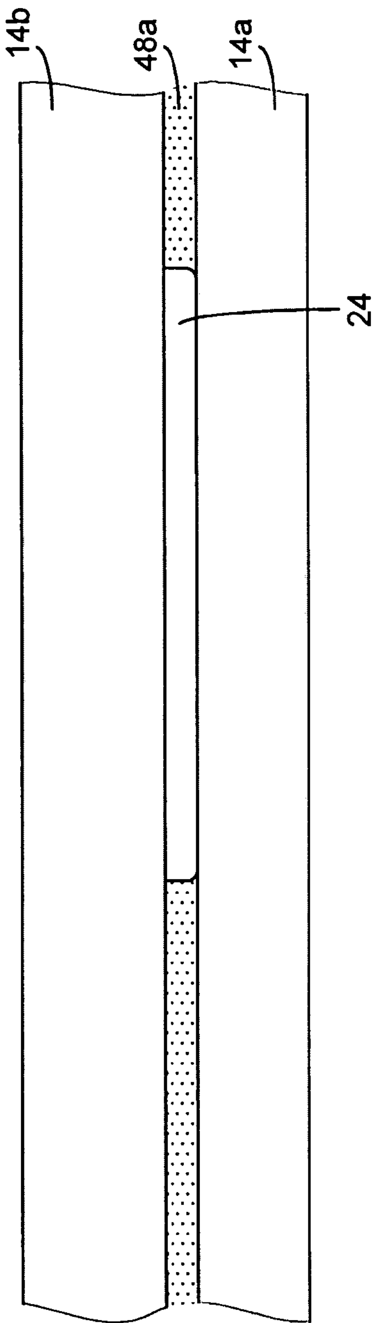


FIGURE 35D

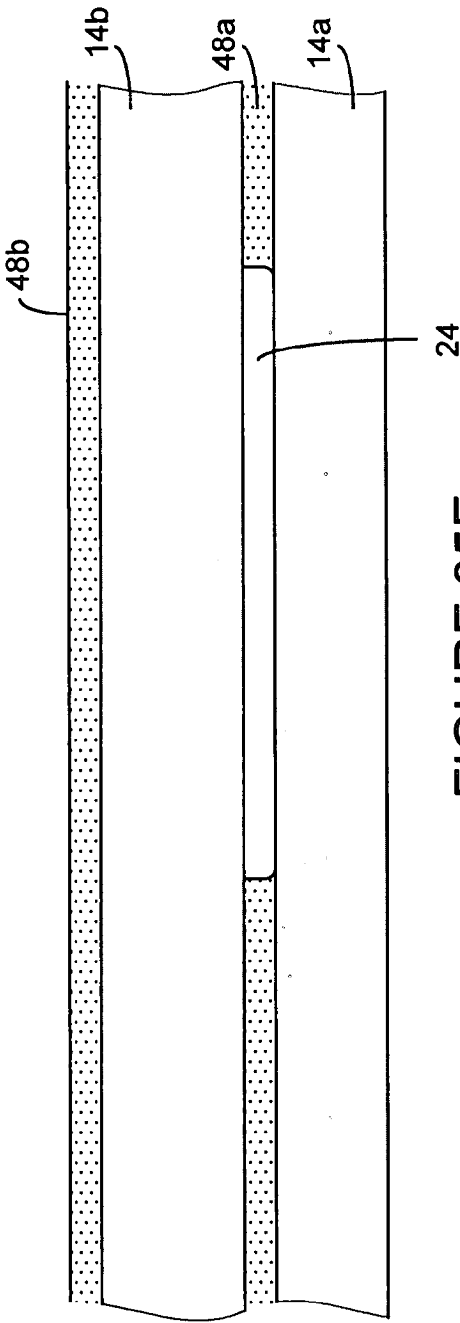


FIGURE 35E

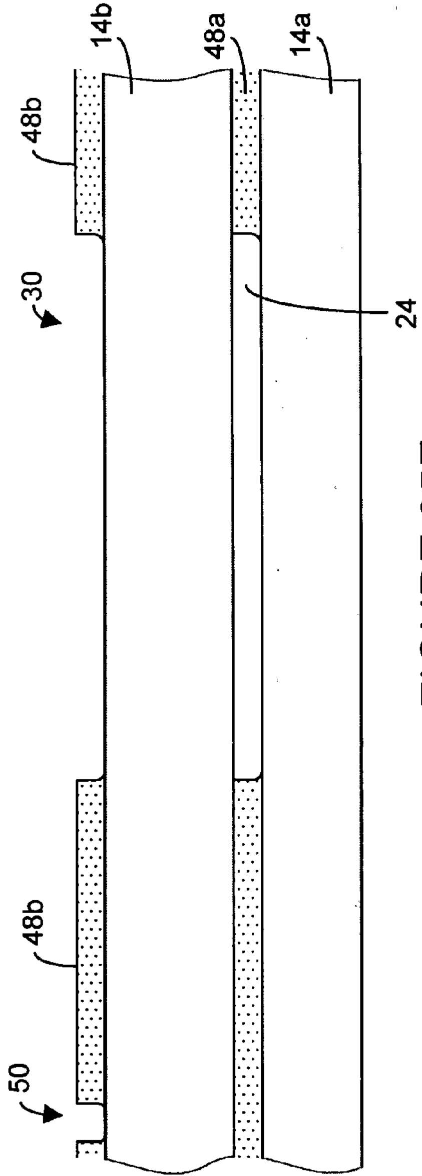


FIGURE 35F

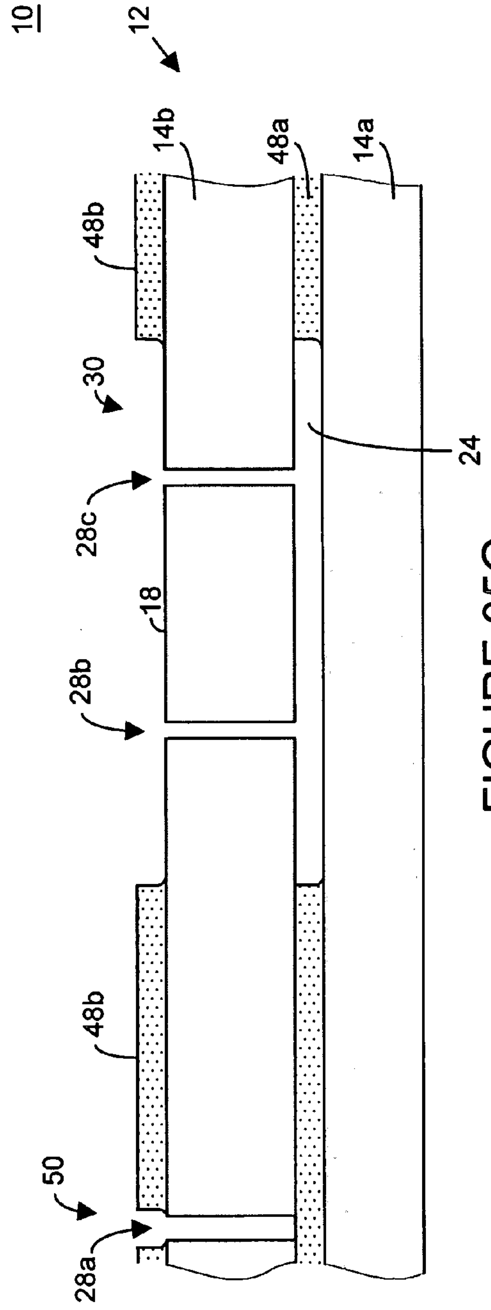


FIGURE 35G

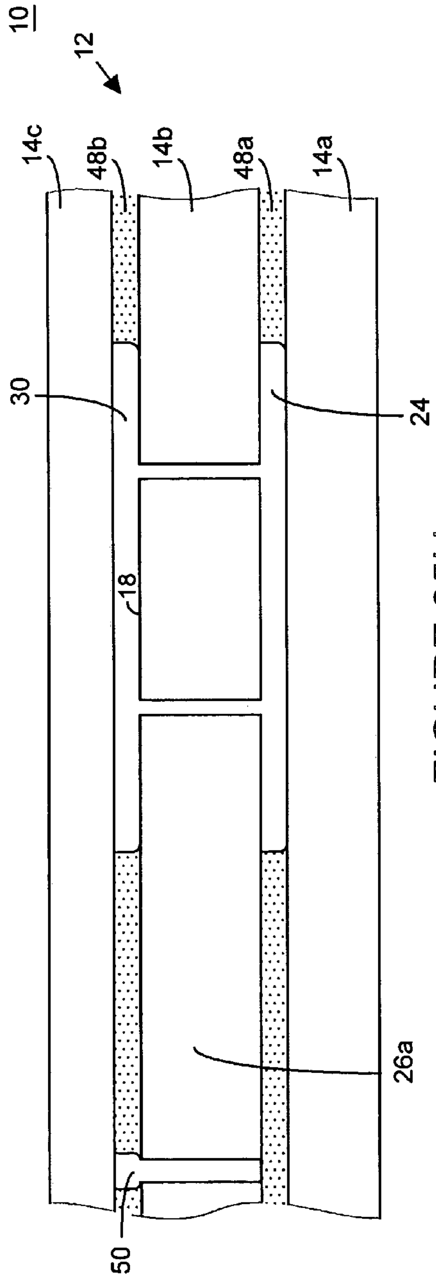


FIGURE 35H

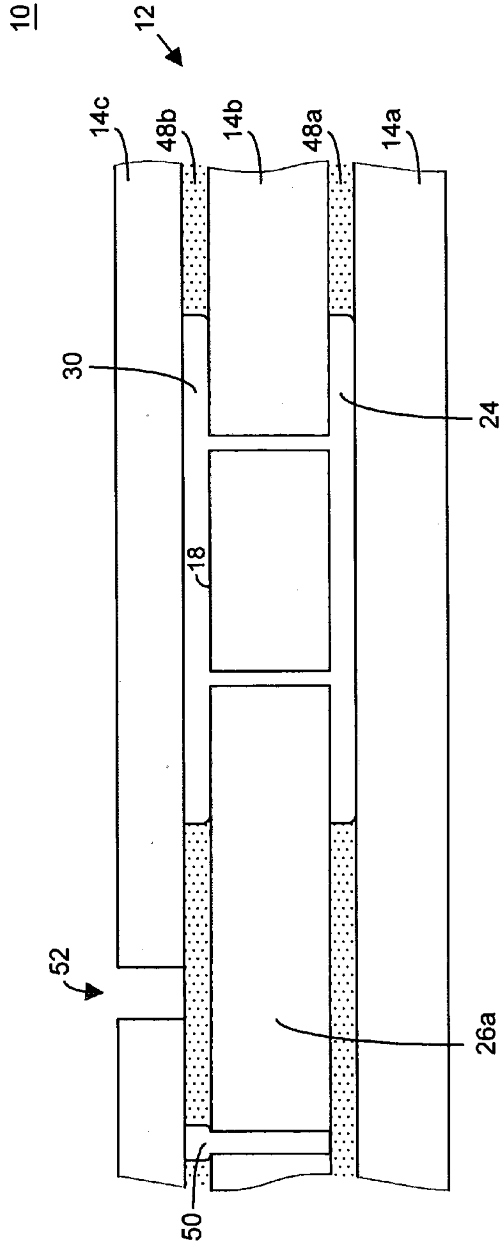


FIGURE 35I

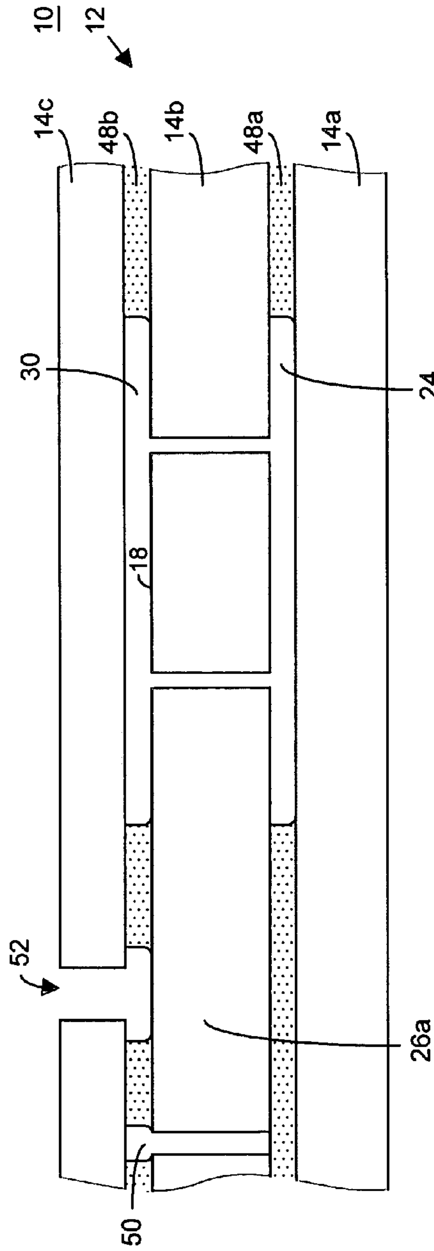


FIGURE 35J

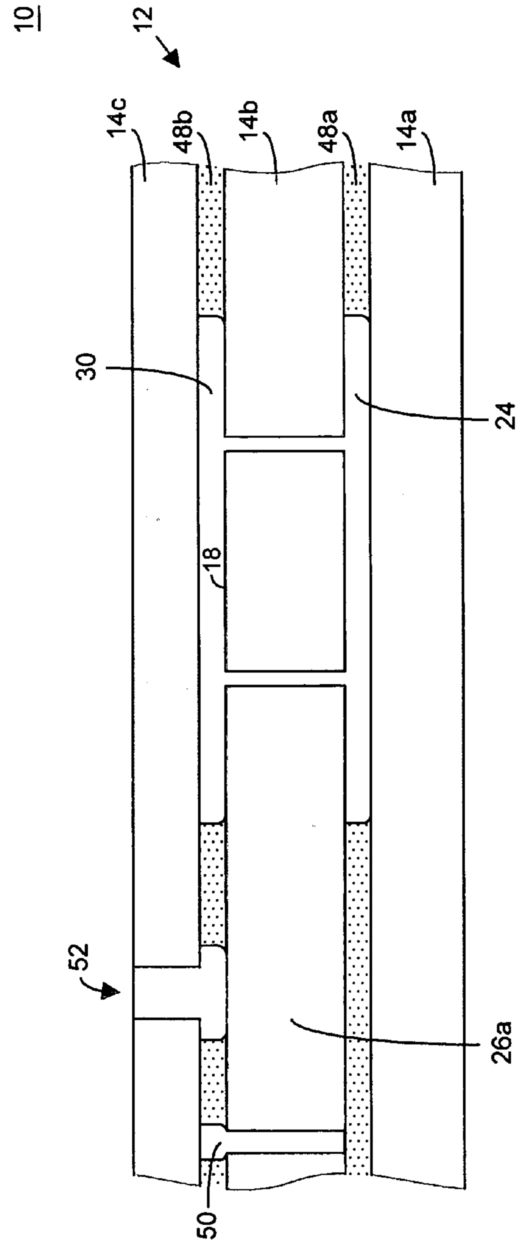


FIGURE 35K

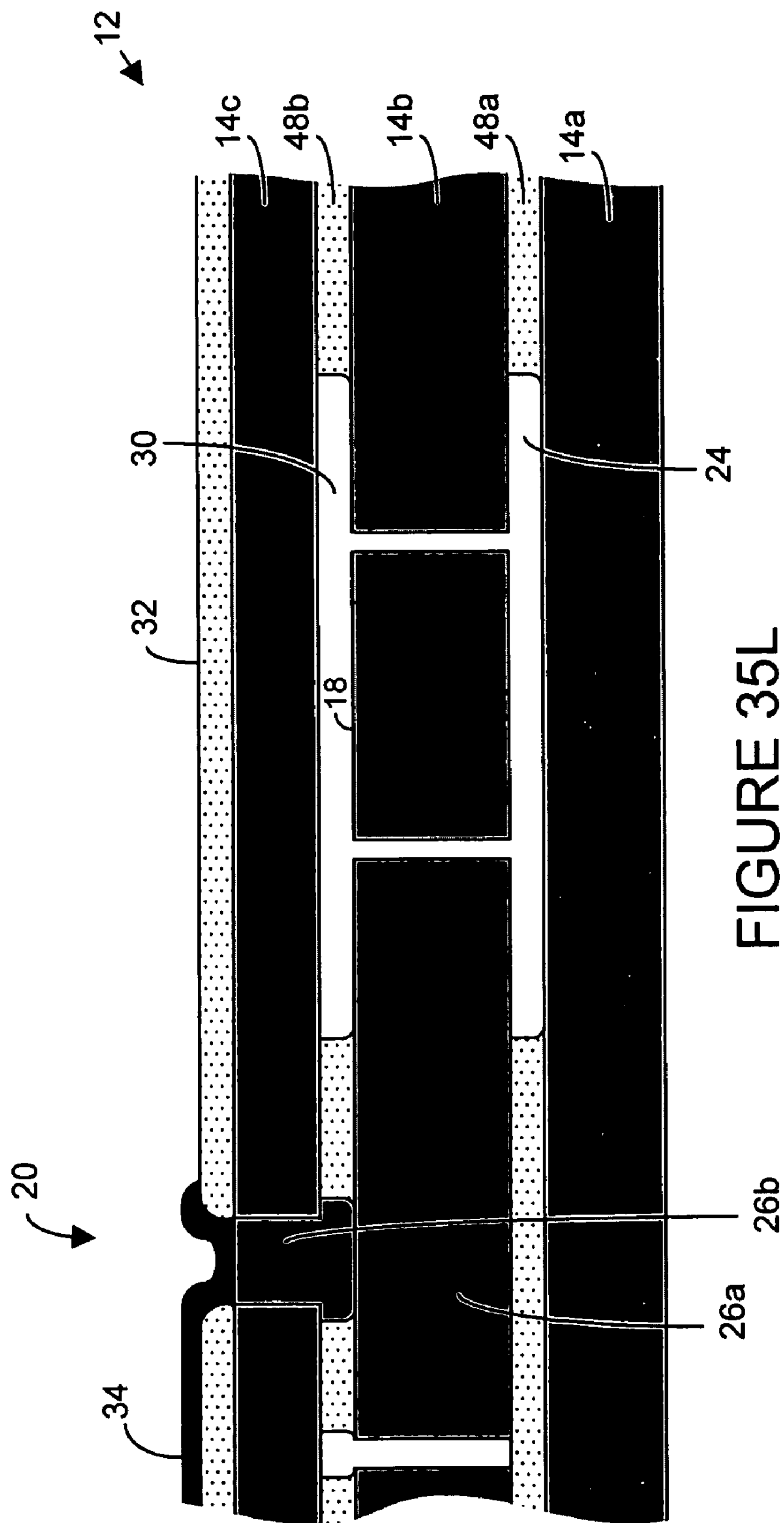


FIGURE 35L

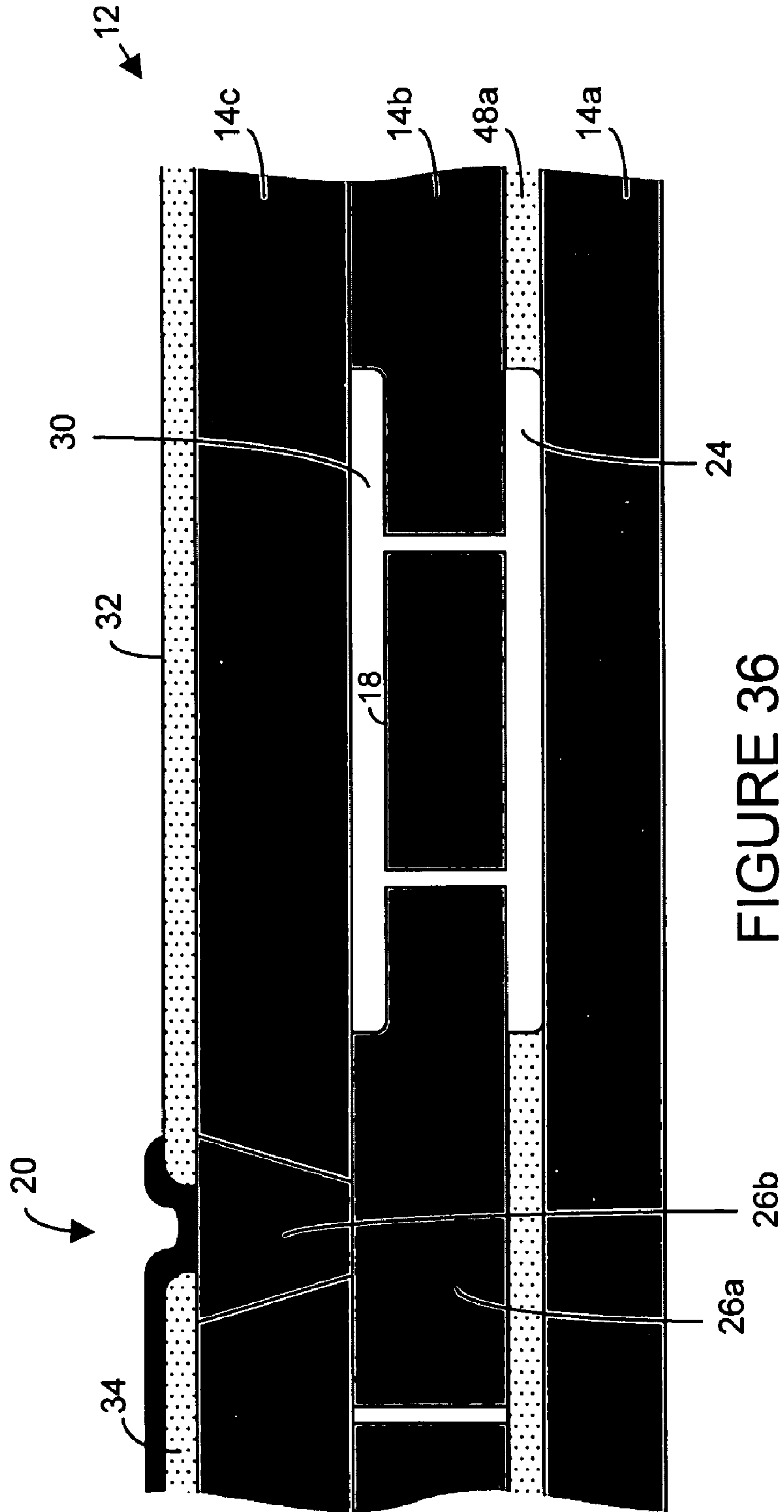


FIGURE 36

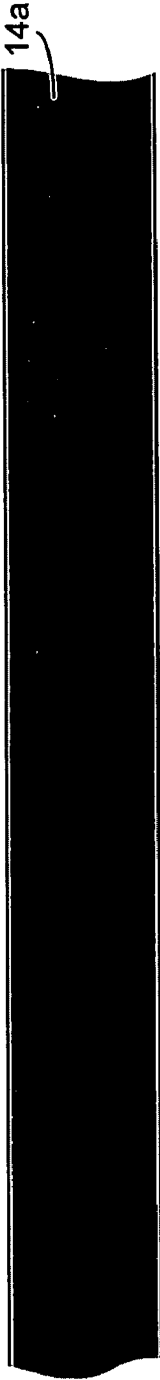


FIGURE 37A

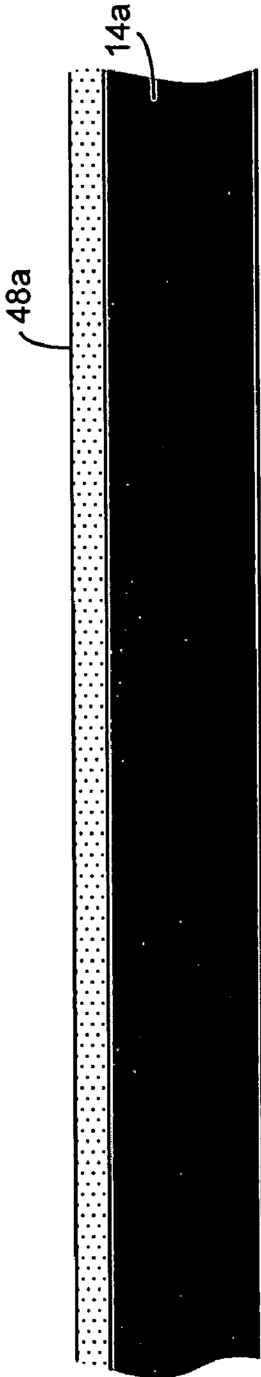


FIGURE 37B

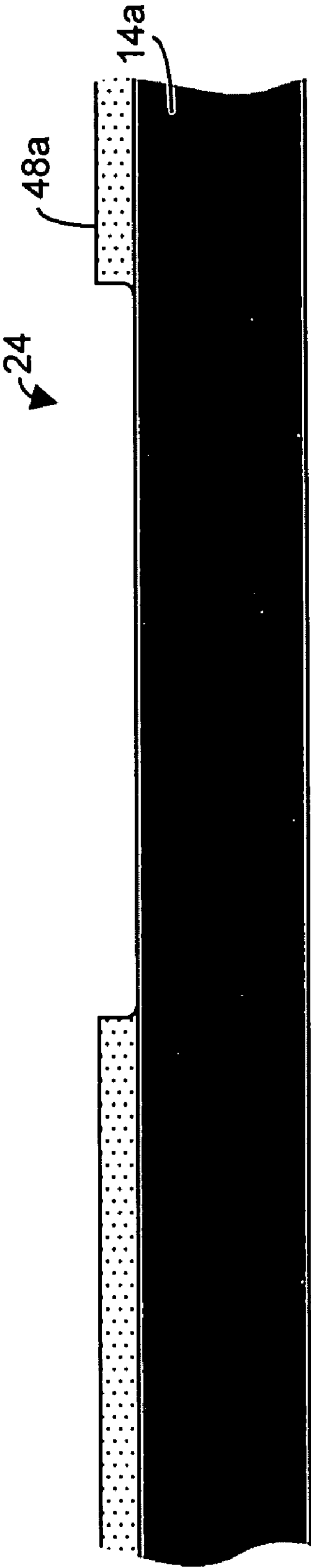


FIGURE 37C

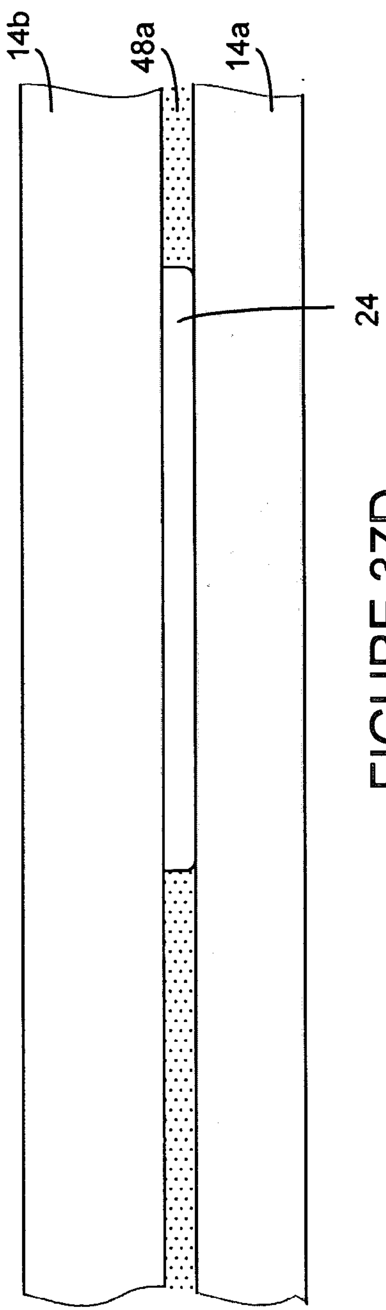


FIGURE 37D

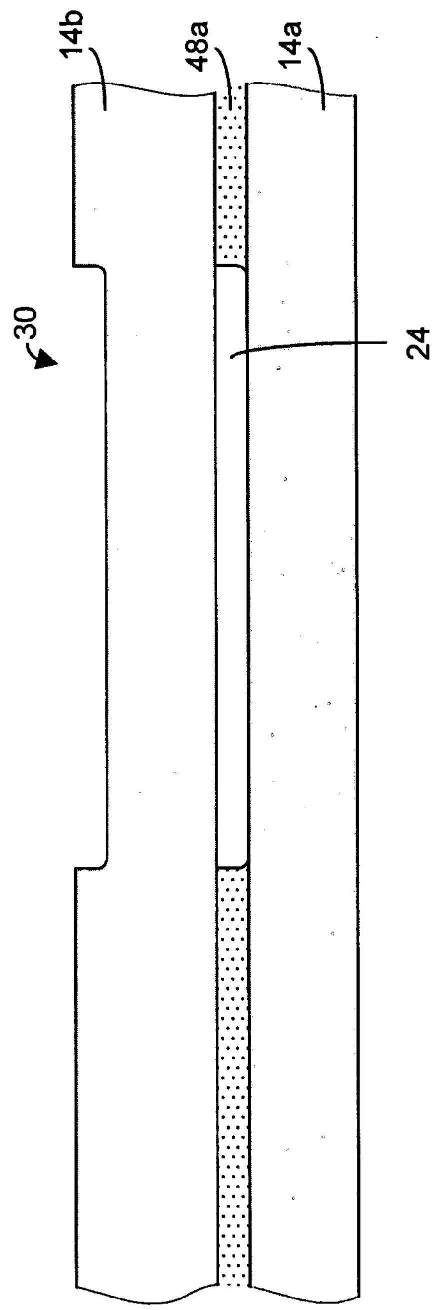


FIGURE 37E

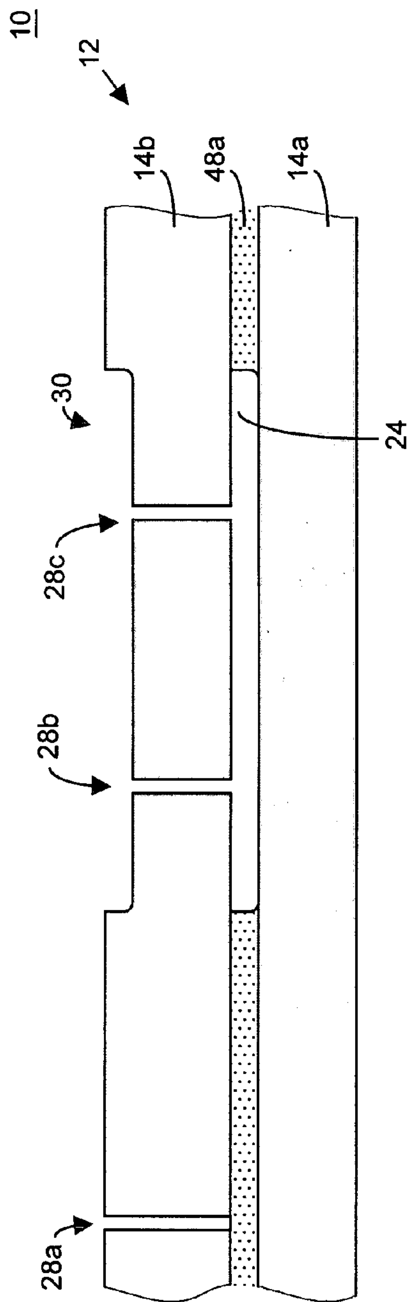


FIGURE 37F

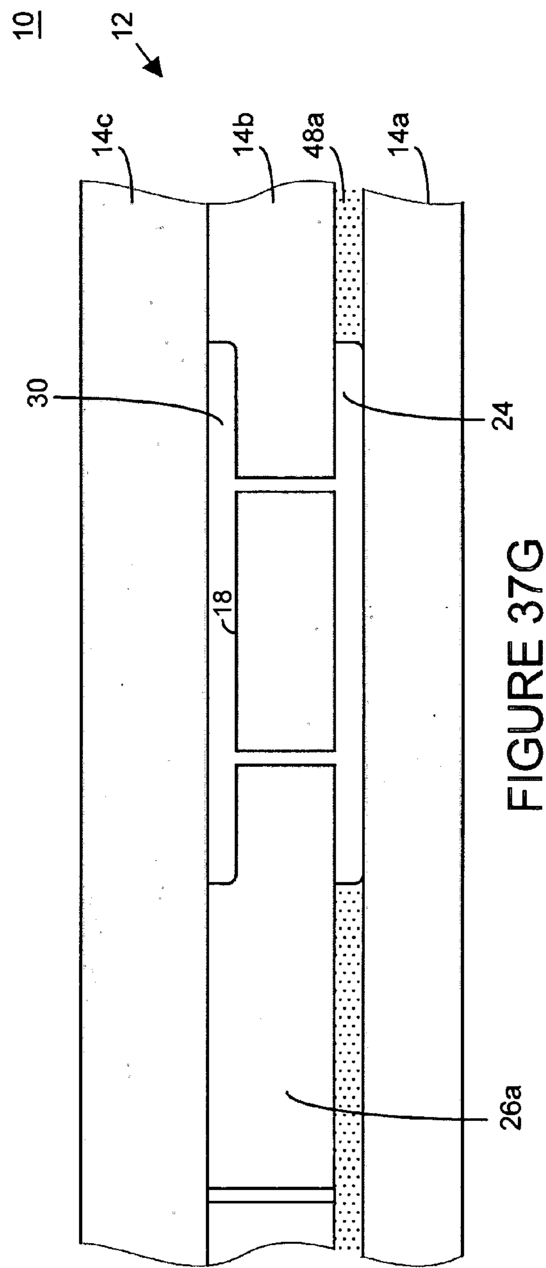


FIGURE 37G

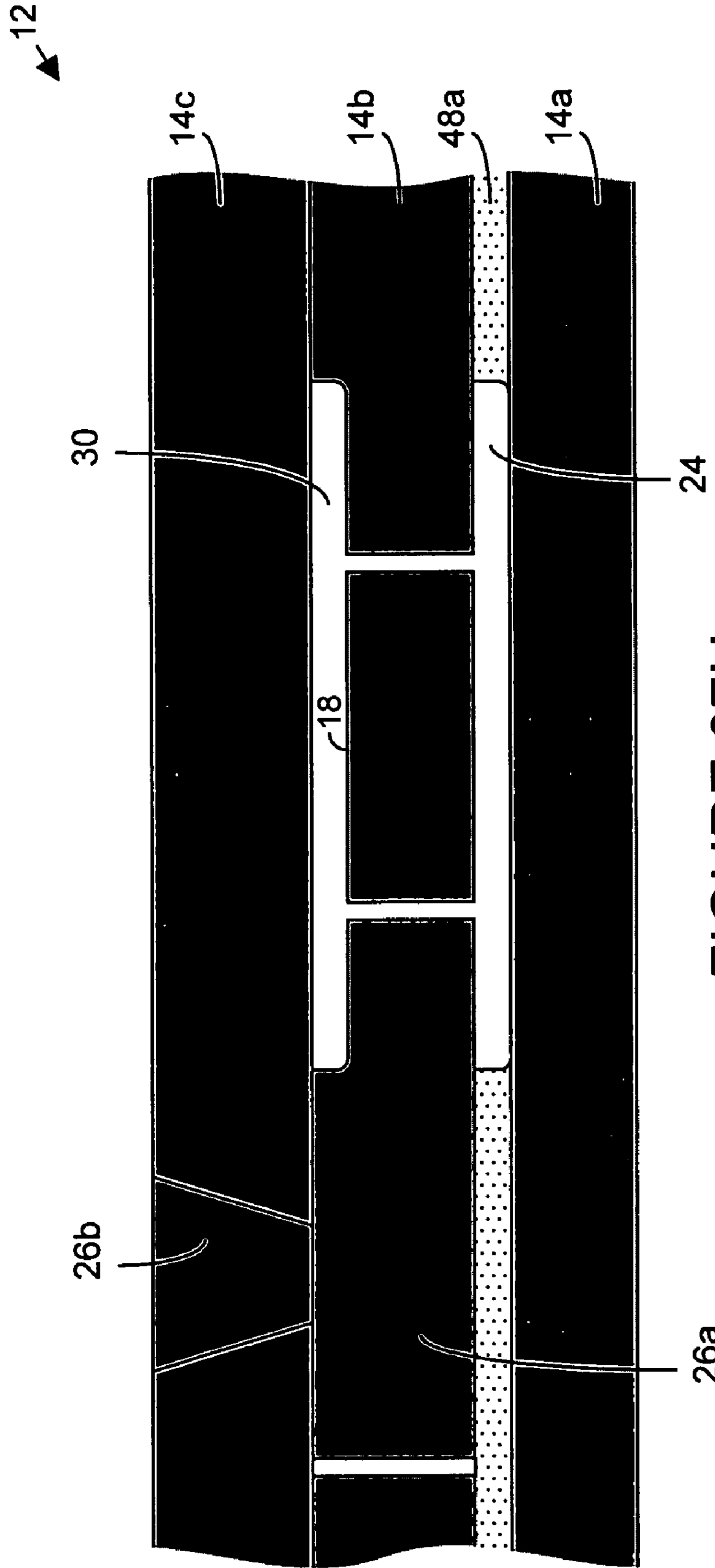


FIGURE 37H

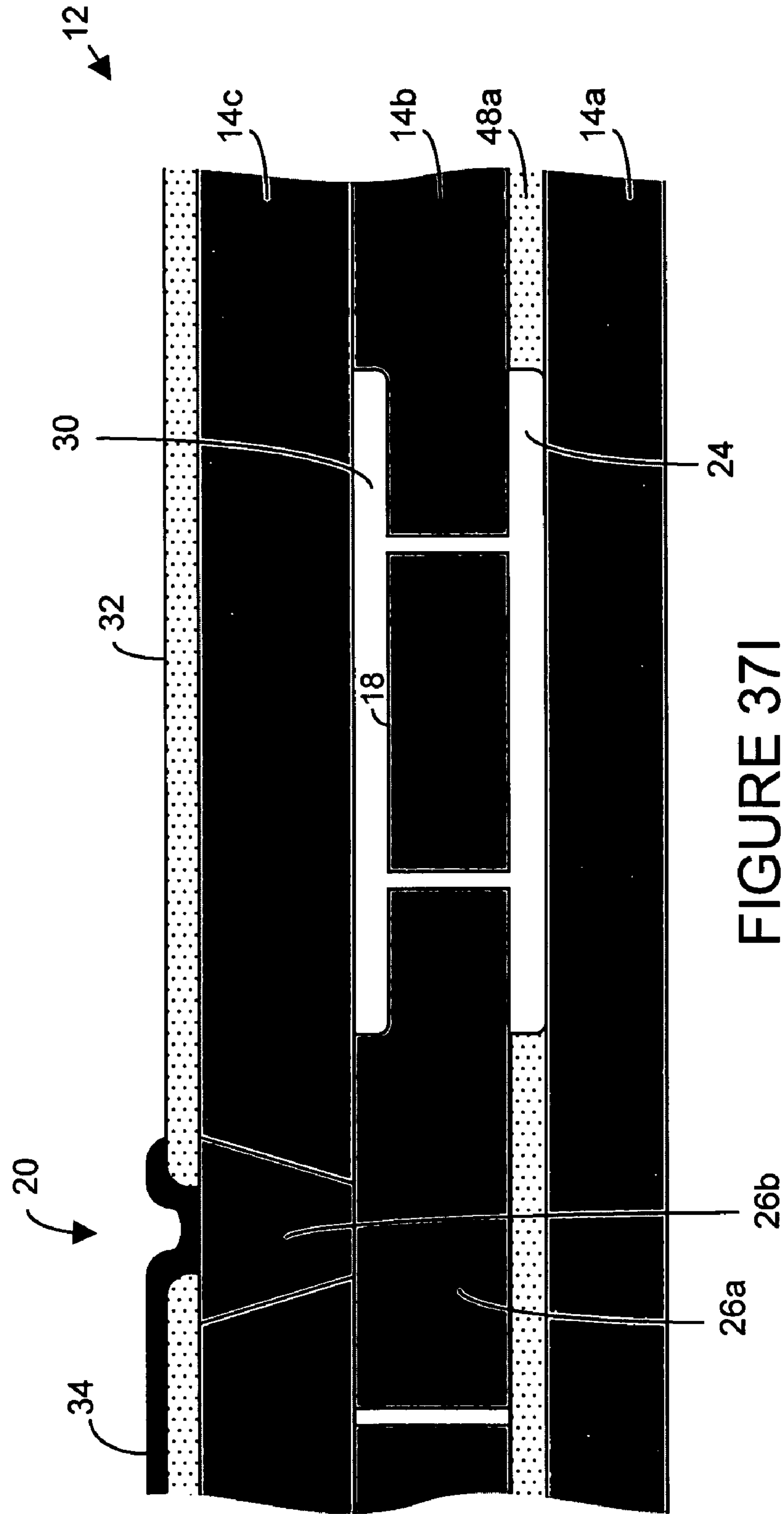


FIGURE 37I

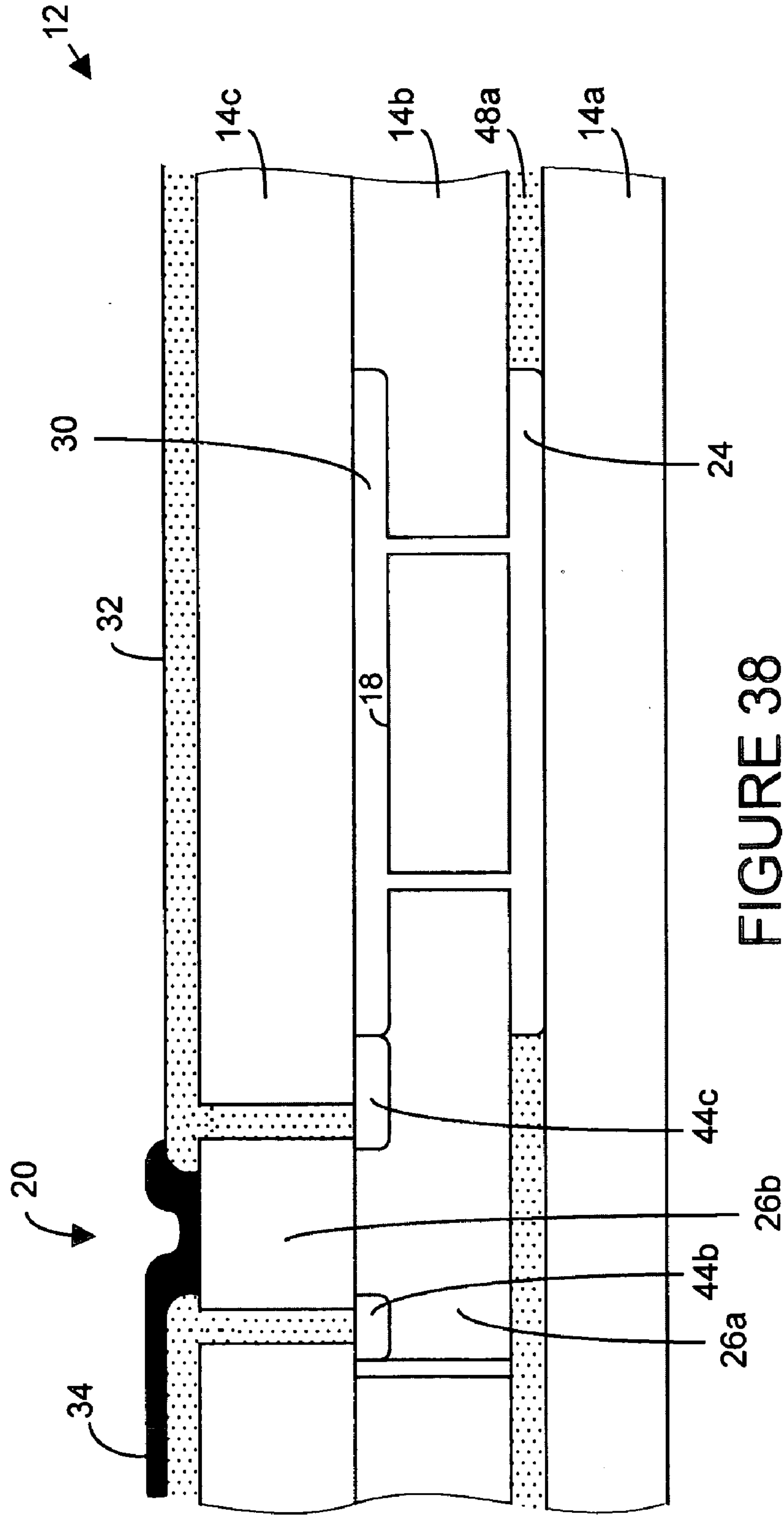


FIGURE 38

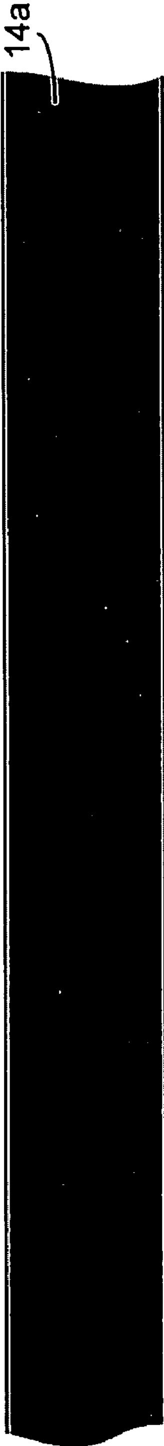


FIGURE 39A

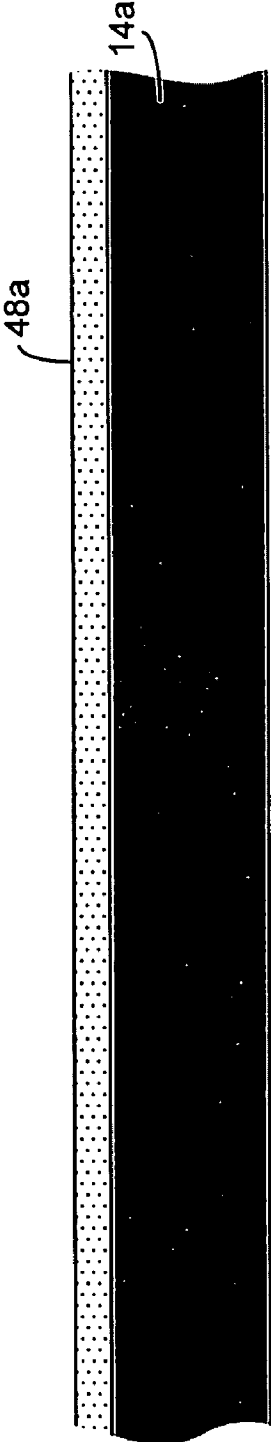


FIGURE 39B

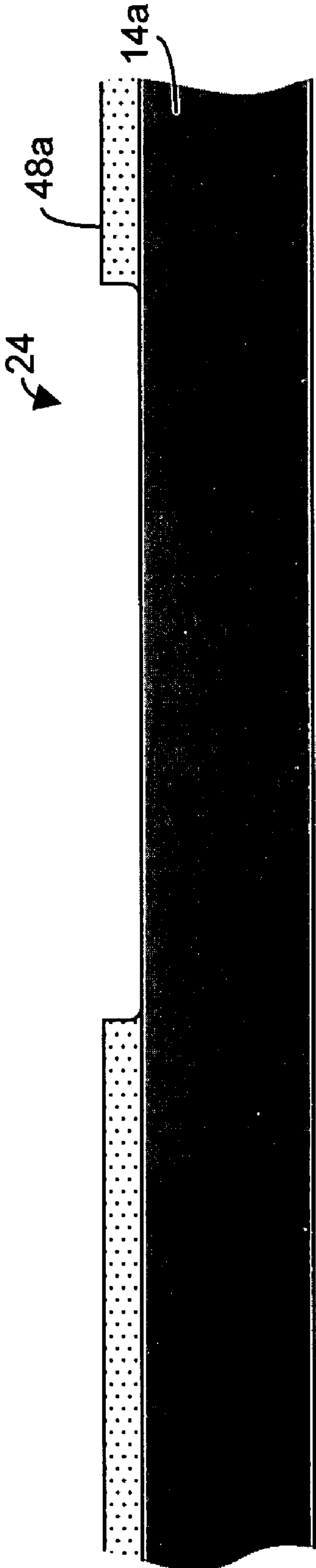


FIGURE 39C

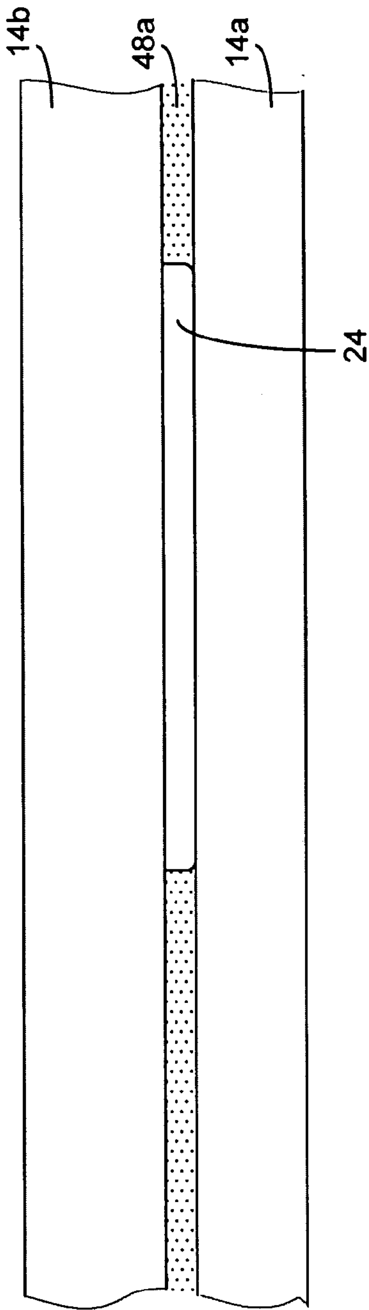


FIGURE 39D

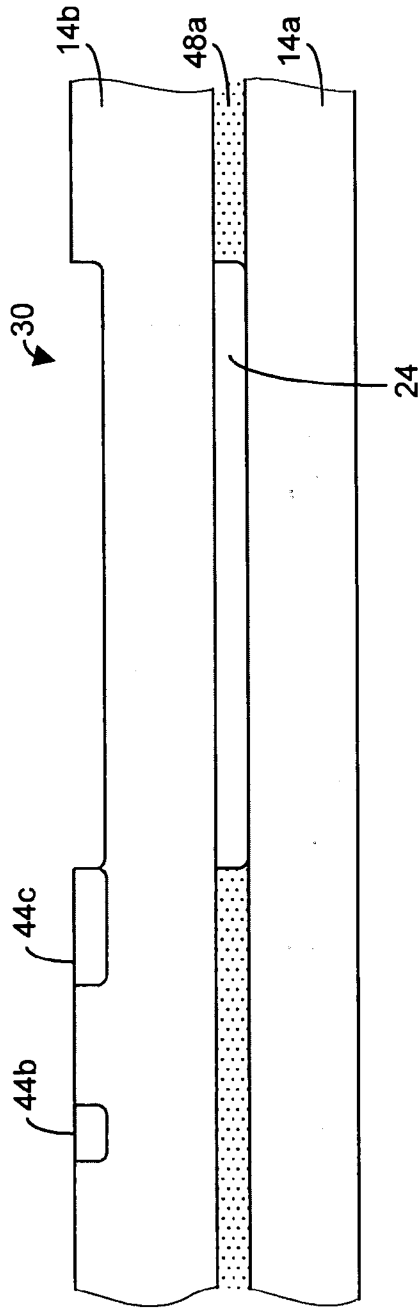


FIGURE 39E

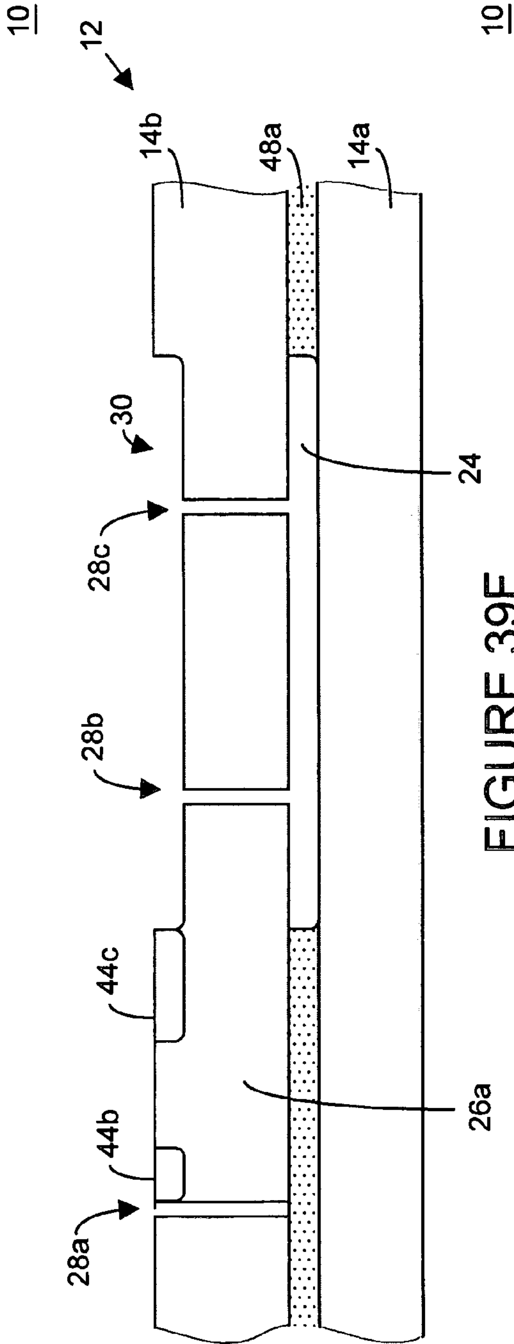


FIGURE 39F

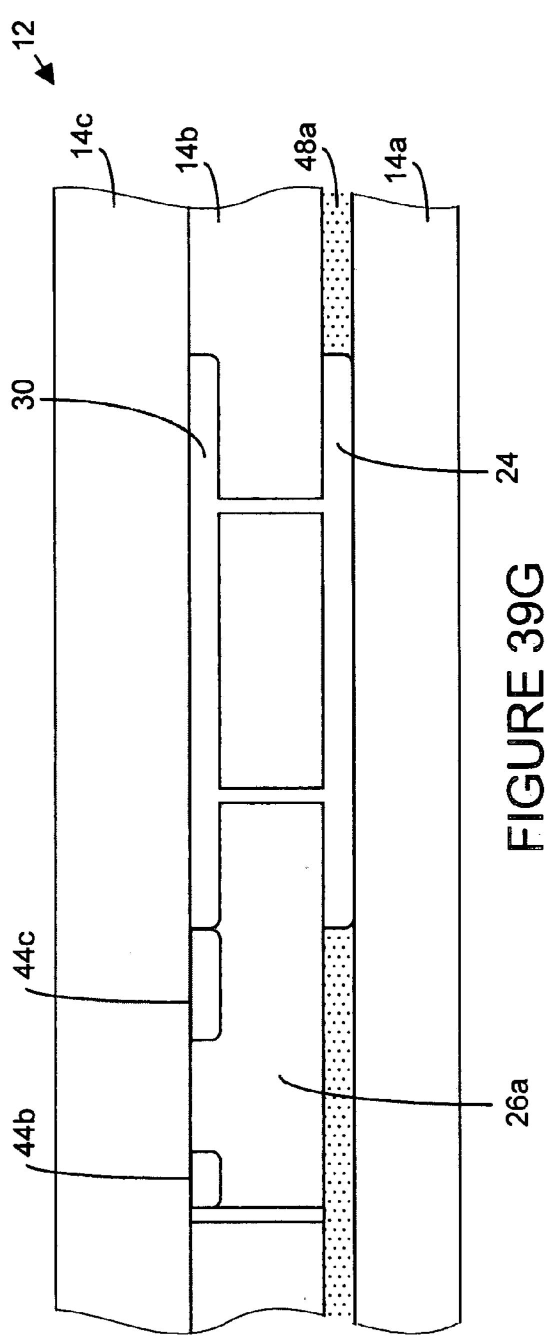


FIGURE 39G

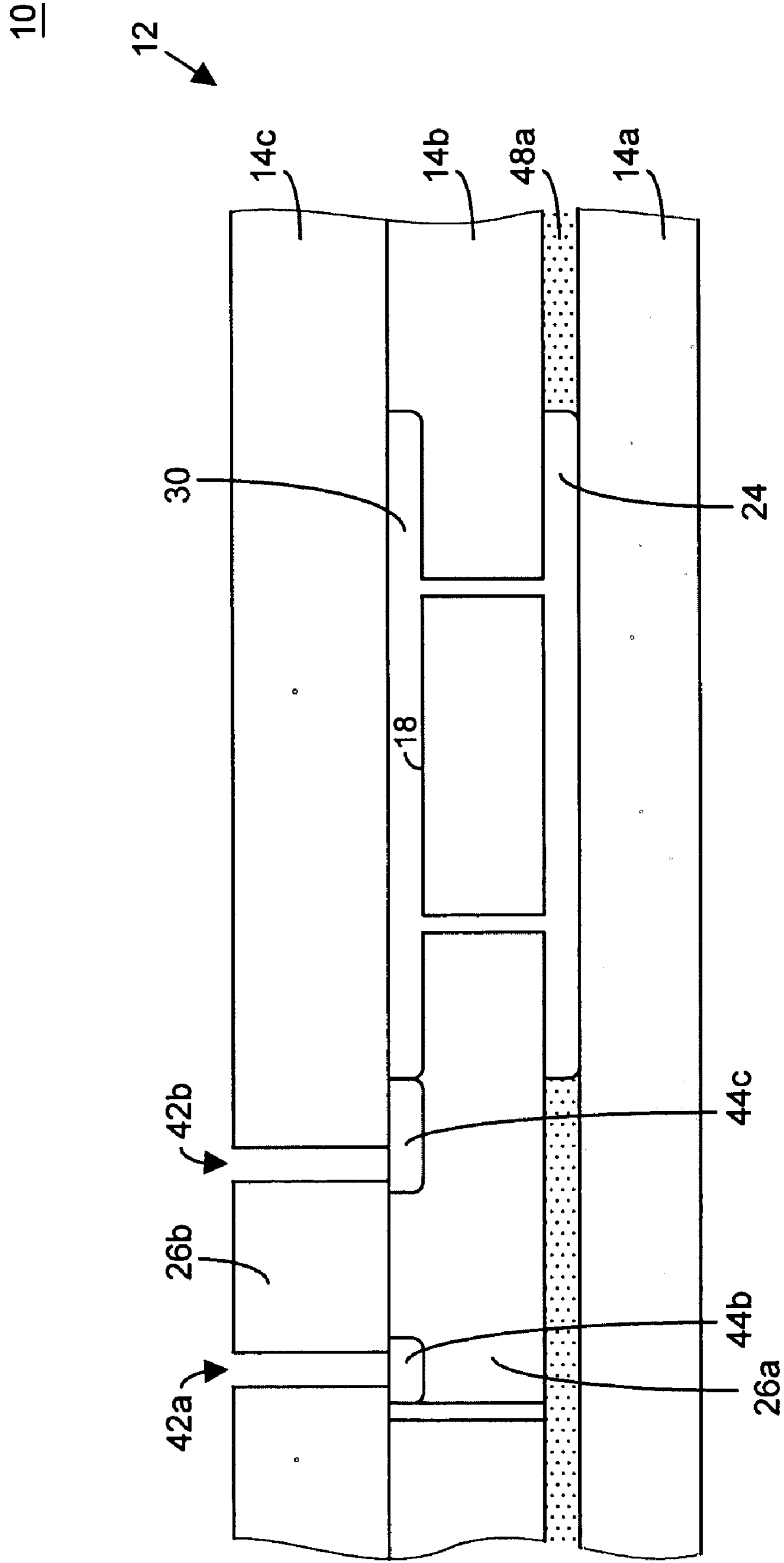


FIGURE 39H

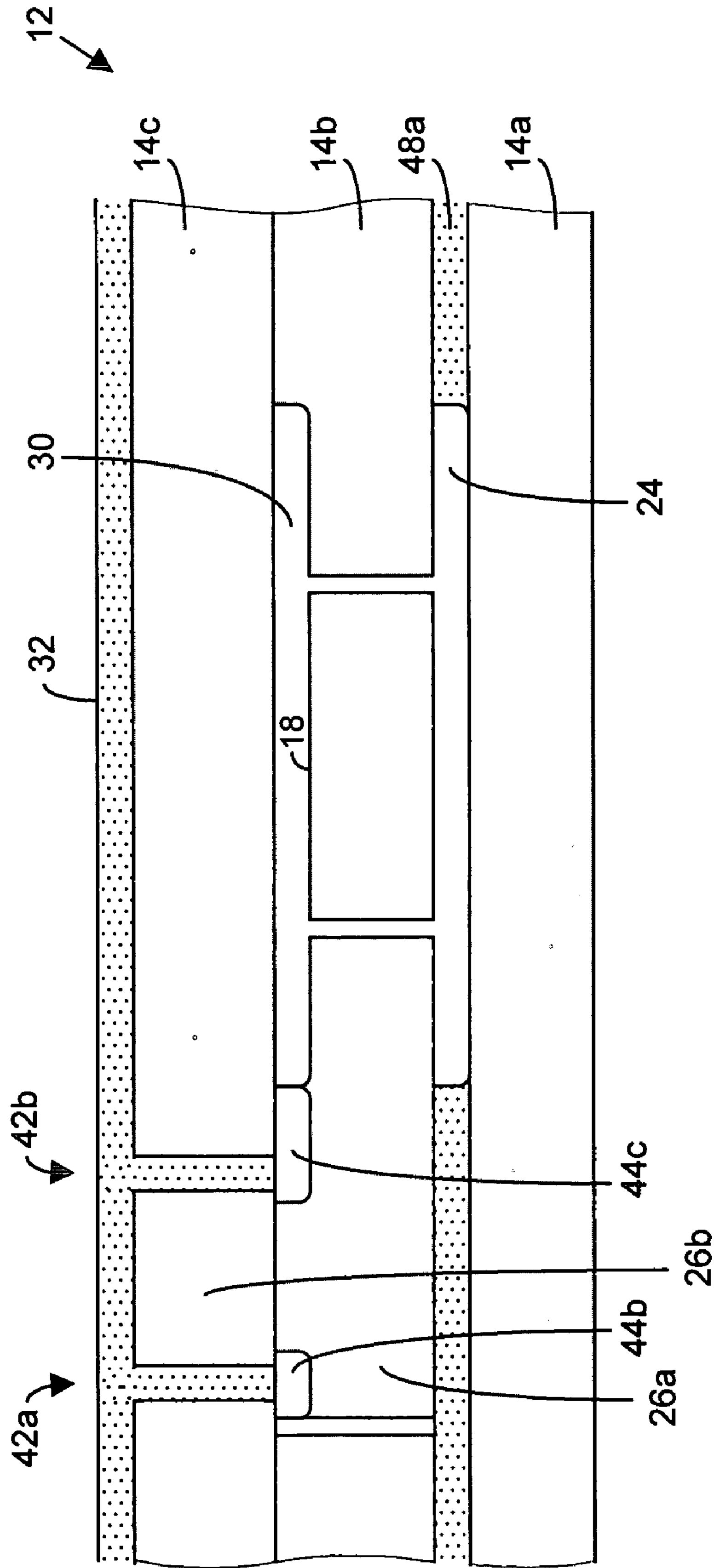


FIGURE 39I

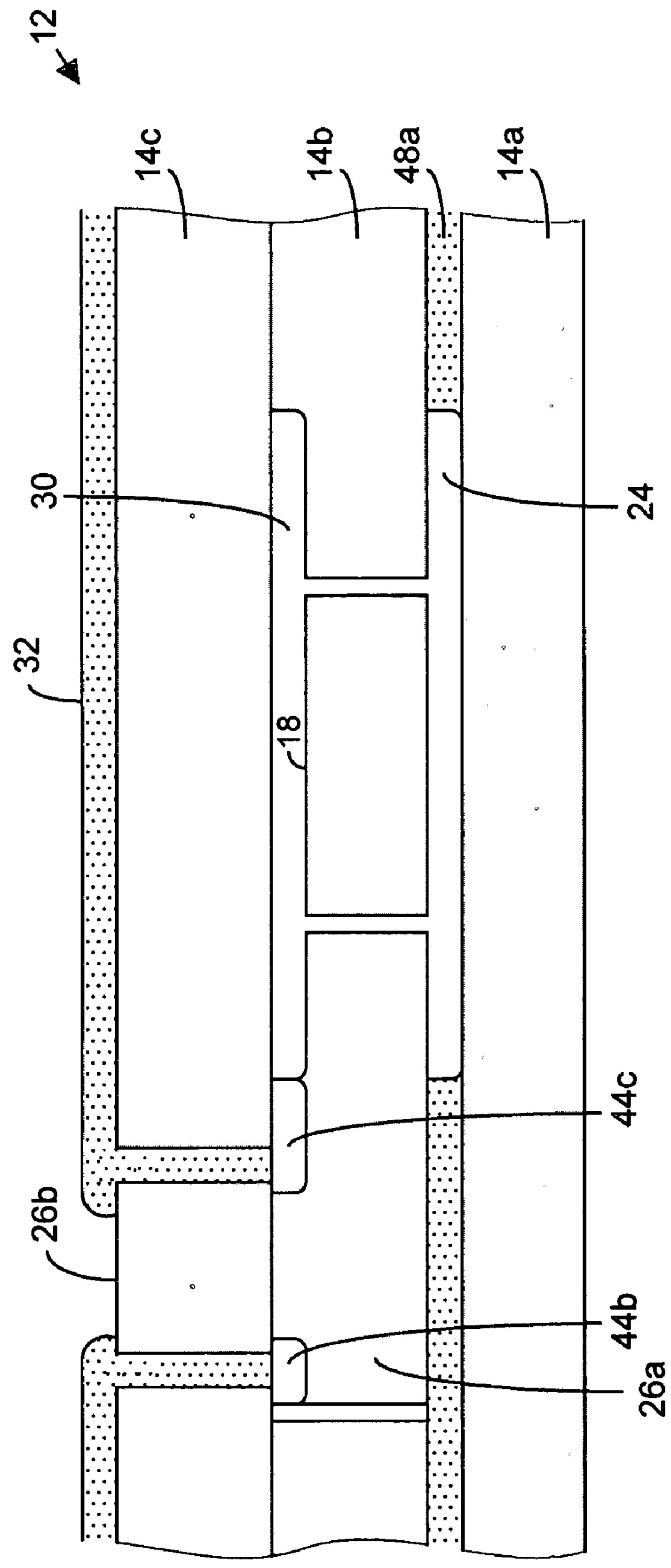


FIGURE 39J

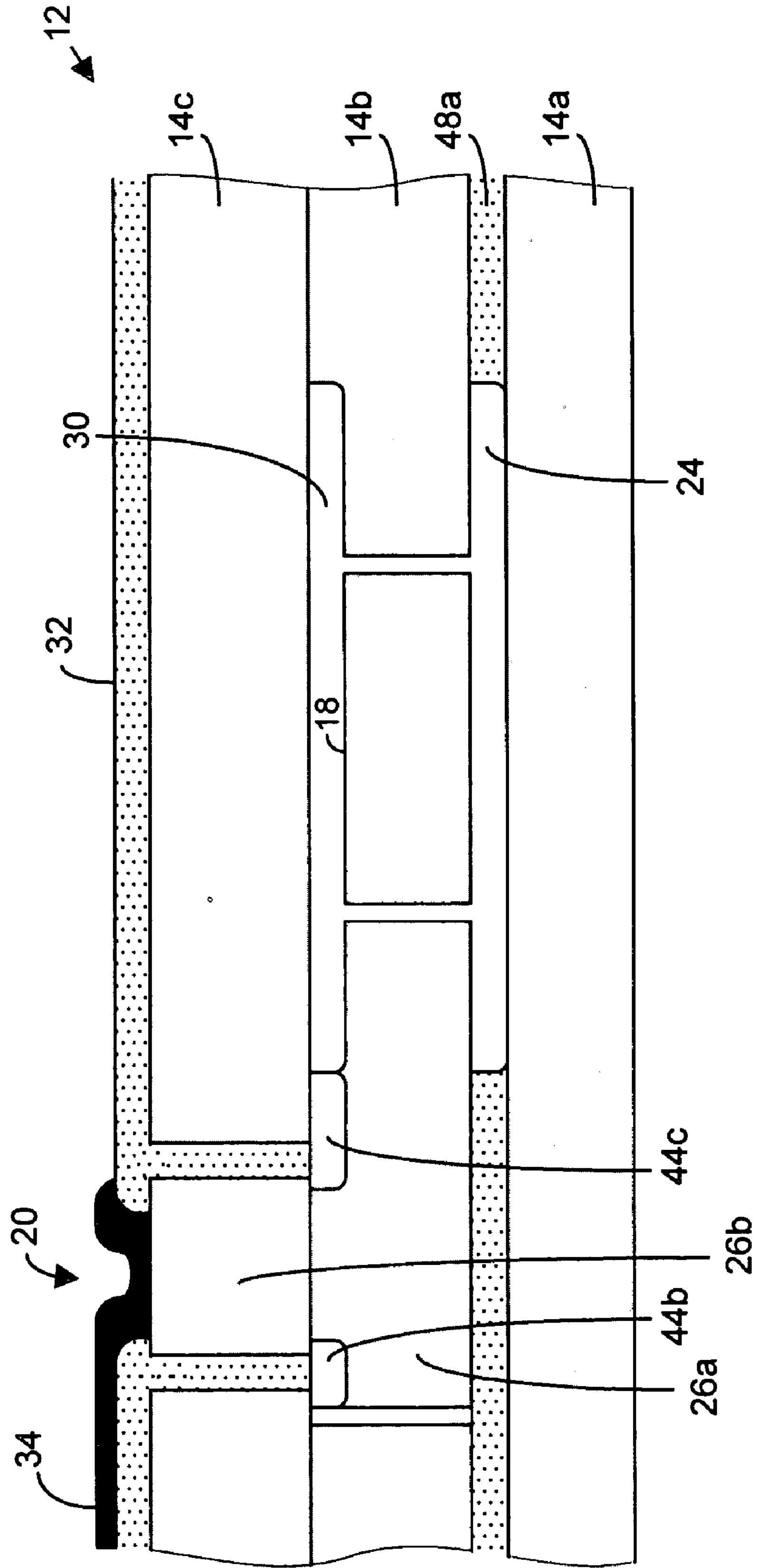


FIGURE 39K

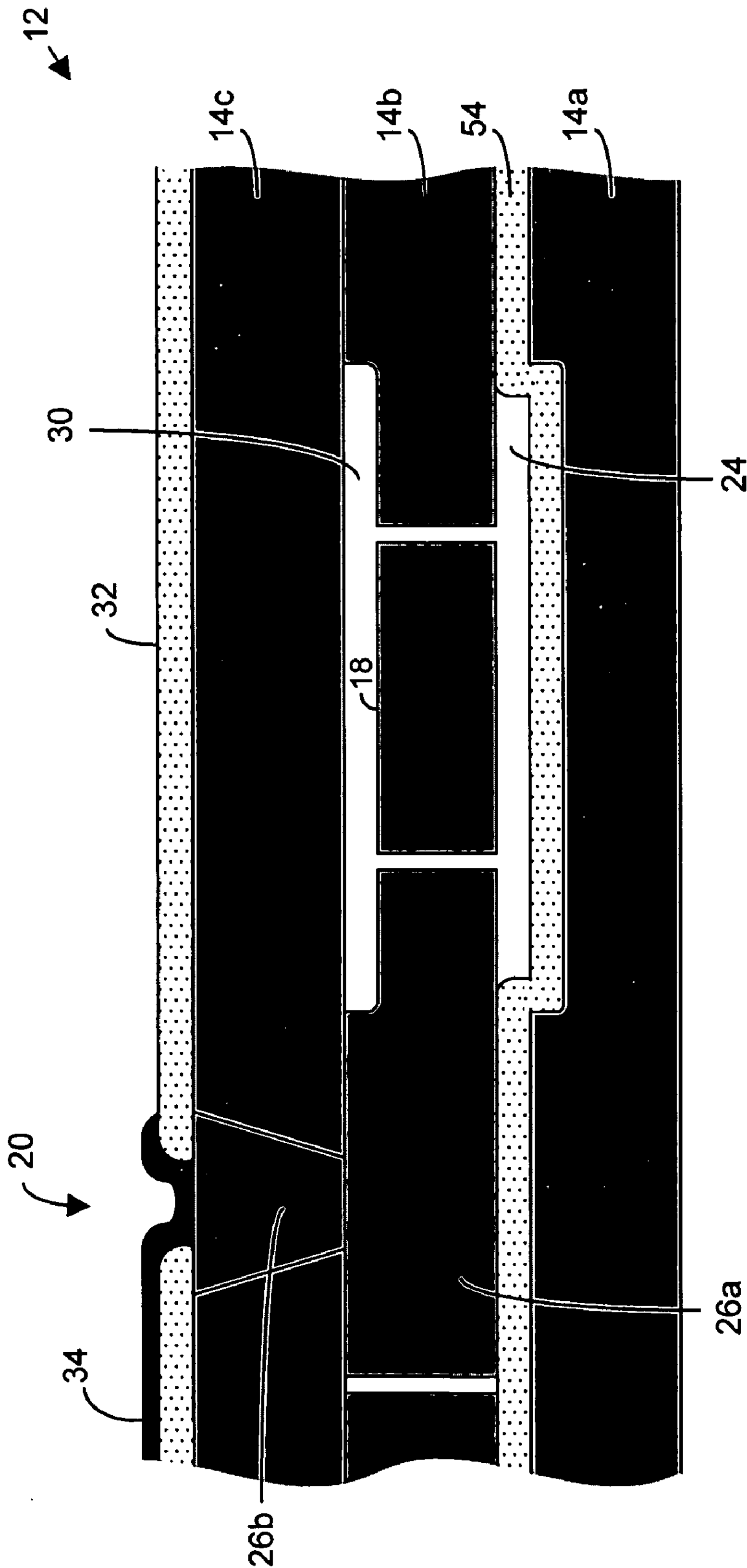


FIGURE 40

FIGURE 41A

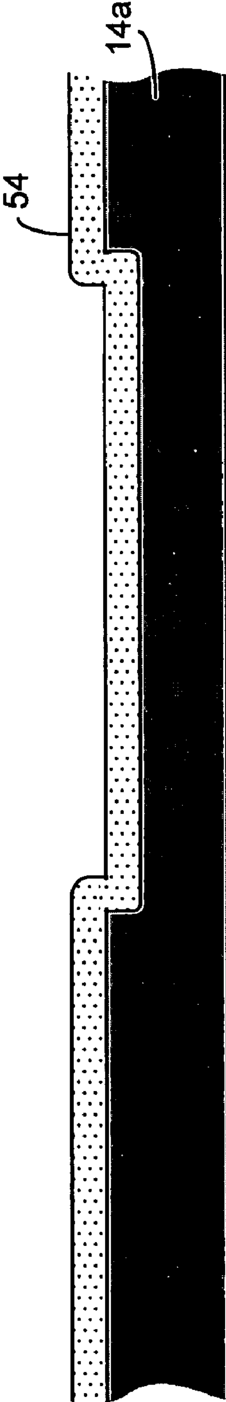


FIGURE 41B

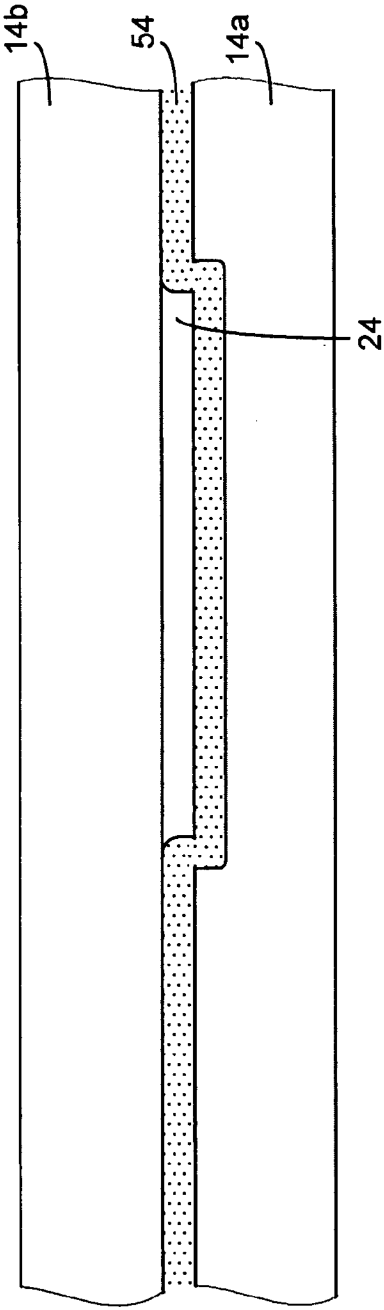


FIGURE 41C

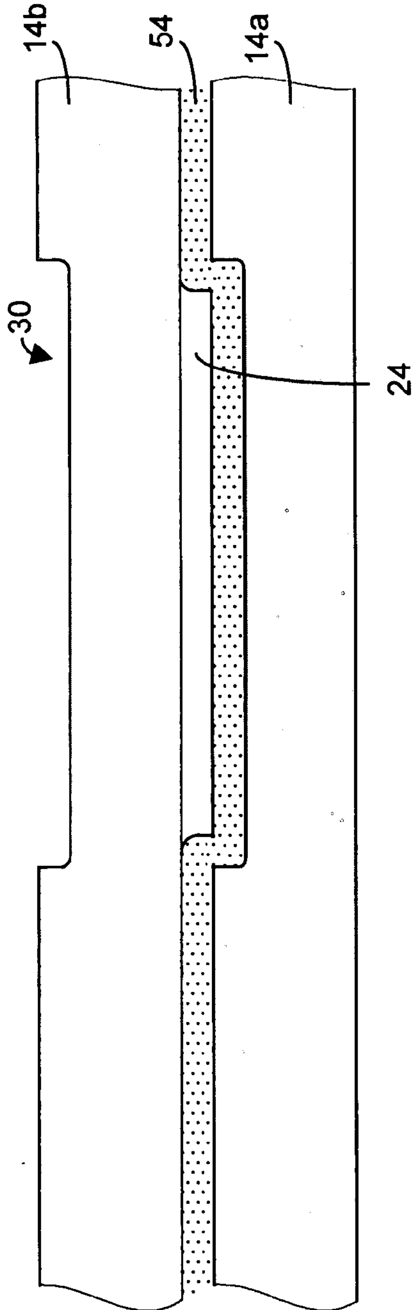


FIGURE 41D

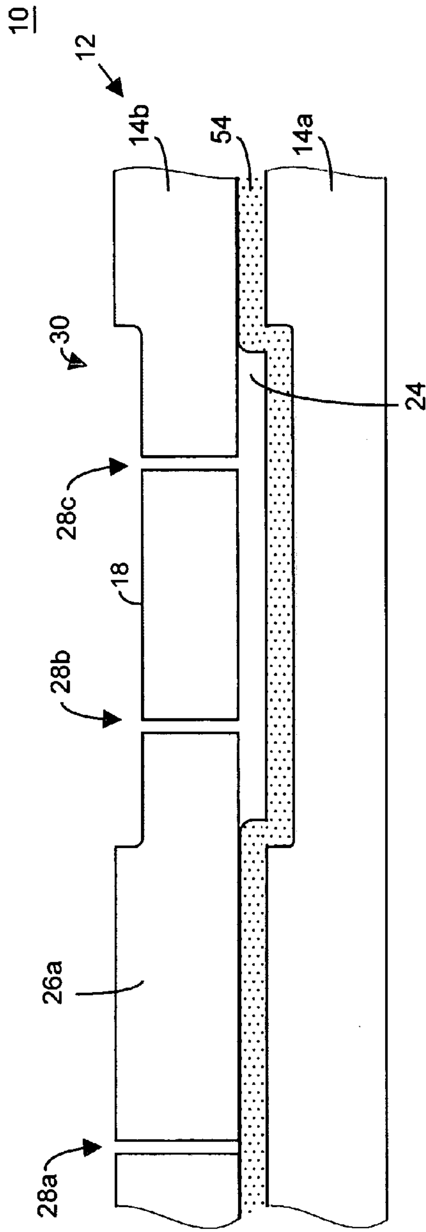


FIGURE 41E

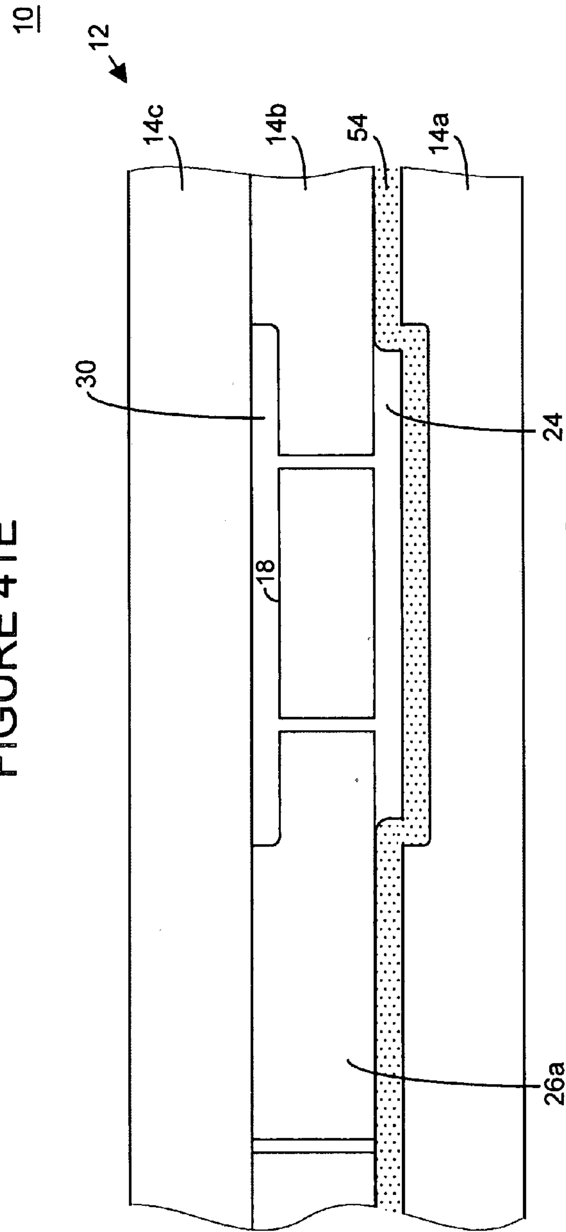


FIGURE 41F

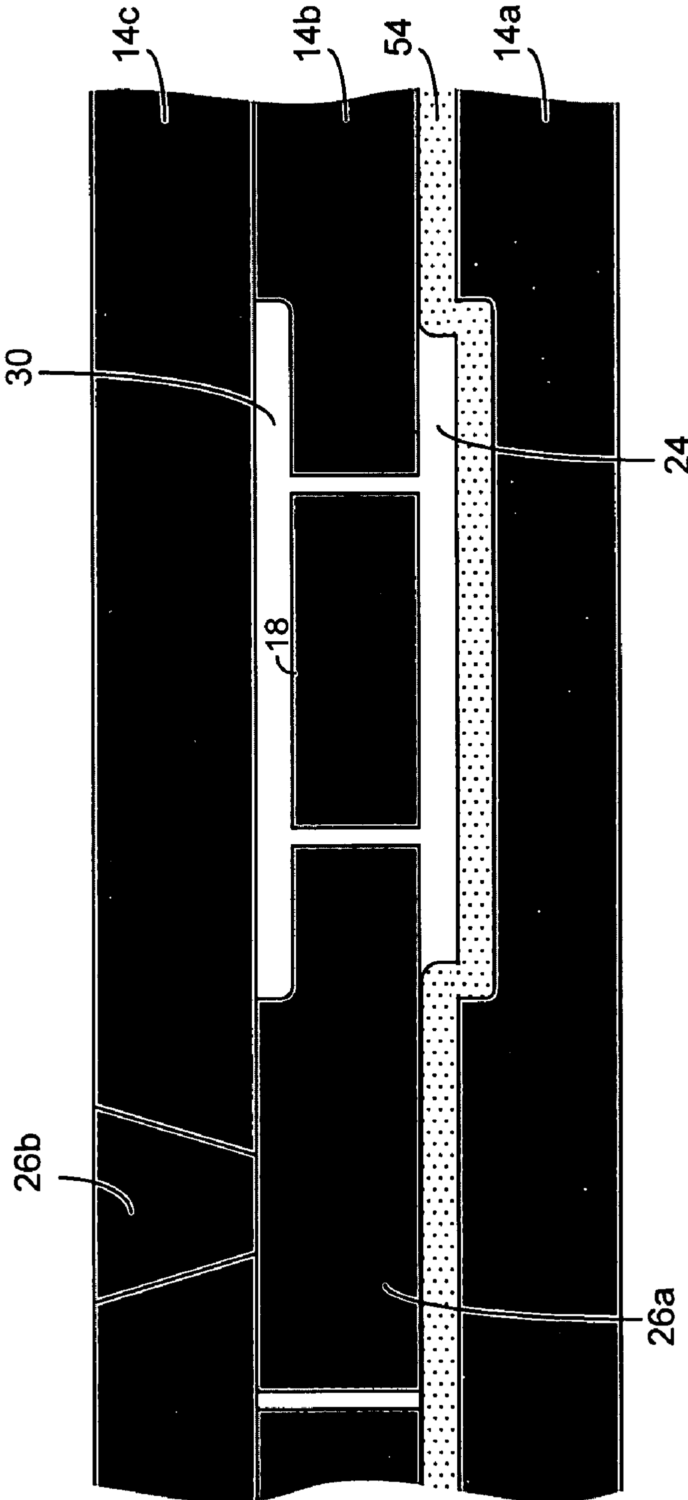


FIGURE 41G

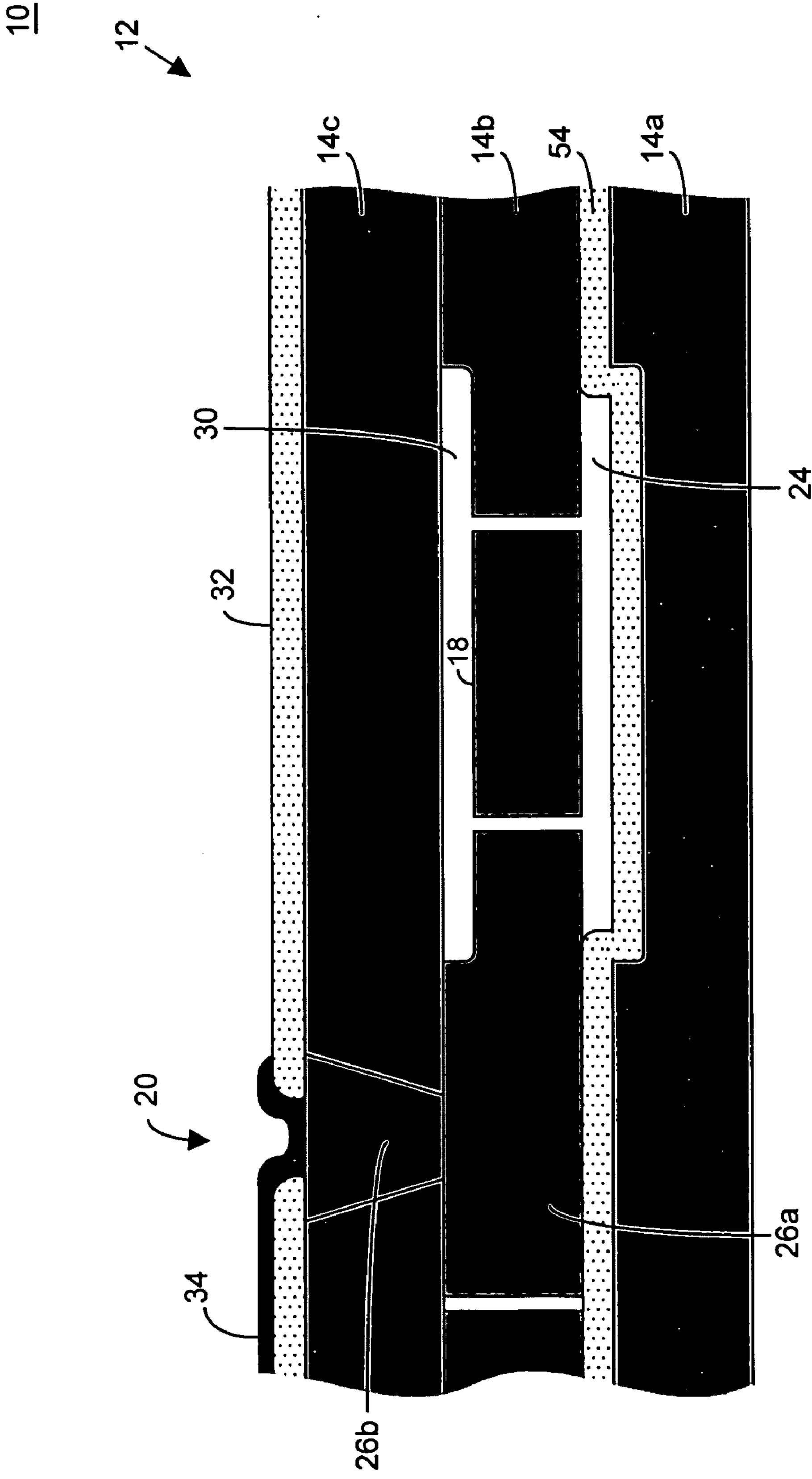


FIGURE 41H

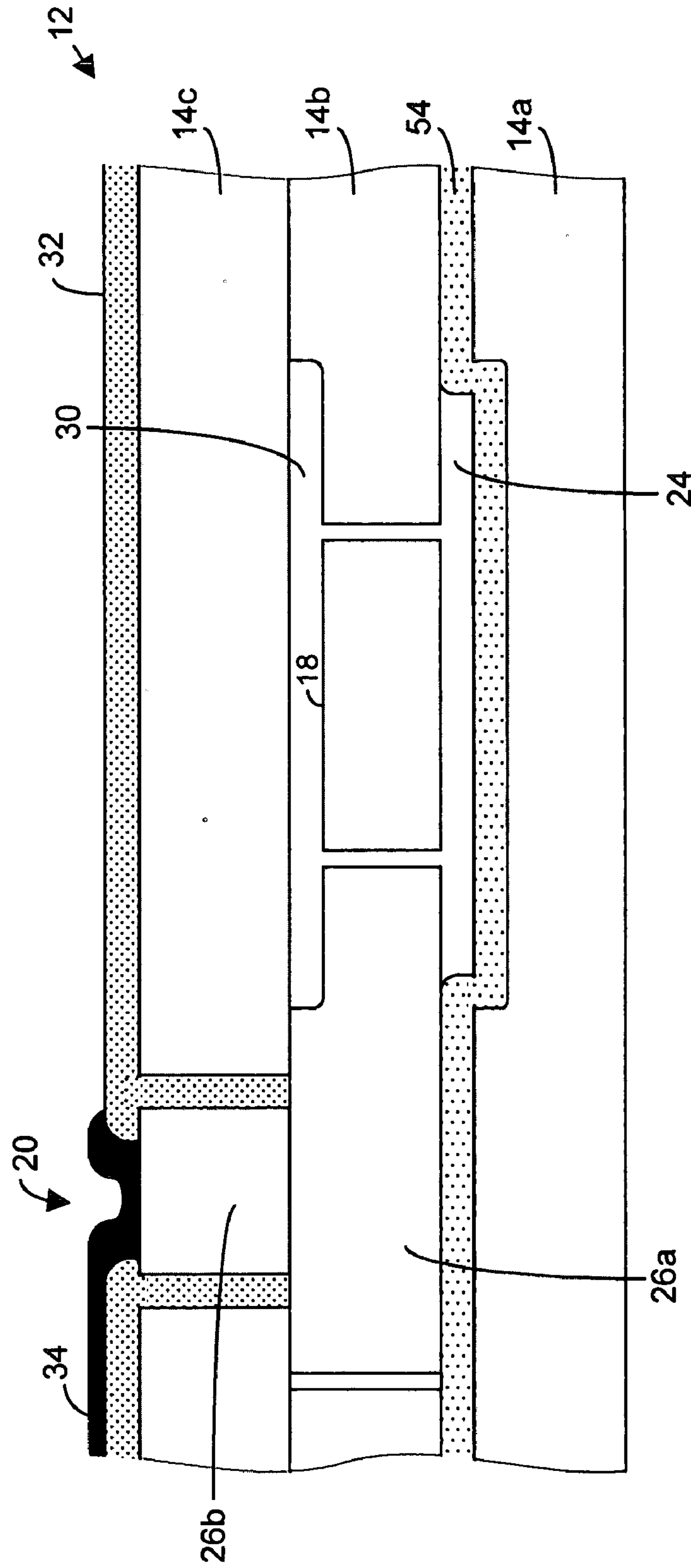


FIGURE 42A

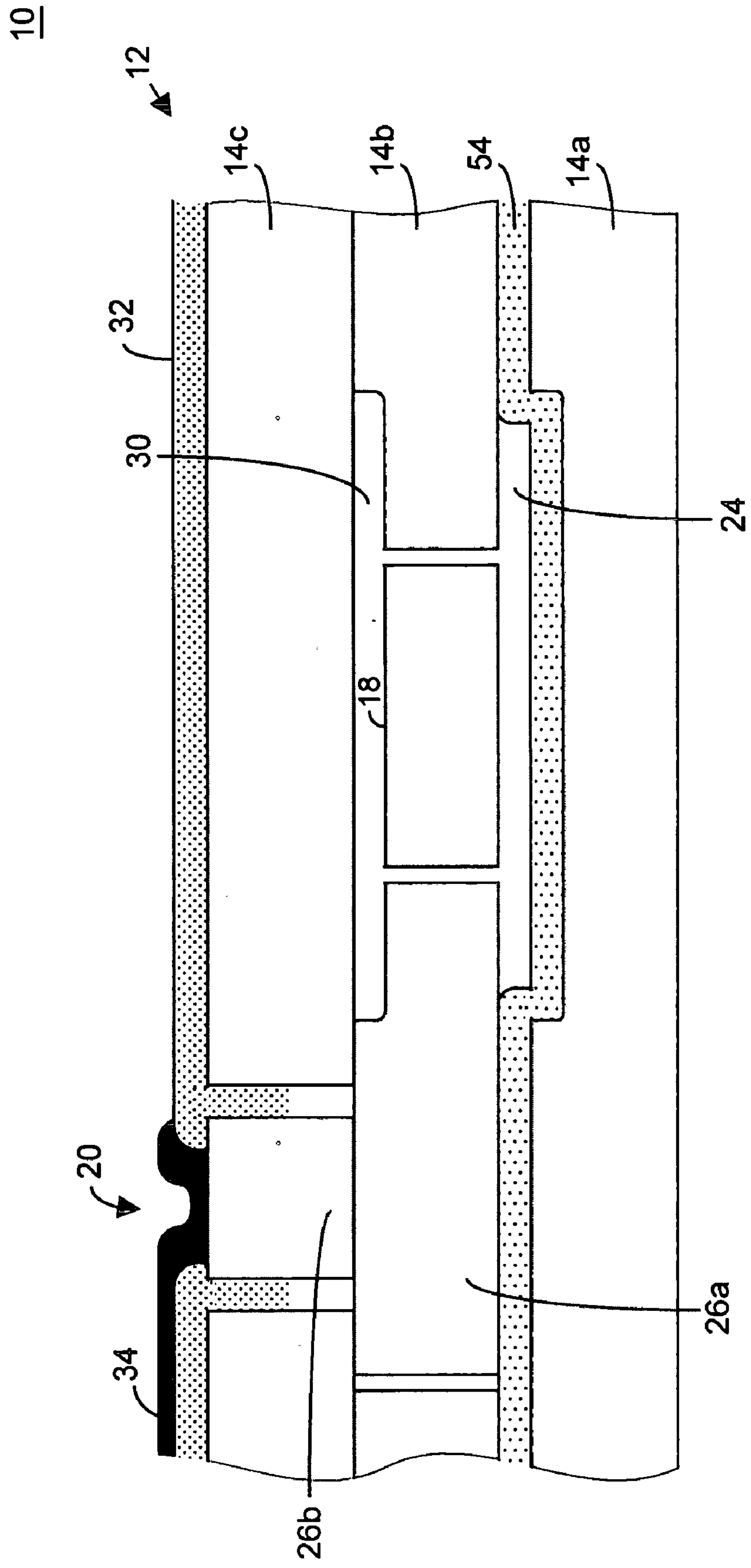


FIGURE 42B

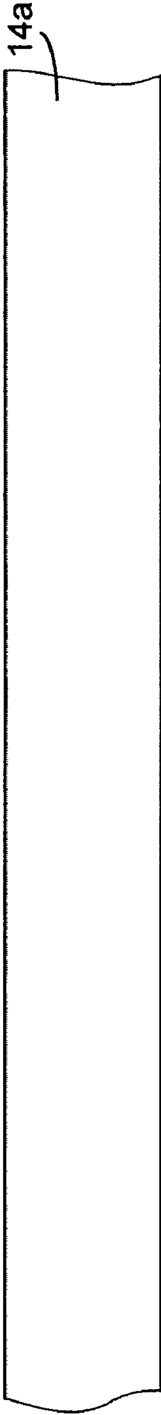


FIGURE 43A

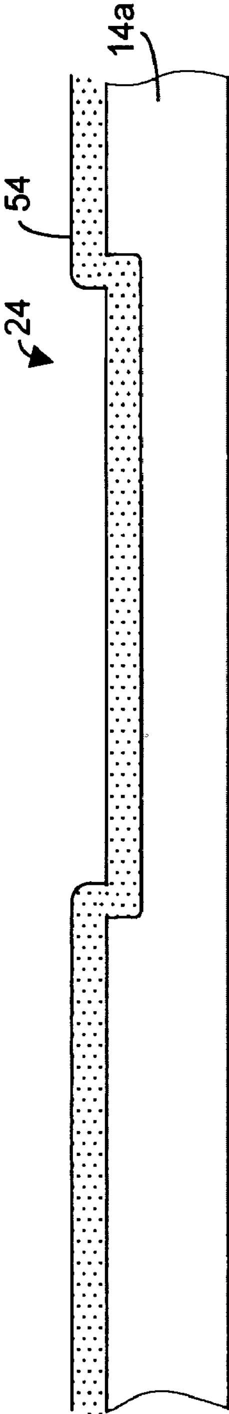


FIGURE 43B

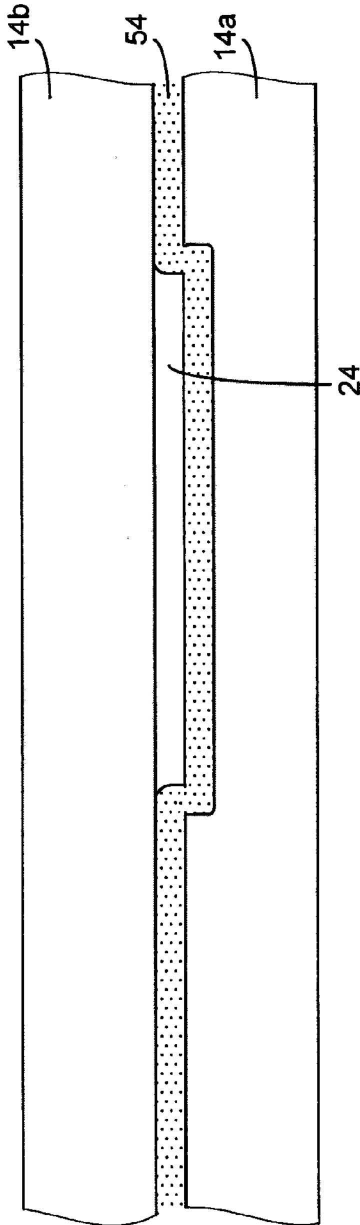


FIGURE 43C

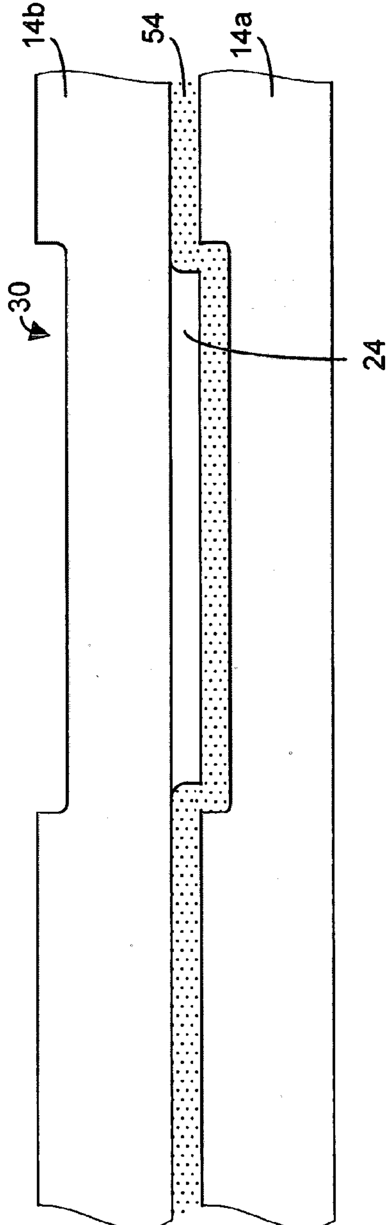


FIGURE 43D

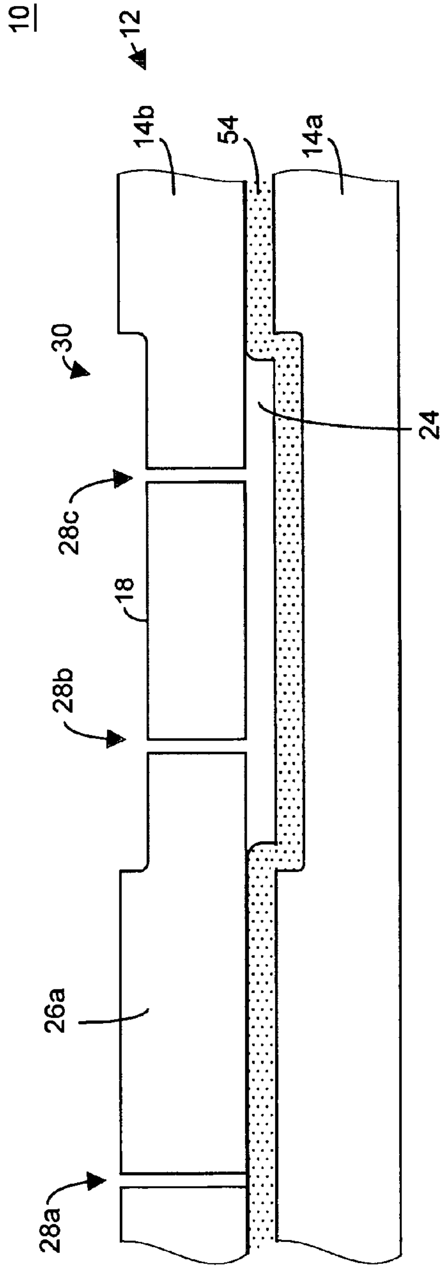


FIGURE 43E

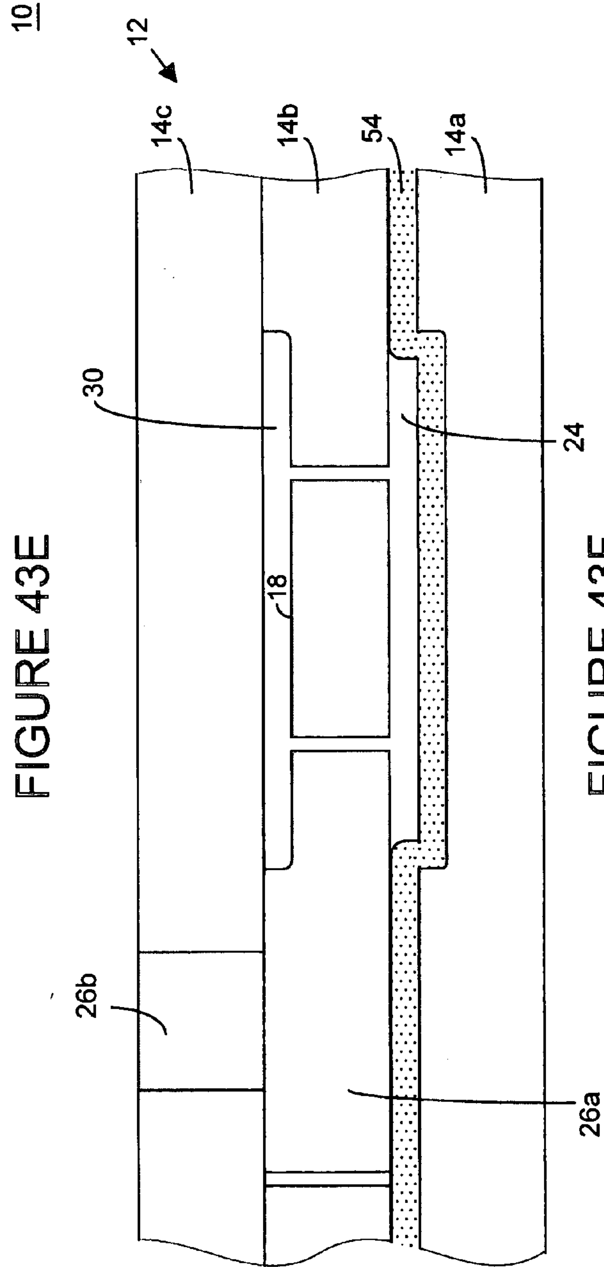


FIGURE 43F

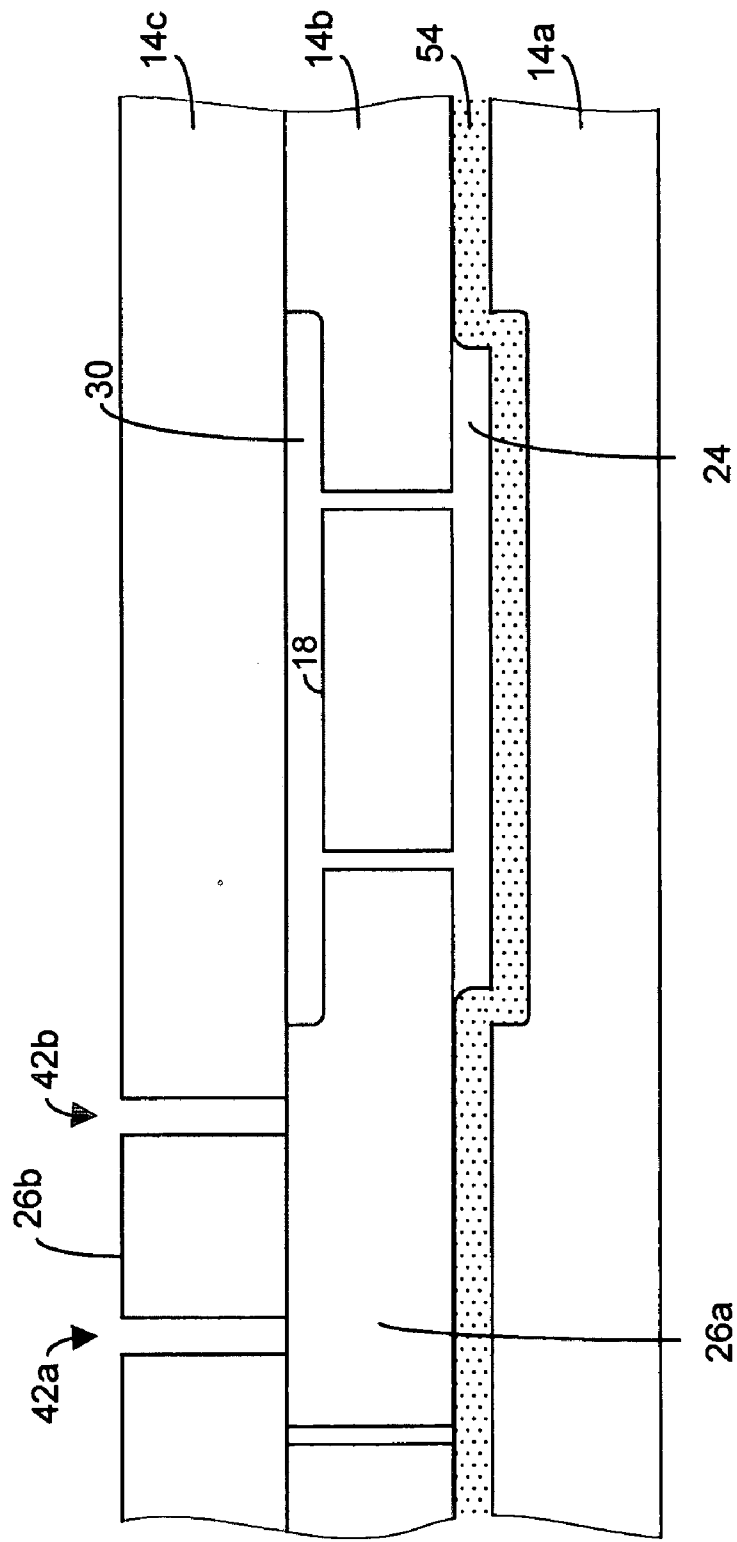


FIGURE 43G

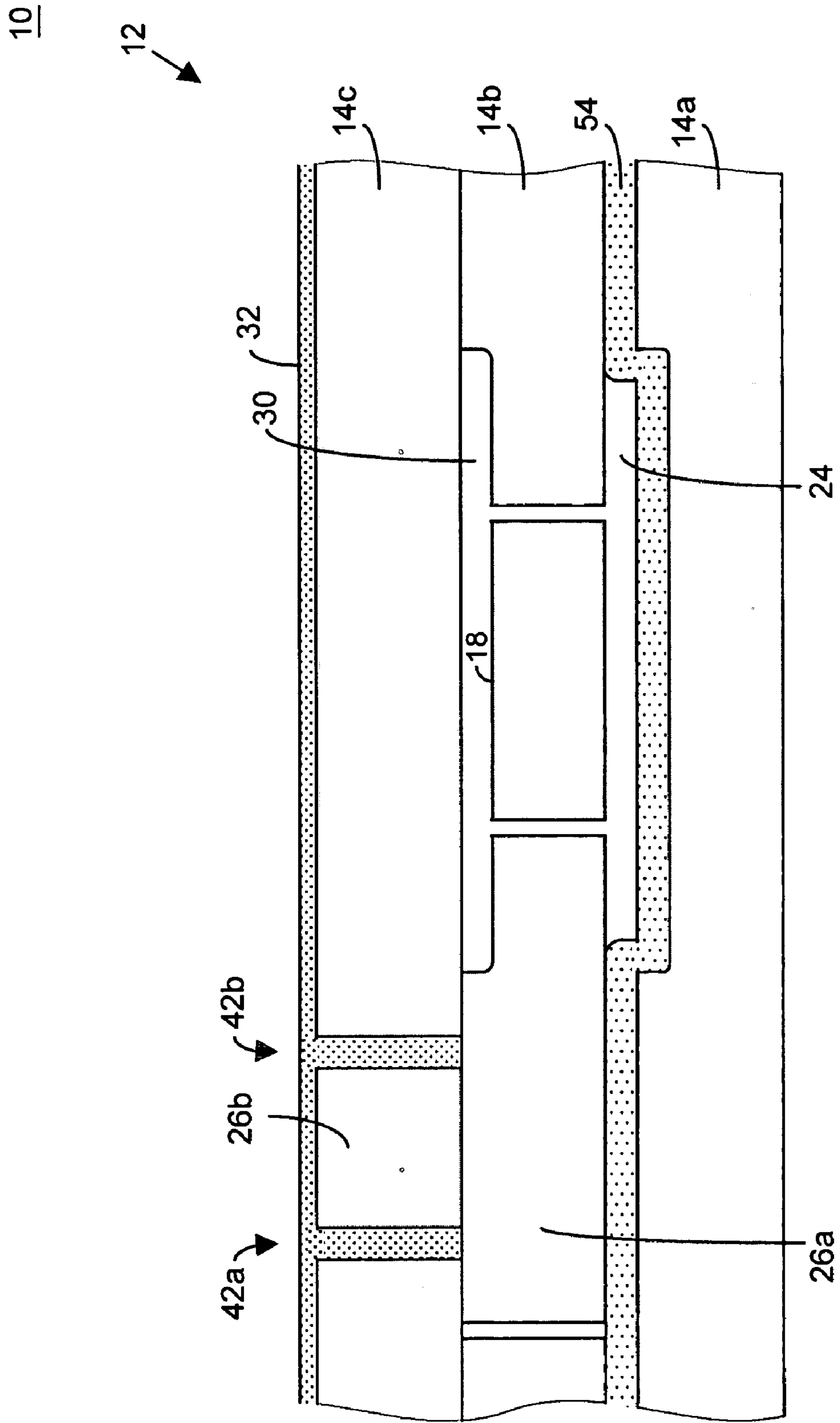


FIGURE 43H

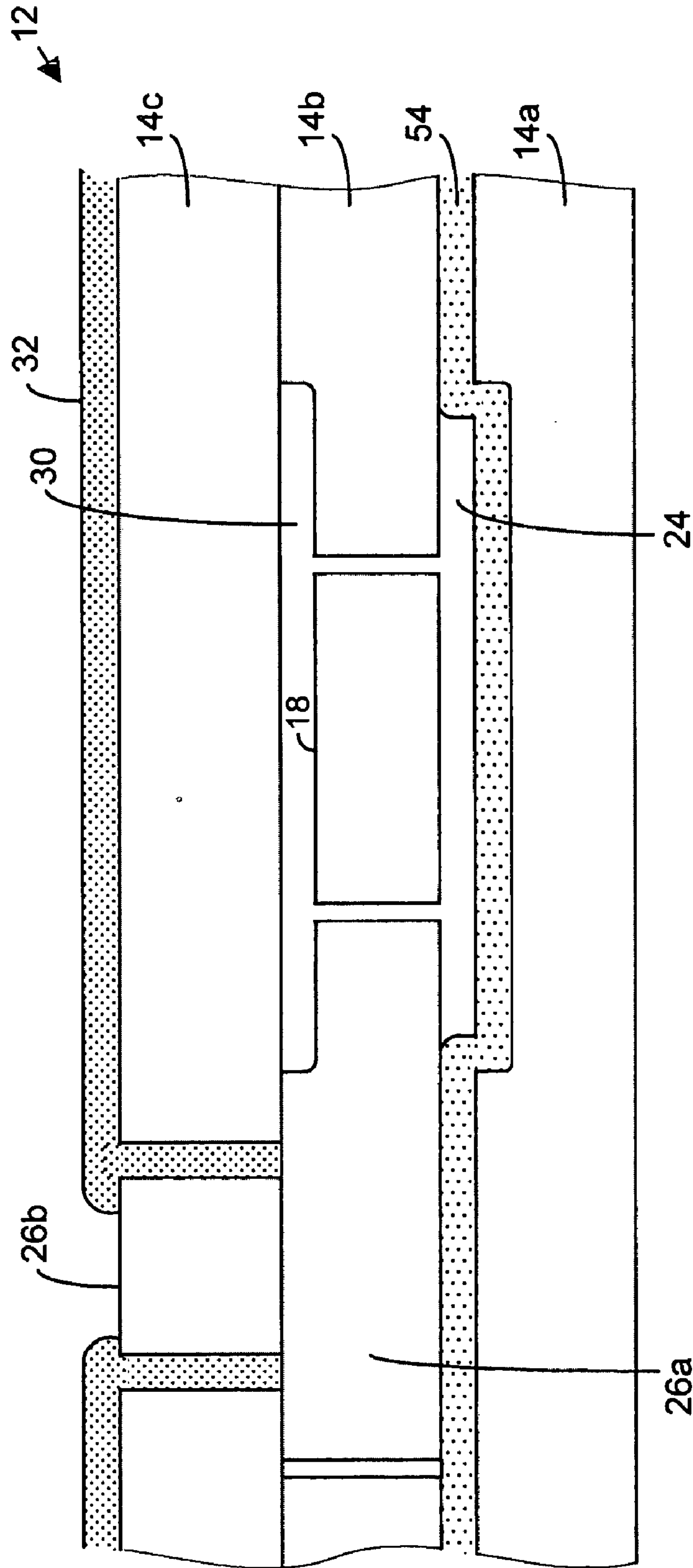


FIGURE 43I

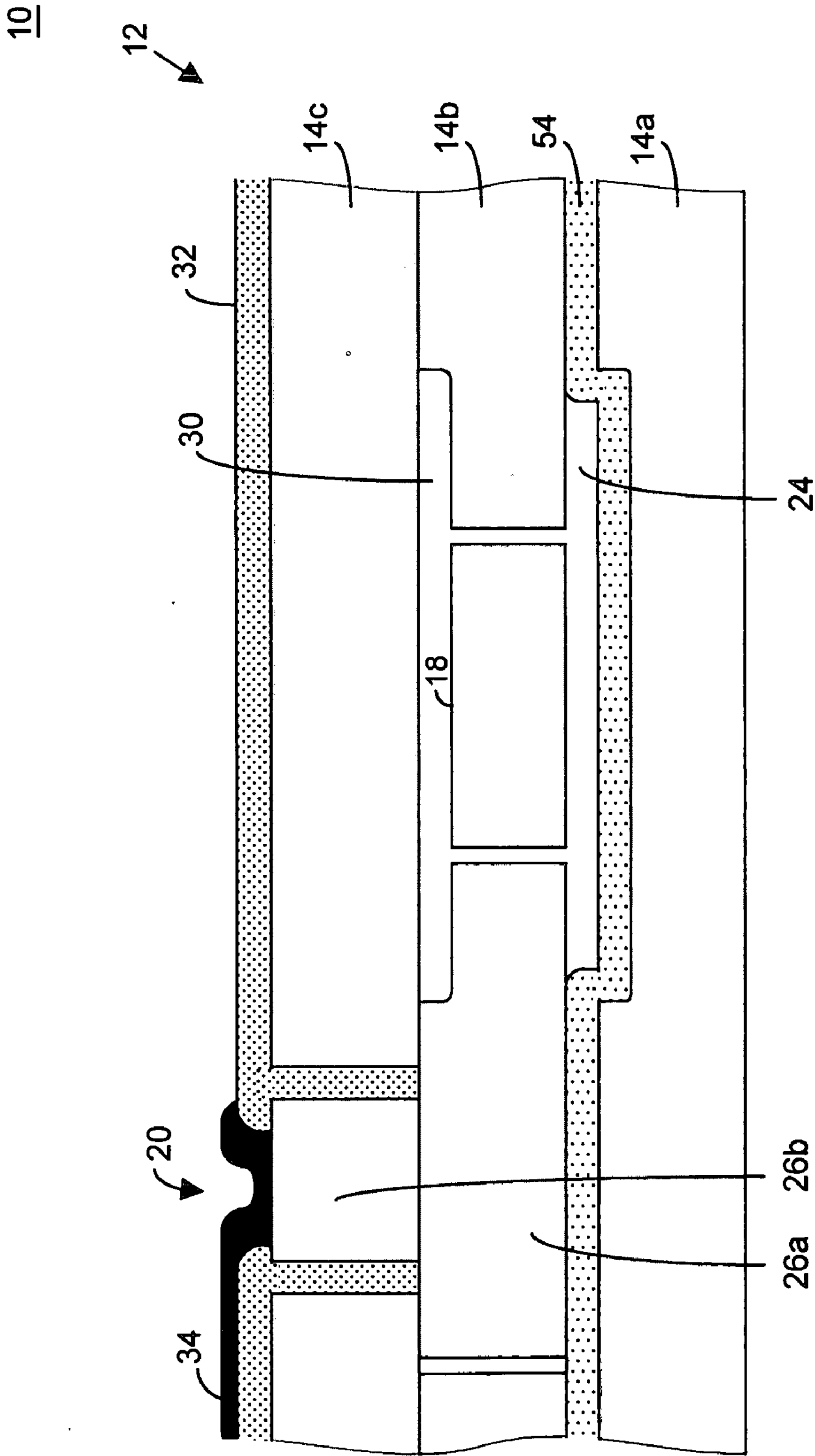


FIGURE 43J

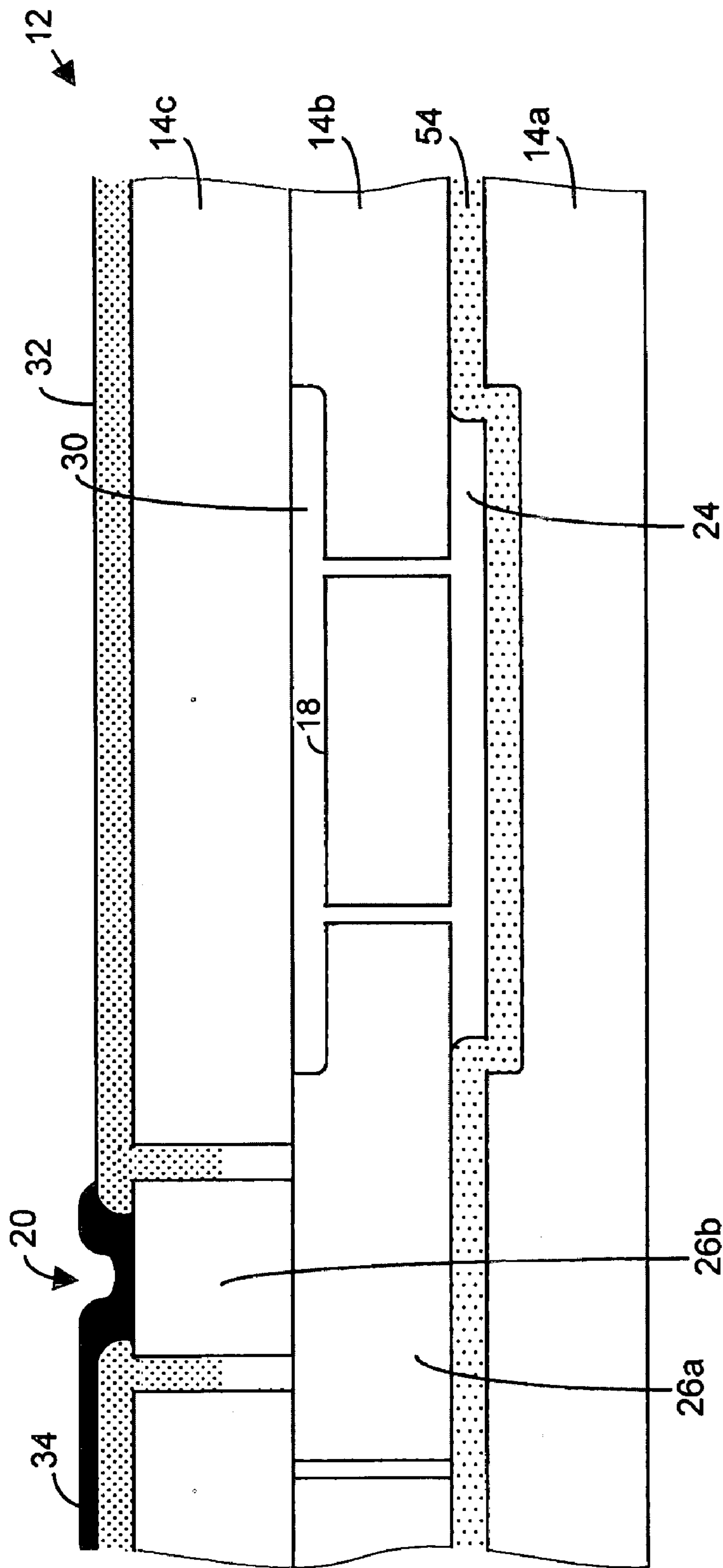


FIGURE 43K

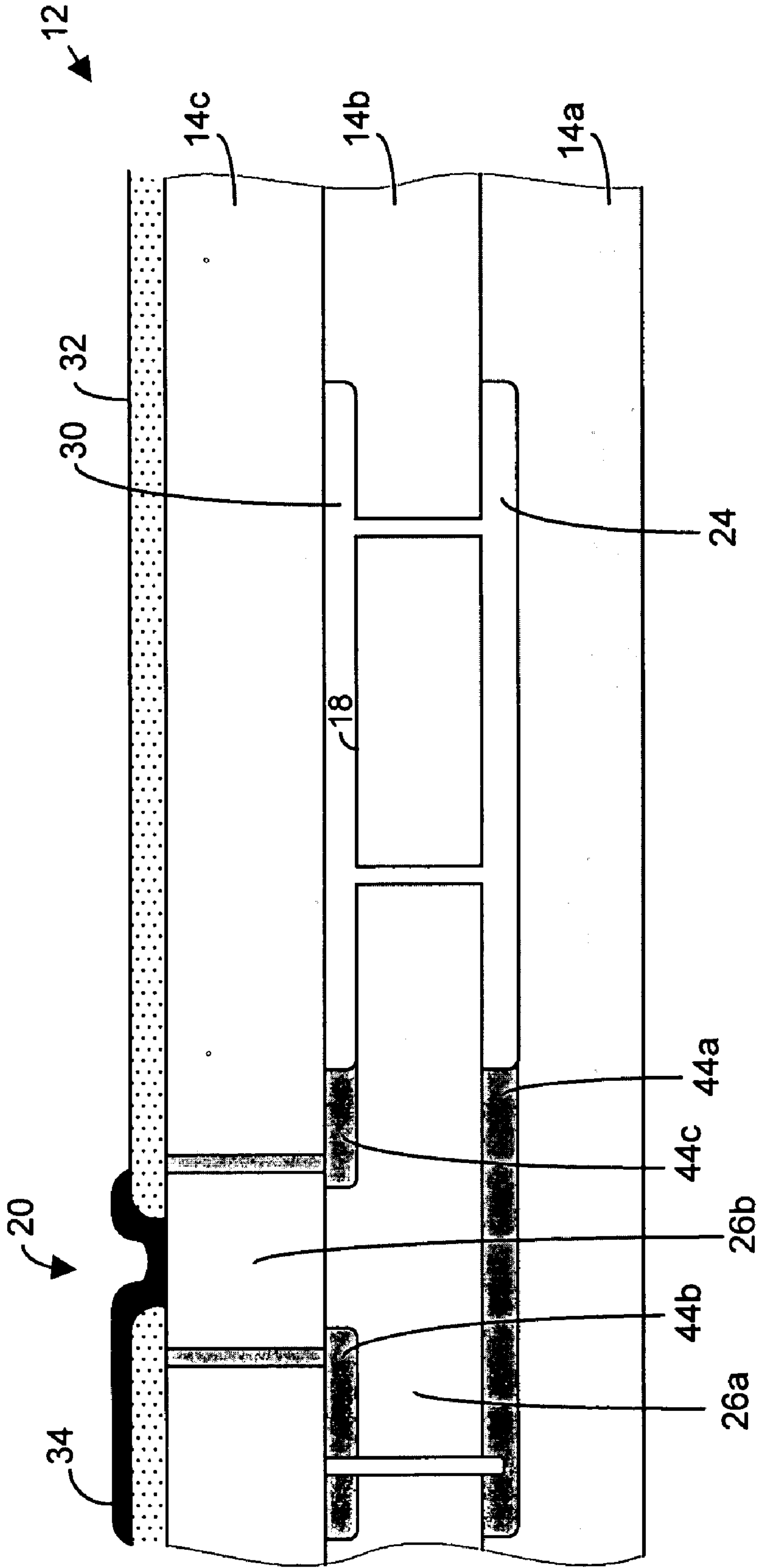


FIGURE 44

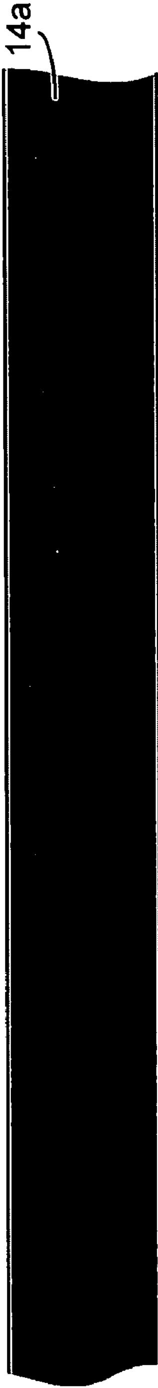


FIGURE 45A

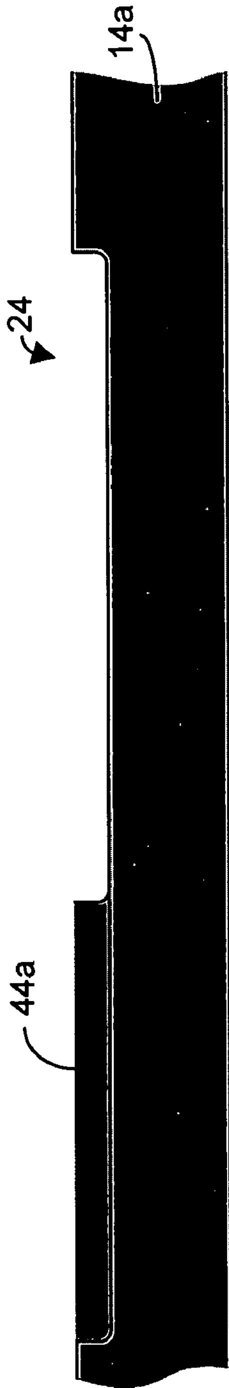


FIGURE 45B

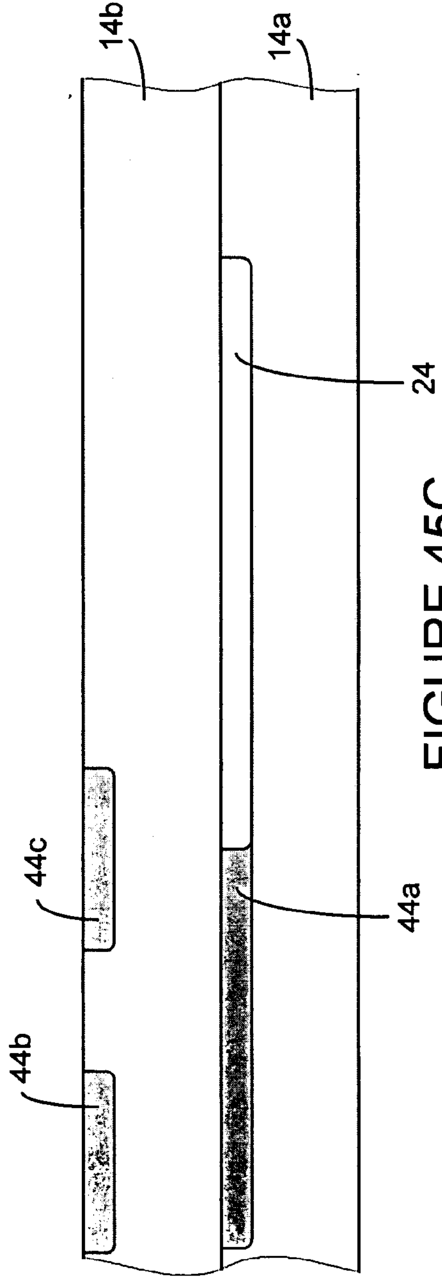


FIGURE 45C

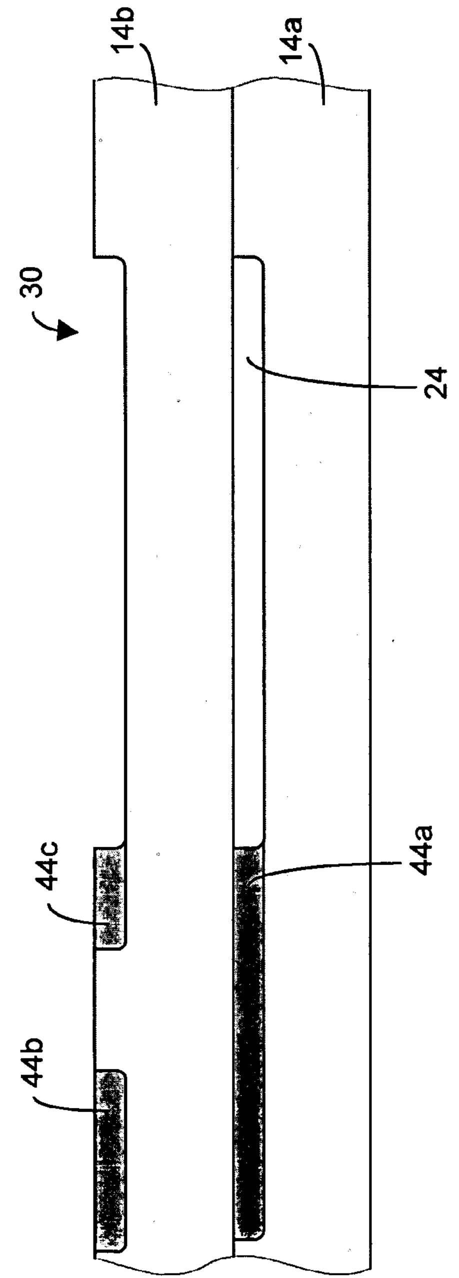


FIGURE 45D

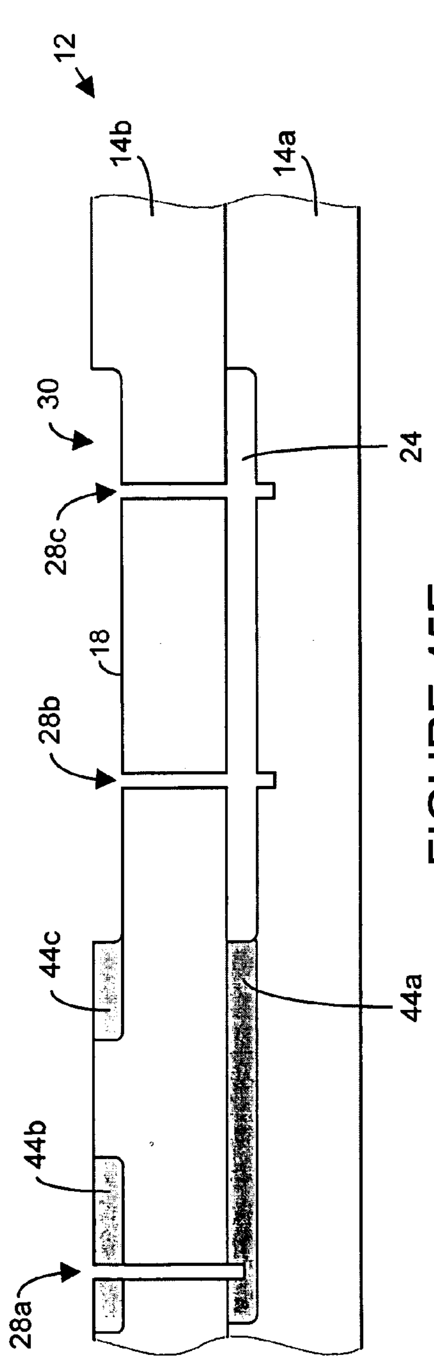


FIGURE 45E

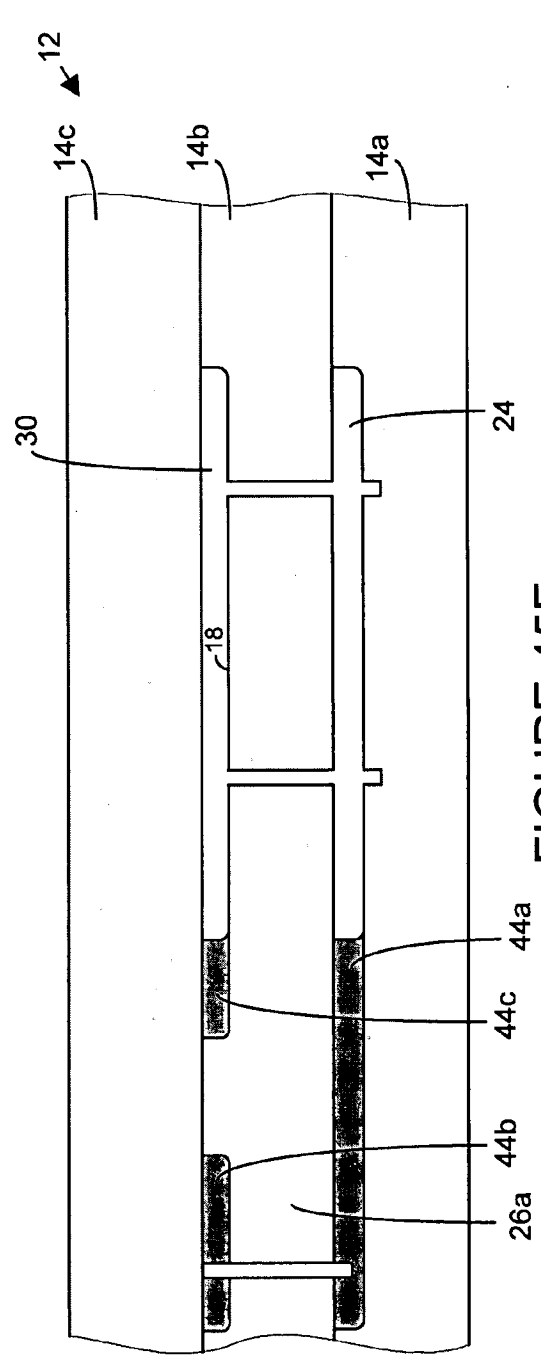


FIGURE 45F

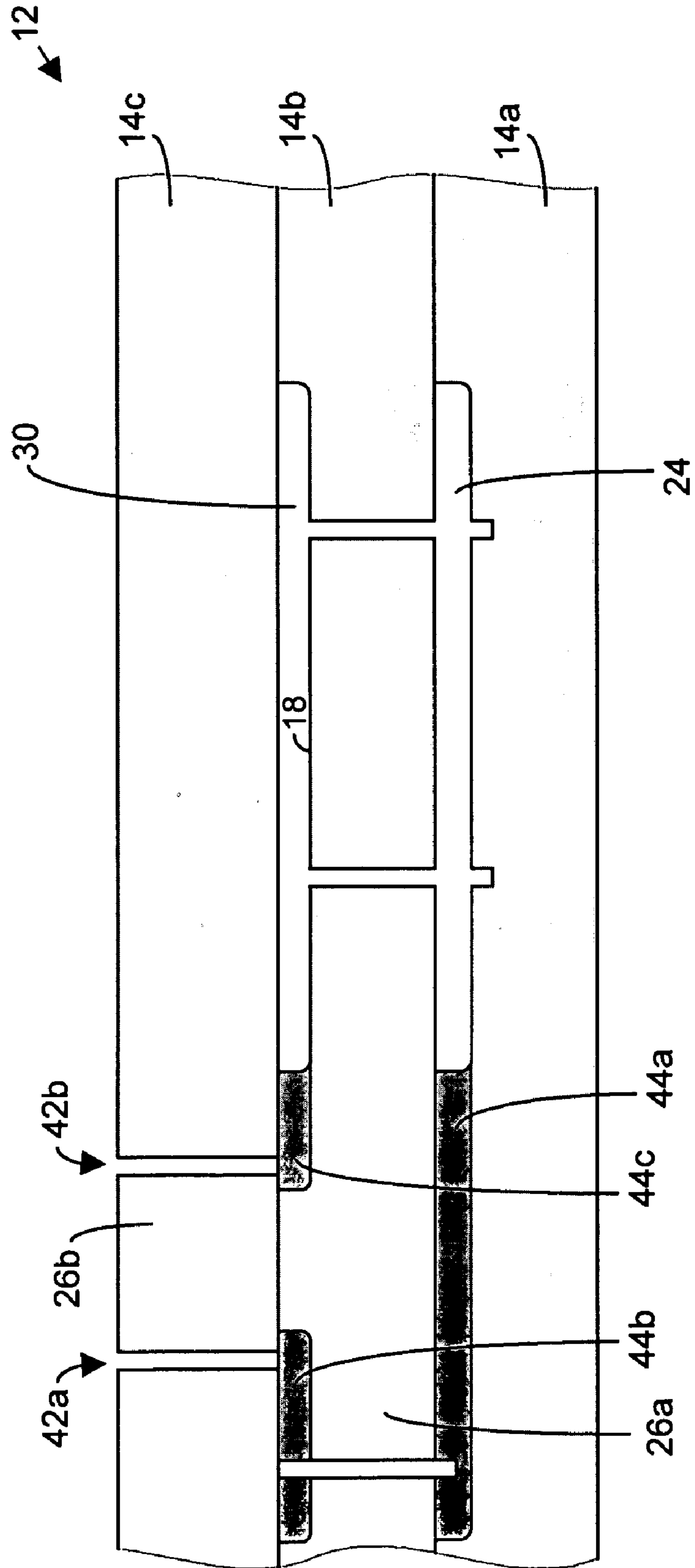


FIGURE 45G

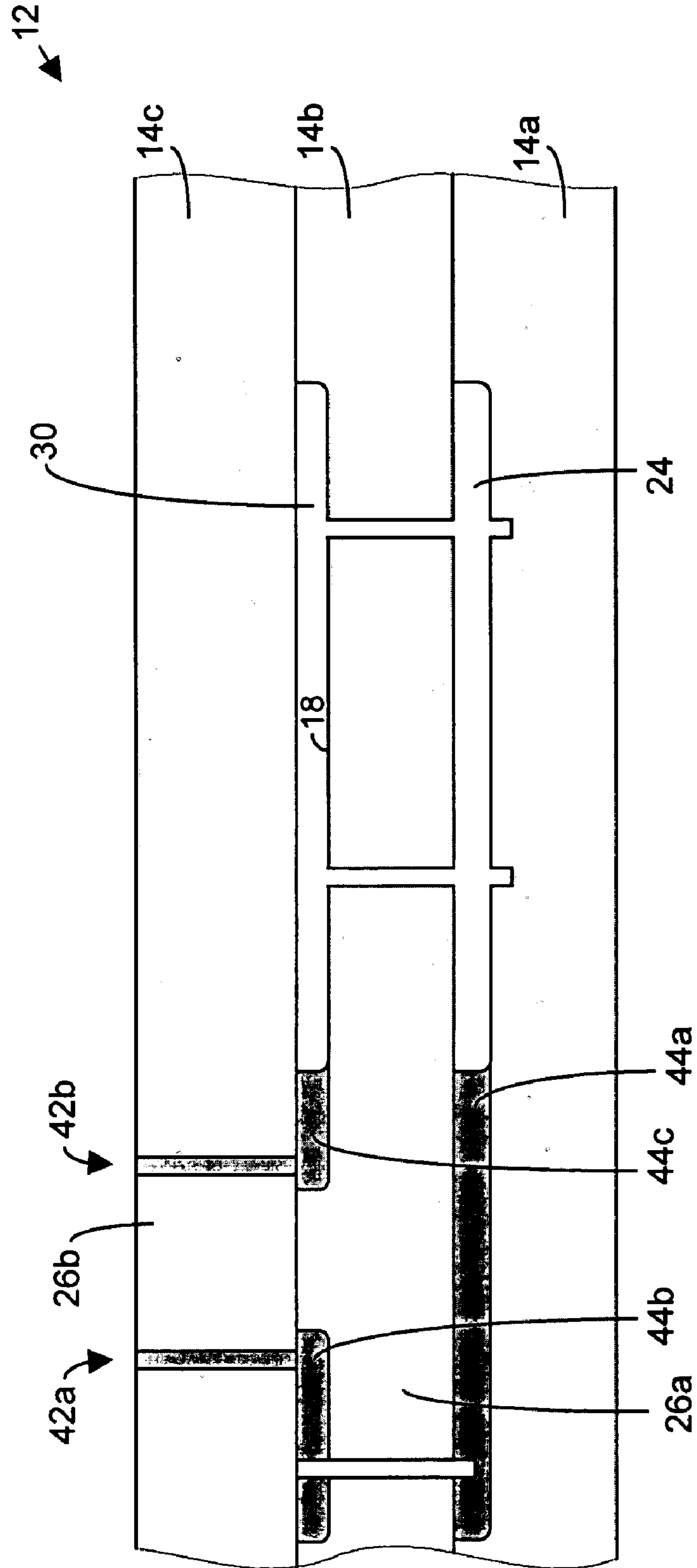


FIGURE 45H

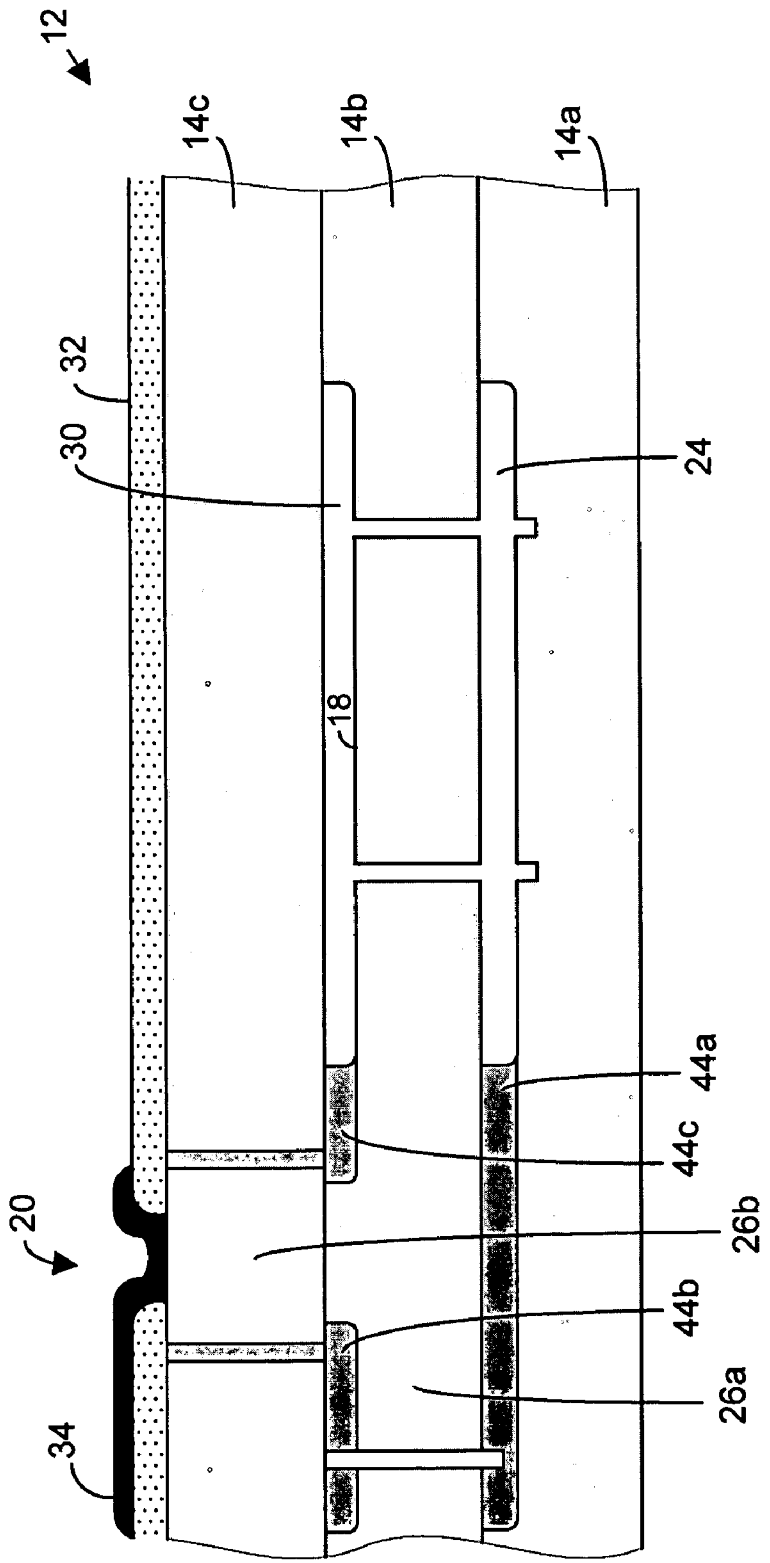


FIGURE 45I

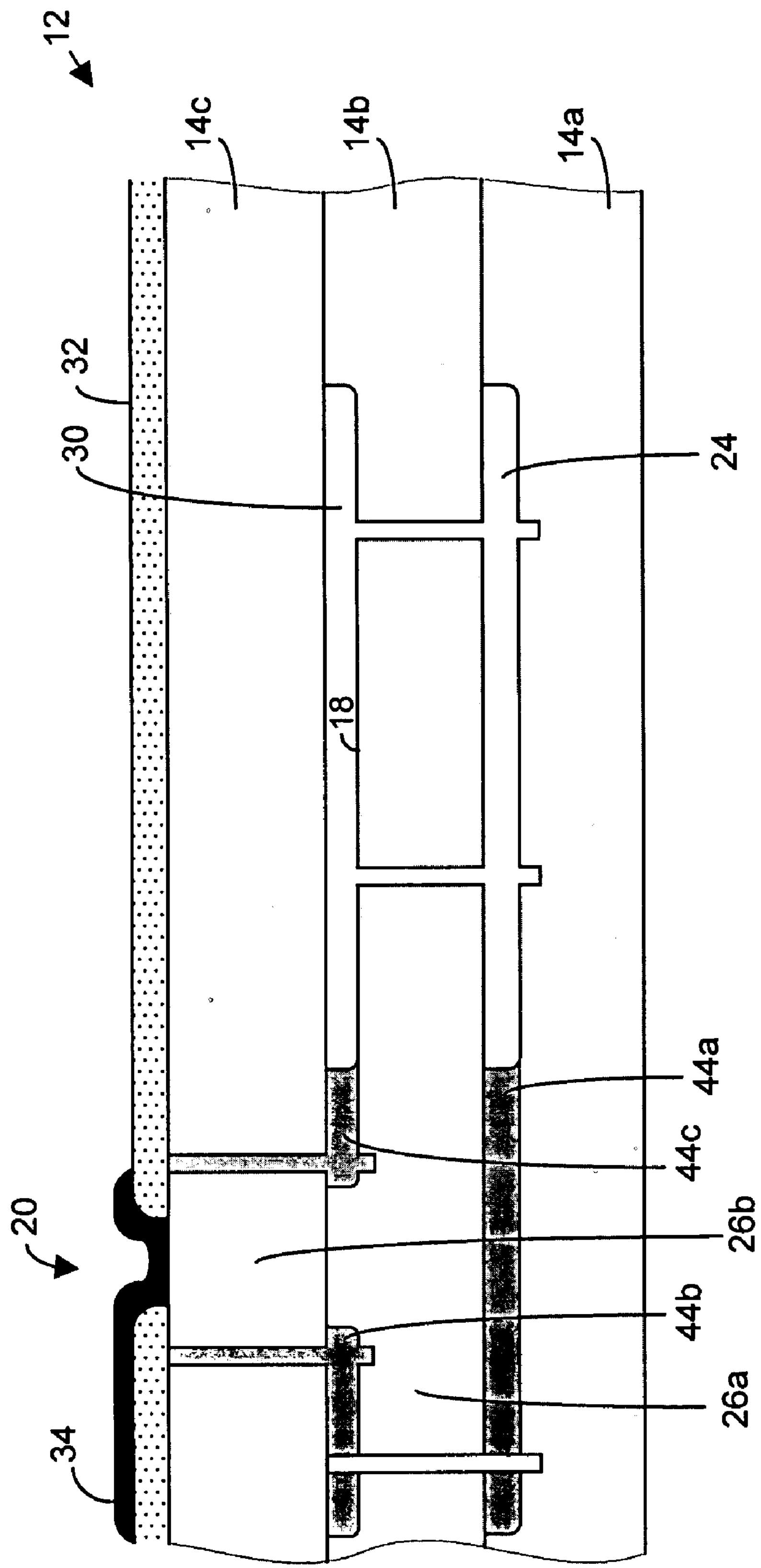


FIGURE 46A

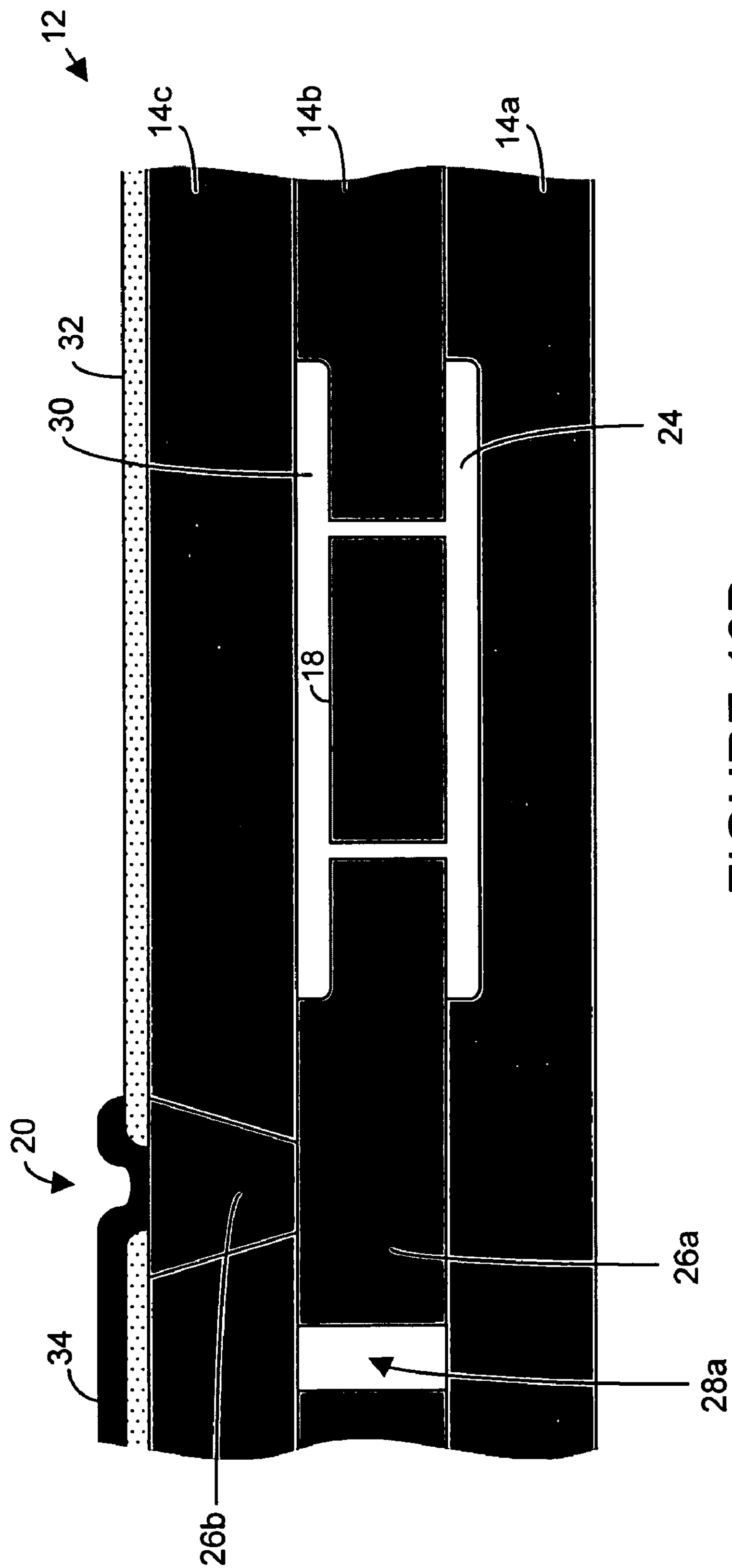


FIGURE 46B

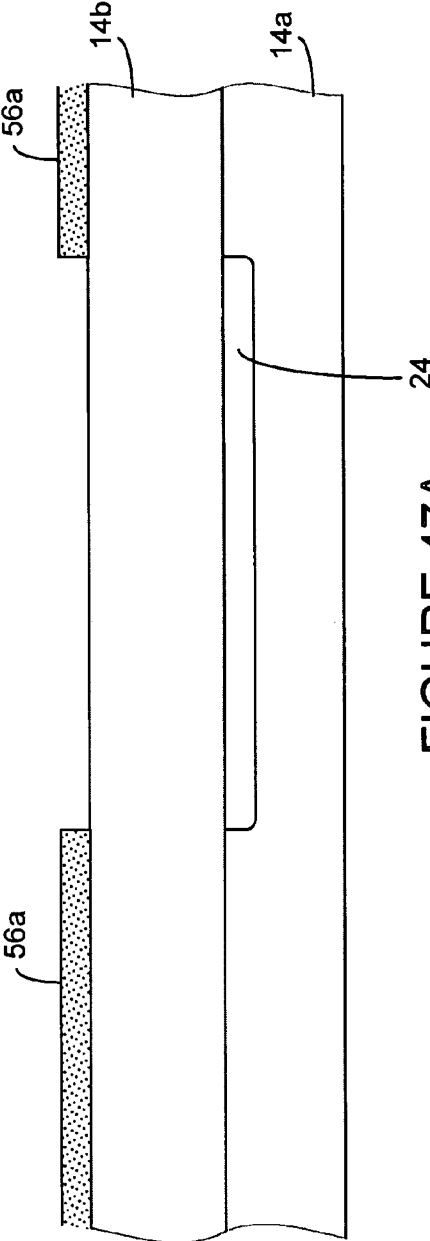


FIGURE 47A

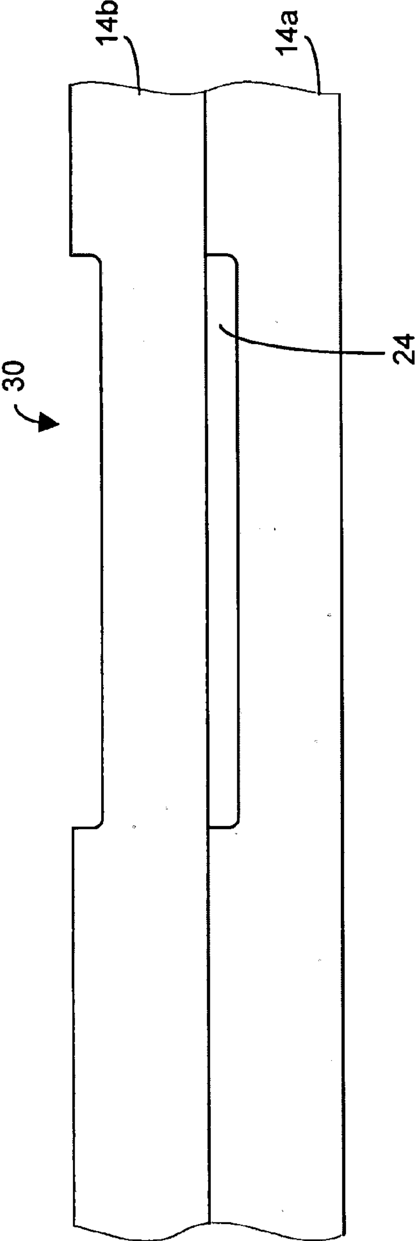


FIGURE 47B

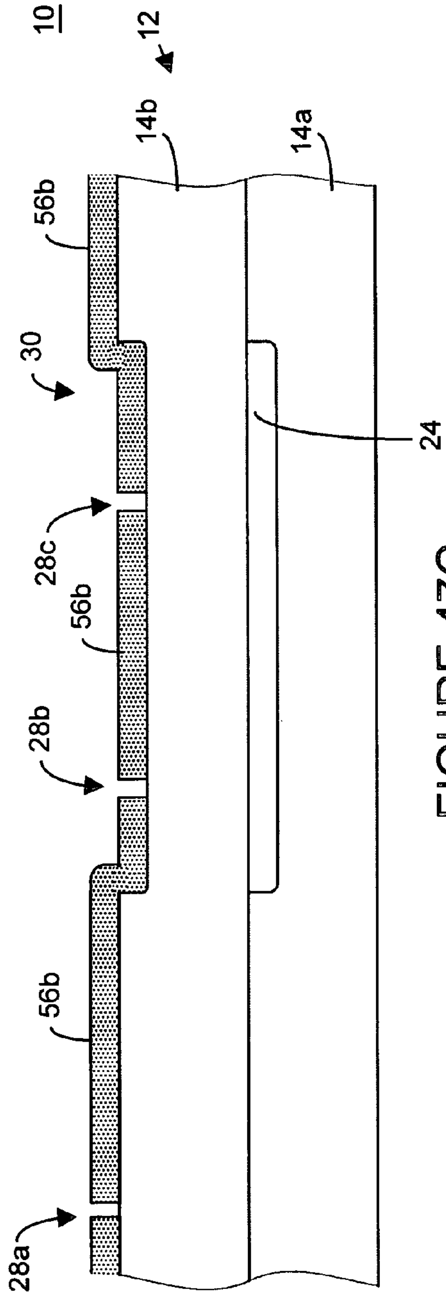


FIGURE 47C

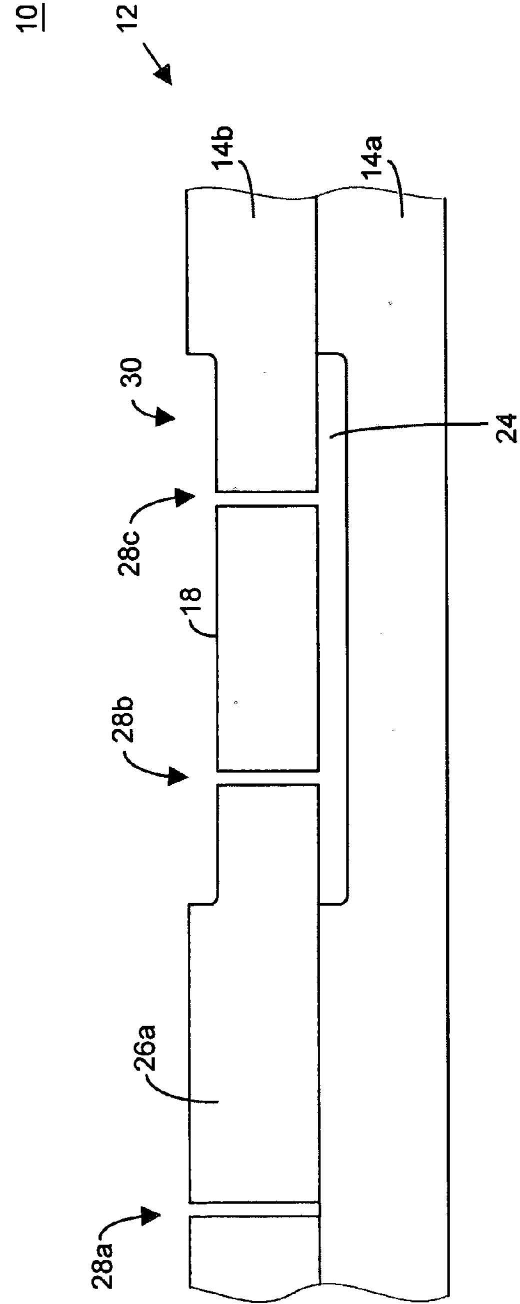


FIGURE 47D

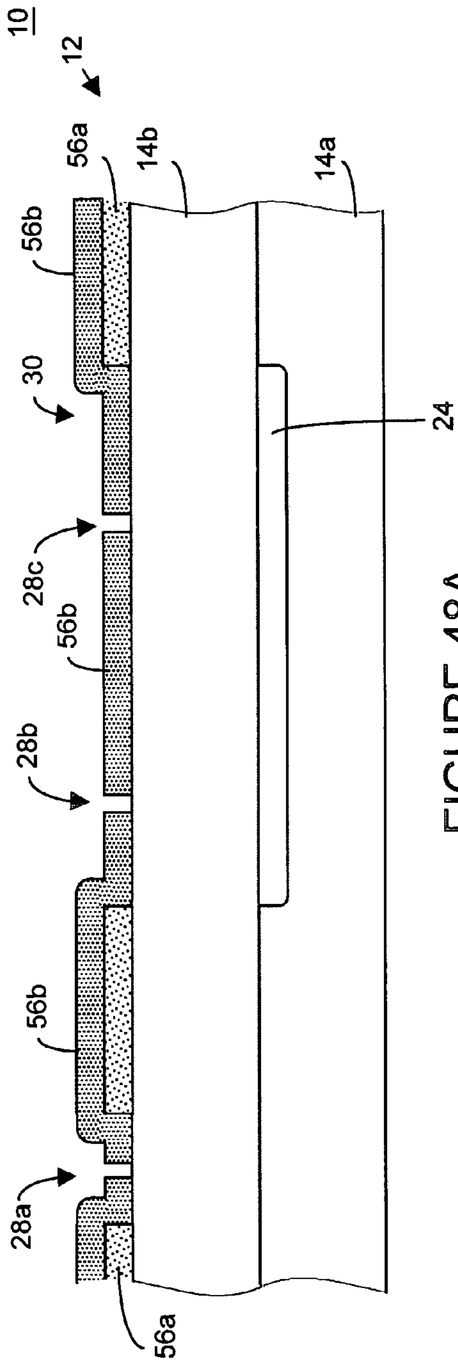


FIGURE 48A

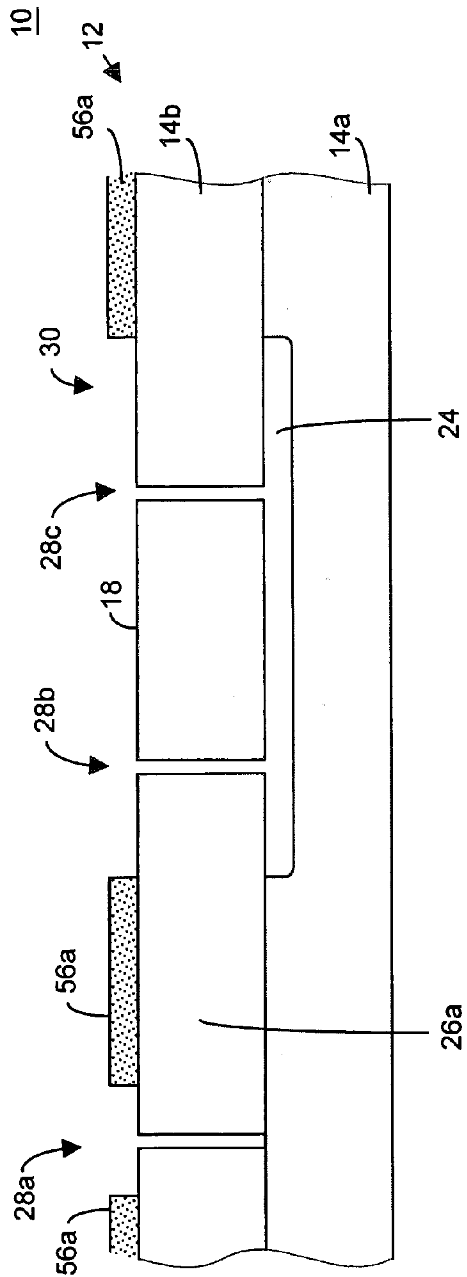


FIGURE 48B

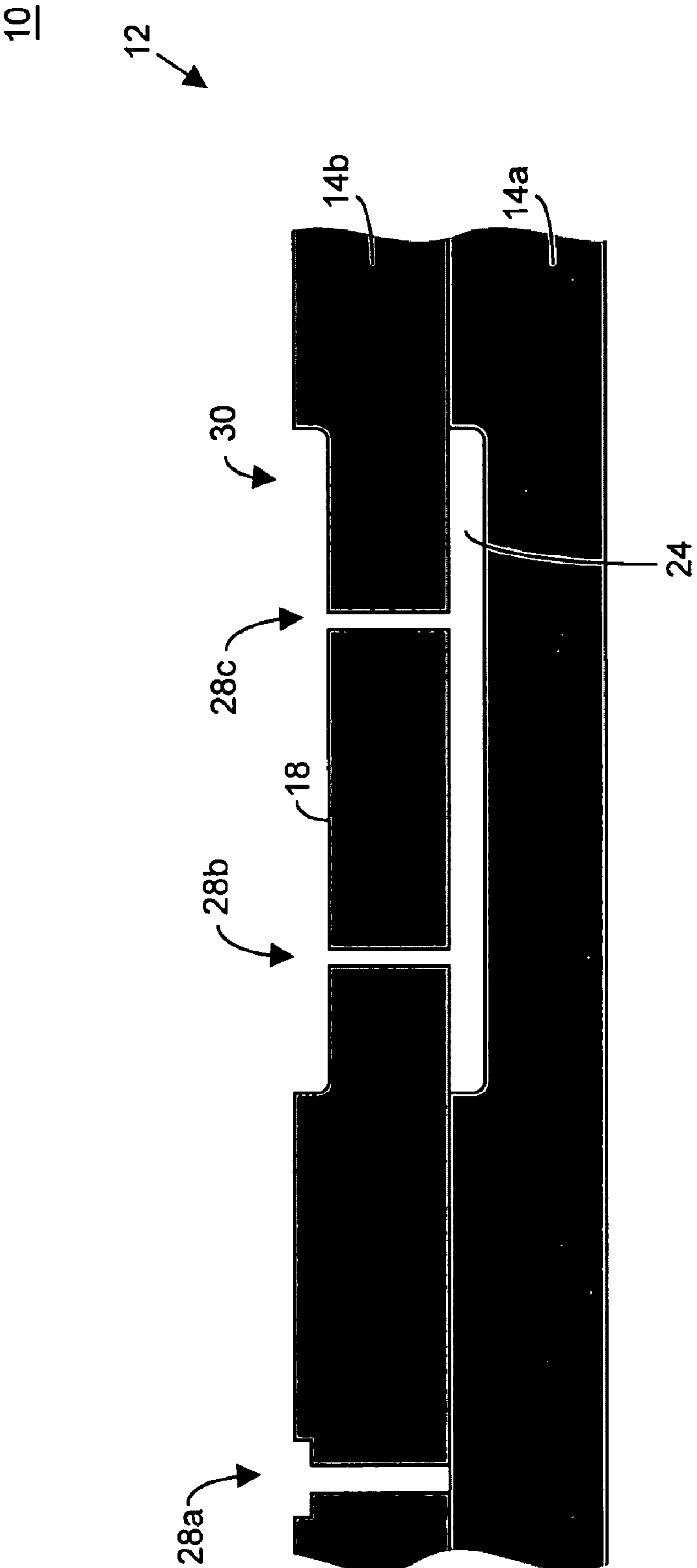


FIGURE 48C

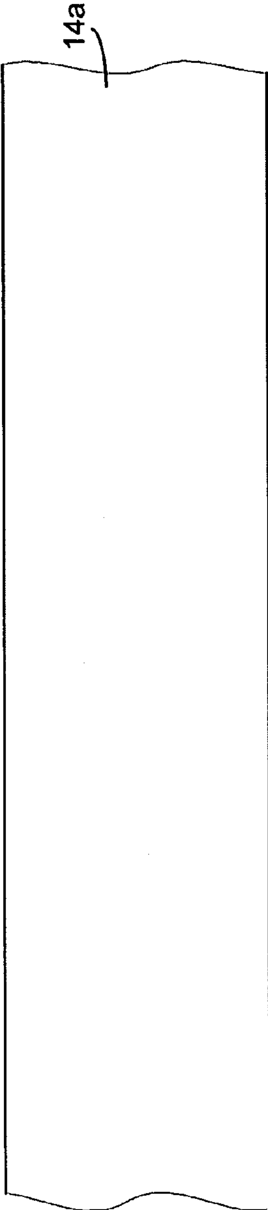


FIGURE 49A

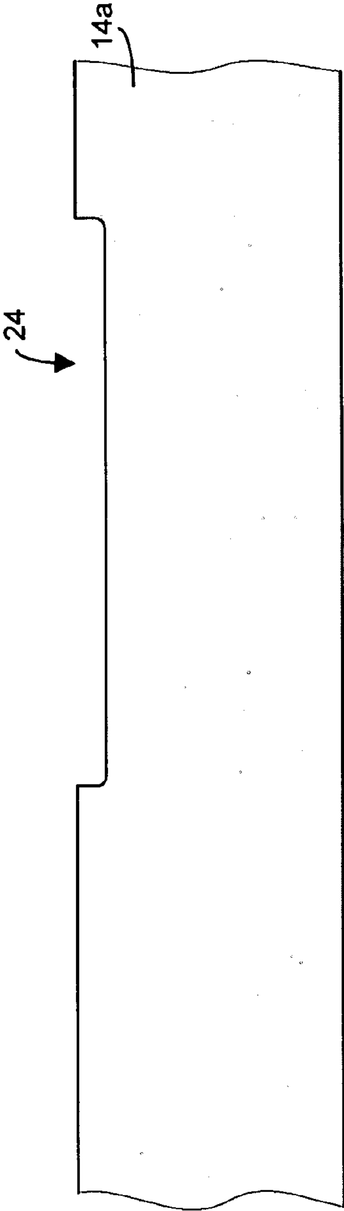


FIGURE 49B

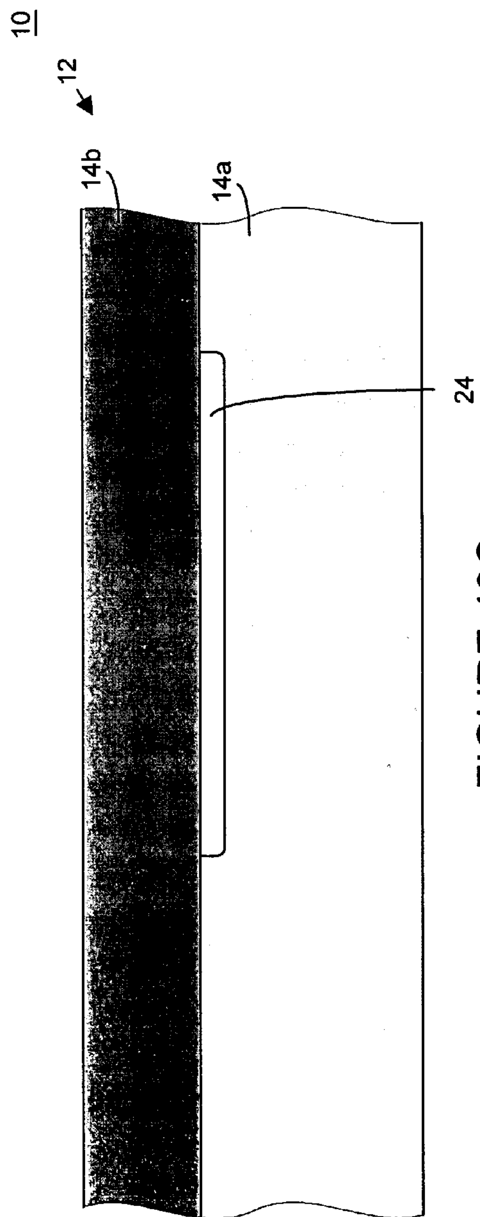


FIGURE 49C

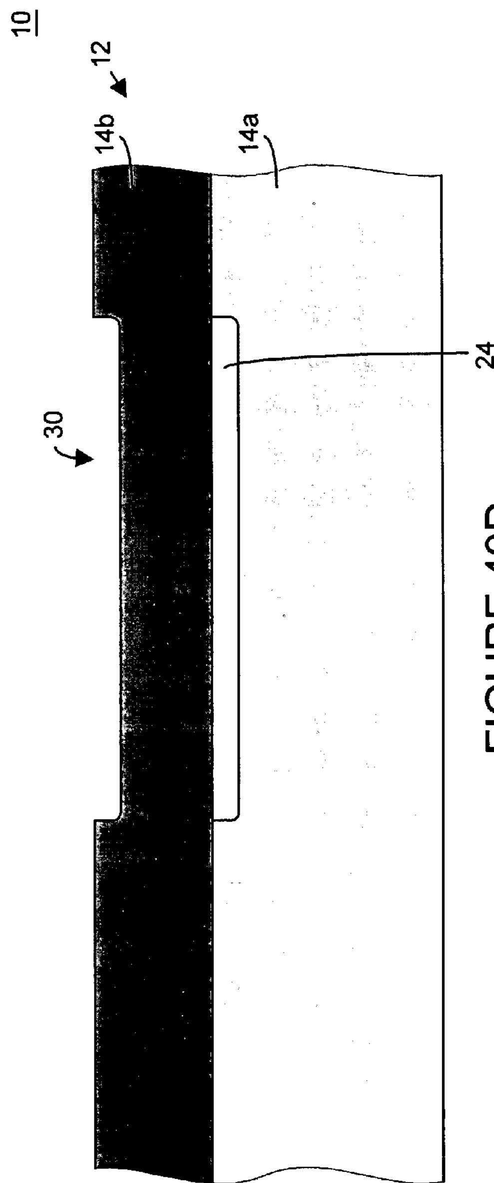


FIGURE 49D

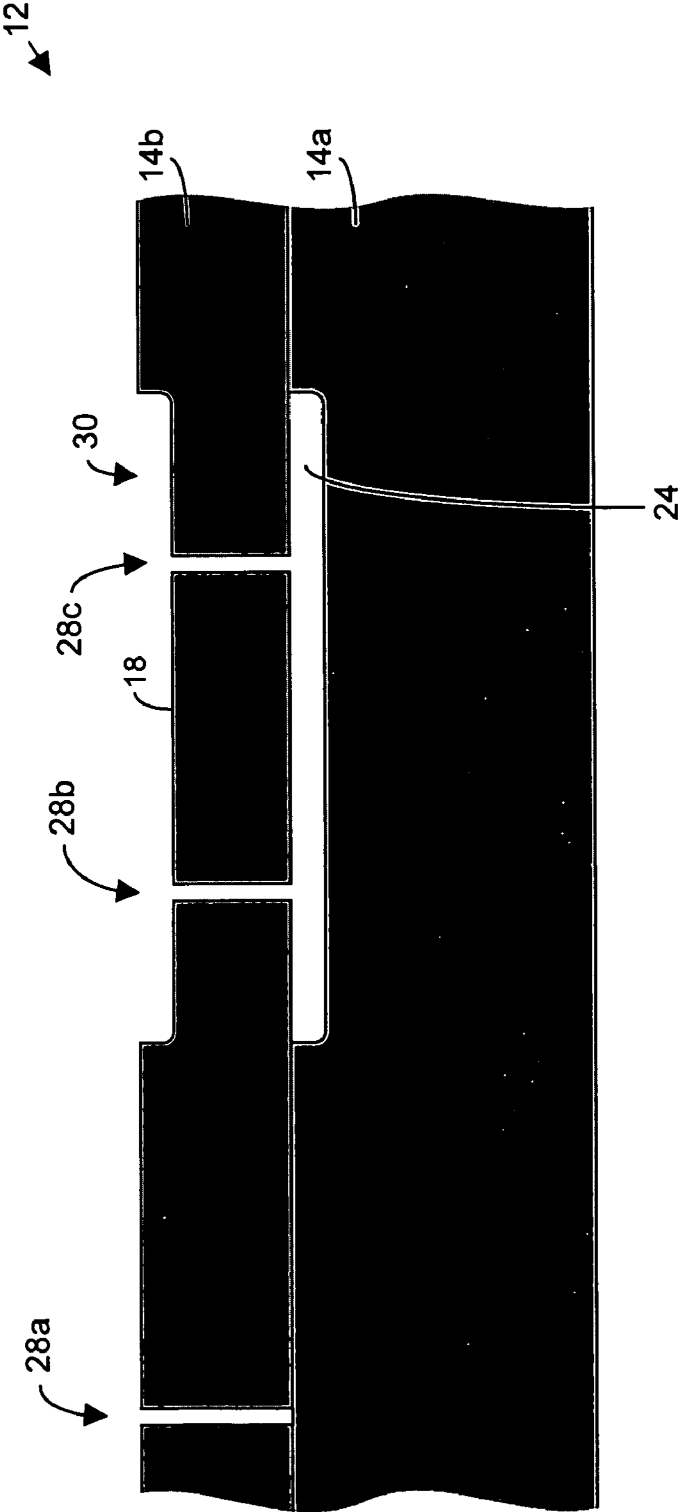


FIGURE 49E

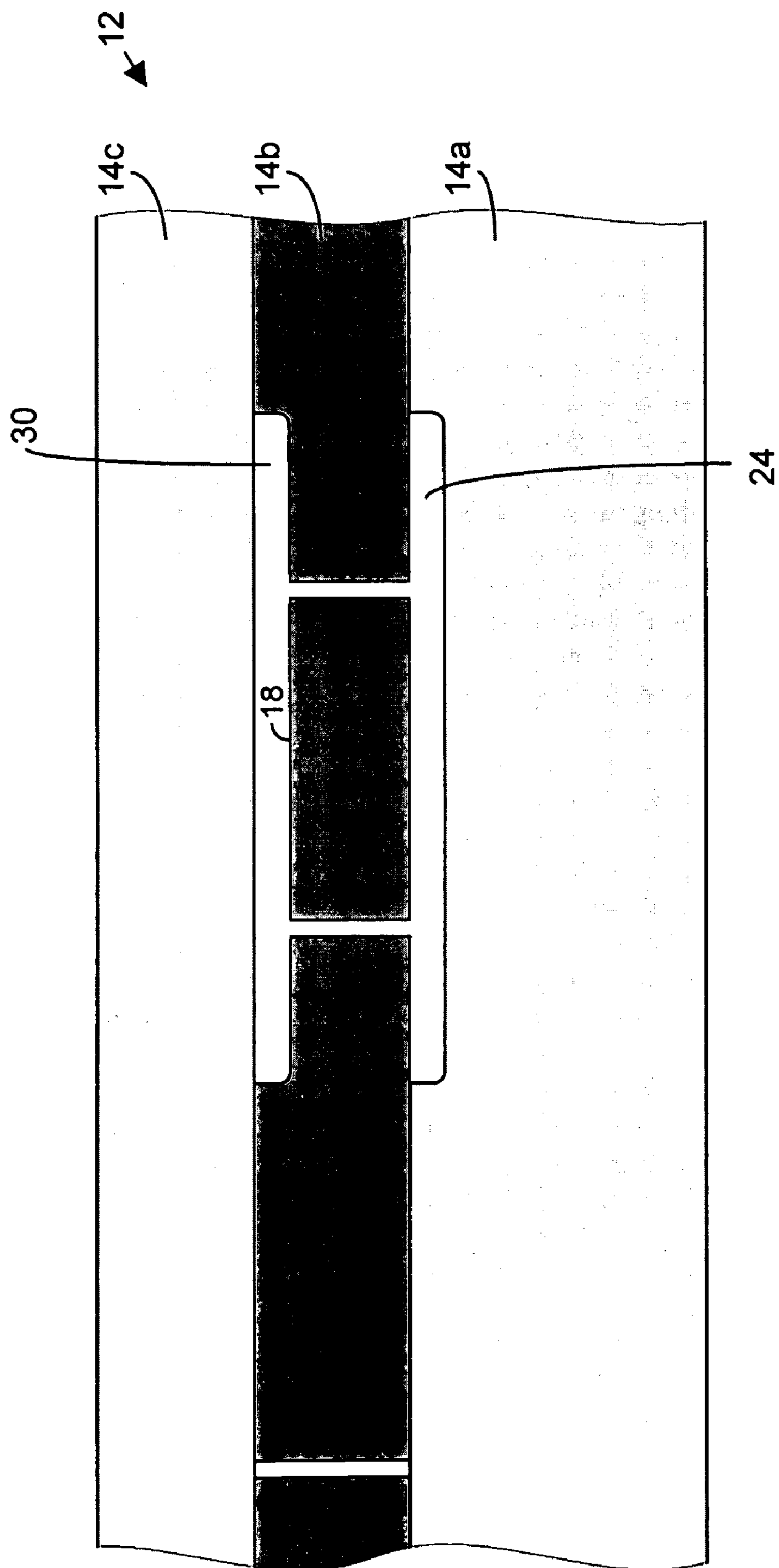


FIGURE 49F

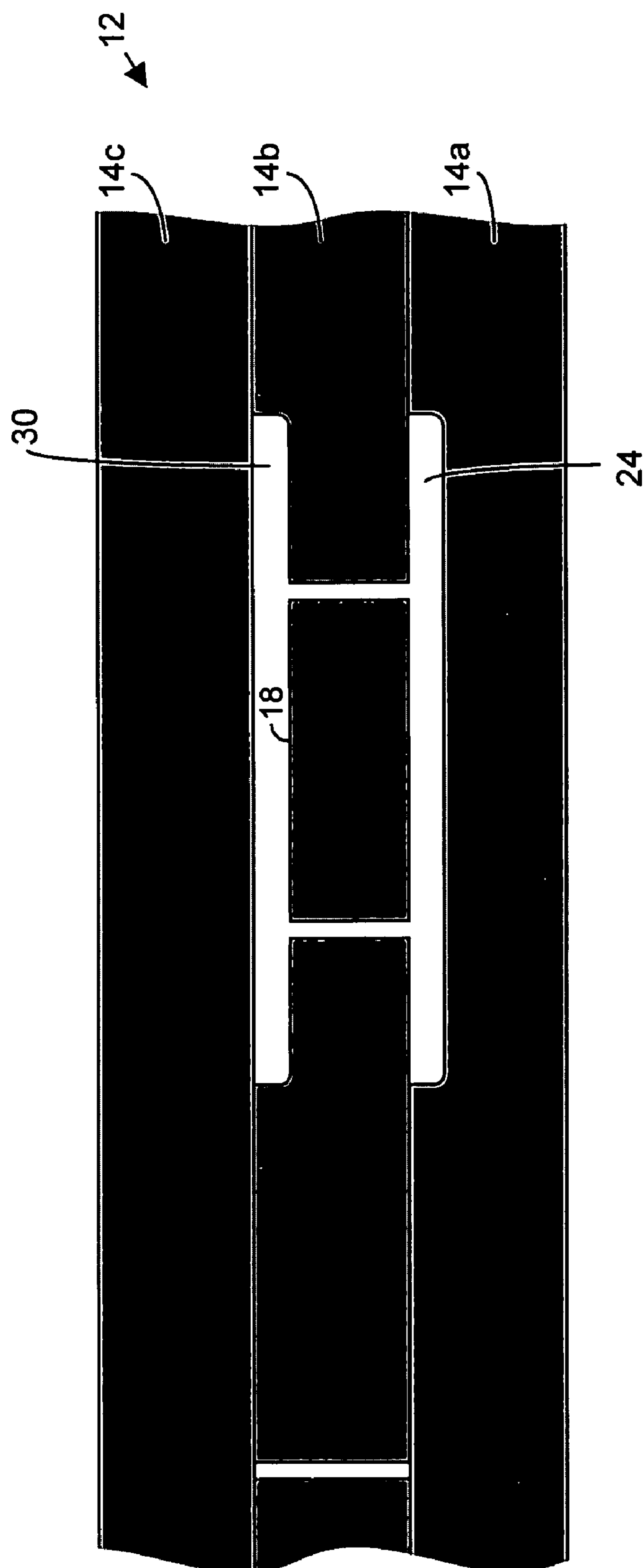


FIGURE 49G

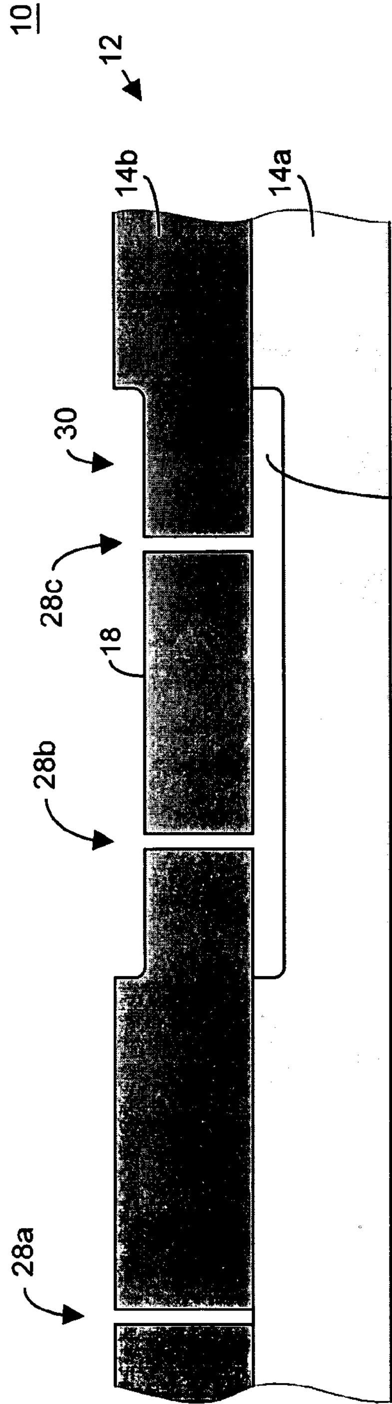


FIGURE 50A

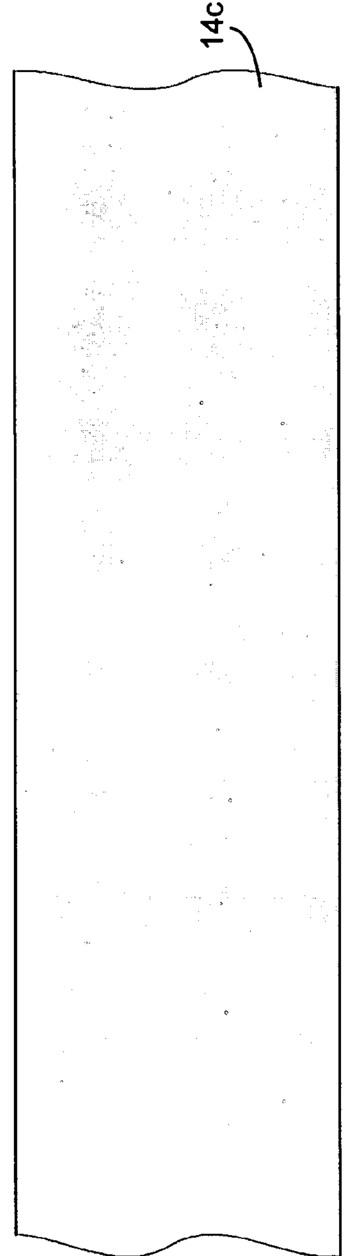


FIGURE 50B

FIGURE 50C

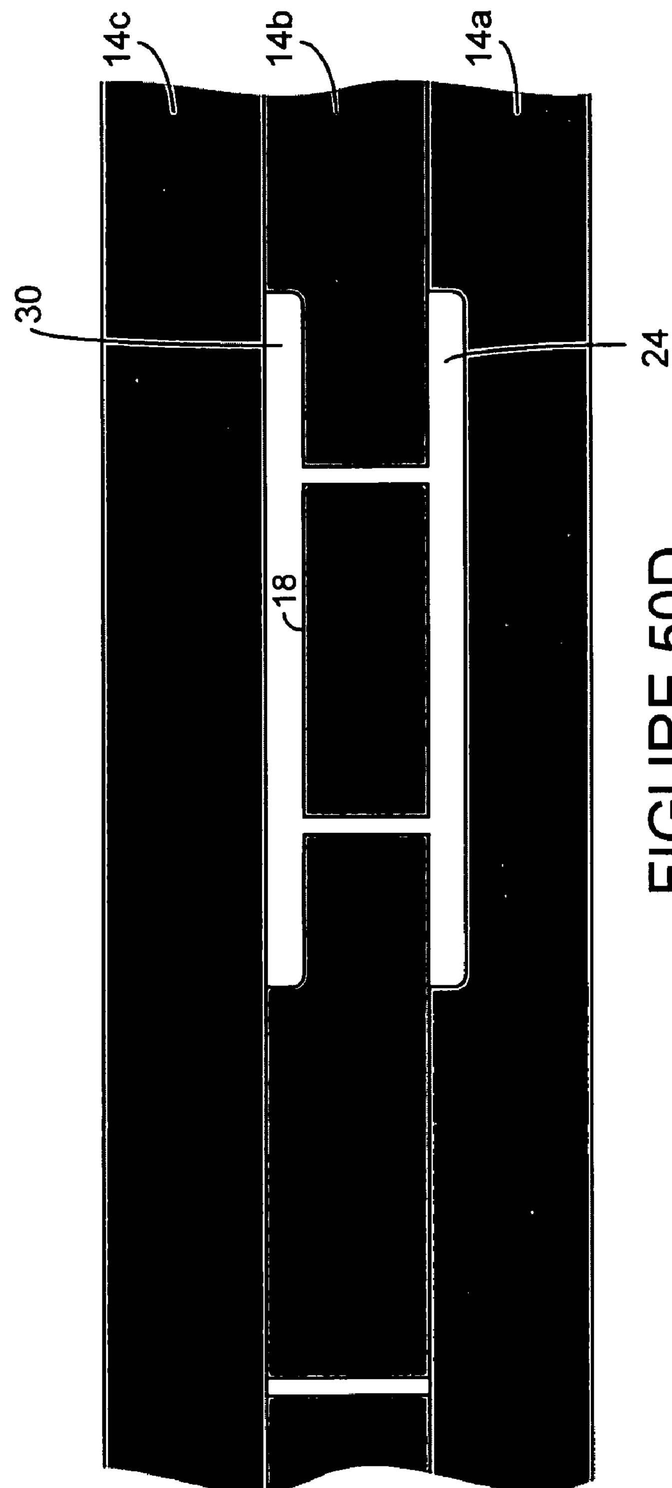


FIGURE 50D

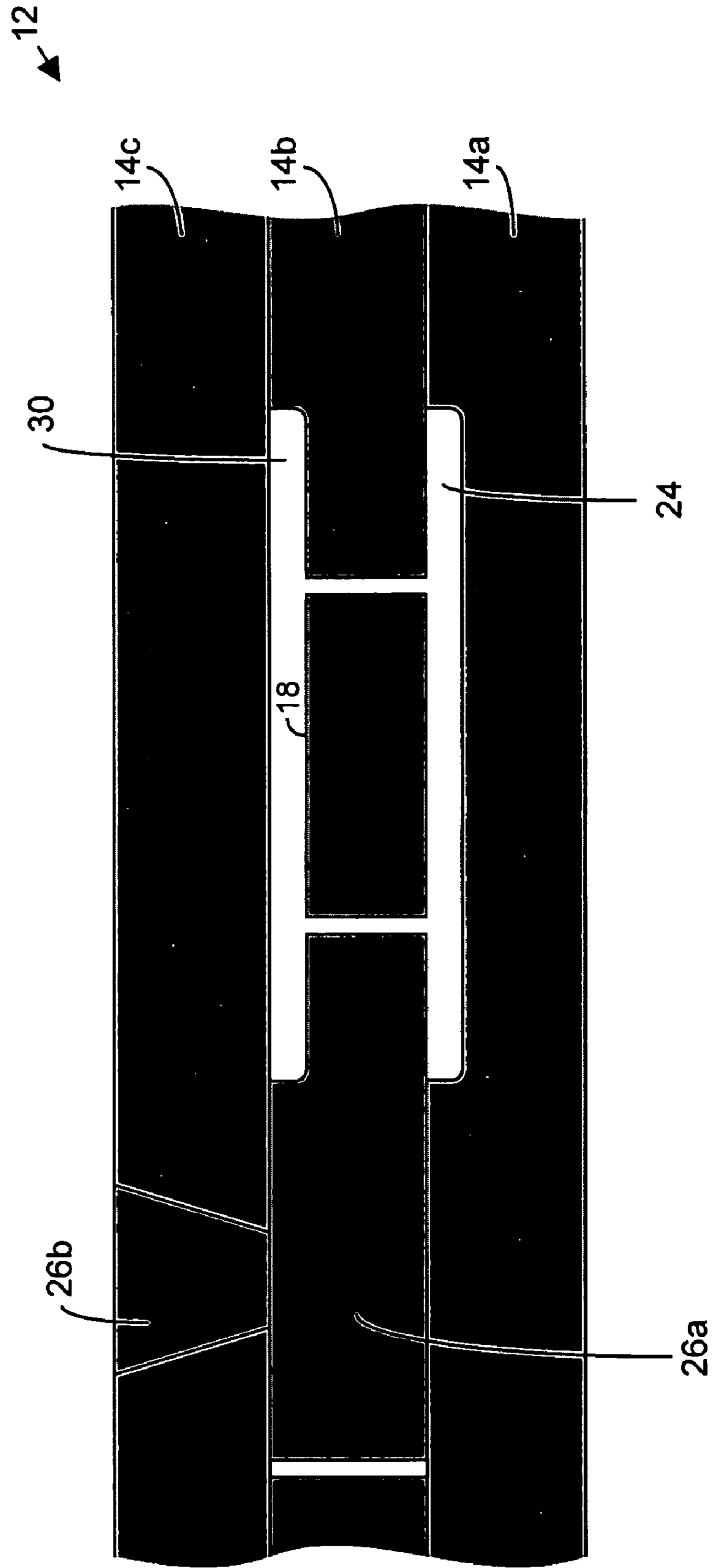
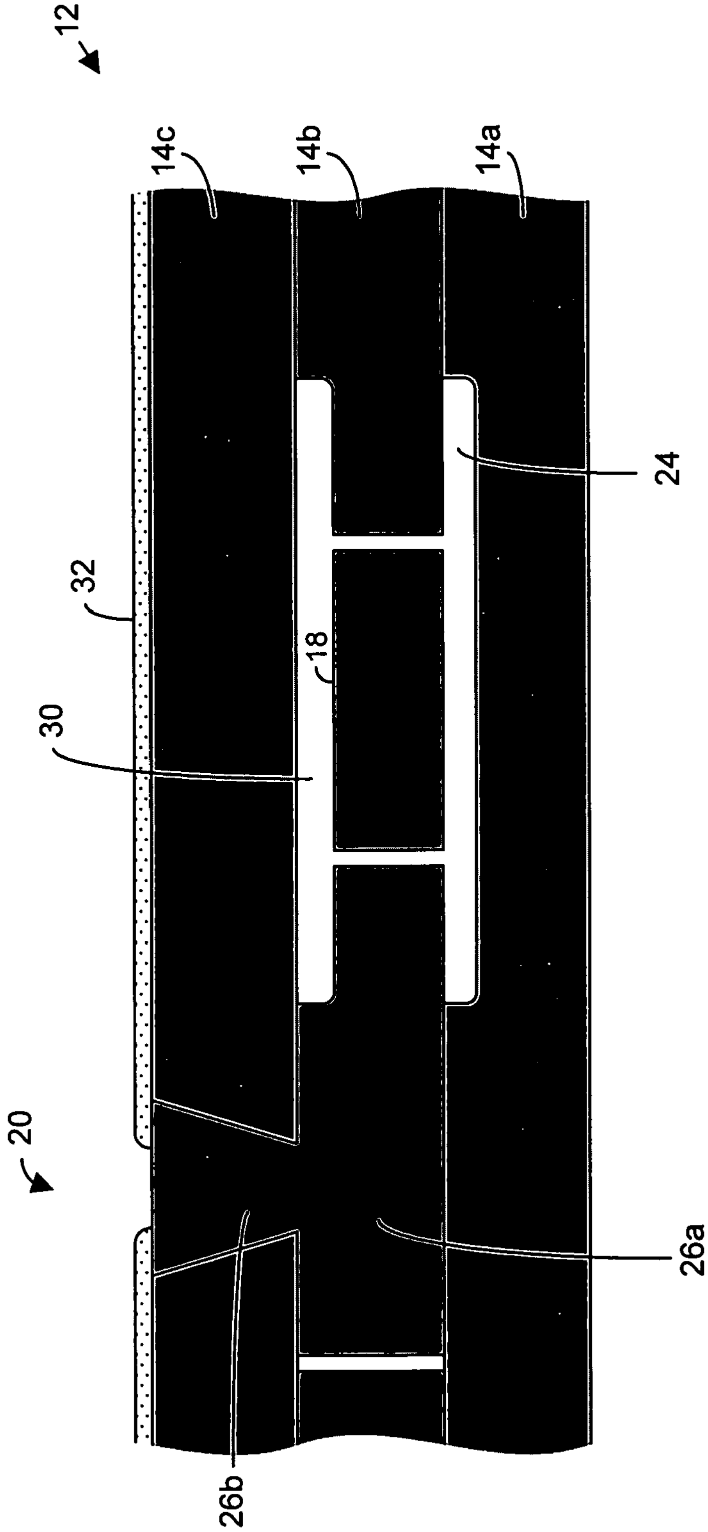


FIGURE 50E


10
12
14c
14b
14a
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26a
26b
FIGURE 50F

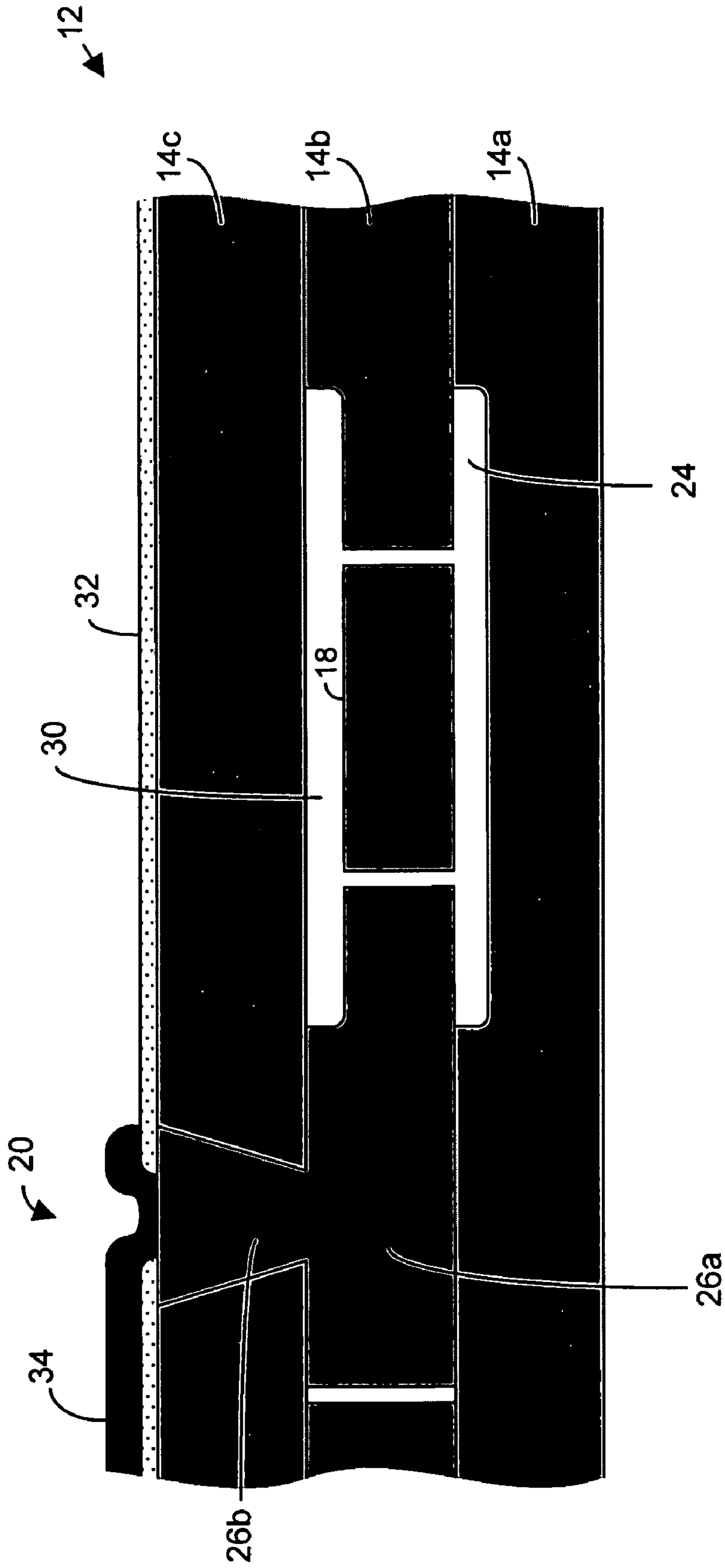

FIGURE 50G

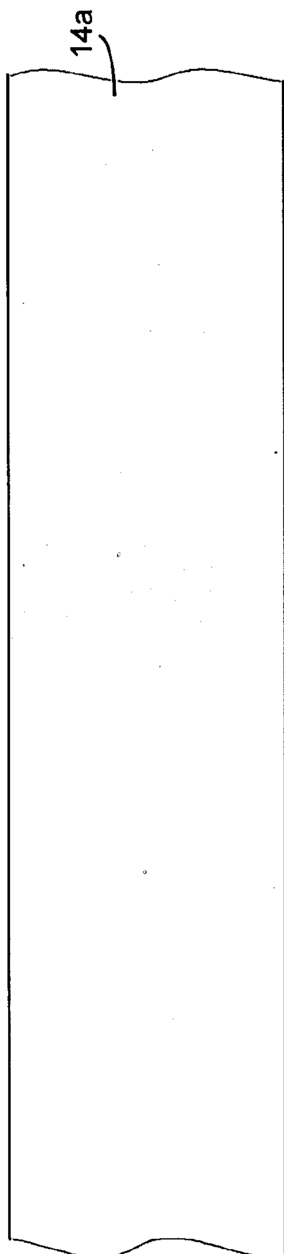

FIGURE 51A

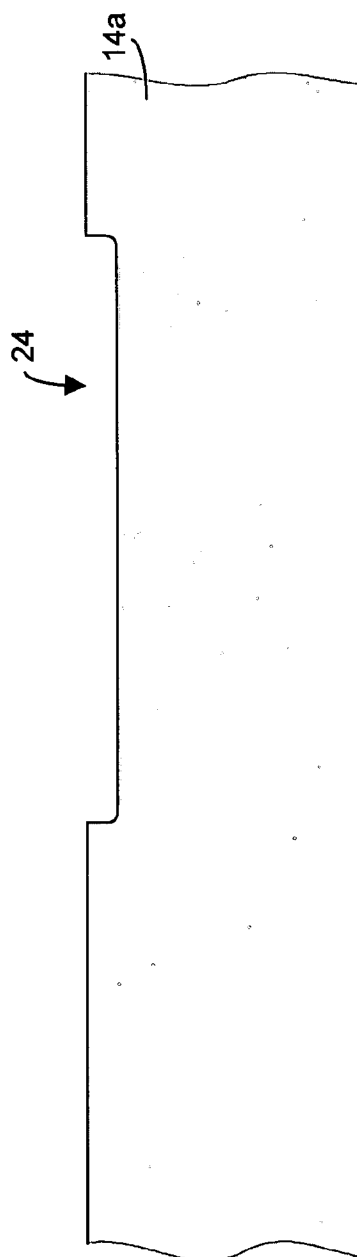

FIGURE 51B

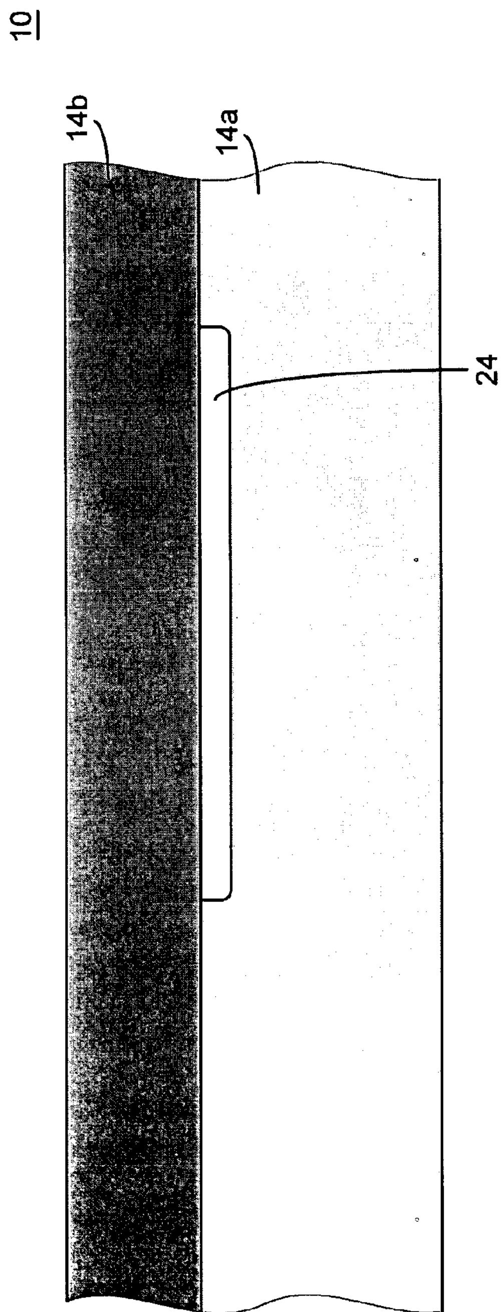

FIGURE 51C

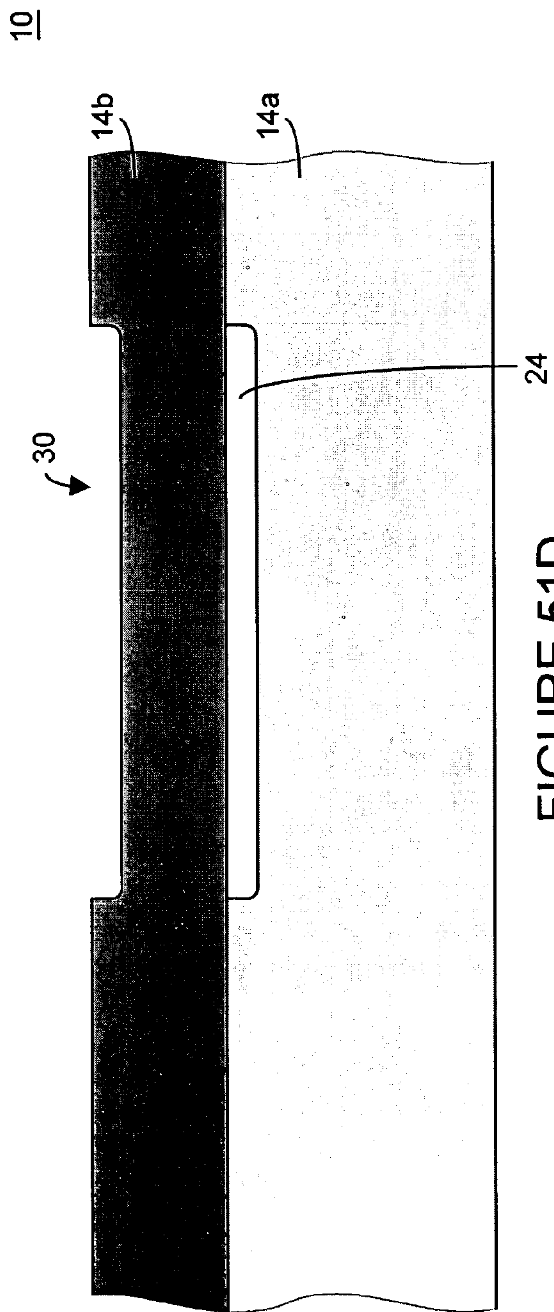

FIGURE 51D

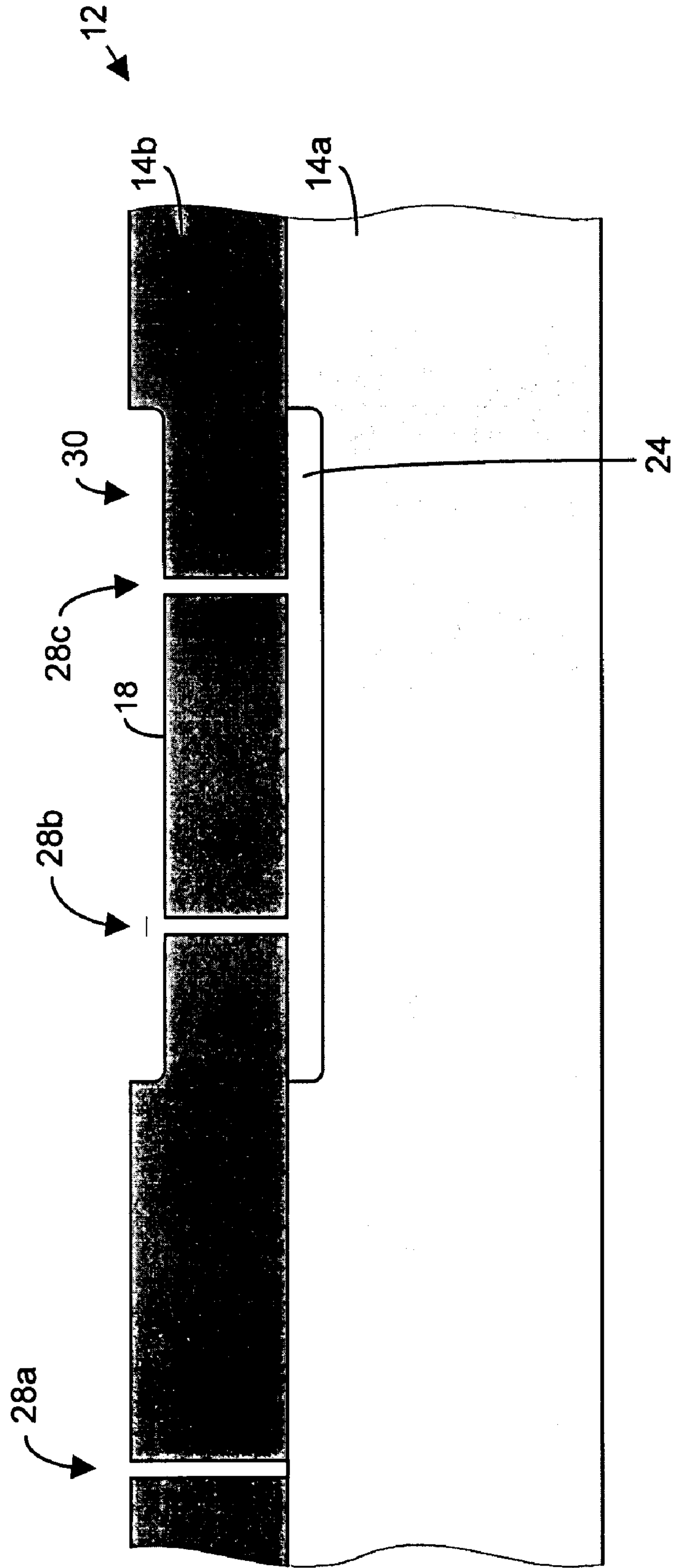

FIGURE 51E

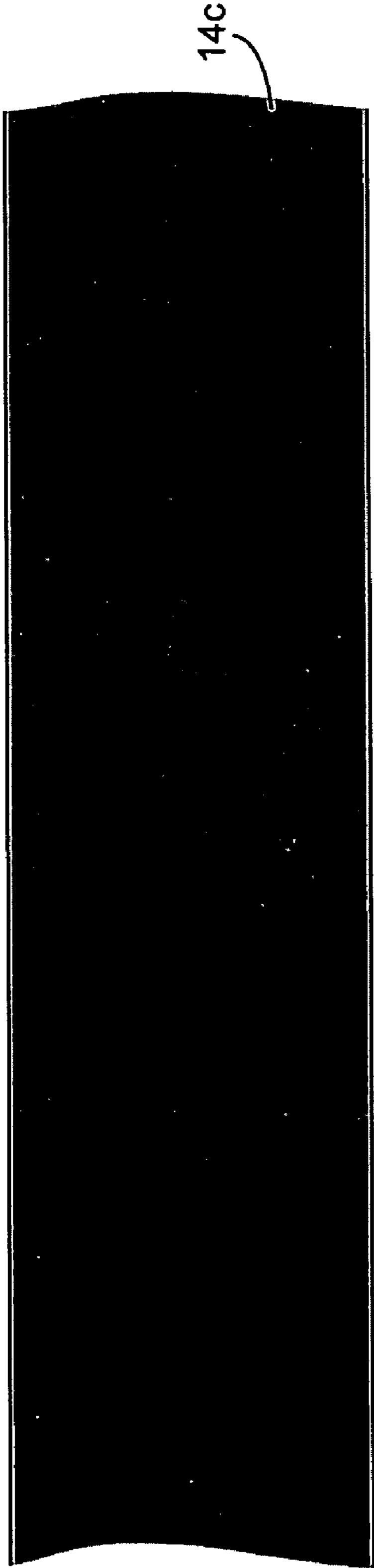

FIGURE 51F

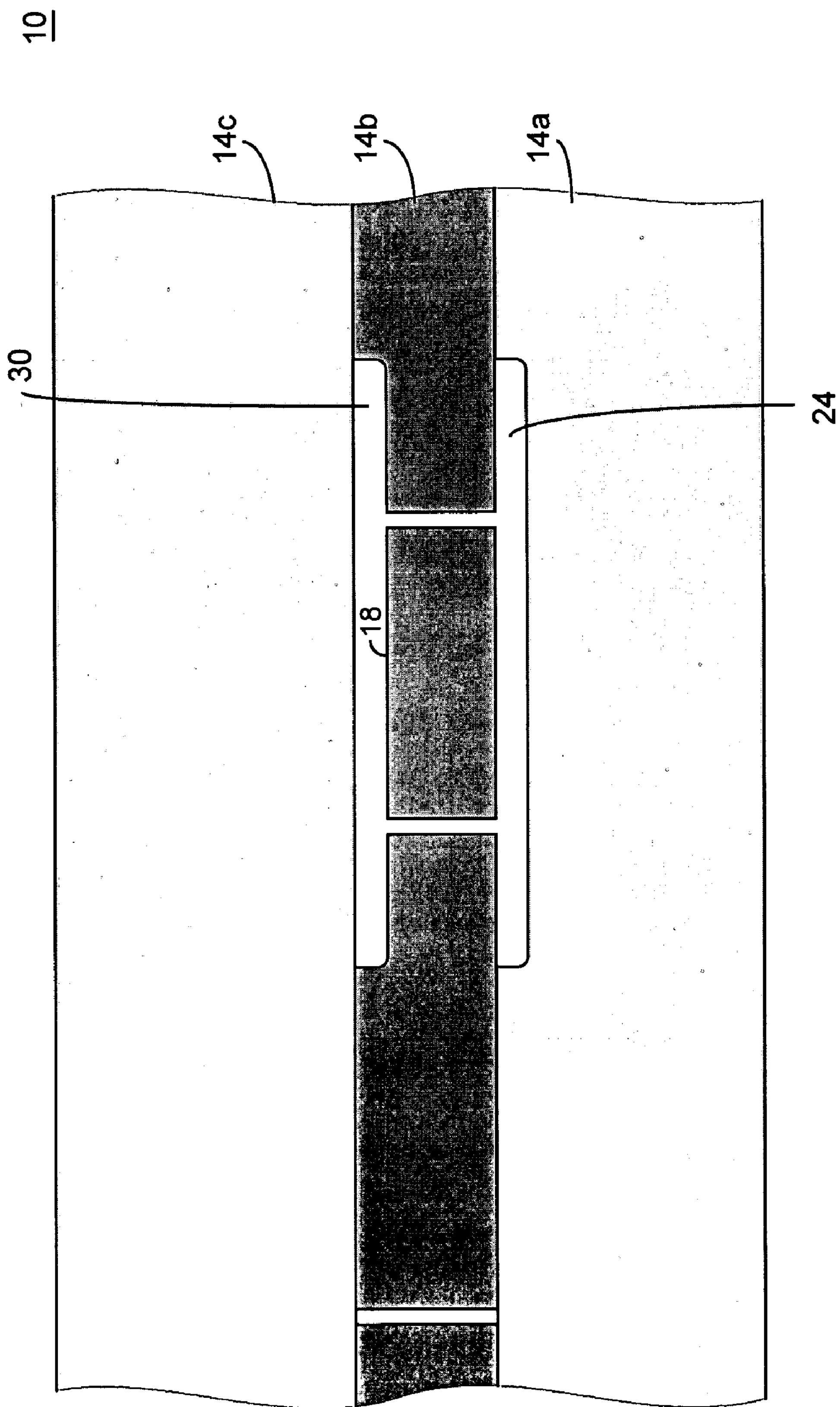

FIGURE 51G

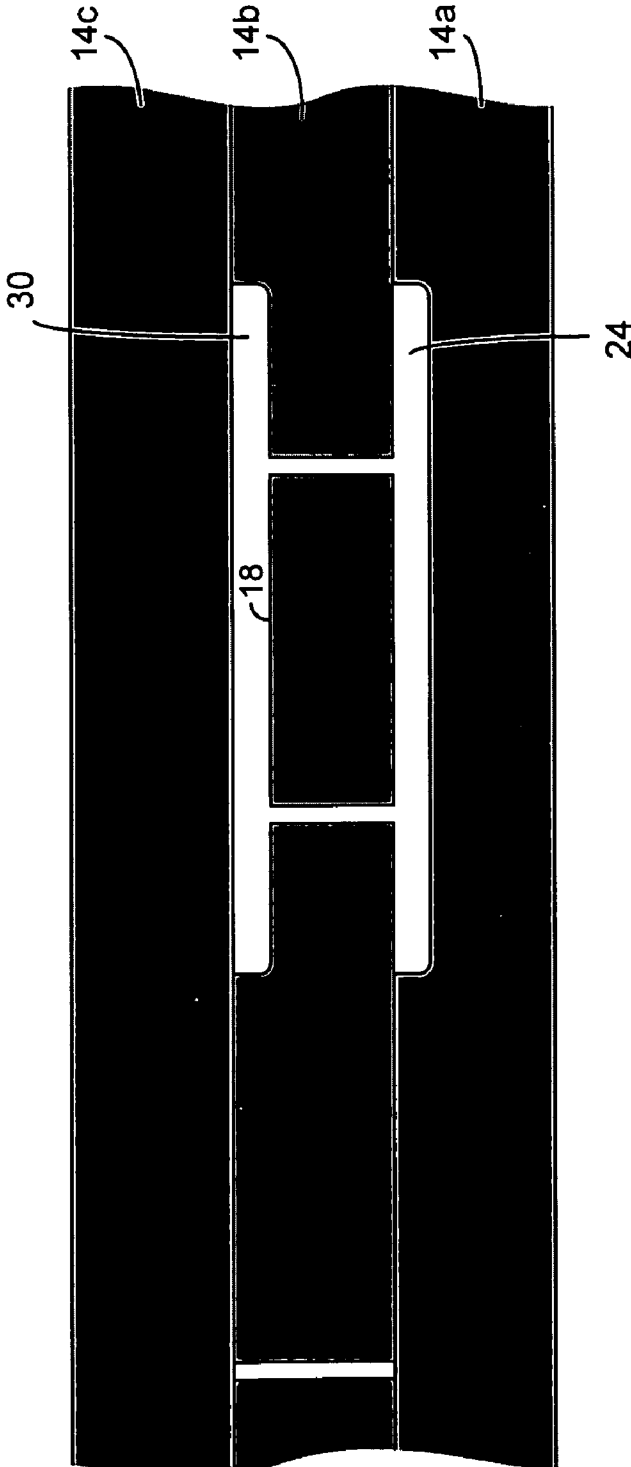

FIGURE 51H

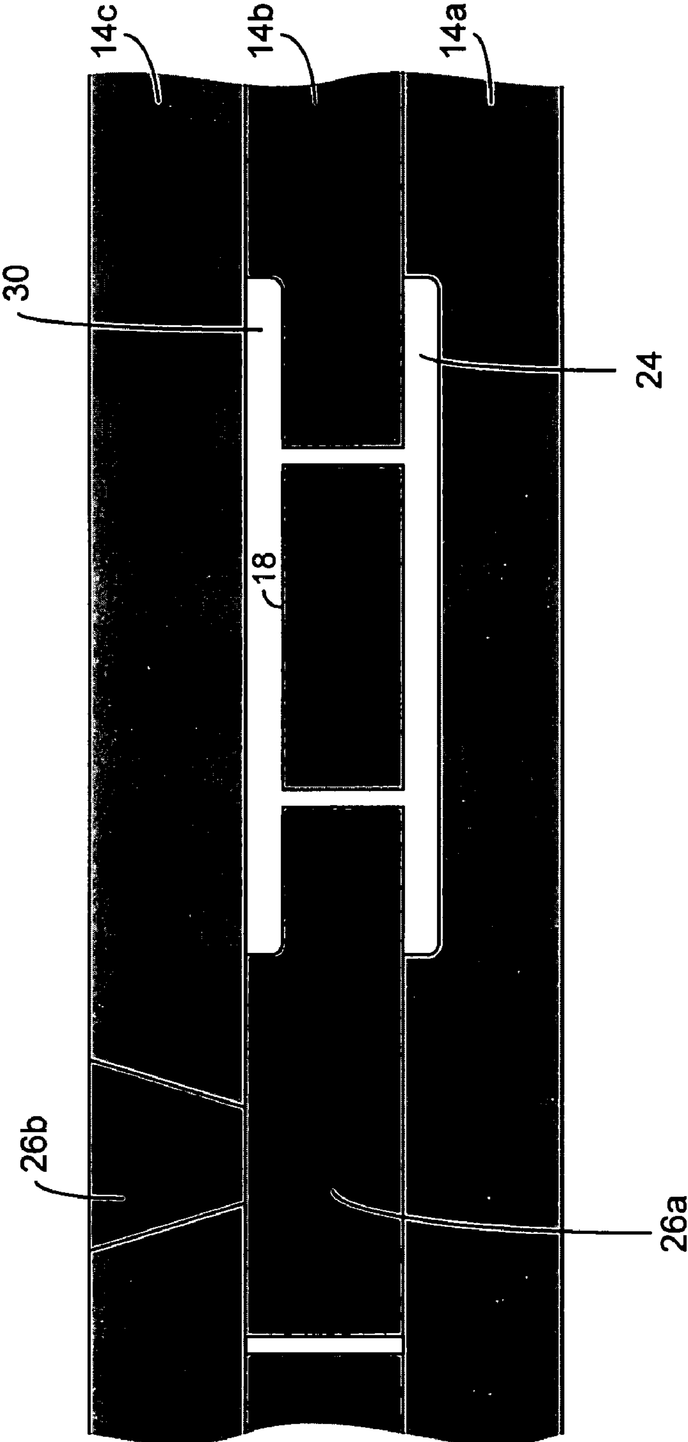

FIGURE 51I

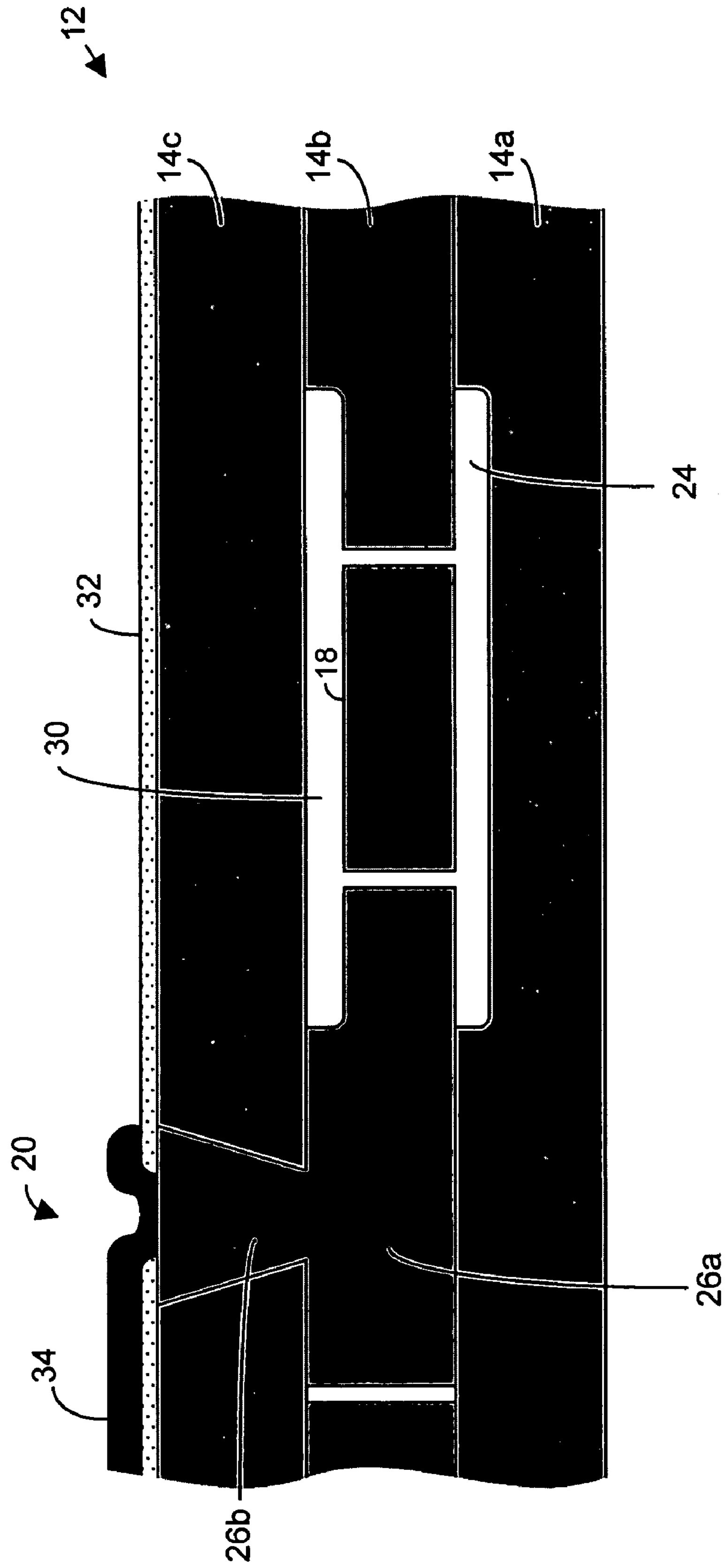

FIGURE 51J

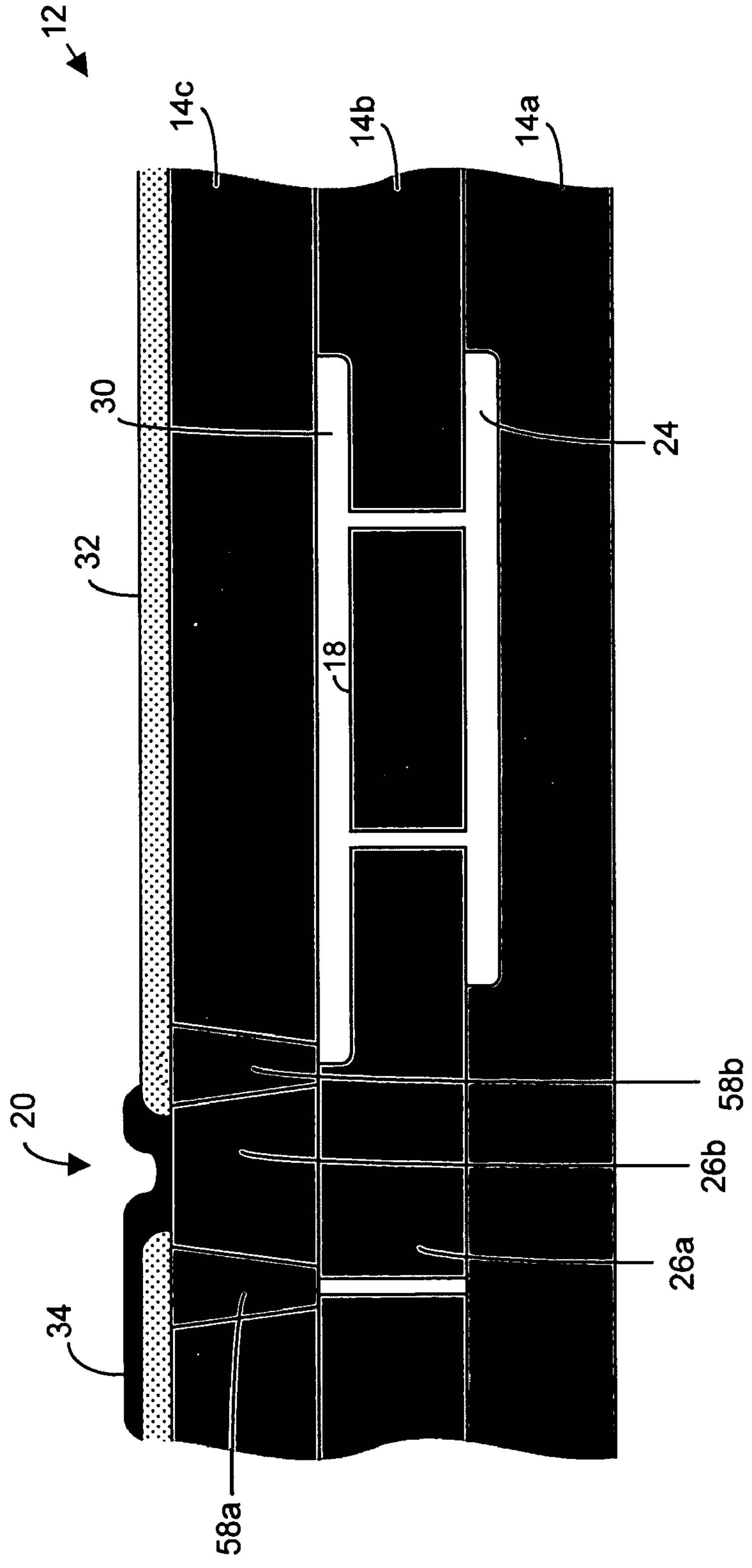

FIGURE 52

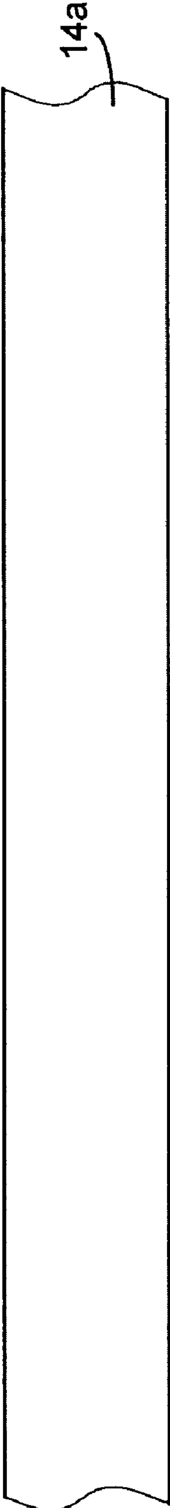

FIGURE 53A

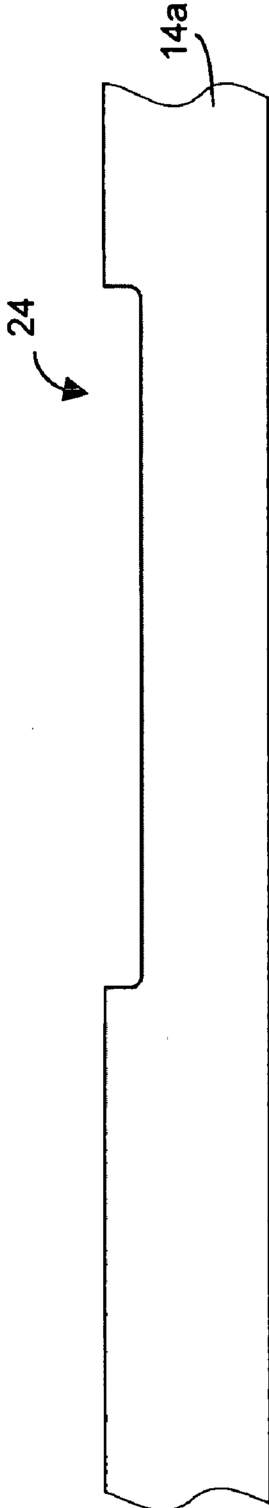

FIGURE 53B

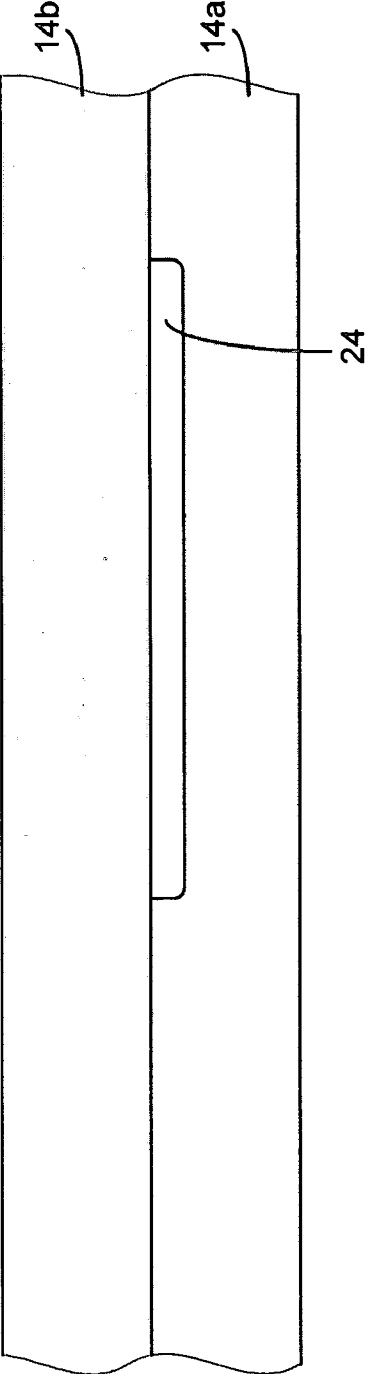

FIGURE 53C

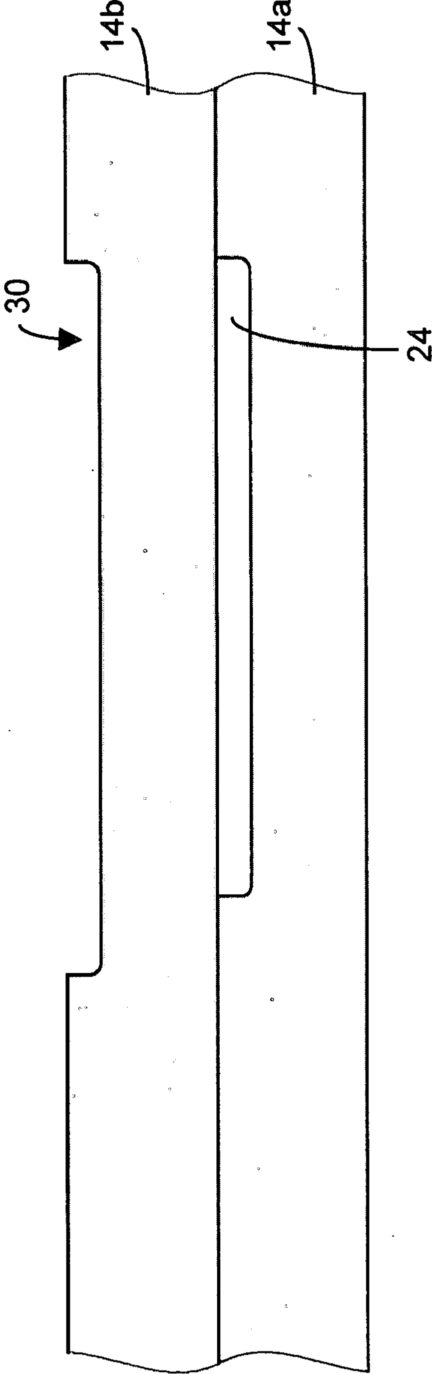

FIGURE 53D

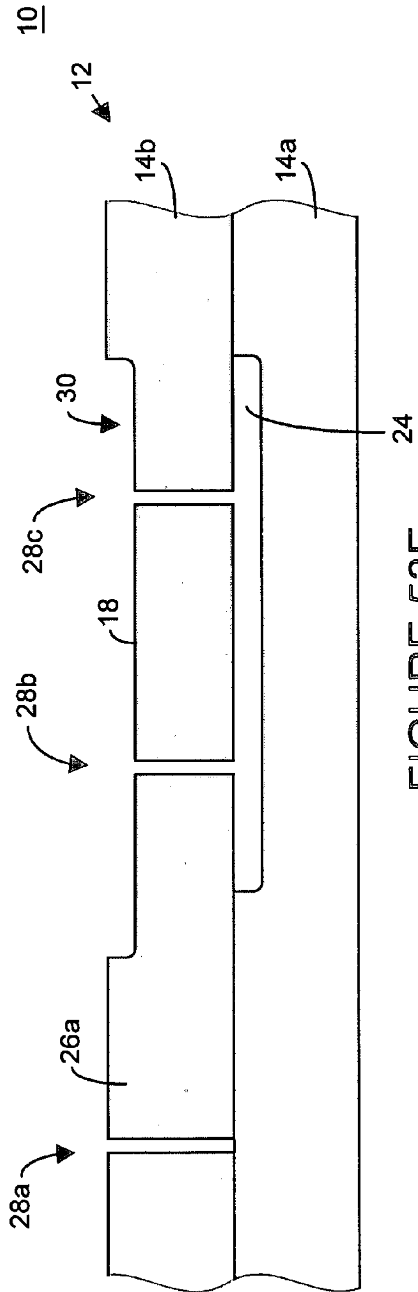

FIGURE 53E

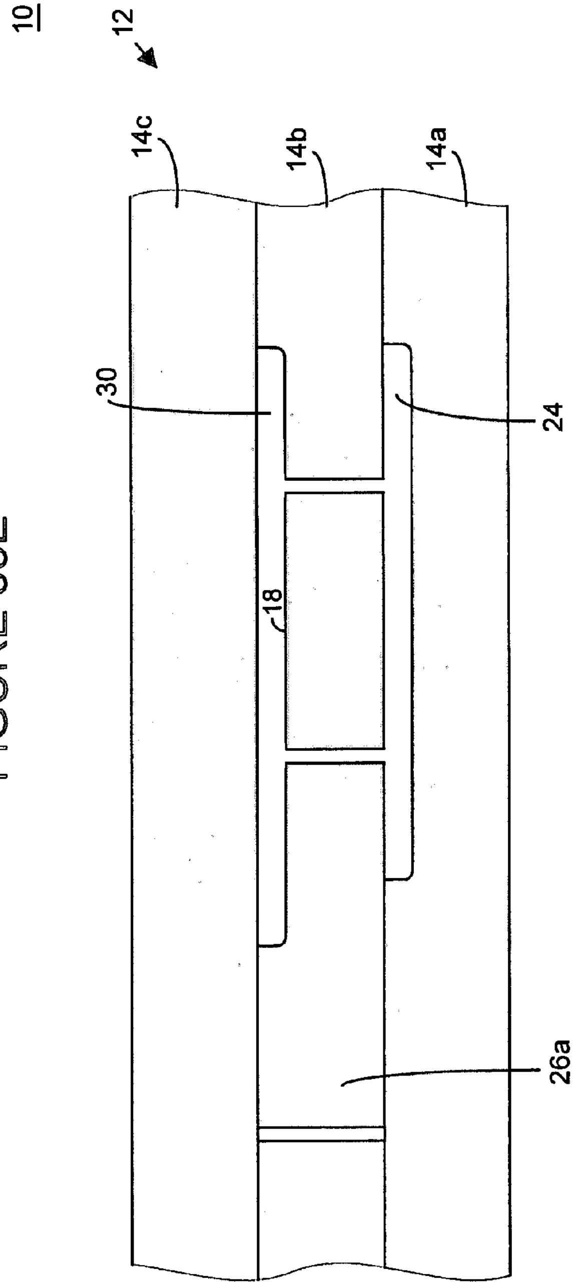

FIGURE 53F

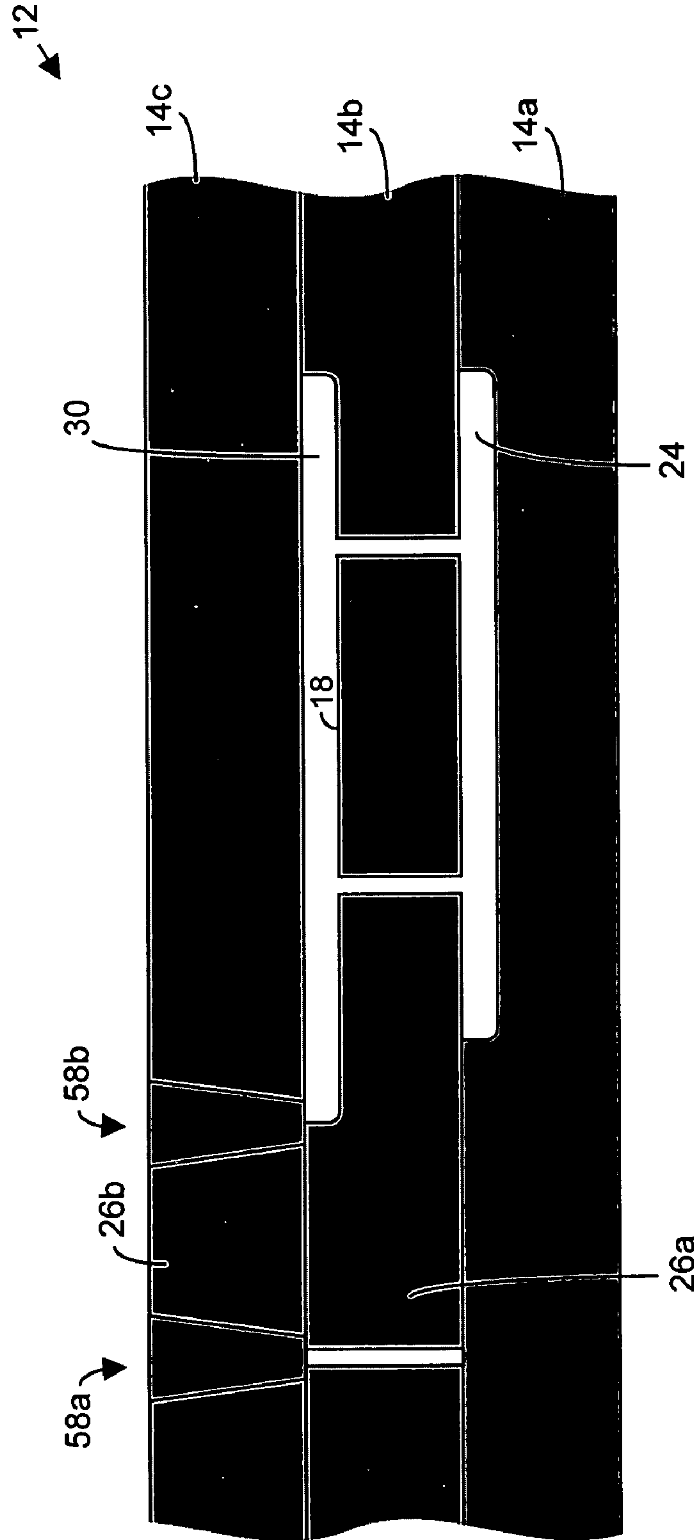

FIGURE 53G

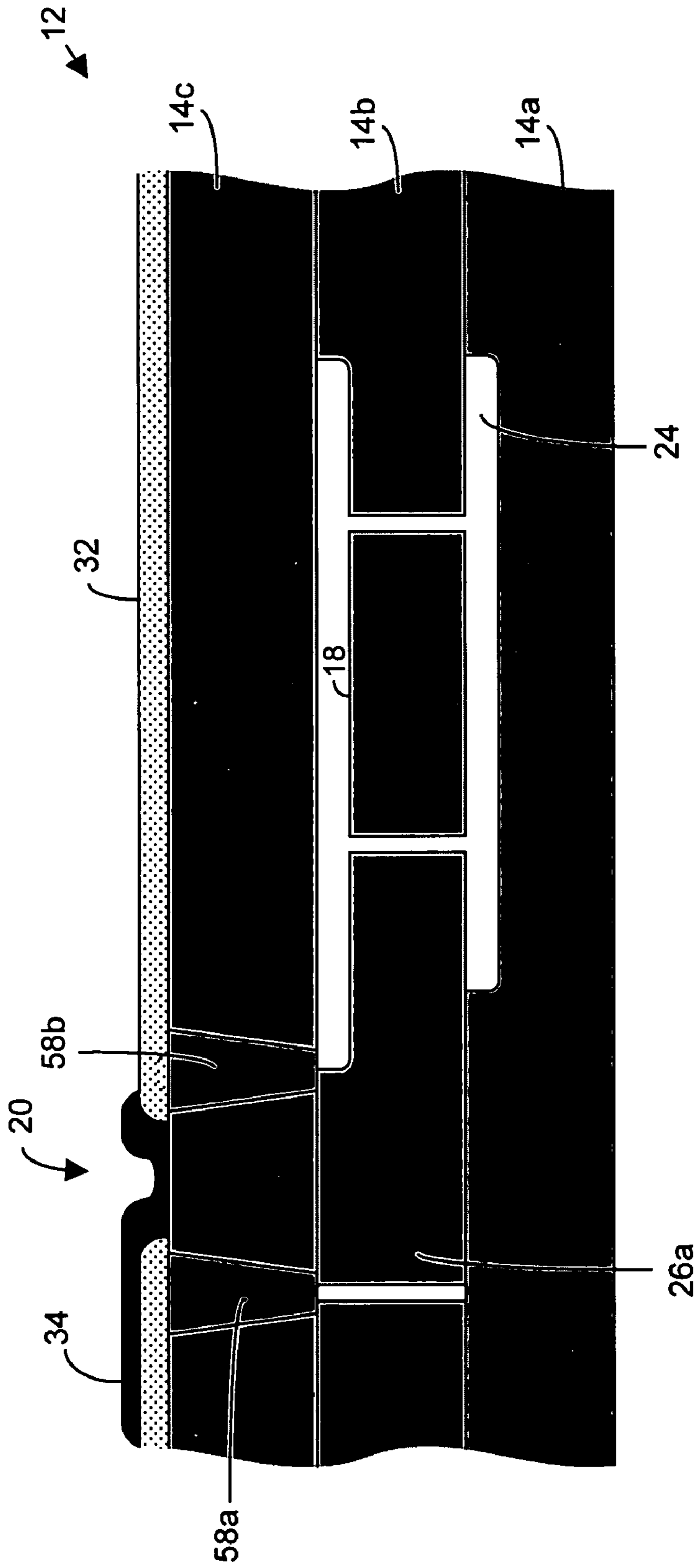

FIGURE 53H

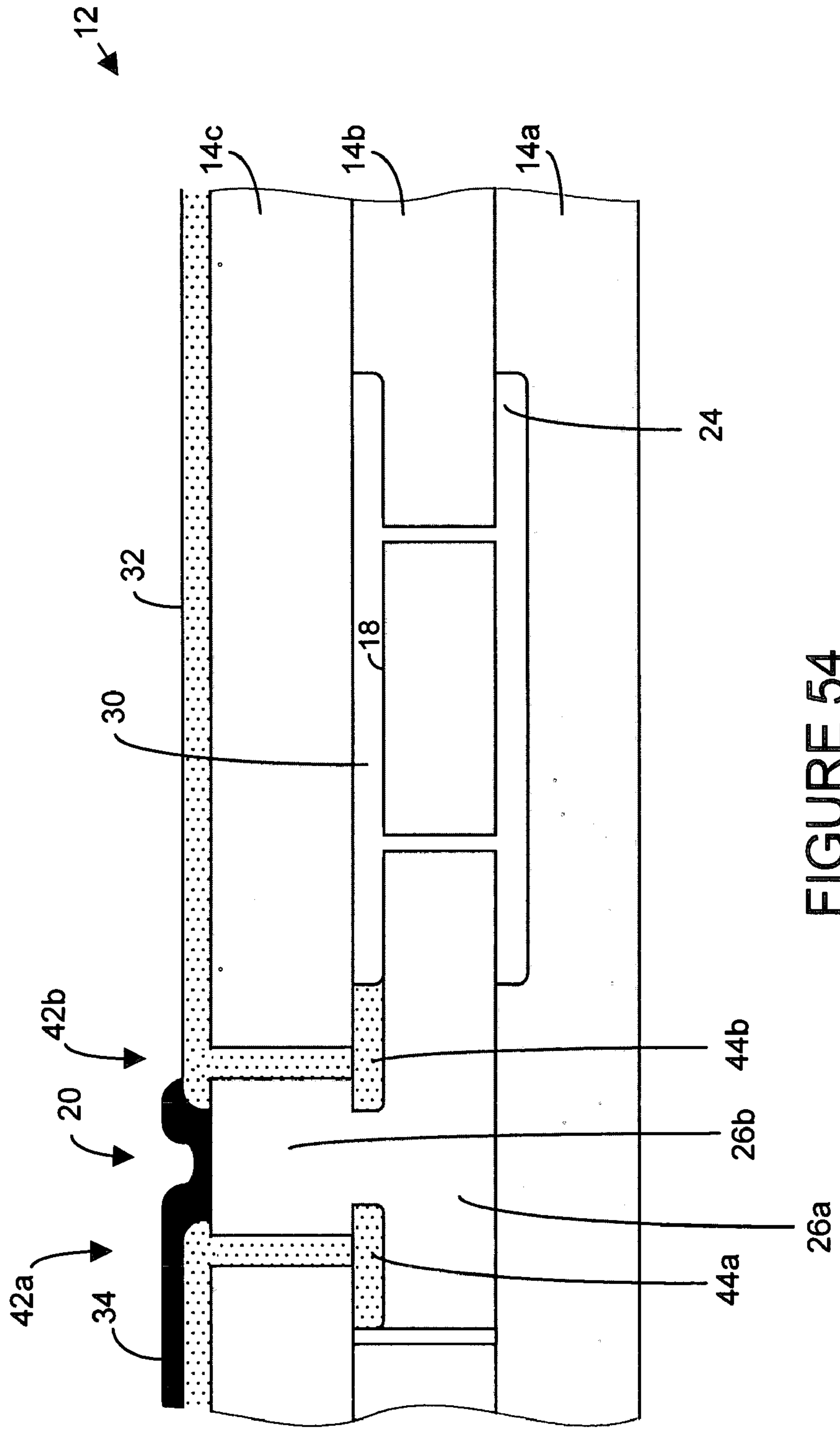

FIGURE 54

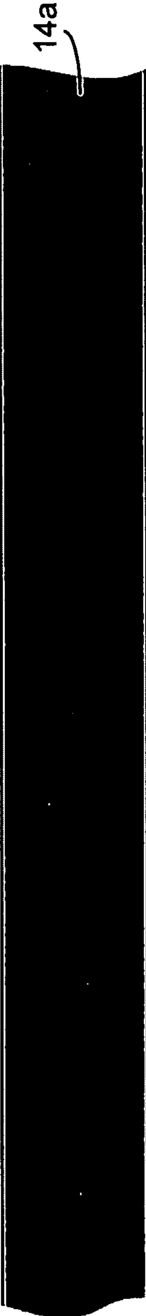

FIGURE 55A

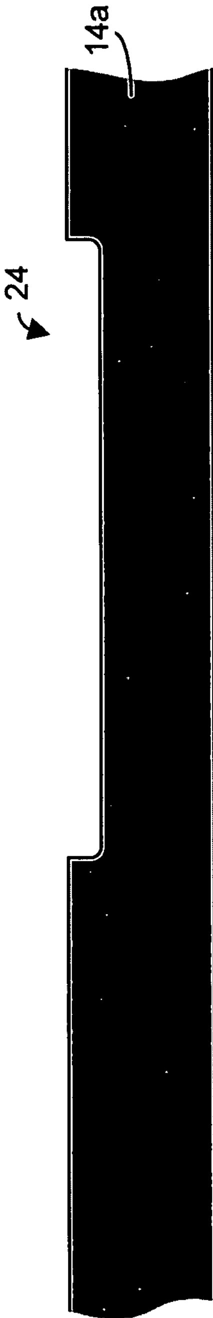

FIGURE 55B

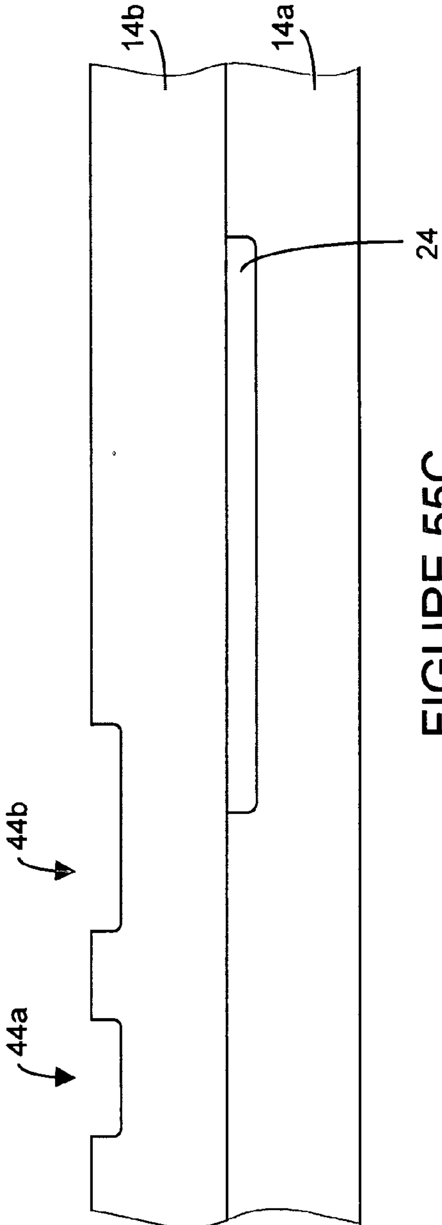

FIGURE 55C

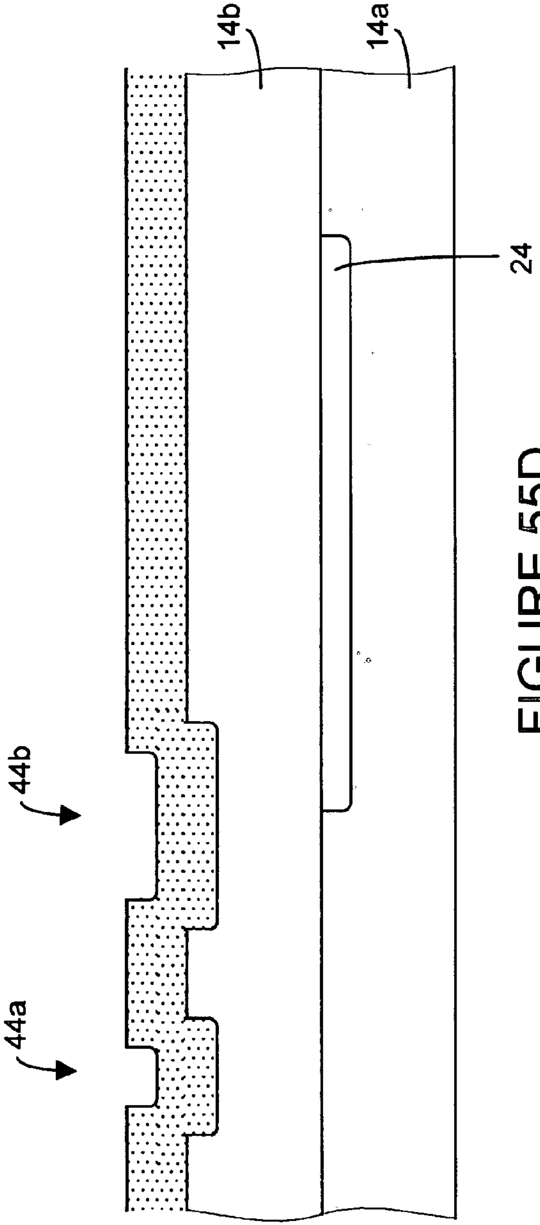

FIGURE 55D

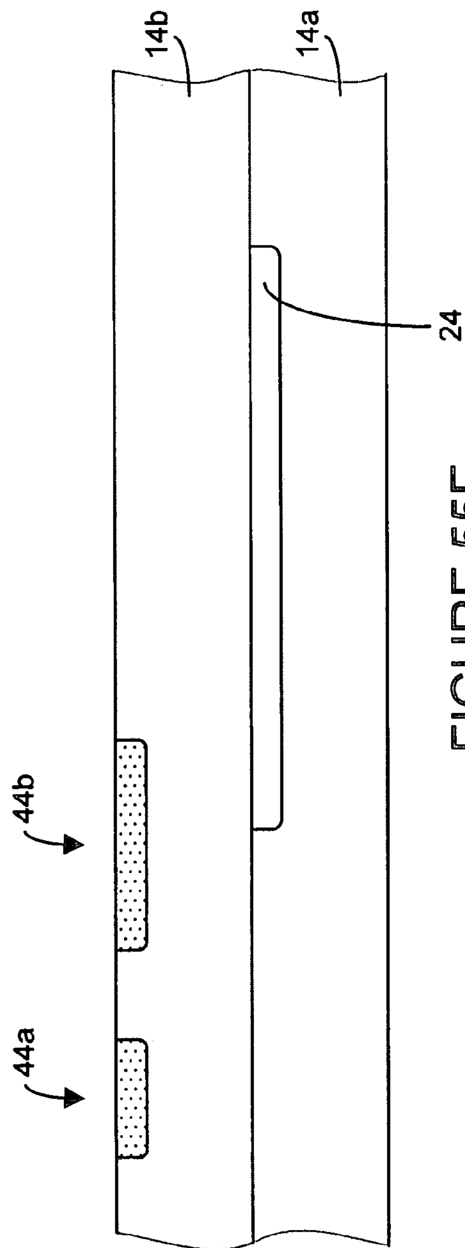

FIGURE 55E

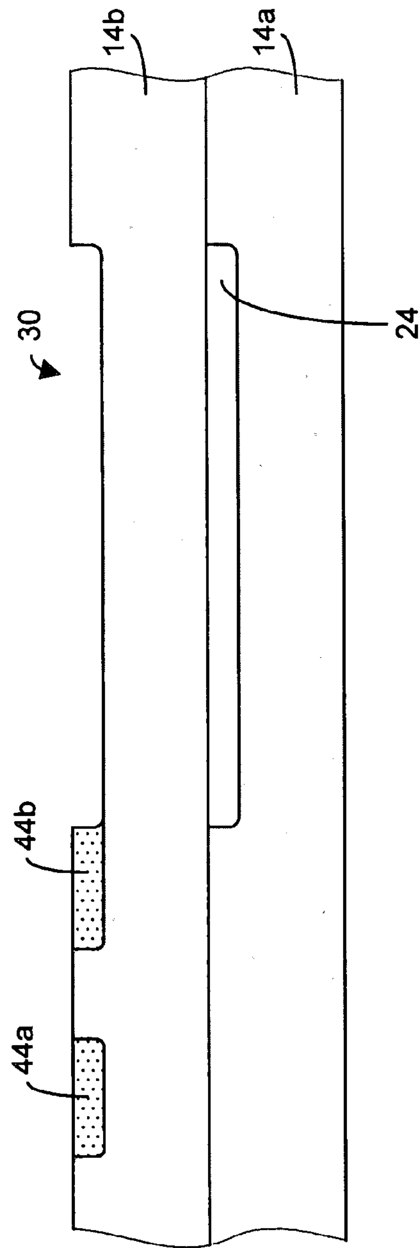

FIGURE 55F

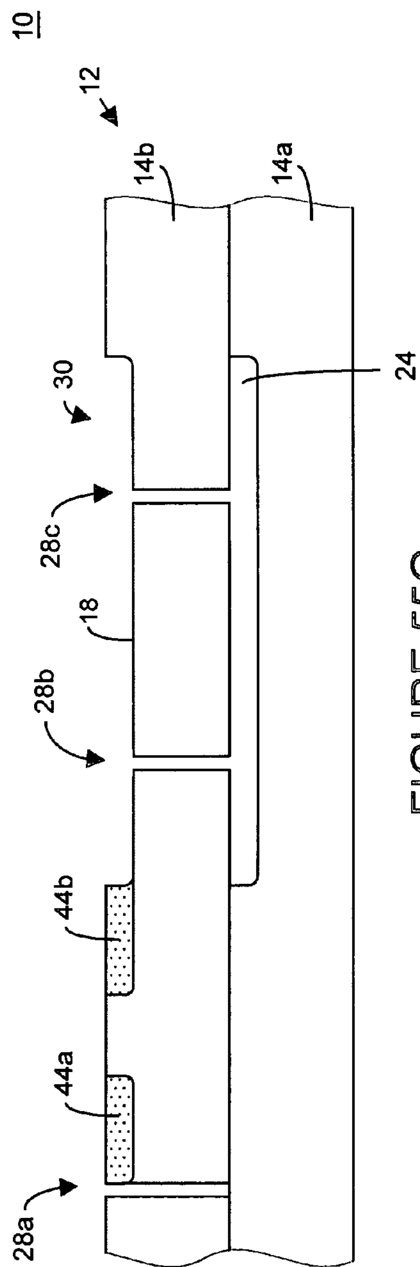

FIGURE 55G

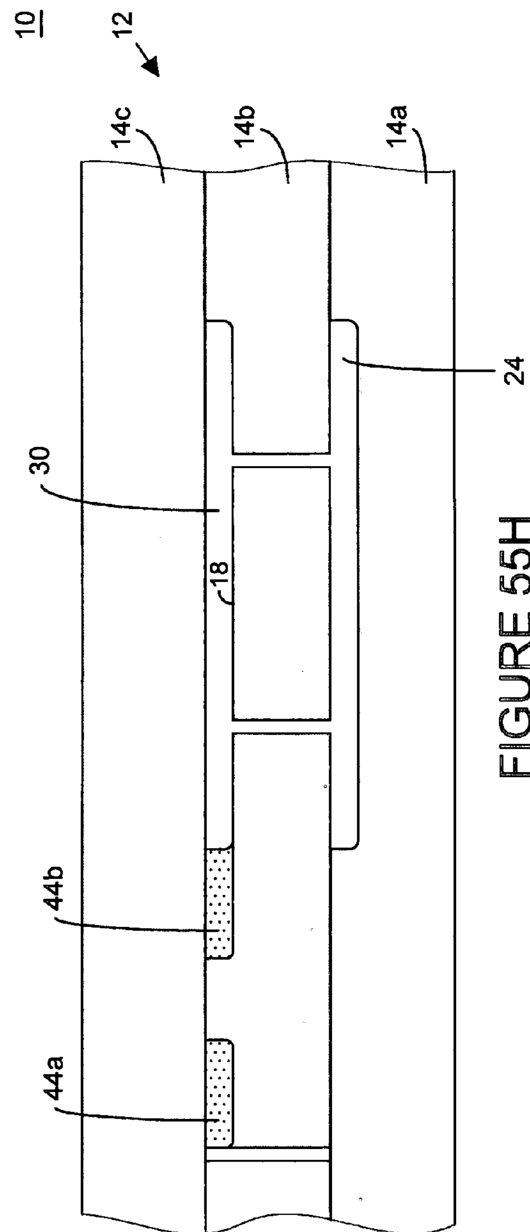

FIGURE 55H

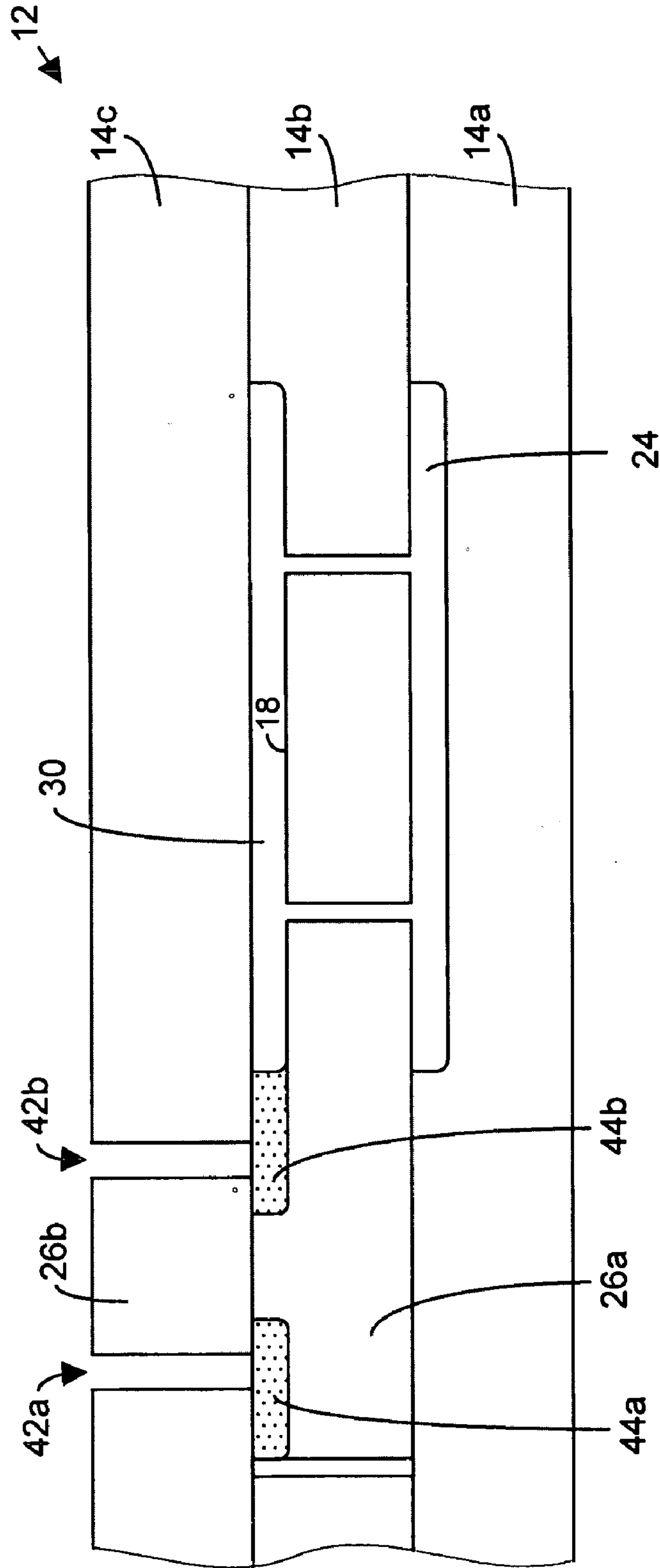

FIGURE 55I

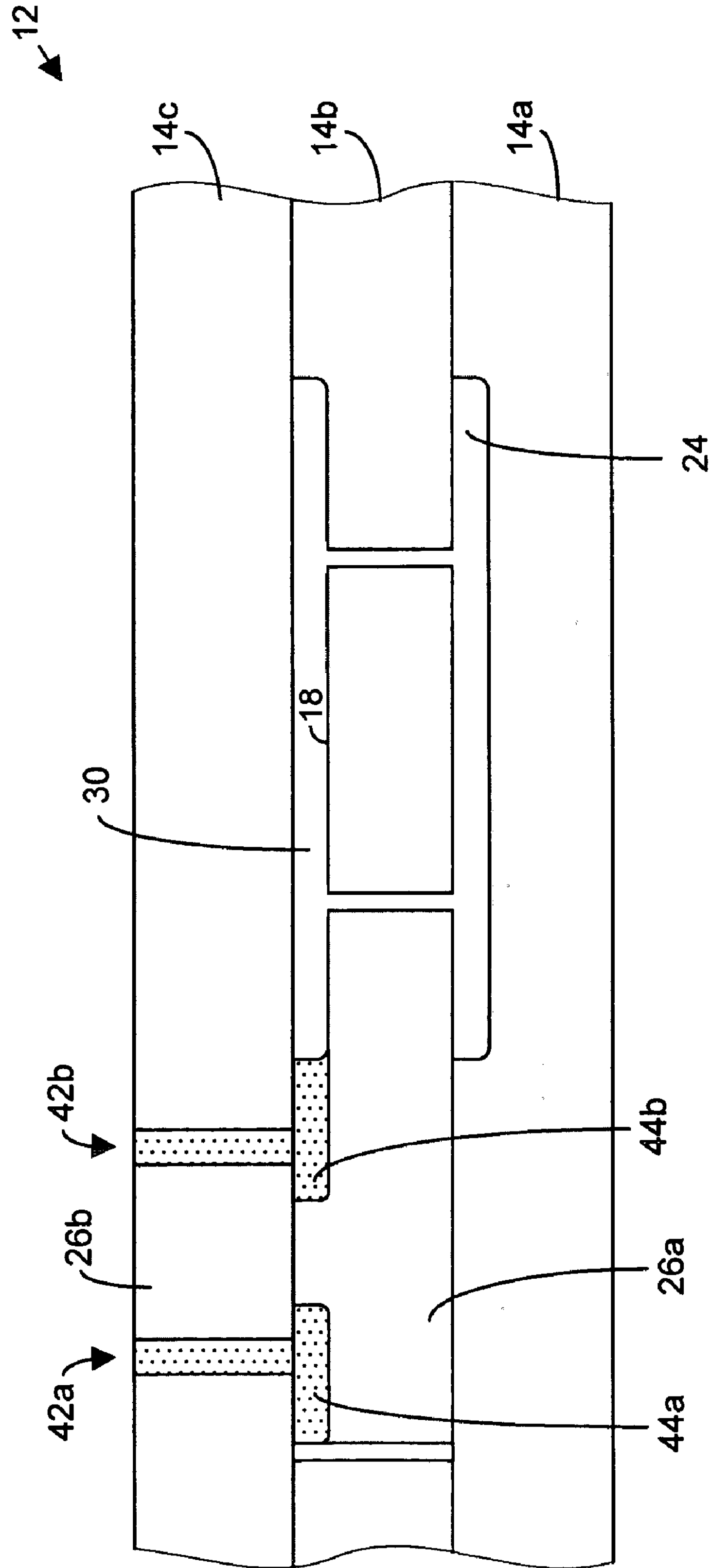

FIGURE 55J

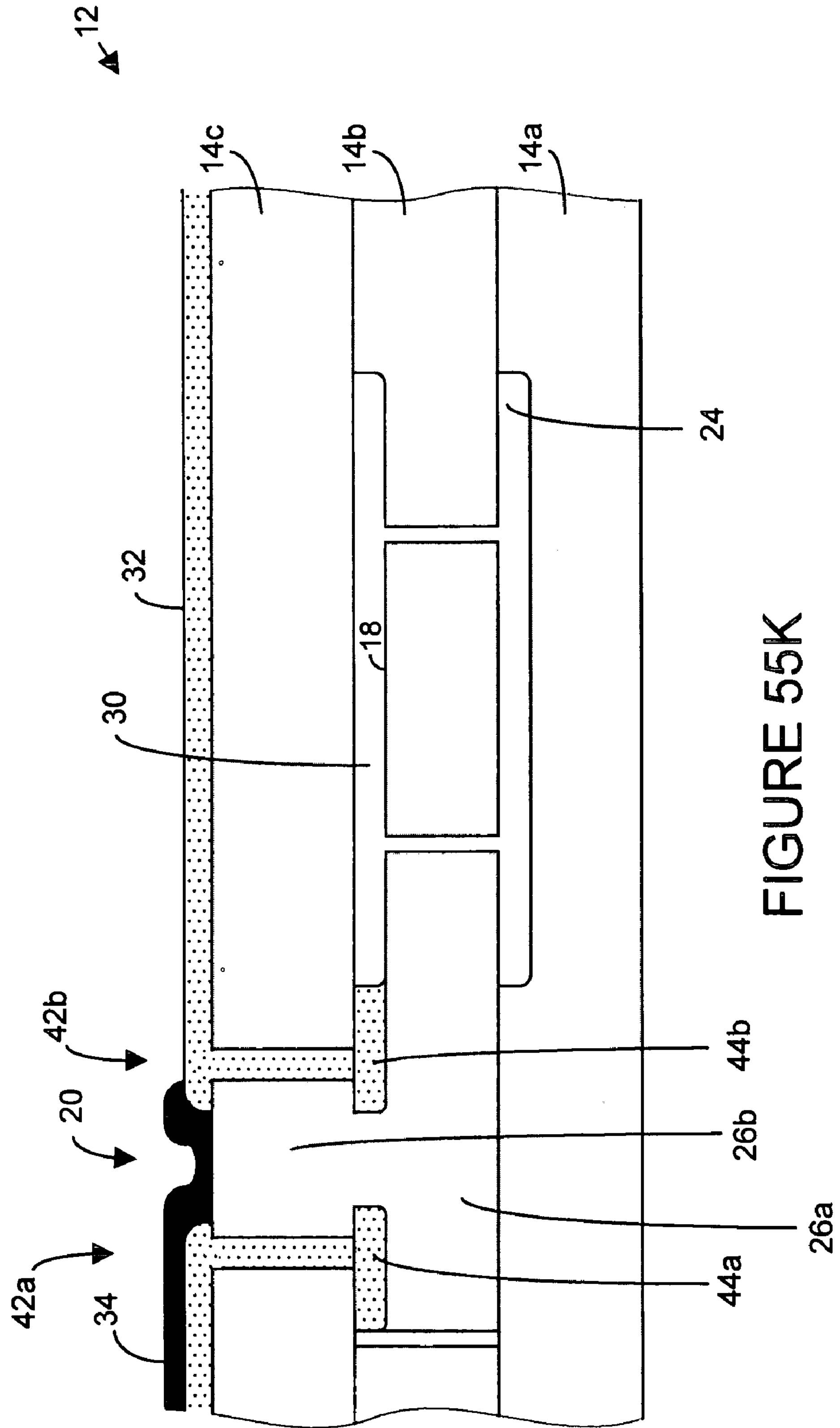

FIGURE 55K

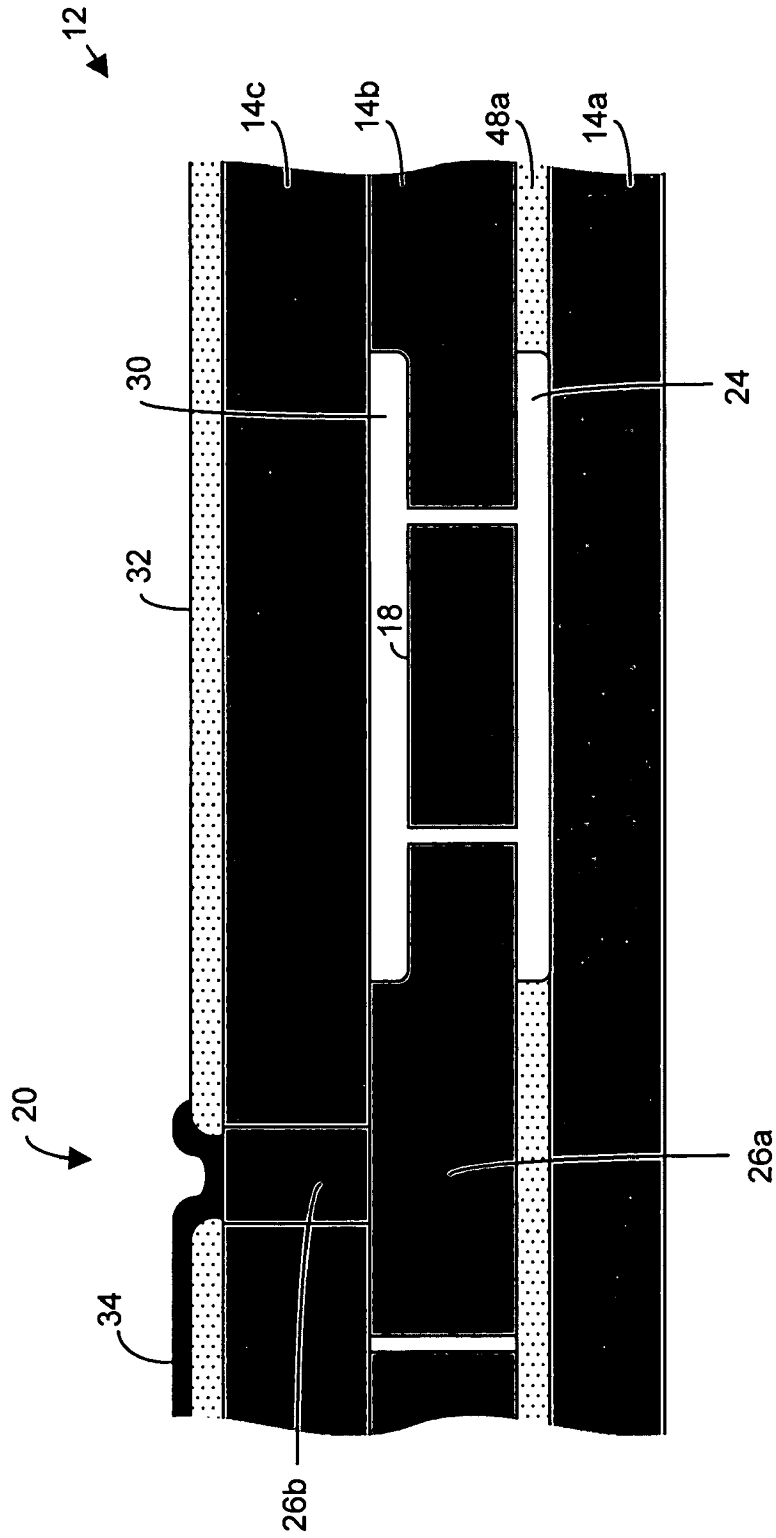

FIGURE 56

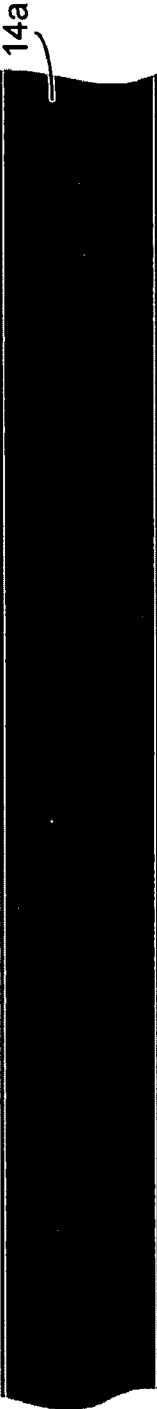

FIGURE 57A

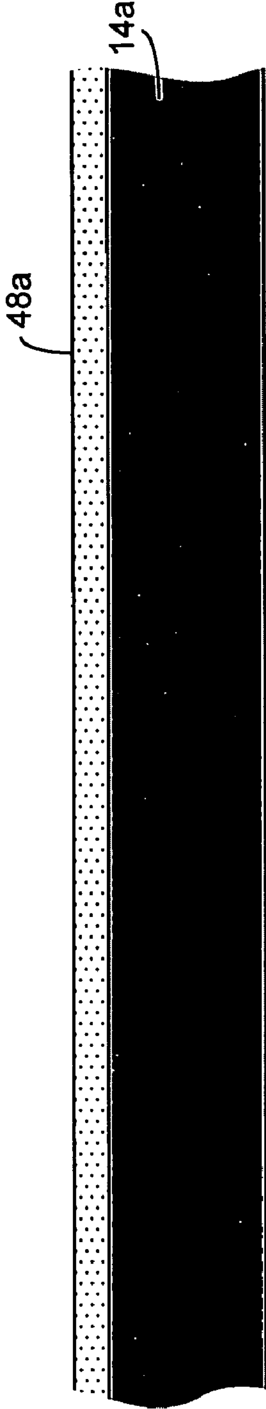

FIGURE 57B

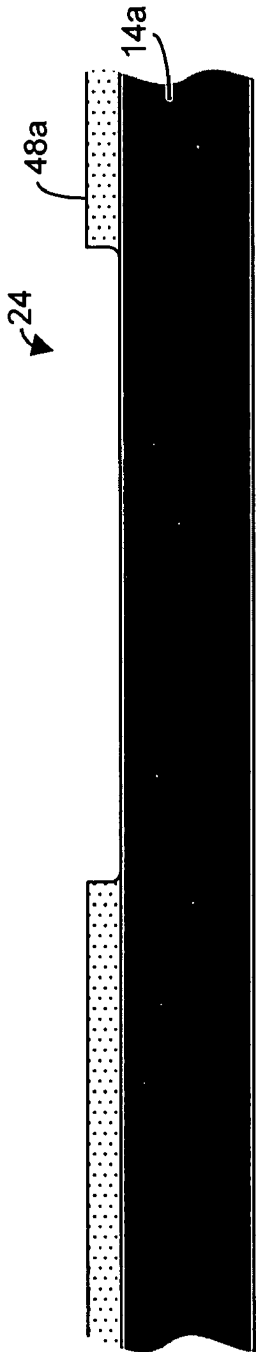

FIGURE 57C

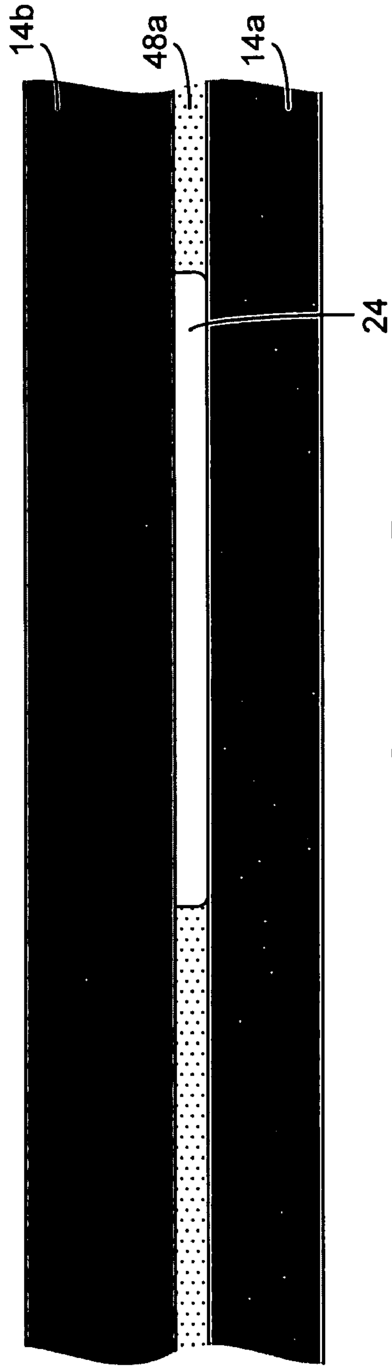

FIGURE 57D

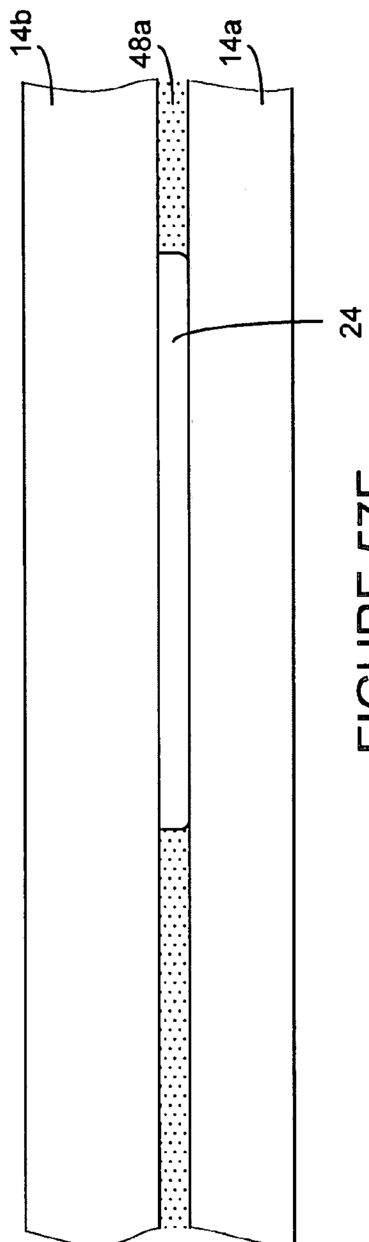

FIGURE 57E

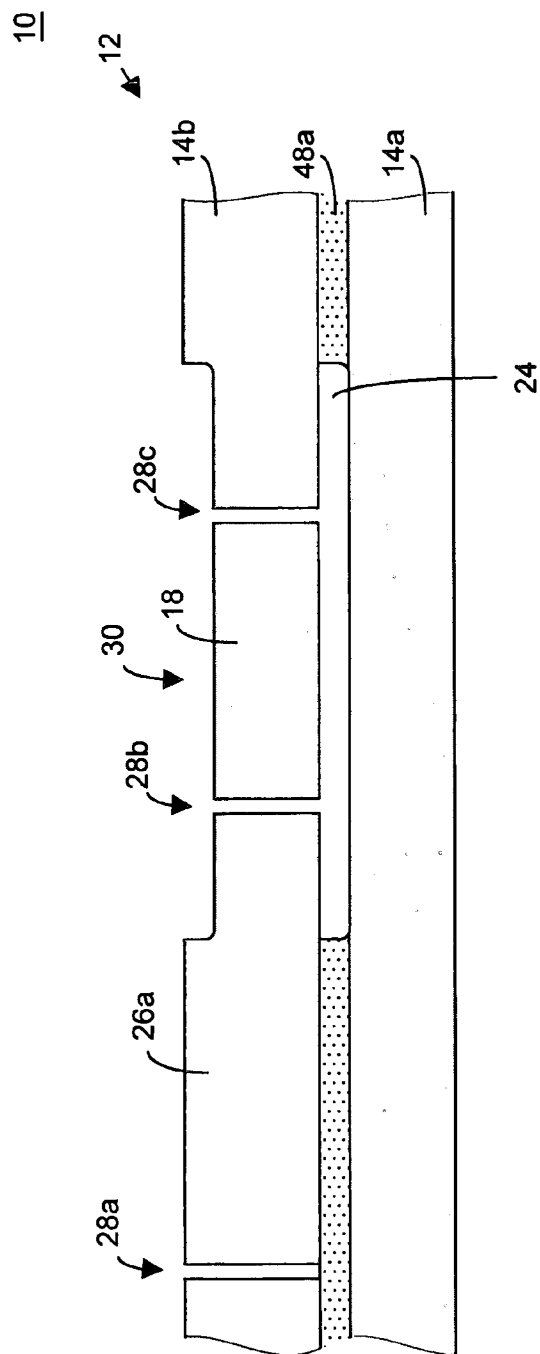

FIGURE 57F

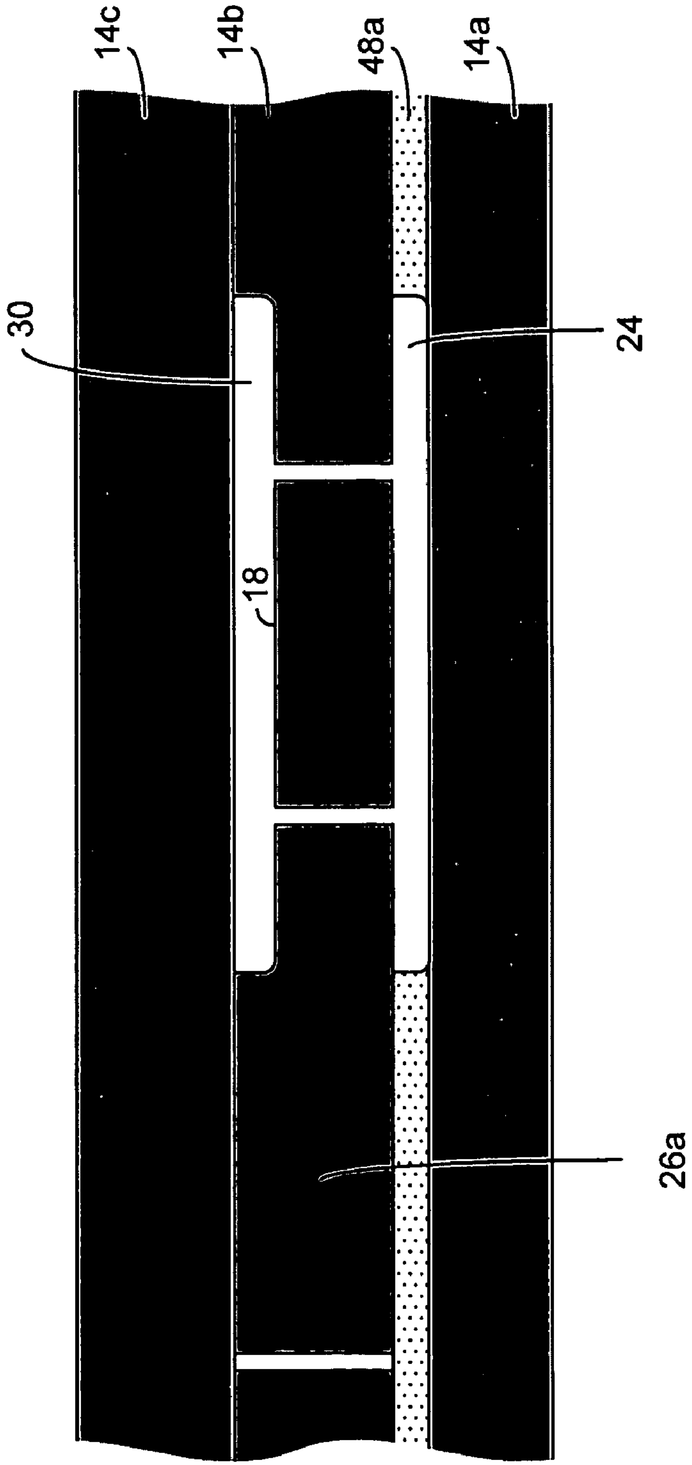

FIGURE 57G

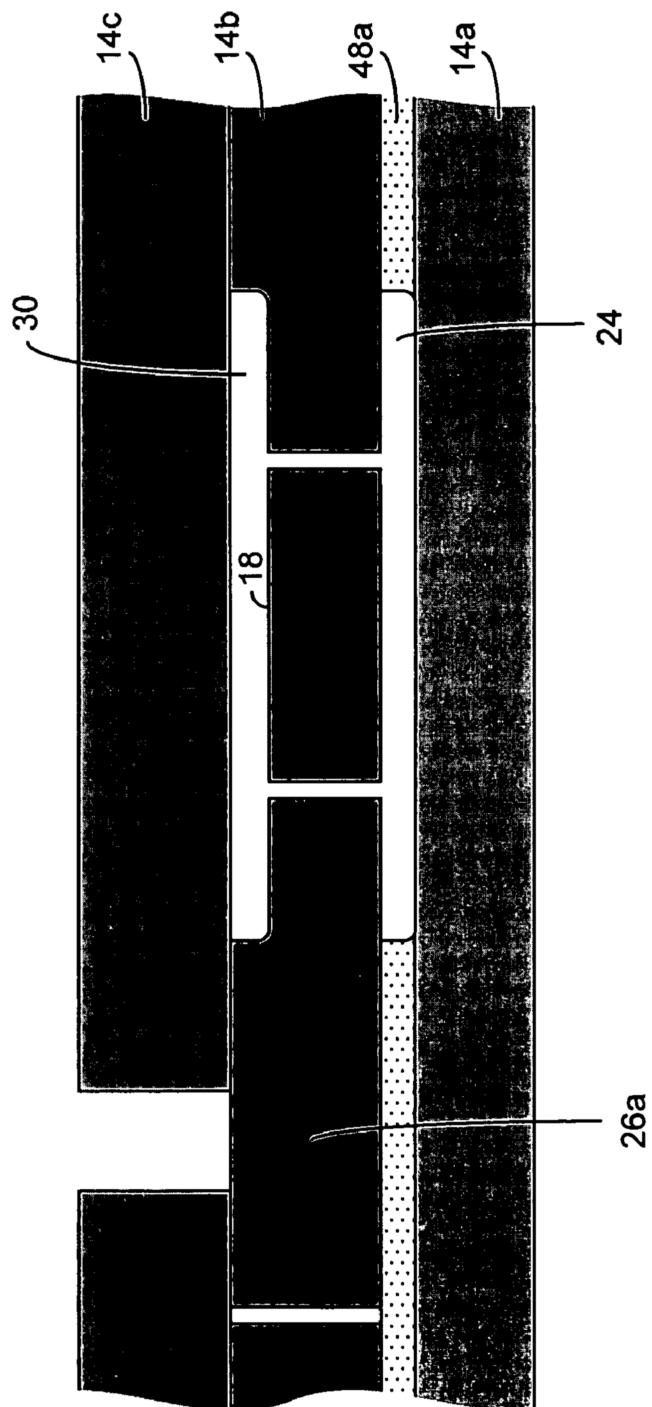

FIGURE 57H

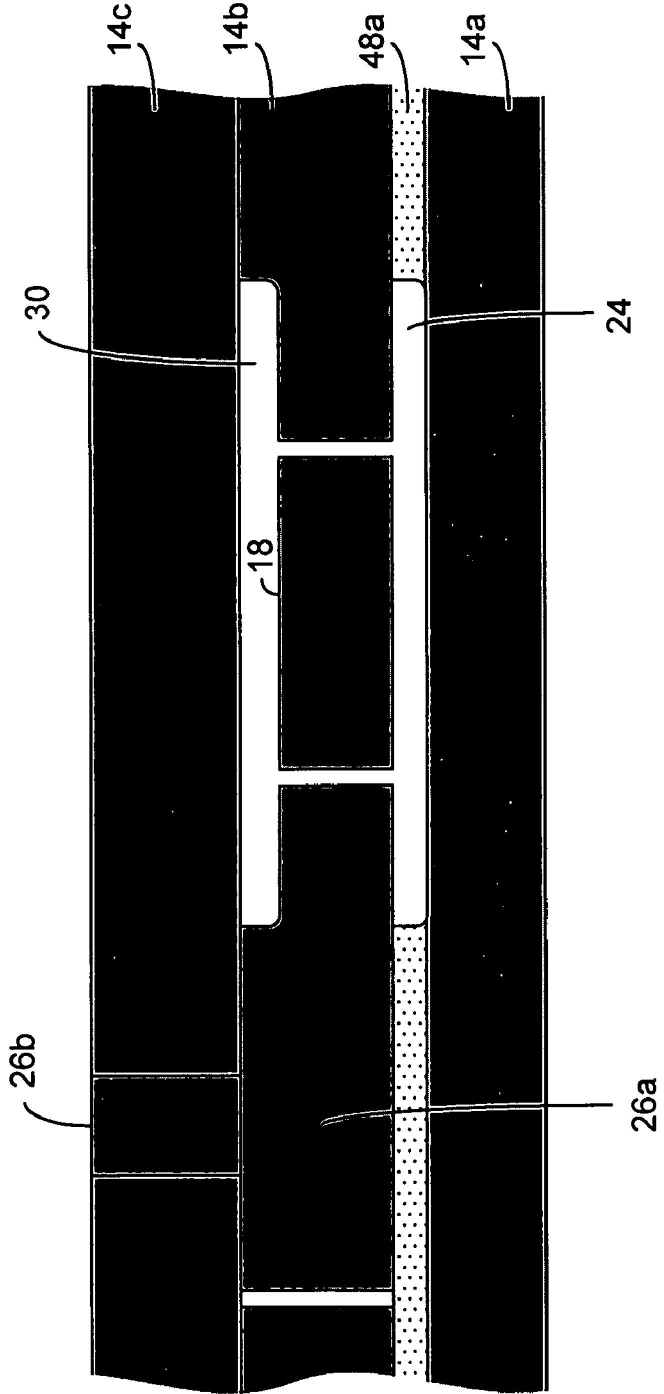

FIGURE 57I

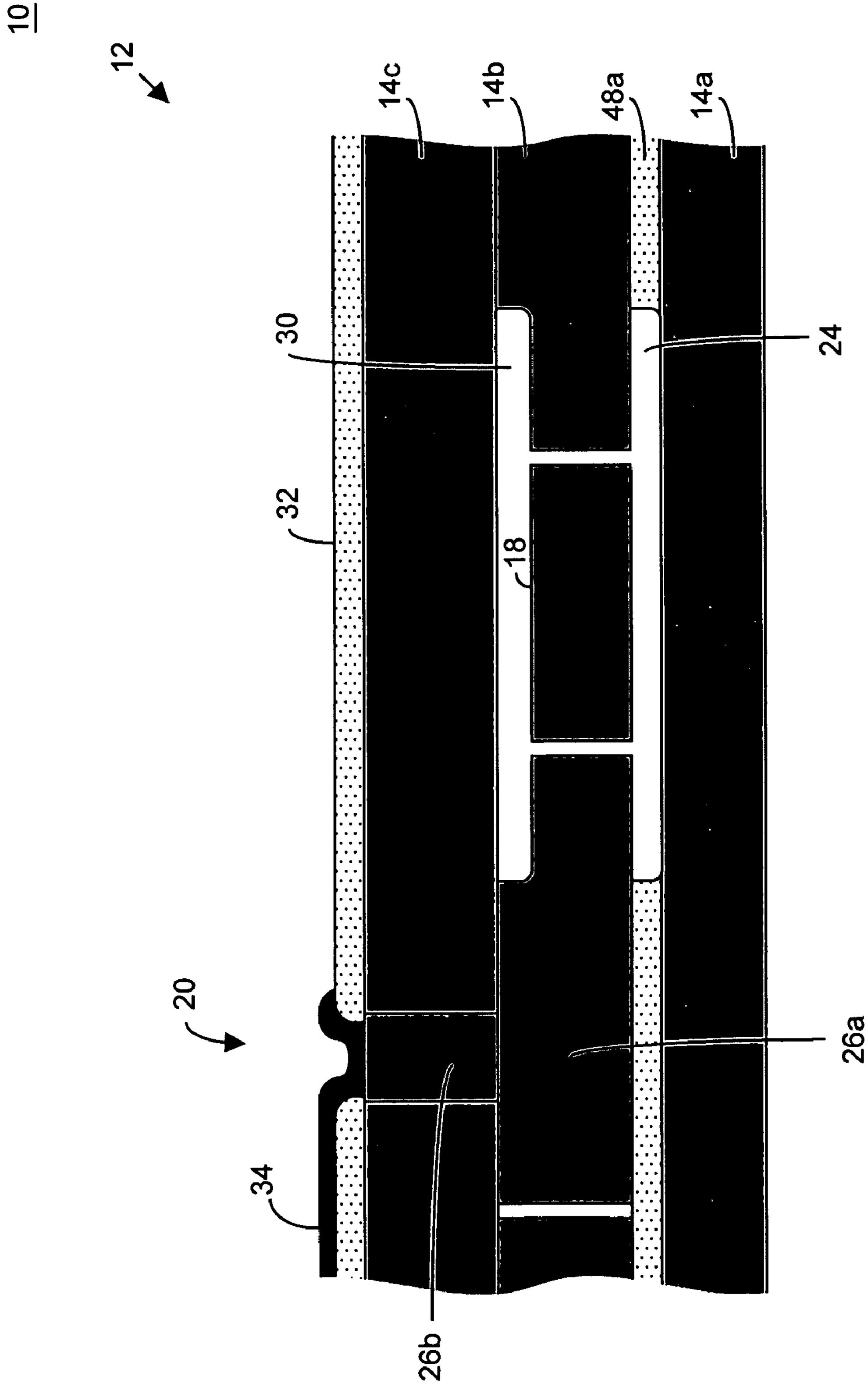

FIGURE 57J

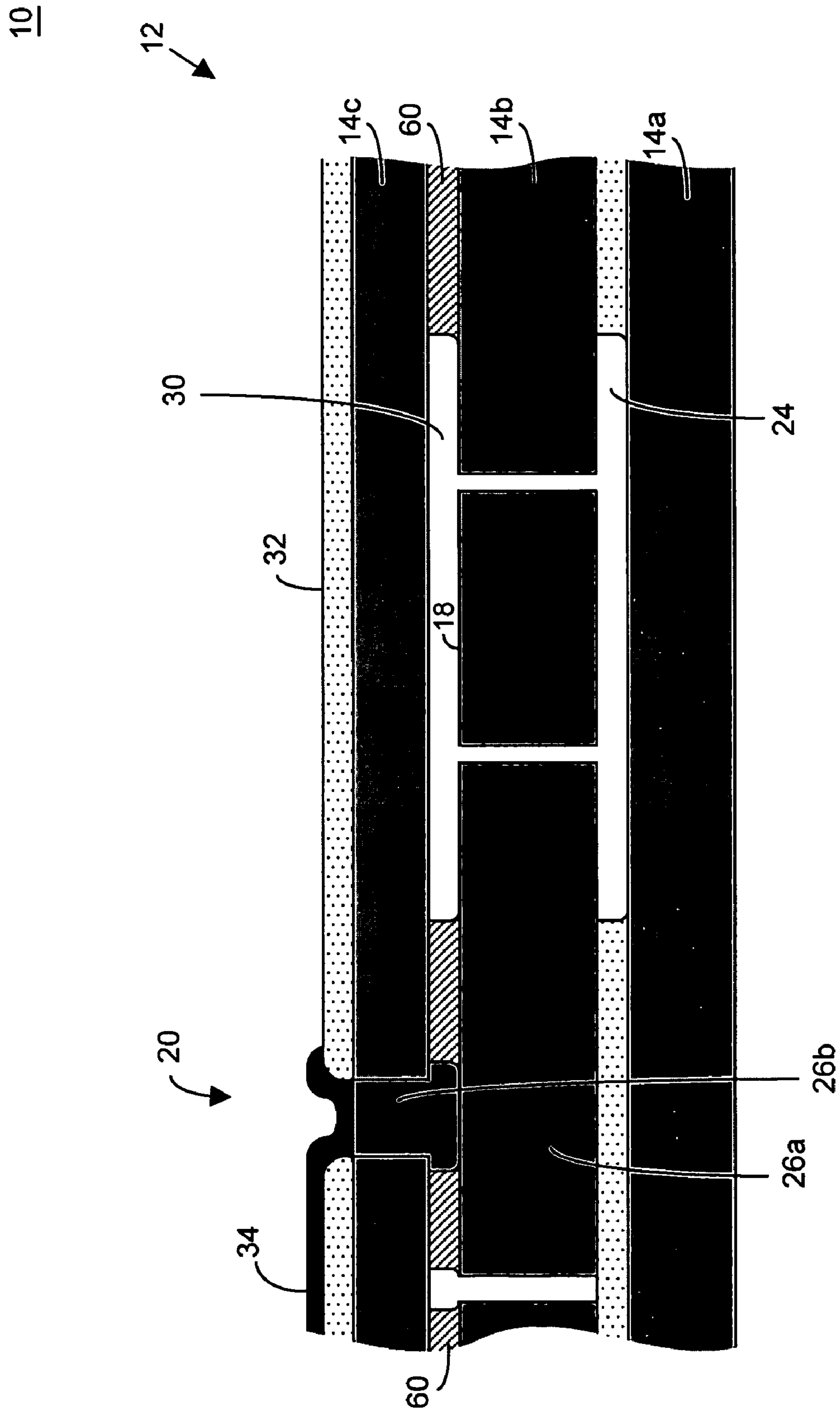

FIGURE 58

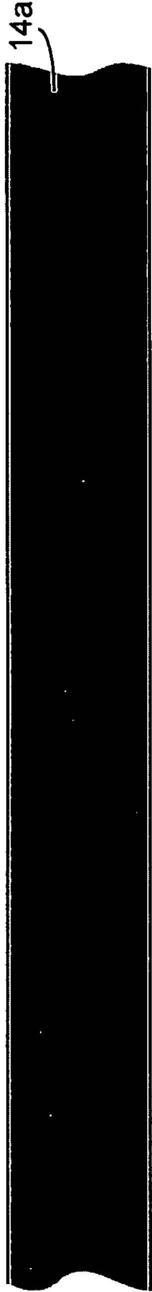

FIGURE 59A

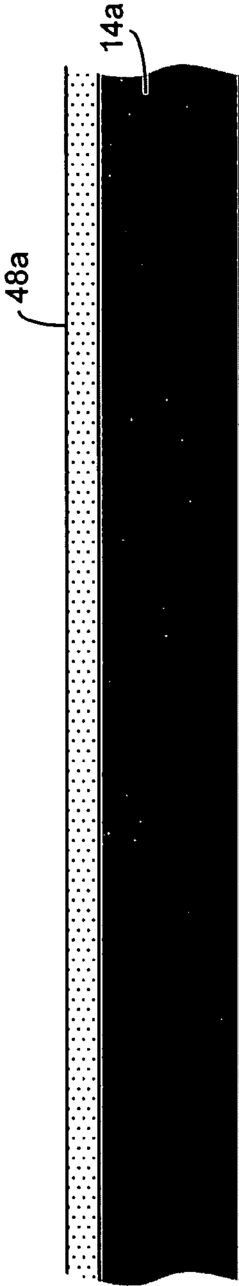

FIGURE 59B

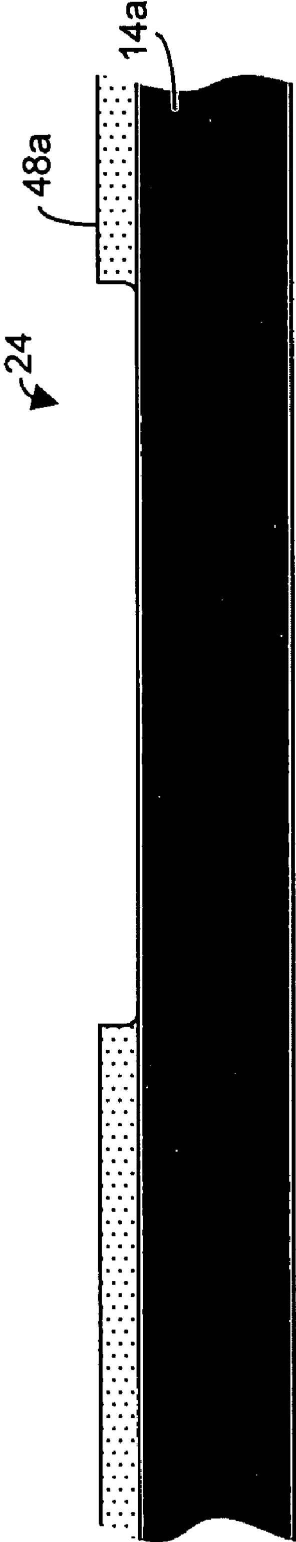

FIGURE 59C

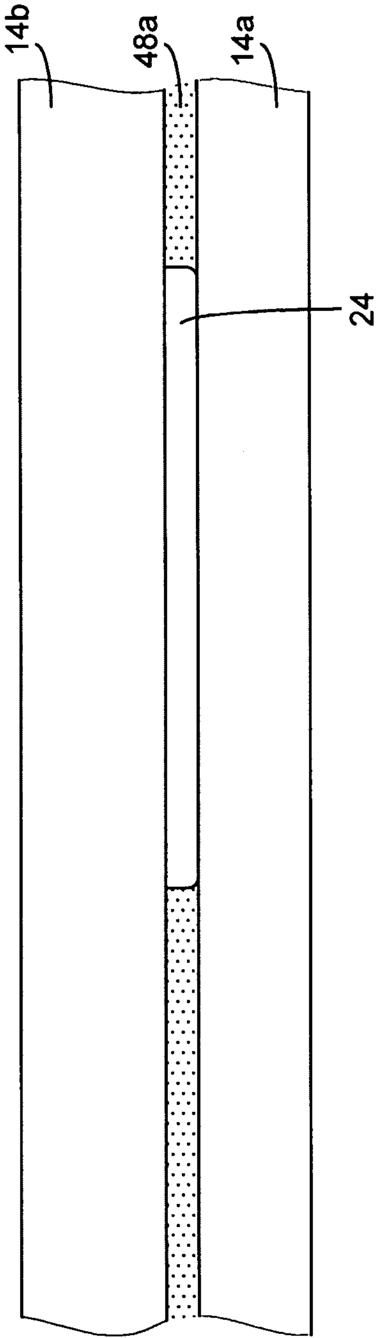

FIGURE 59D

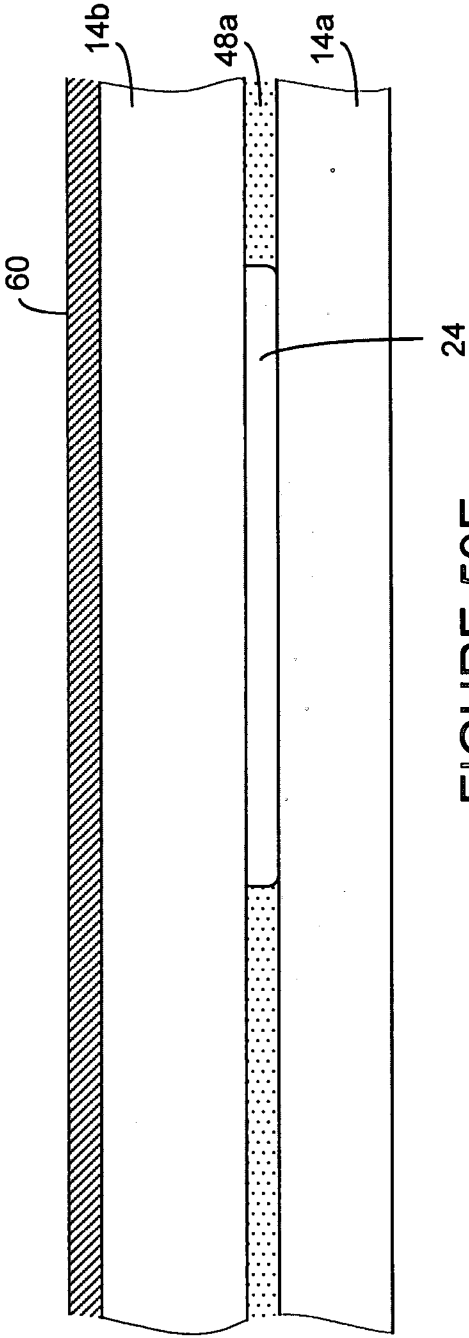

FIGURE 59E

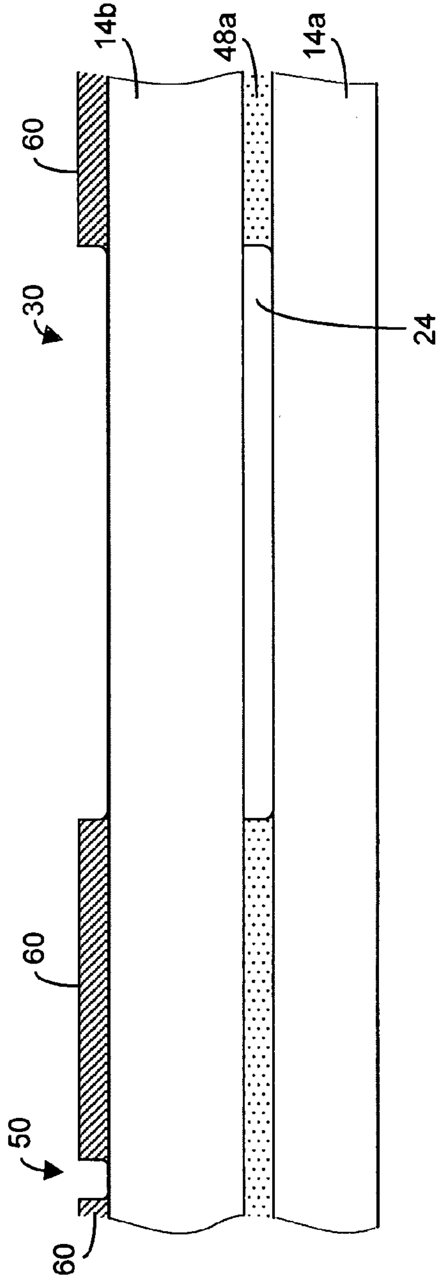

FIGURE 59F

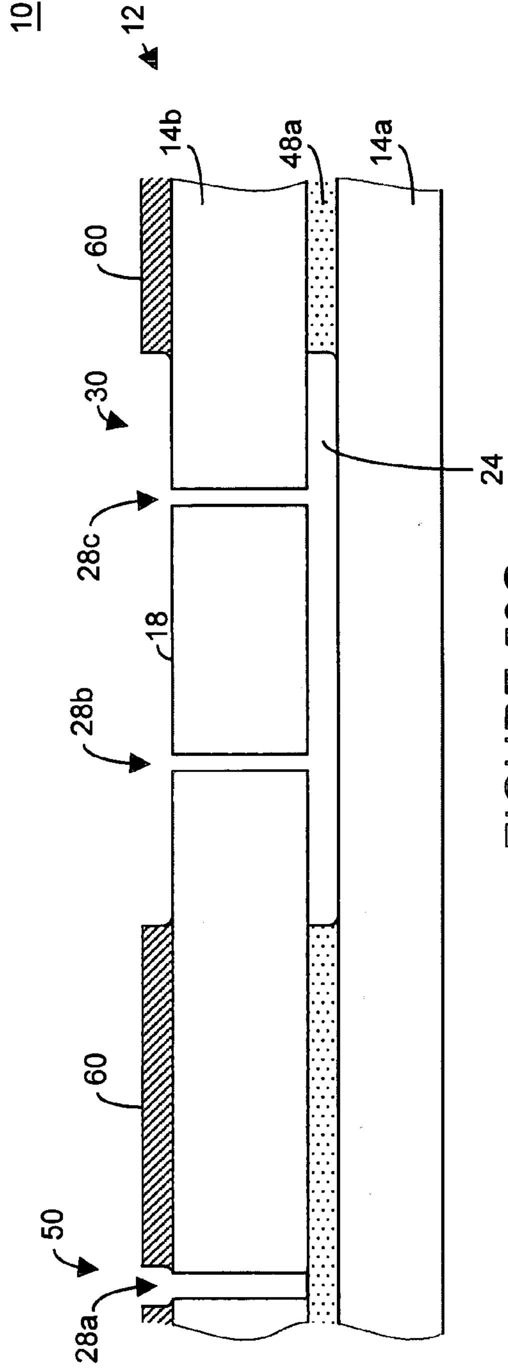

FIGURE 59G

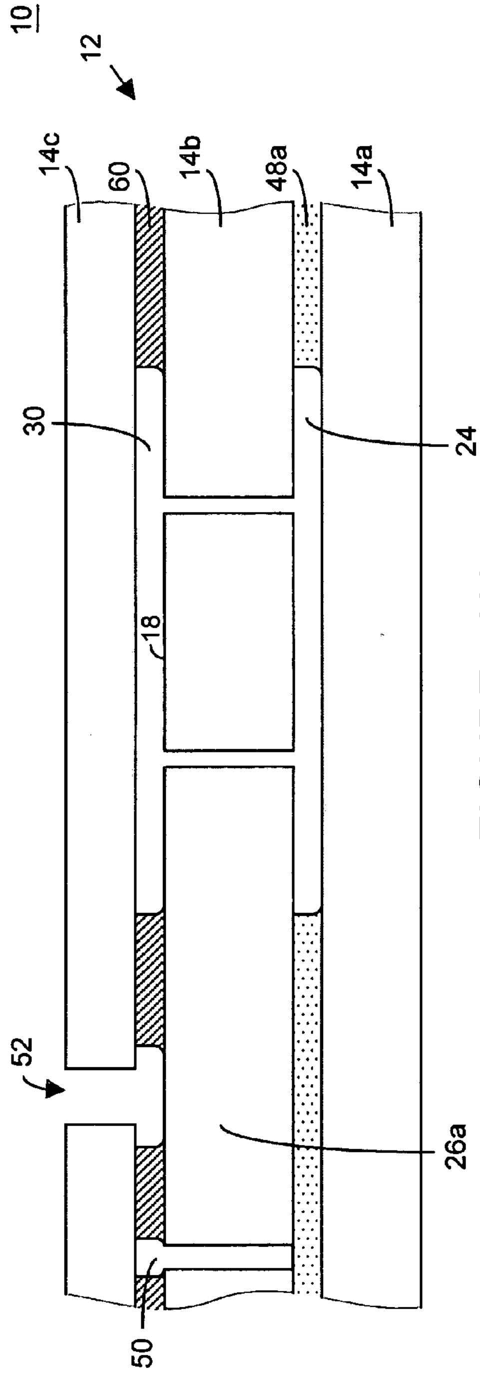

FIGURE 59H

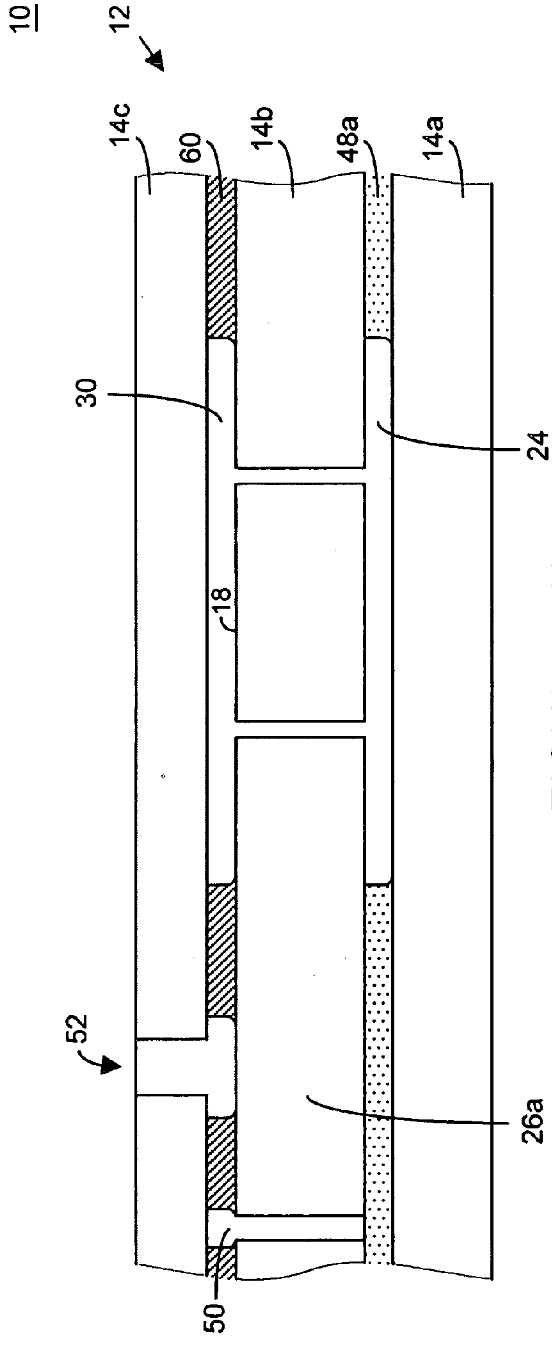

FIGURE 59I

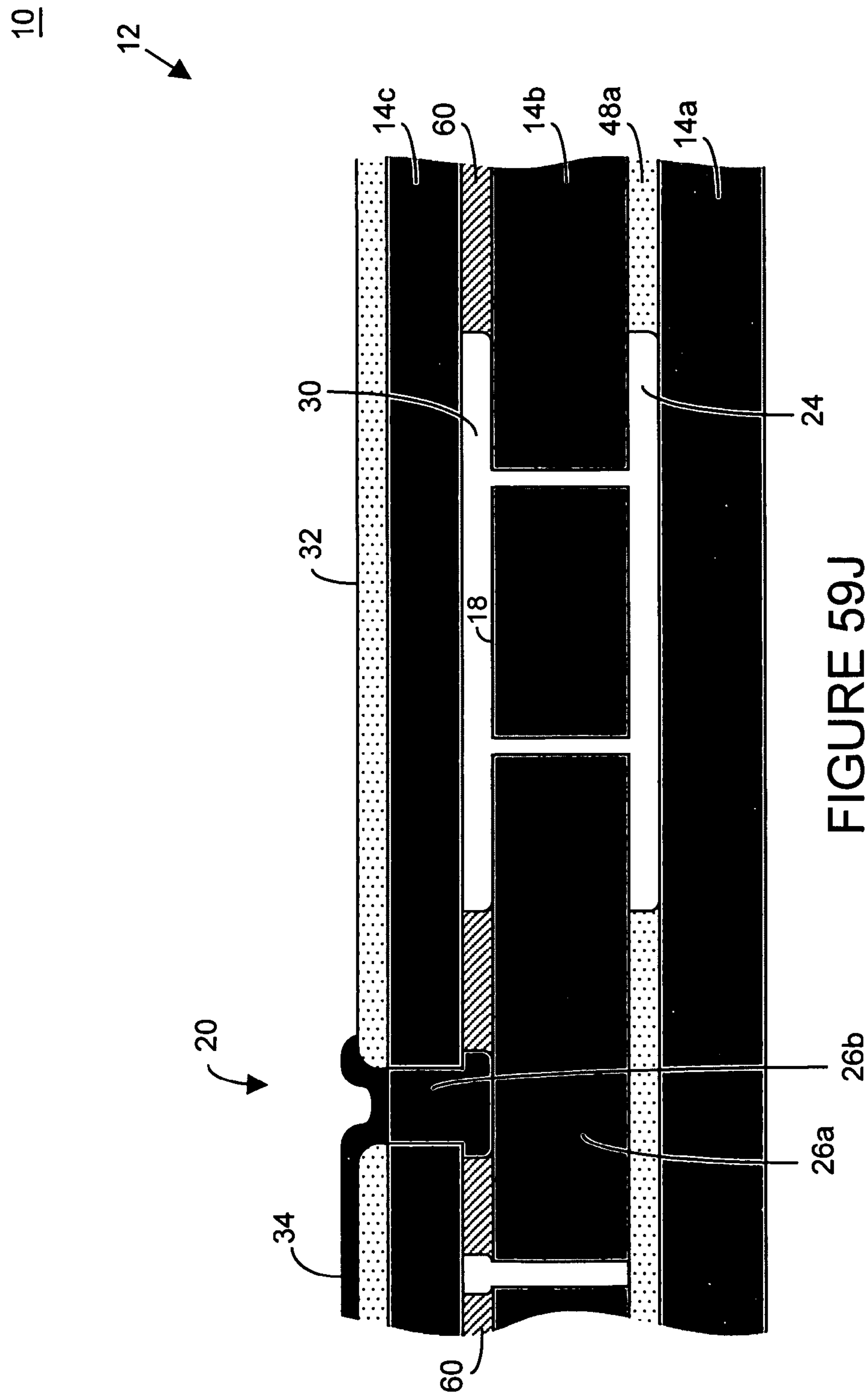

FIGURE 59J

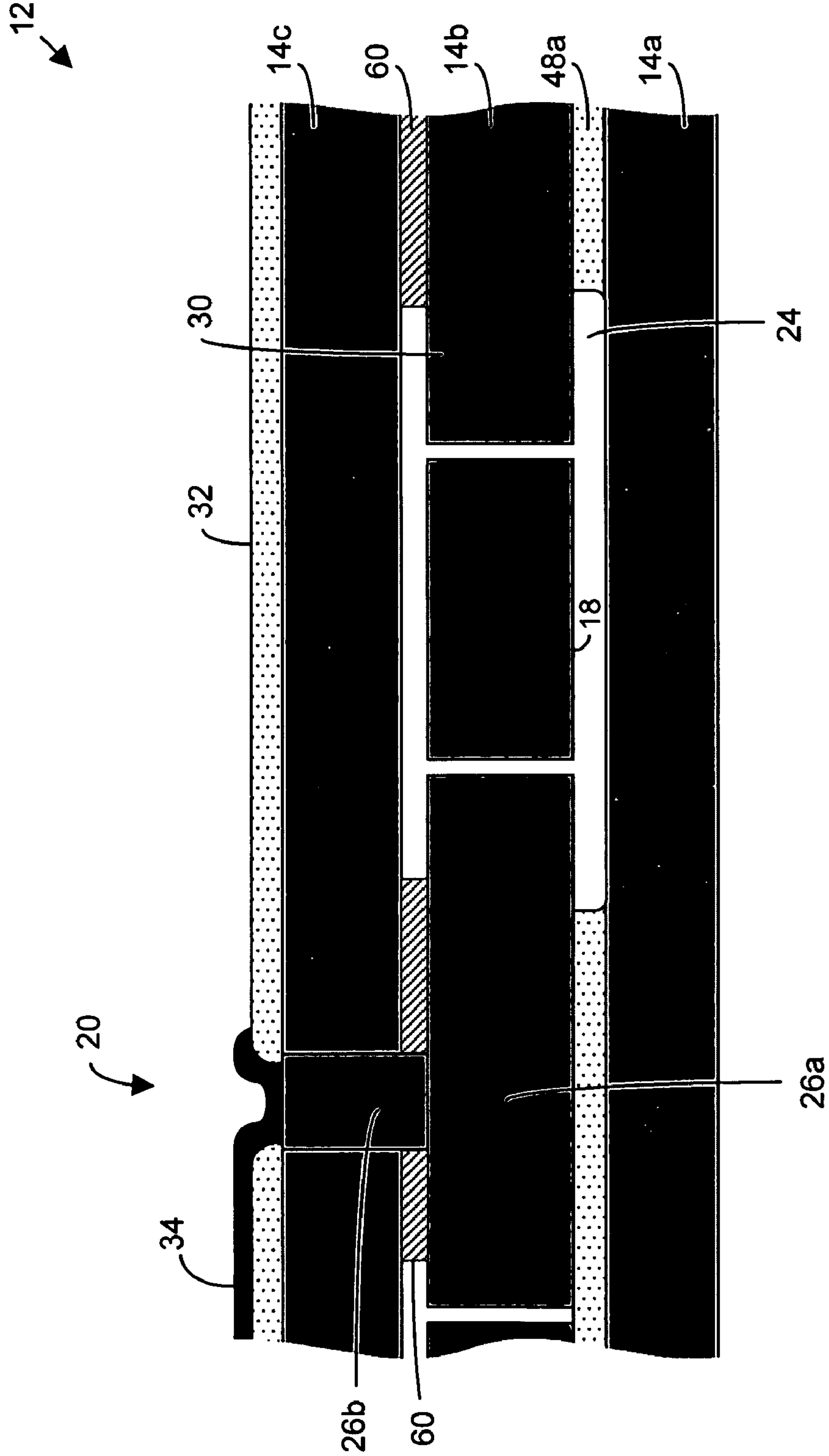

FIGURE 60

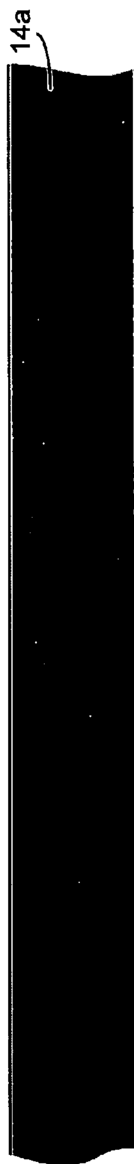

FIGURE 61A

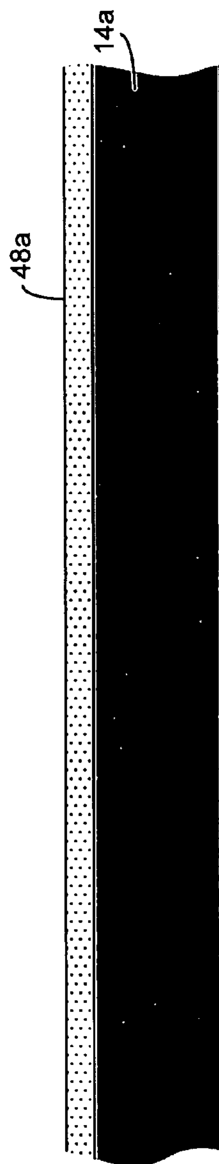

FIGURE 61B

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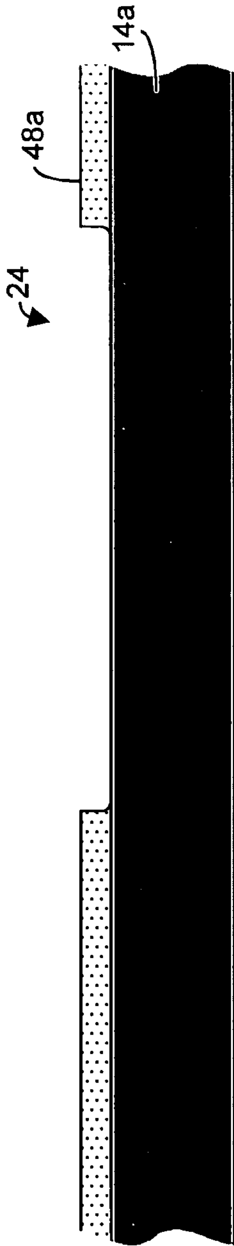

FIGURE 61C

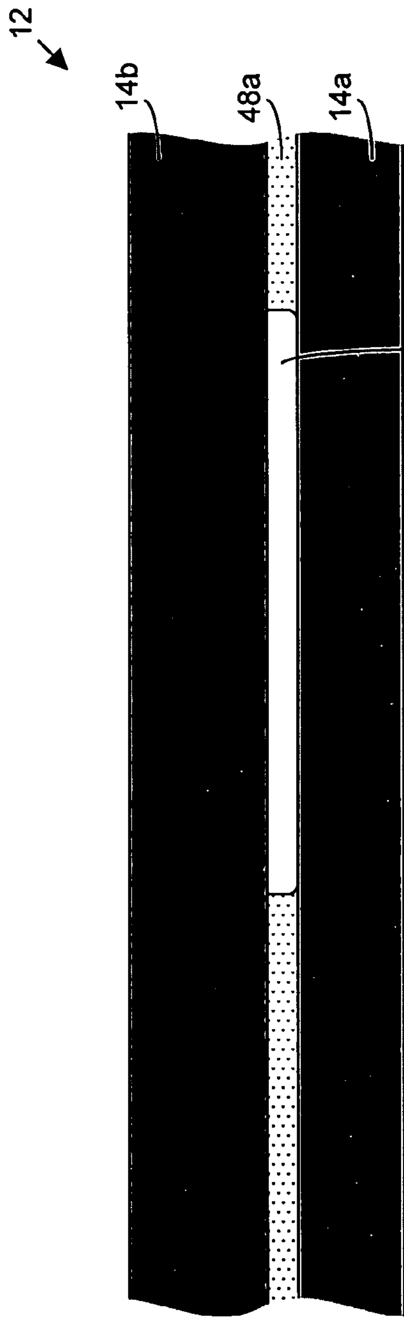

FIGURE 61D

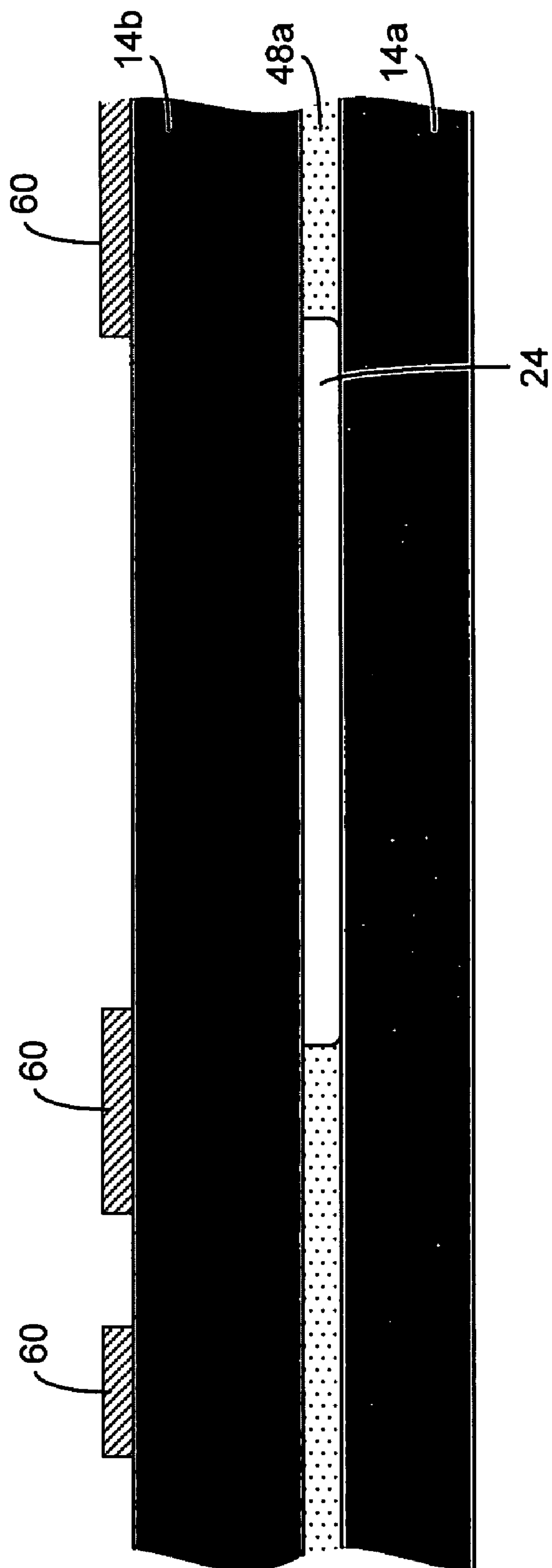

FIGURE 61E

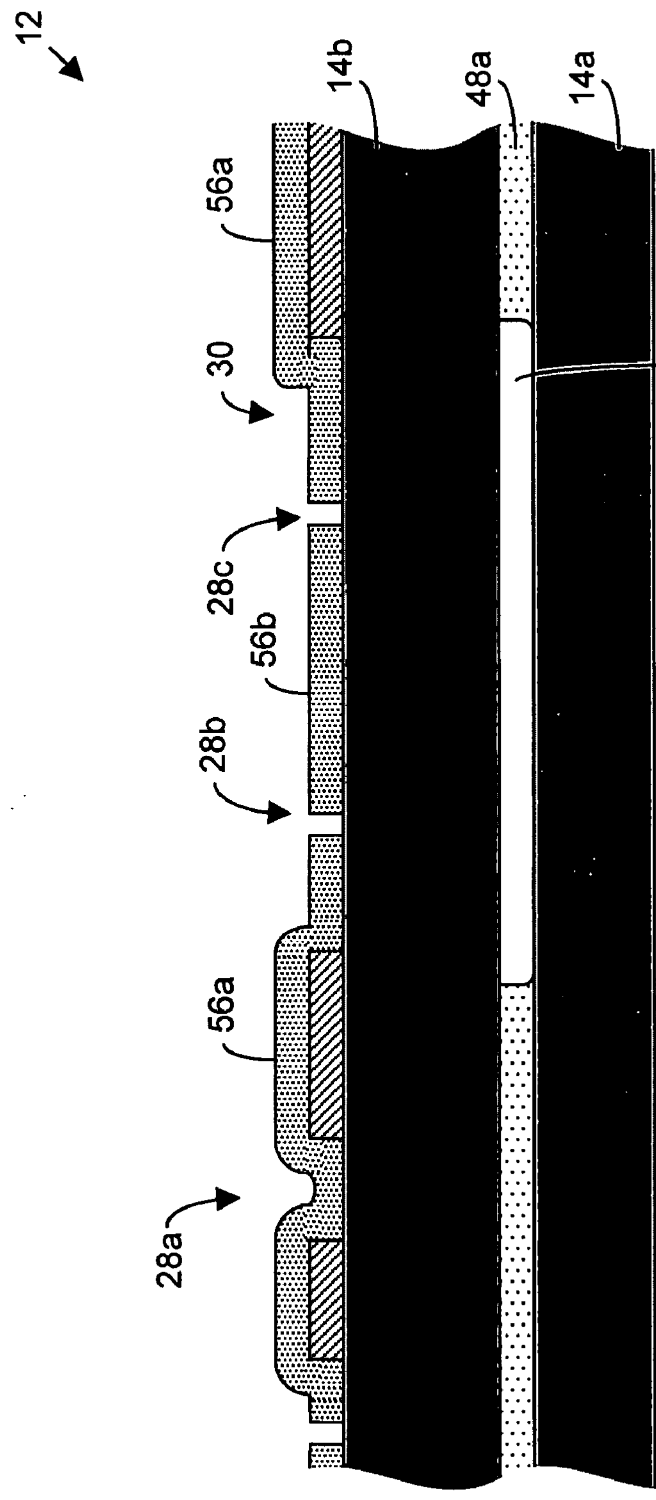

FIGURE 61F

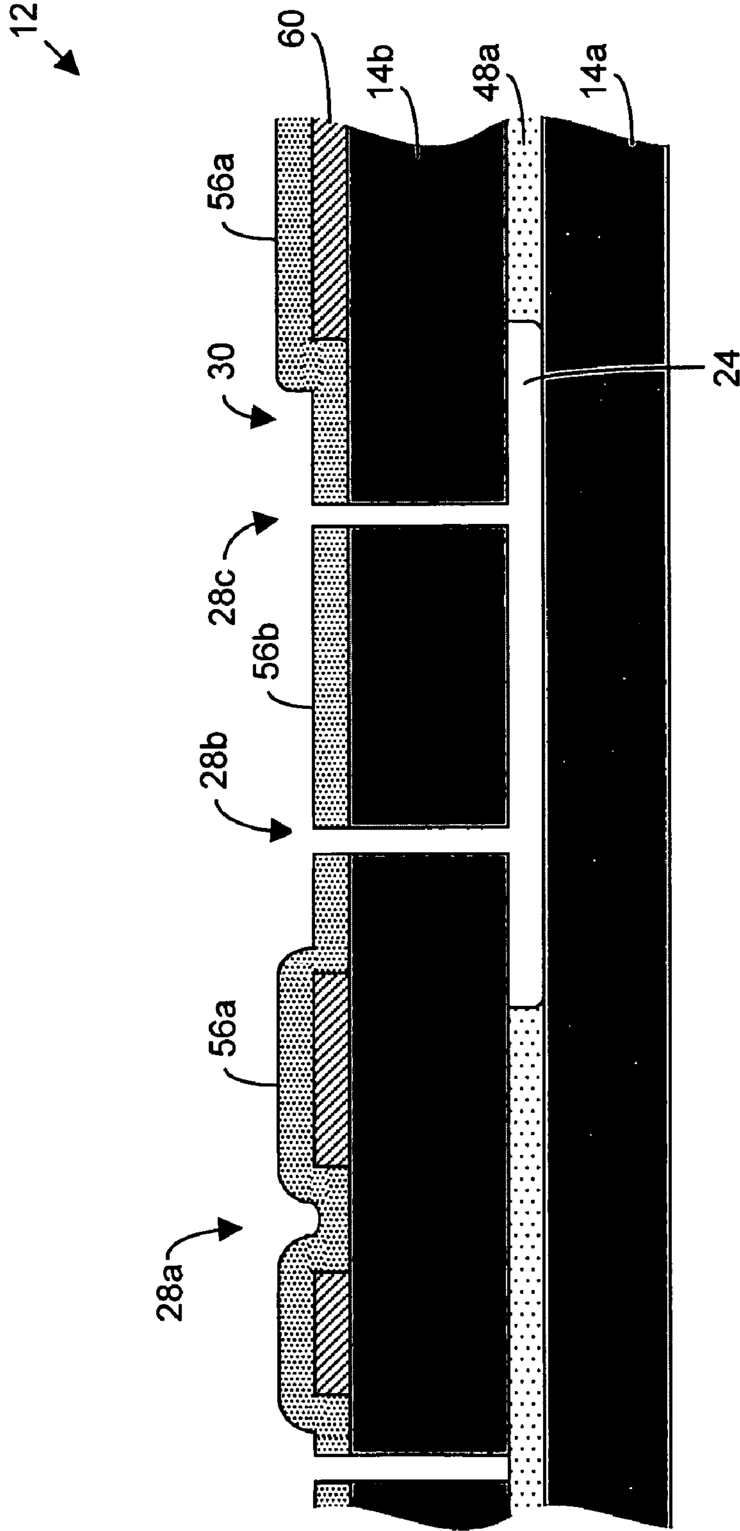

FIGURE 61G

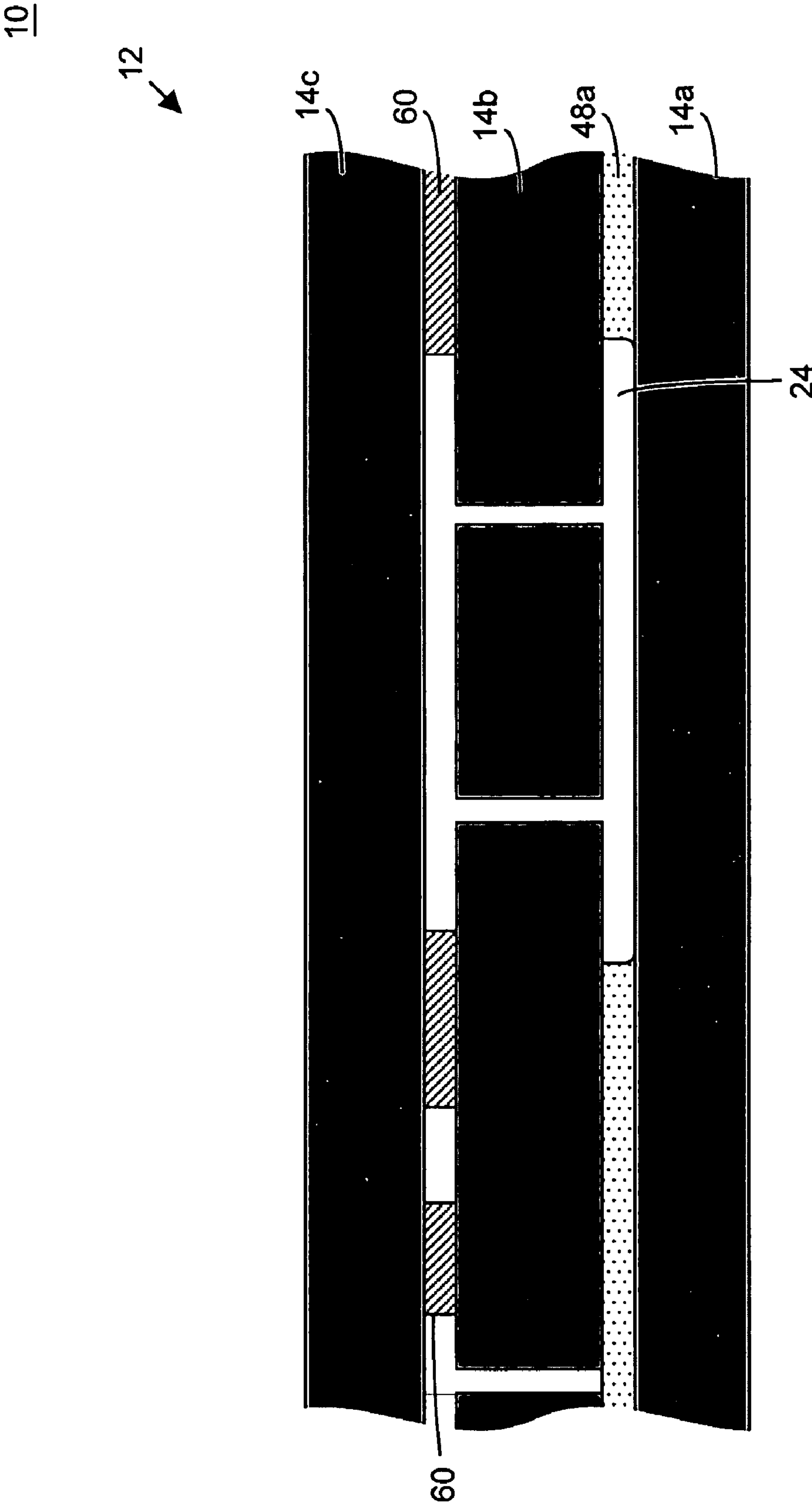

FIGURE 61H

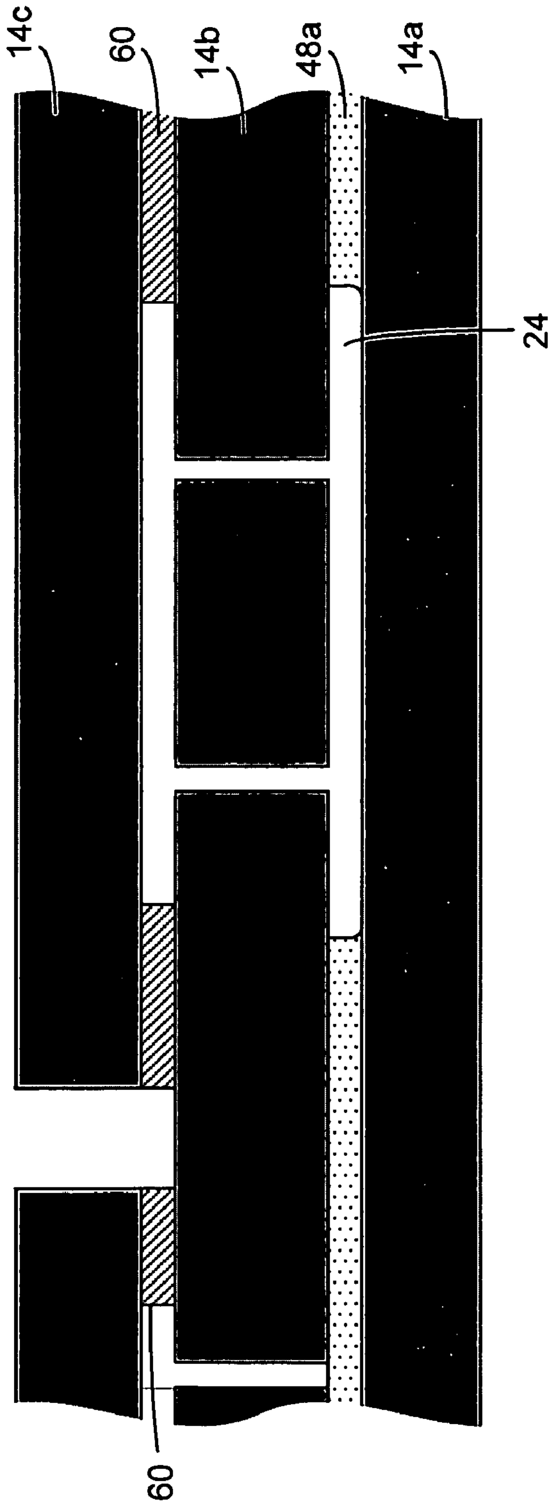

FIGURE 61I

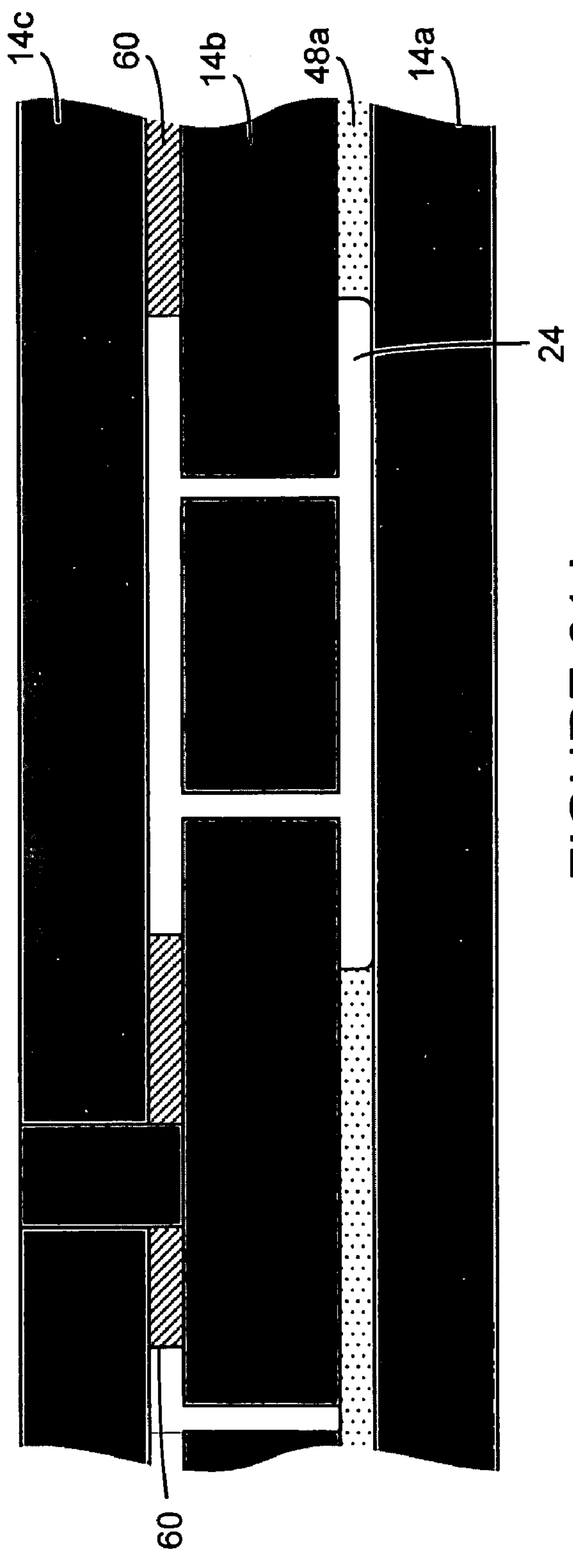

FIGURE 61J

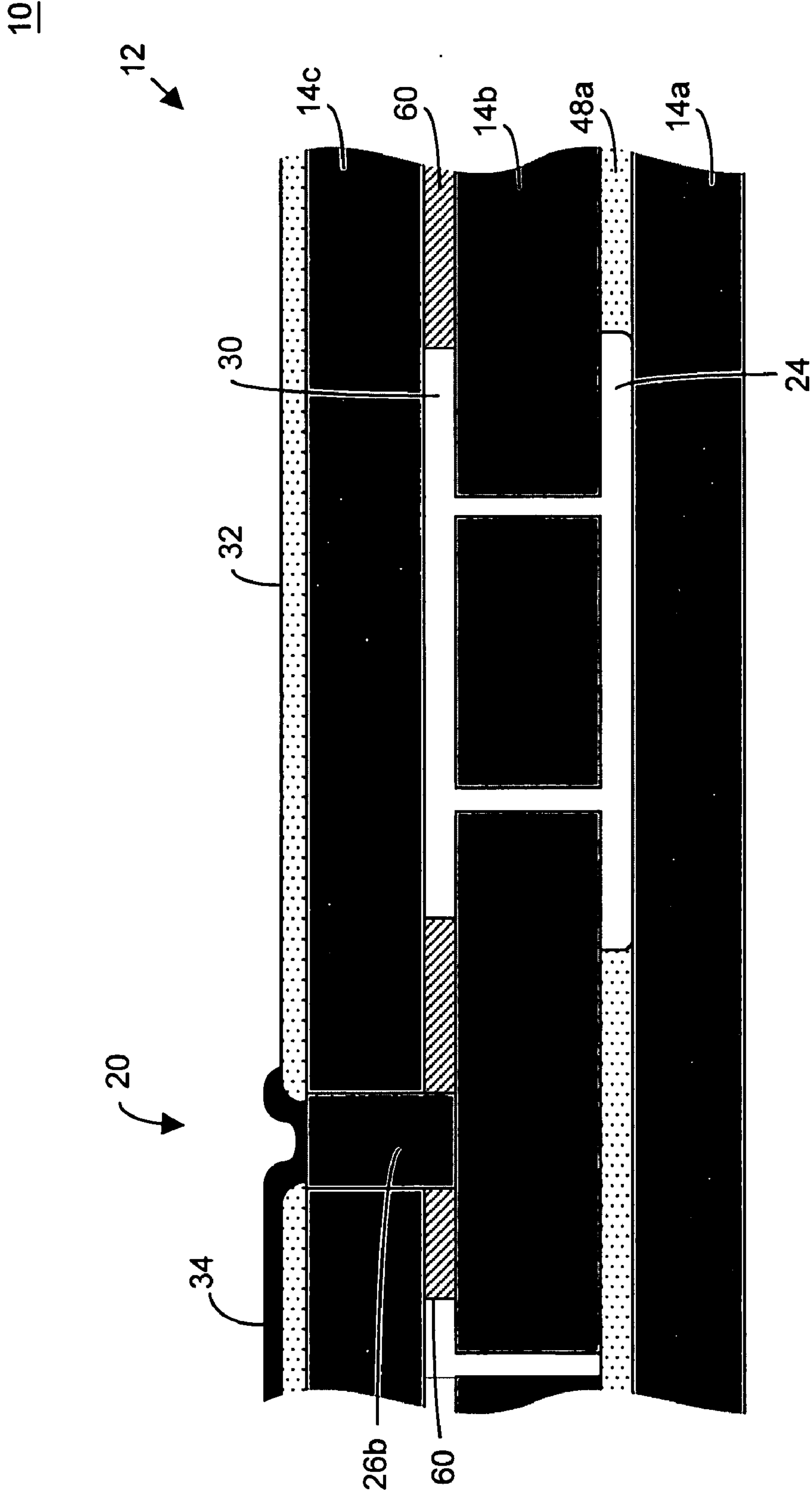

FIGURE 61K

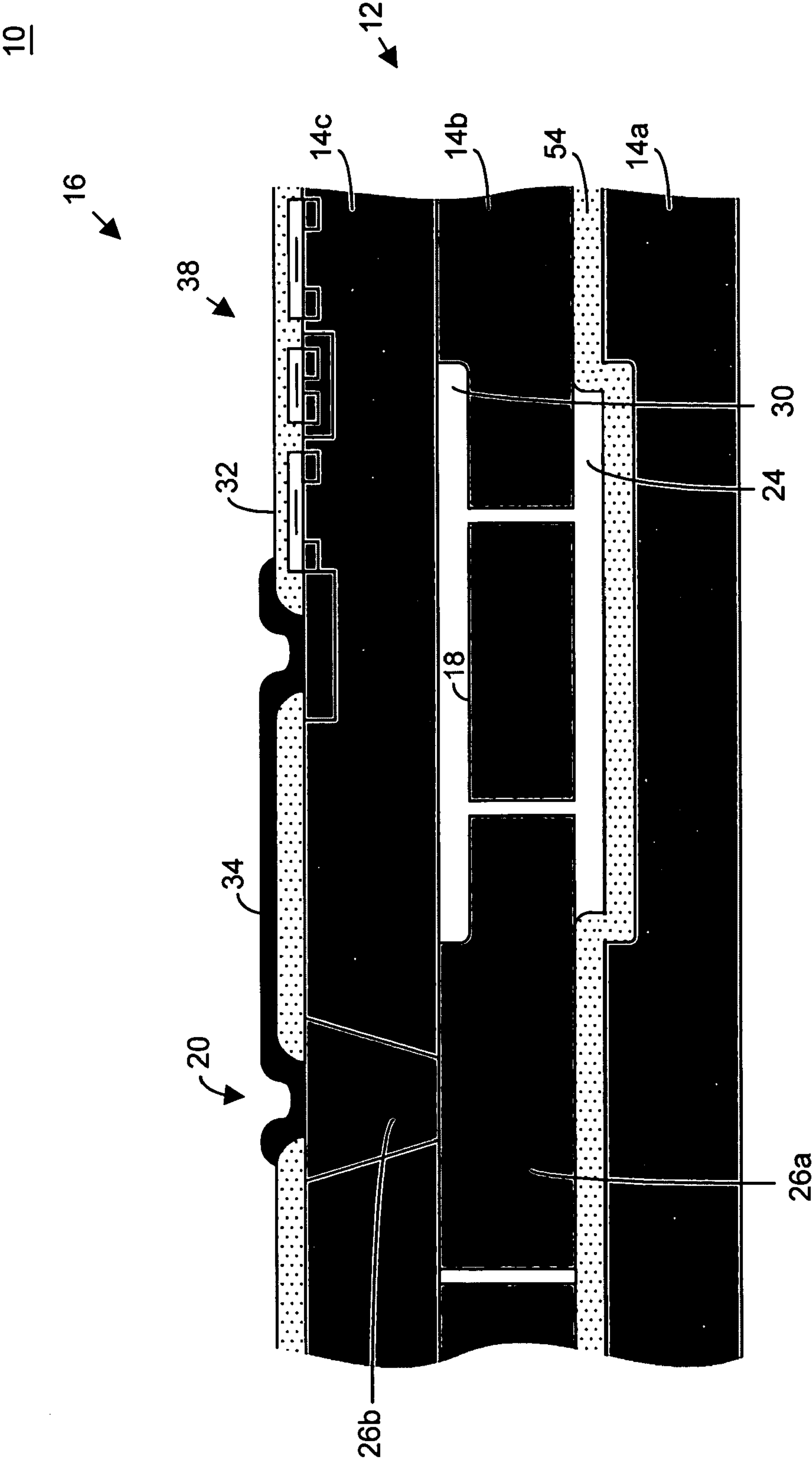

FIGURE 62

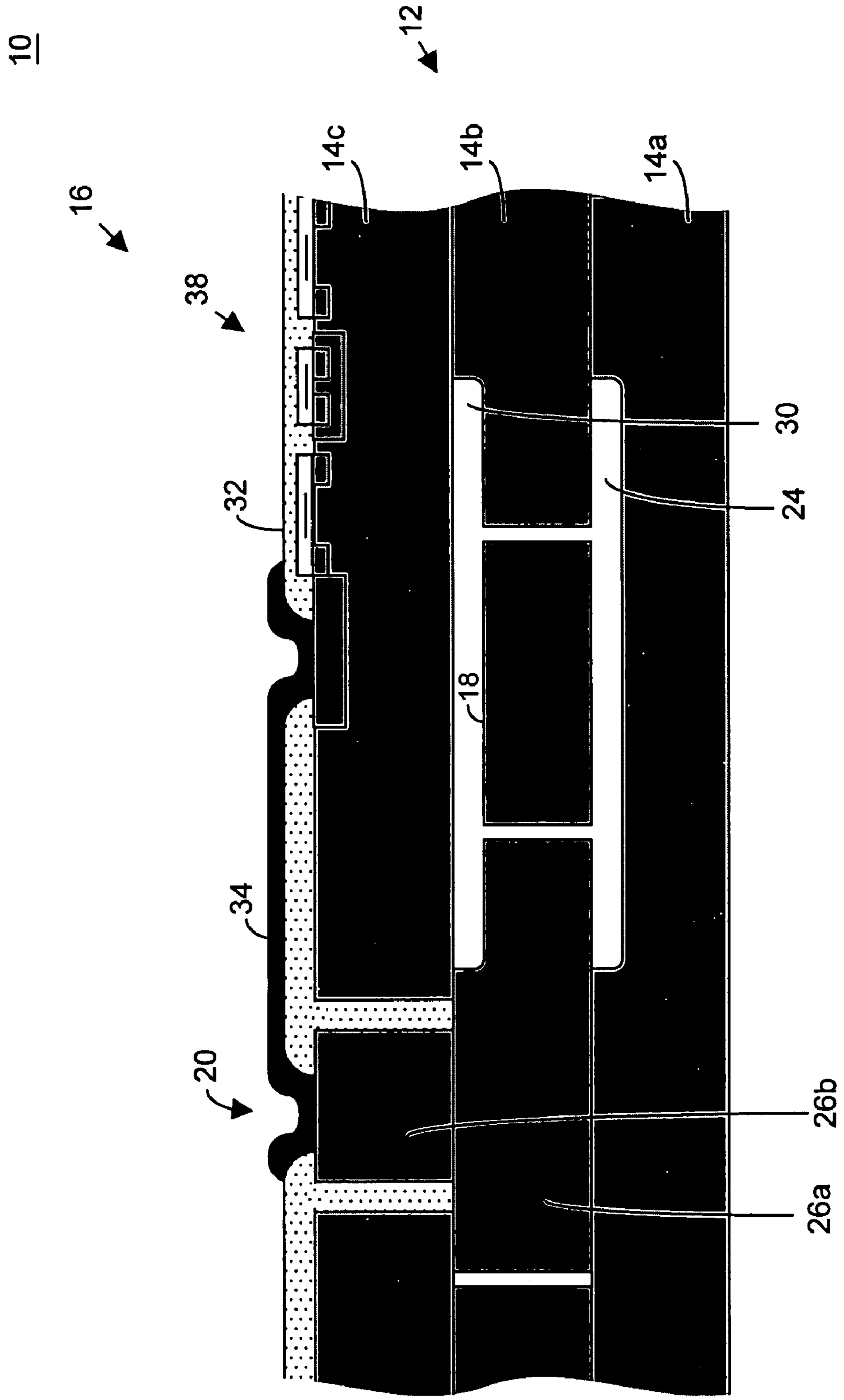

FIGURE 63

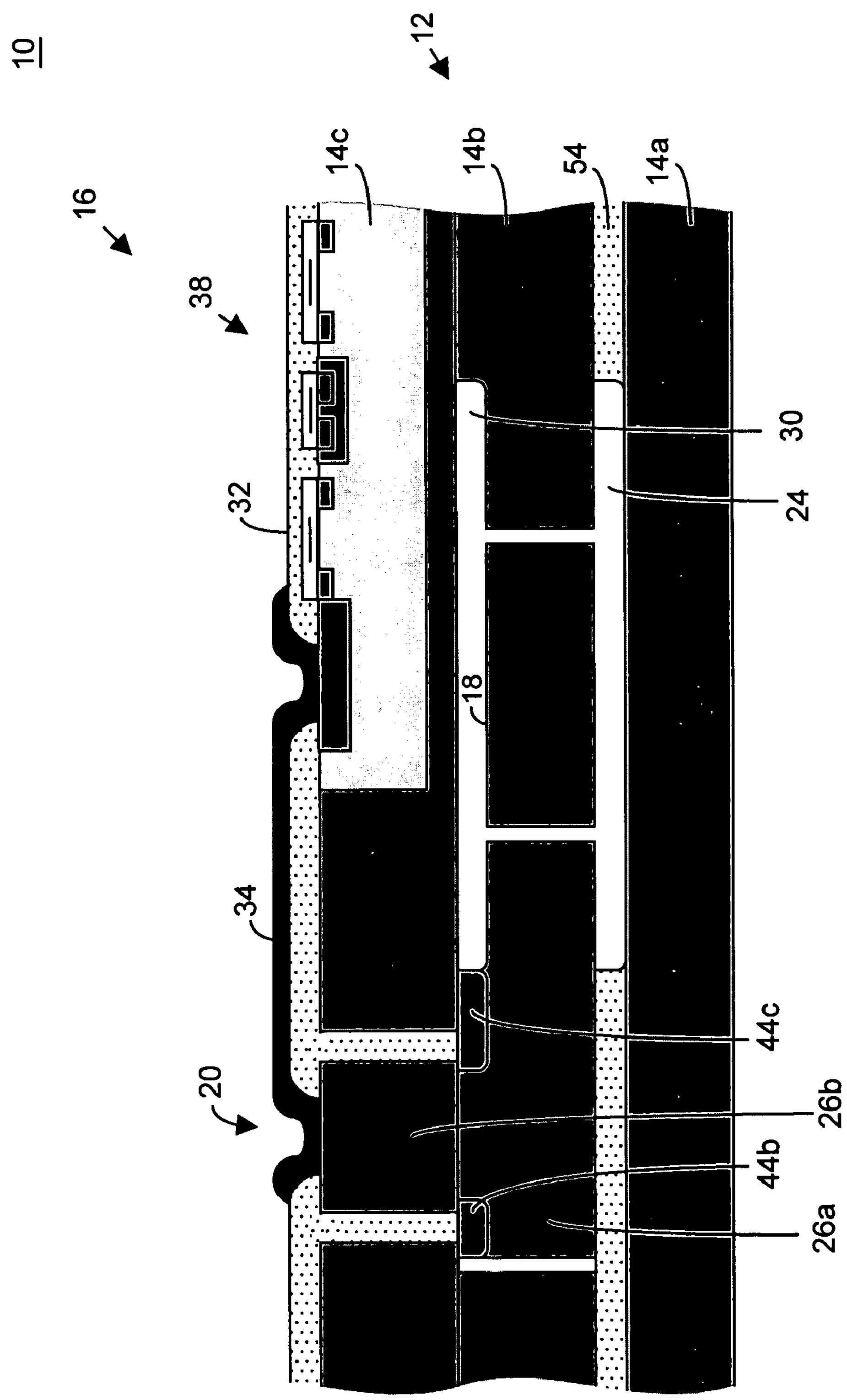

FIGURE 64

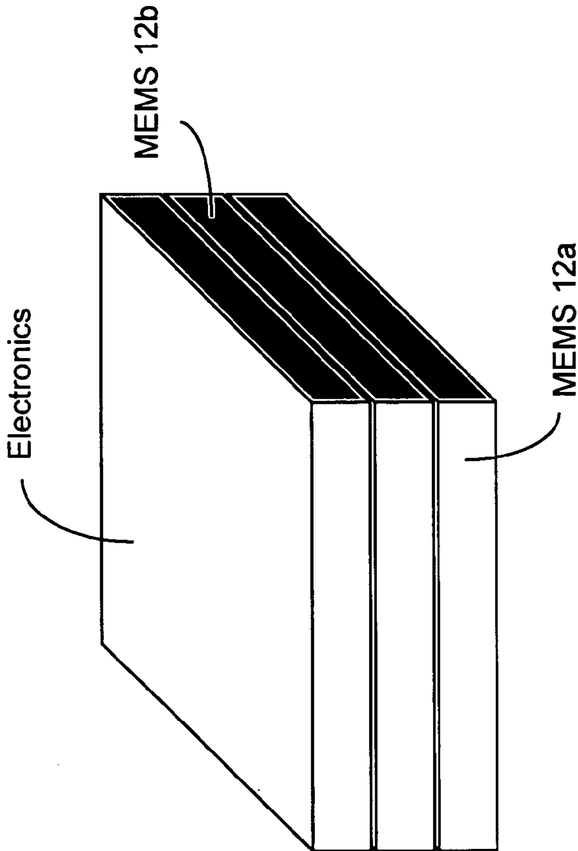

FIGURE 66A

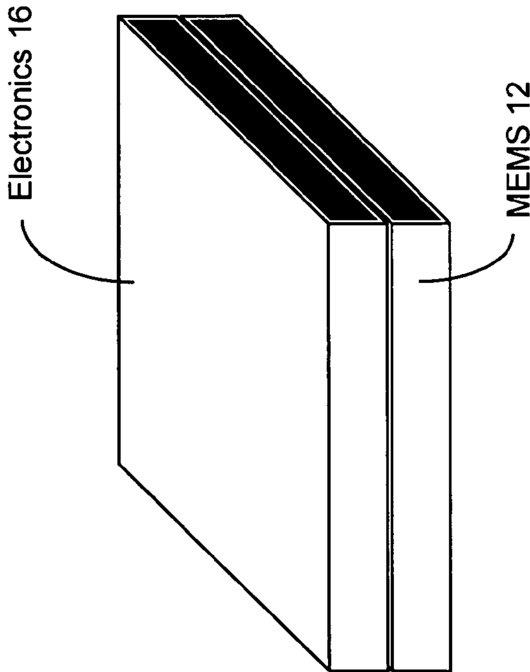

FIGURE 65

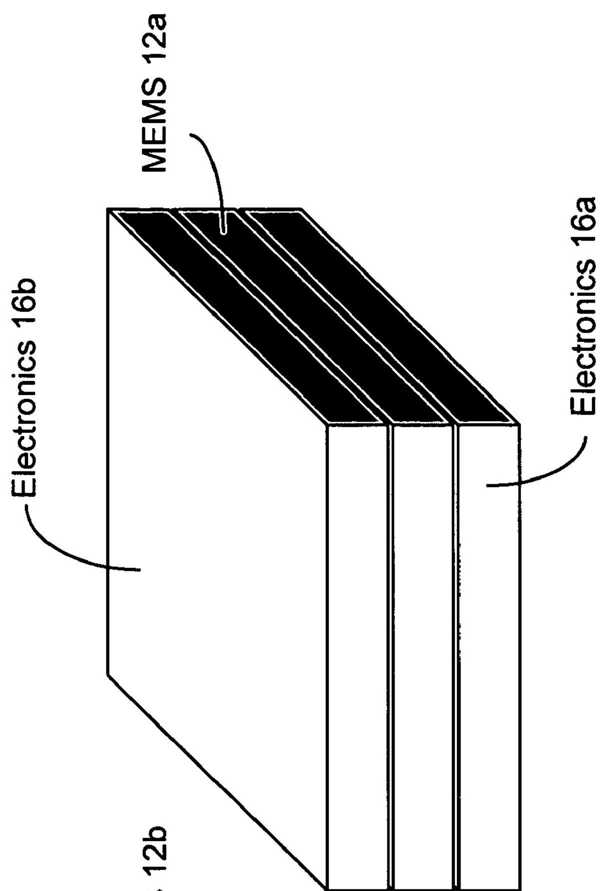

FIGURE 66C

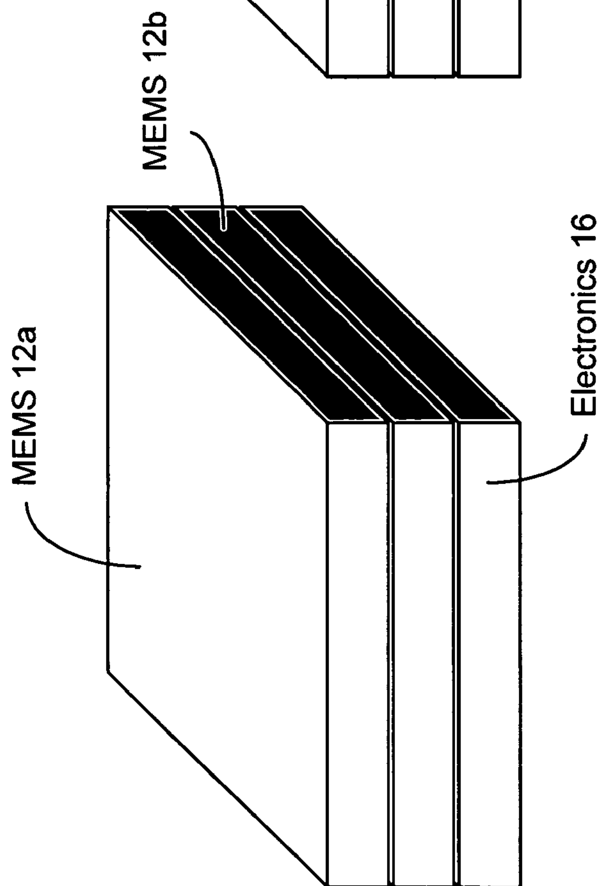

FIGURE 66B

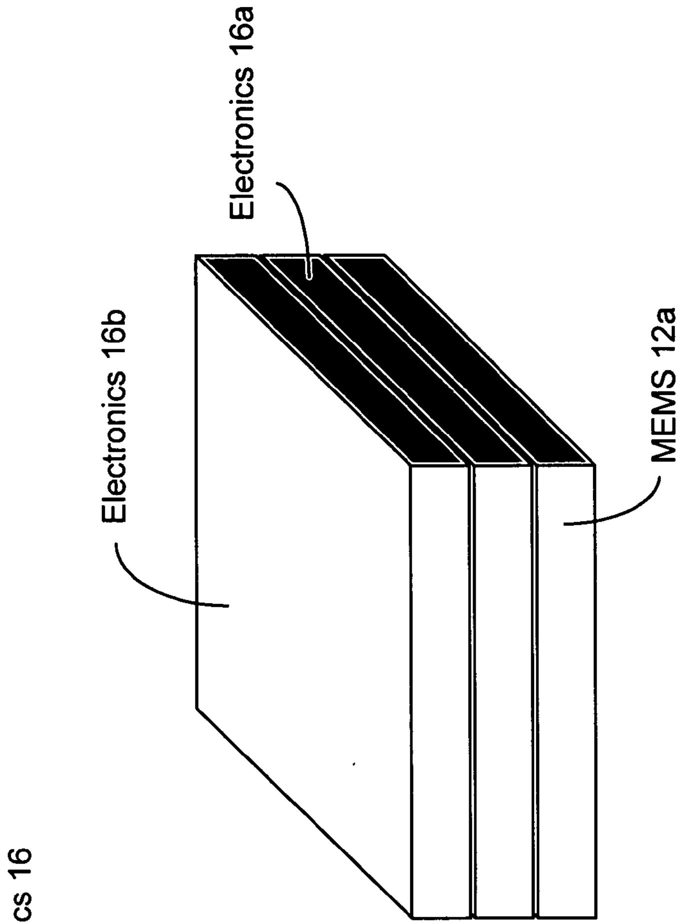

FIGURE 66E

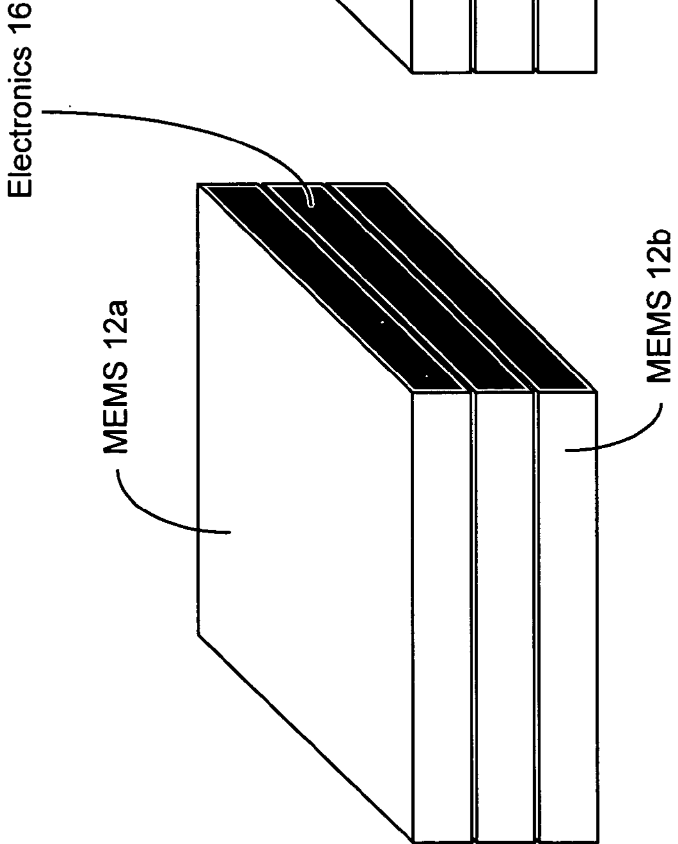

FIGURE 66D

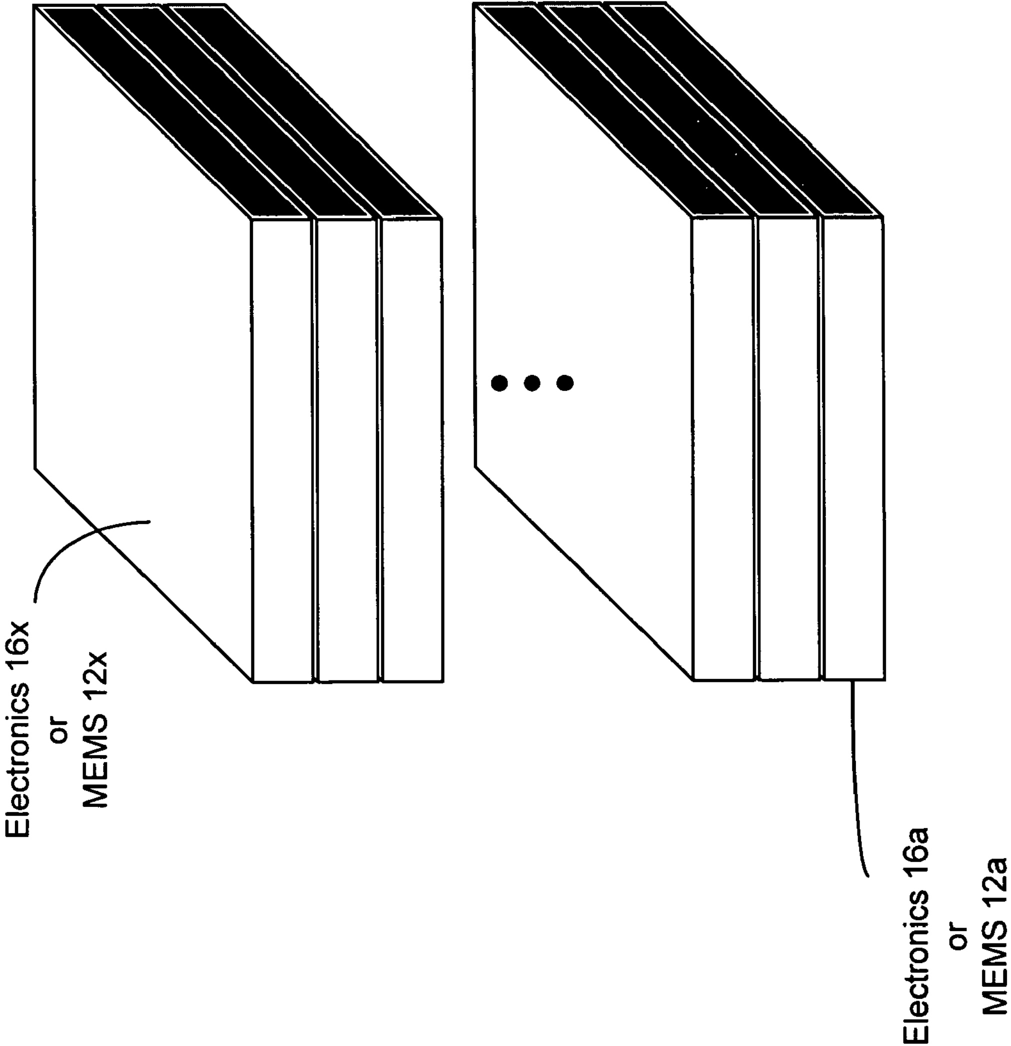

FIGURE 66F

WAFER ENCAPSULATED MICROELECTROMECHANICAL STRUCTURE AND METHOD OF MANUFACTURING SAME

BACKGROUND

[0001] There are many inventions described and illustrated herein. The Inventions relate to encapsulation electromechanical structures, for example, microelectromechanical and/or nanoelectromechanical structure (collectively hereinafter "microelectromechanical structures") and devices/systems including same; and more particularly, in one aspect, for fabricating or manufacturing microelectromechanical systems having mechanical structures that are encapsulated using wafer level encapsulation techniques, and devices/systems incorporated same.

[0002] Microelectromechanical systems, for example, gyroscopes, resonators and accelerometers, utilize micromachining techniques (i.e., lithographic and other precision fabrication techniques) to reduce mechanical components to a scale that is generally comparable to microelectronics. Microelectromechanical systems typically include a mechanical structure fabricated from or on, for example, a silicon substrate using micromachining techniques.

[0003] The mechanical structures are typically sealed in a chamber. The delicate mechanical structure may be sealed in, for example, a hermetically sealed metal or ceramic container or bonded to a semiconductor or glass-like substrate having a chamber to house, accommodate or cover the mechanical structure. In the context of the hermetically sealed metal or ceramic container, the substrate on, or in which, the mechanical structure resides may be disposed in and affixed to the metal or ceramic container. The hermetically sealed metal or ceramic container often also serves as a primary package as well.

[0004] In the context of the semiconductor or glass-like substrate packaging technique, the substrate of the mechanical structure may be bonded to another substrate (i.e., a "cover" wafer) whereby the bonded substrates form a chamber within which the mechanical structure resides. In this way, the operating environment of the mechanical structure may be controlled and the structure itself protected from, for example, inadvertent contact.

SUMMARY OF THE INVENTIONS

[0005] There are many inventions described and illustrated herein. The present inventions are neither limited to any single aspect nor embodiment thereof, nor to any combinations and/or permutations of such aspects and/or embodiments. Moreover, each of the aspects of the present inventions, and/or embodiments thereof, may be employed alone or in combination with one or more of the other aspects of the present inventions and/or embodiments thereof. For the sake of brevity, many of those permutations and combinations will not be discussed separately herein.

[0006] In one aspect, the present inventions are directed to a microelectromechanical device comprising a first substrate, a chamber, and a microelectromechanical structure, wherein the microelectromechanical structure is (i) formed from a portion of the first substrate and (ii) at least partially disposed in the chamber. In addition, in this aspect, the microelectromechanical device further includes a second substrate, bonded to the first substrate, wherein a surface of the second substrate forms a wall of the chamber, as well as a contact. The contact includes (1) a first portion of the contact is (i) formed from a portion of the first substrate and (ii) at least a portion thereof is disposed outside the chamber, and (2) a second portion of the contact is formed from a portion of the second substrate.

[0007] In one embodiment, the second substrate includes polycrystalline silicon, porous polycrystalline silicon, amorphous silicon, silicon carbide, silicon/germanium, germanium, or gallium arsenide. The first substrate may include polycrystalline silicon, porous polycrystalline silicon, amorphous silicon, silicon carbide, silicon/germanium, germanium, or gallium arsenide.

[0008] In addition, in one embodiment, the first portion of the contact is a semiconductor material having a first conductivity, the second substrate is a semiconductor material having a second conductivity, and the second portion of the contact is a semiconductor material having the first conductivity. Notably, the second portion of the contact may be a polycrystalline or monocrystalline silicon that is counterdoped to include the first conductivity.

[0009] The microelectromechanical device may further include a trench, disposed in the second substrate and around at least a portion of the second portion of the contact. The trench may include a first material (for example, an insulation material) disposed therein to electrically isolate the second portion of the contact from the second substrate.

[0010] Notably, the first substrate is a semiconductor on insulator substrate.

[0011] In another principle aspect, the present inventions are directed to a microelectromechanical device comprising a first substrate, a second substrate, wherein the second substrate is bonded to the first substrate, a chamber, and a microelectromechanical structure, wherein the microelectromechanical structure is (i) formed from a portion of the second substrate and (ii) at least partially disposed in the chamber. The microelectromechanical device may further include a third substrate, bonded to the second substrate, wherein a surface of the third substrate forms a wall of the chamber. The microelectromechanical device may also include a contact having (1) a first portion of the contact is (i) formed from a portion of the second substrate and (ii) at least a portion thereof is disposed outside the chamber, and (2) a second portion of the contact is formed from a portion of the third substrate.

[0012] The second substrate may include polycrystalline silicon, porous polycrystalline silicon, amorphous silicon, silicon carbide, silicon/germanium, germanium, or gallium arsenide. The third substrate may include polycrystalline silicon, porous polycrystalline silicon, amorphous silicon, silicon carbide, silicon/germanium, germanium, or gallium arsenide.

[0013] In one embodiment, the first portion of the contact is a semiconductor material having a first conductivity, the third substrate is a semiconductor material having a second conductivity, and the second portion of the contact is a semiconductor material having the first conductivity. Notably, in one embodiment, the second portion of the contact may be a polycrystalline or monocrystalline silicon that is counterdoped to include the first conductivity.

[0014] The microelectromechanical device may further include a trench, disposed in the third substrate and around at least a portion of the second portion of the contact. The trench may include a first material (for example, an insula-

tion material) disposed therein to electrically isolate the second portion of the contact from the third substrate.

[0015] The microelectromechanical device may also include an isolation region disposed in the second substrate such that the trench is aligned with and juxtaposed to the isolation region. In this embodiment, the first portion of the contact may be a semiconductor material having a first conductivity, the isolation region may be a semiconductor material having a second conductivity, and the second portion of the contact may be a semiconductor material having the first conductivity. A trench may be included to electrically isolate the second portion of the contact from the second substrate. The trench may include a semiconductor material, disposed therein, having the second conductivity.

[0016] In another embodiment, the microelectromechanical device may include an isolation region disposed in the first substrate such that the first portion of the contact is aligned with and juxtaposed to the isolation region.

[0017] In yet another embodiment, the microelectromechanical device may include a first isolation region and a second isolation region. The first isolation region may be disposed in the first substrate such that the first portion of the contact is aligned with and juxtaposed to the first isolation region. The second isolation region may be disposed in the second substrate such that the second portion of the contact is aligned with and juxtaposed to the second isolation region. In this embodiment, the first and second portions of the contact may be semiconductor materials having a first conductivity, and the first and second isolation regions may be semiconductor materials having the second conductivity.

[0018] The microelectromechanical device of this embodiment may also include a trench, disposed in the third substrate and around at least a portion of the second portion of the contact. The trench may include a first material (for example, an insulator material) disposed therein to electrically isolate the second portion of the contact from the third substrate. The trench may be aligned with and juxtaposed to the second isolation region.

[0019] Notably, all forms of bonding, whether now known or later developed, are intended to fall within the scope of the present invention. For example, bonding techniques such as fusion bonding, anodic-like bonding, silicon direct bonding, soldering (for example, eutectic soldering), thermo compression, thermo-sonic bonding, laser bonding and/or glass reflow bonding, and/or combinations thereof.

[0020] Moreover, any of the embodiments described and illustrated herein may employ a bonding material and/or a bonding facilitator material (disposed between substrates, for example, the second and third substrates) to, for example, enhance the attachment of or the "seal" between the substrates (for example, the first and second, and/or the second and third), address/compensate for planarity considerations between substrates to be bonded (for example, compensate for differences in planarity between bonded substrates), and/or to reduce and/or minimize differences in thermal expansion (that is materials having different coefficients of thermal expansion) of the substrates and materials therebetween (if any). Such materials may be, for example, solder, metals, frit, adhesives, BPSG, PSG, or SOG, or combinations thereof.

[0021] Again, there are many inventions, and aspects of the inventions, described and illustrated herein. This Summary of the Inventions is not exhaustive of the scope of the present inventions. Moreover, this Summary of the Inventions is not intended to be limiting of the inventions and should not be interpreted in that manner. While certain embodiments have been described and/or outlined in this Summary of the Inventions, it should be understood that the present inventions are not limited to such embodiments, description and/or outline, nor are the claims limited in such a manner. Indeed, many others embodiments, which may be different from and/or similar to, the embodiments presented in this Summary, will be apparent from the description, illustrations and claims, which follow. In addition, although various features, attributes and advantages have been described in this Summary of the Inventions and/or are apparent in light thereof, it should be understood that such features, attributes and advantages are not required whether in one, some or all of the embodiments of the present inventions and, indeed, need not be present in any of the embodiments of the present inventions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] In the course of the detailed description to follow, reference will be made to the attached drawings. These drawings show different aspects of the present inventions and, where appropriate, reference numerals illustrating like structures, components, materials and/or elements in different figures are labeled similarly. It is understood that various combinations of the structures, components, materials and/or elements, other than those specifically shown, are contemplated and are within the scope of the present inventions.

[0023] FIG. **1**A is a block diagram representation of a mechanical structure disposed on a substrate and encapsulated via at least a second substrate;

[0024] FIG. **1**B is a block diagram representation of a mechanical structure and circuitry, each disposed on one or more substrates and encapsulated via a substrate;

[0025] FIG. **2** illustrates a top view of a portion of a mechanical structure of a conventional resonator, including moveable electrode, fixed electrode, and a contact;

[0026] FIG. **3** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the first substrate employs an SOI wafer;

[0027] FIGS. **4**A-**4**G illustrate cross-sectional views (sectioned along dotted line A-A' of FIG. **2**) of the fabrication of the mechanical structure of FIGS. **2** and **3** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0028] FIG. **5** illustrates a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2**, wherein microelectromechanical system includes electronic or electrical circuitry in conjunction with micromachined mechanical structure of FIG. **2**, in accordance with an exemplary embodiment of the present inventions;

[0029] FIGS. **6**A-**6**D illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **5** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0030] FIGS. **7**A-**7**C, and **8**A and **8**B illustrate cross-sectional views of two exemplary embodiments of the fabrication of the portion of the microelectromechanical system of FIG. **5** using processing techniques wherein

electronic or electrical circuitry (at various stages of completeness) is formed in the second substrate prior to encapsulating the mechanical structure via securing the second substrate to the first substrate;

[0031] FIG. **9** illustrates a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2**, wherein micromachined mechanical structure of FIG. **2** includes an isolation trench to electrically isolate the contact, in accordance with an exemplary embodiment of the present inventions;

[0032] FIGS. **10**A-**10**I illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **9** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0033] FIG. **11** illustrates a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2**, wherein micromachined mechanical structure of FIG. **2** includes isolation regions and an isolation trench (aligned therewith) to electrically isolate the contact, in accordance with an exemplary embodiment of the present inventions;

[0034] FIGS. **12**A-**12**J illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **11** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0035] FIG. **13**A illustrates a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2**, wherein micromachined mechanical structure of FIG. **2** includes isolation regions and an isolation trench (aligned therewith), including an oppositely doped semiconductor (relative to the conductivity of second substrate **14***b*), to electrically isolate the contact, in accordance with an exemplary embodiment of the present inventions;

[0036] FIGS. **13**B and **13**C illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **13**A at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0037] FIG. **14** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an embodiment of the present inventions wherein the microelectromechanical system employs three substrates;

[0038] FIGS. **15**A-**15**H illustrate cross-sectional views (sectioned along dotted line A-A' of FIG. **2**) of the fabrication of the mechanical structure of FIGS. **2** and **14** at various stages of a process that employs an encapsulation technique according to certain aspects of the present inventions;

[0039] FIG. **16** illustrates a cross-sectional view of an embodiment of the fabrication of the microelectromechanical system of FIG. **14** wherein electronic or electrical circuitry (after fabrication) is formed in the third substrate according to certain aspects of the present inventions;

[0040] FIG. **17** illustrates a cross-sectional view of an exemplary embodiment of the present inventions of the microelectromechanical system including a plurality of micromachined mechanical structures wherein a first micromachined mechanical structure is formed in the second substrate and a second micromachined mechanical structure is formed in the third substrate wherein a fourth substrate encapsulates one or more of the micromachined mechanical structures according to certain aspects of the present inventions;

[0041] FIG. **18** illustrates a cross-sectional view of an exemplary embodiment of the present inventions of the microelectromechanical system including a plurality of micromachined mechanical structures wherein a first micromachined mechanical structure is formed in the second substrate and a second micromachined mechanical structure is formed in the third substrate wherein a fourth substrate encapsulates one or more of the micromachined mechanical structures and includes electronic or electrical circuitry according to certain aspects of the present inventions;

[0042] FIG. **19** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates and cavities are formed in the first and third substrates;

[0043] FIGS. **20**A-**20**H illustrate cross-sectional views (sectioned along dotted line A-A' of FIG. **2**) of the fabrication of the mechanical structure of FIGS. **2** and **19** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0044] FIG. **21** illustrates a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2**, wherein the first cavity is formed in the second substrate and a second cavity is formed in a third substrate according to certain aspects of the present inventions;

[0045] FIG. **22** illustrates a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2**, wherein the first and second cavities are formed in the second substrate, according to certain aspects of the present inventions;

[0046] FIG. **23** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates and the second and third substrates include the same conductivity types;

[0047] FIGS. **24**A-**24**I illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **23** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0048] FIG. **25** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates and the first and second substrates include the same conductivity types;

[0049] FIGS. **26**A-**26**H illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **25** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0050] FIG. **27** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an

exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates which include the same conductivity types;

[0051] FIGS. **28**A-**28**I illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **27** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0052] FIG. **29** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates which include the same conductivity types;

[0053] FIGS. **30**A-**30**I illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **29** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0054] FIGS. **31**A-**31**D illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **27** at various stages of an exemplary process that employs grinding and/or polishing to provide a desired surface, according to certain aspects of the present inventions;

[0055] FIG. **32** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates;

[0056] FIGS. **33**A-**33**I illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **32** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0057] FIG. **34** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates wherein an insulative layer is disposed between each of the substrates;

[0058] FIGS. **35**A-**35**L illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **34** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0059] FIG. **36** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates wherein an insulative layer is disposed between two of the substrates;

[0060] FIGS. **37**A-**37**I illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **36** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0061] FIG. **38** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates wherein an insulative layer is disposed between two of the substrates and isolation trenches and regions electrically isolate the contact;

[0062] FIGS. **39**A-**39**K illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **38** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0063] FIG. **40** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates wherein an intermediate layer (for example, a native oxide layer) is disposed between two of the substrates;

[0064] FIGS. **41**A-**41**H illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **40** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0065] FIGS. **42**A and **42**B are cross-sectional views (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of exemplary embodiments of the present inventions wherein the microelectromechanical system employs three substrates wherein an intermediate layer (for example, a native oxide layer) is disposed (for example, deposited or grown) between two of the substrates;

[0066] FIGS. **43**A-**43**K illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical systems of FIGS. **42**A and **42**B at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0067] FIG. **44** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates and the processing techniques include alternative processing margins;

[0068] FIGS. **45**A-**45**I illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **44** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0069] FIG. **46**A is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates and the processing techniques include alternative processing margins wherein the isolation trenches include an over etch;

[0070] FIG. **46**B is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates and a selected trench includes alternative processing margins;

[0071] FIGS. **47**A-**47**D and **48**A-**48**C are cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the

contact of FIG. **2** of an embodiment of the present inventions having alternative exemplary processing techniques, flows and orders thereof;

[0072] FIGS. **49**A-**49**G, **50**A-**50**G and **51**A-**51**J are cross-sectional views (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of exemplary embodiments of the present inventions having alternative processing techniques, flows and orders thereof relative to one or more of substrates;

[0073] FIG. **52** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates wherein isolation regions are implanted in a cover substrate to electrically isolate the contact;

[0074] FIGS. **53**A-**53**H illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **52** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0075] FIG. **54** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein the microelectromechanical system employs three substrates wherein isolation regions include an insulation material (for example, a silicon nitride or silicon dioxide);

[0076] FIGS. **55**A-**55**K illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **54** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0077] FIG. **56** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein a contact area is etched and formed in one of the "cover" substrate to provide for electrical conductivity with the an underlying contact area;

[0078] FIGS. **57**A-**57**J illustrate cross-sectional views of an exemplary flow of the fabrication of the portion of the microelectromechanical system of FIG. **56** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0079] FIG. **58** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of an exemplary embodiment of the present inventions wherein bonding material and/or a bonding facilitator material is employed between substrates;

[0080] FIGS. **59**A-**59**J illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **58** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0081] FIG. **60** is a cross-sectional view (sectioned along dotted line A-A' of FIG. **2**) of a portion of the moveable electrode, fixed electrode, and the contact of FIG. **2** of another exemplary embodiment of the present inventions wherein bonding material and/or a bonding facilitator material is employed between substrates;

[0082] FIGS. **61**A-**61**K illustrate cross-sectional views of the fabrication of the portion of the microelectromechanical system of FIG. **58** at various stages of an exemplary process that employs an encapsulation technique according to certain aspects of the present inventions;

[0083] FIGS. **62**-**64** illustrates cross-sectional views of several embodiments of the fabrication of microelectromechanical systems of the present inventions wherein the microelectromechanical systems include electronic or electrical circuitry formed in a substrate, according to certain aspects of the present inventions; and

[0084] FIGS. **65** and **66**A-**66**F are block diagram illustrations of various embodiments of the microelectromechanical systems of the present inventions wherein the microelectromechanical systems includes at least three substrates wherein one or more substrates include one or more micromachined mechanical structures and/or electronic or electrical circuitry, according to certain aspects of the present inventions.

DESCRIPTION OF THE INVENTIONS

[0085] There are many inventions described and illustrated herein. In one aspect, the present inventions relate to devices, systems and/or methods of encapsulating and fabricating electromechanical structures or elements, for example, accelerometer, gyroscope or other transducer (for example, pressure sensor, strain sensor, tactile sensor, magnetic sensor and/or temperature sensor), filter or resonator The fabricating or manufacturing microelectromechanical systems of the present invention, and the systems manufactured thereby, employ wafer bonding encapsulation techniques.

[0086] With reference to FIGS. **1**A, **1**B and **2**, in one exemplary embodiment, microelectromechanical device **10** includes micromachined mechanical structure **12** that is disposed on substrate **14**, for example, a semiconductor, a glass, or an insulator material. The microelectromechanical device **10** may include electronics or electrical circuitry **16** (hereinafter collectively "circuitry **16**") to, for example, drive mechanical structure **12**, sense information from mechanical structure **12**, process or analyze information generated by, and/or control or monitor the operation of micromachined mechanical structure **12**. In addition, circuitry **16** (for example, CMOS circuitry) may generate clock signals using, for example, an output signal of micromachined mechanical structure **12**, which may be a resonator type electromechanical structure. Under these circumstances, circuitry **16** may include frequency and/or phase compensation circuitry (hereinafter "compensation circuitry **18**"), which receives the output of the resonator and adjusts, compensates, corrects and/or controls the frequency and/or phase of the output of resonator. In this regard, compensation circuitry uses the output of resonator to provide an adjusted, corrected, compensated and/or controlled output having, for example, a desired, selected and/or predetermined frequency and/or phase.

[0087] Notably, circuitry **16** may include interface circuitry to provide information (from, for example, micromachined mechanical structure **12**) to an external device (not illustrated), for example, a computer, indicator/display and/or sensor.

[0088] With continued reference to FIGS. **1**A, **1**B and **2**, micromachined mechanical structure **12** may include and/or be fabricated from, for example, materials in column IV of

the periodic table, for example silicon, germanium, carbon; also combinations of these, for example silicon germanium, or silicon carbide; also of III-V compounds for example gallium phosphide, aluminum gallium phosphide, or other III-V combinations; also combinations of III, IV, V, or VI materials, for example silicon nitride, silicon oxide, aluminum carbide, or aluminum oxide; also metallic silicides, germanides, and carbides, for example nickel silicide, cobalt silicide, tungsten carbide, or platinum germanium silicide; also doped variations including phosphorus, arsenic, antimony, boron, or aluminum doped silicon or germanium, carbon, or combinations like silicon germanium; also these materials with various crystal structures, including single crystalline, polycrystalline, nanocrystalline, or amorphous; also with combinations of crystal structures, for instance with regions of single crystalline and polycrystalline structure (whether doped or undoped).

[0089] As mentioned above, micromachined mechanical structure **12** illustrated in FIG. **2** may be a portion of an accelerometer, gyroscope or other transducer (for example, pressure sensor, strain sensor, tactile sensor, magnetic sensor and/or temperature sensor), filter or resonator. The micromachined mechanical structure **12** may also include mechanical structures of a plurality of transducers or sensors including one or more accelerometers, gyroscopes, pressure sensors, tactile sensors and temperature sensors. In the illustrated embodiment, micromachined mechanical structure **12** include moveable electrode **18**.

[0090] With continued reference to FIG. **2**, micromachined mechanical structure **12** may also include contact **20** disposed on or in substrate **14***a*. The contact **20** may provide an electrical path between micromachined mechanical structure **12** and circuitry **16** and/or an external device (not illustrated). The contact **20** may include and/or be fabricated from, for example, a semiconductor or conductive material, including, for example, silicon, (whether doped or undoped), germanium, silicon/germanium, silicon carbide, and gallium arsenide, and combinations and/or permutations thereof. Notably, micromachined mechanical structure **12** and circuitry **16** may include multiple contacts **20**.

[0091] In one embodiment, the present inventions employ two or more substrates to form and encapsulate micromachined mechanical structure **12**. For example, with reference to FIG. **3**, in one embodiment, microelectromechanical system **10** includes semiconductor on insulator ("SOI") substrate **14***a* and cover substrate **14***b*. Briefly, by way of overview, in this embodiment, micromachined mechanical structure **12** (including moveable electrode **18** and contact **20**) is formed in or on SOI substrate **14***a* and encapsulated via cover substrate **14***b*. In this regard, micromachined mechanical structure **12** is formed in the semiconductor portion of SOI substrate **14***a* that resides on the insulator portion of SOI substrate **14***a*. Thereafter, substrate **14***b* is secured (for example, bonded) to the exposed surface of the semiconductor portion of SOI substrate **14***a* to encapsulate micromachined mechanical structure **12**.

[0092] In particular, with reference to FIG. **4**A, microelectromechanical system **10** is formed in or on SOI substrate **14***a*. The SOI substrate **14***a* may include first substrate layer **22***a* (for example, a semiconductor (such as silicon), glass or sapphire), insulation layer **22***b* (for example, a silicon dioxide or silicon nitride layer) and first semiconductor layer **22***c* (for example, a materials in column IV of the periodic table, for example silicon, germanium, carbon, as well as combinations of such materials, for example silicon germanium, or silicon carbide). In one embodiment, SOI substrate **14***a* is a SIMOX wafer. Where SOI substrate **36** is a SIMOX wafer, such wafer may be fabricated using well-known techniques including those disclosed, mentioned or referenced in U.S. Pat. Nos. 5,053,627; 5,080,730; 5,196,355; 5,288,650; 6,248,642; 6,417,078; 6,423,975; and 6,433,342 and U.S. Published Patent Applications 2002/0081824 and 2002/0123211, the contents of which are hereby incorporated by reference.

[0093] In another embodiment, SOI substrate **14***a* may be a conventional SOI wafer having a relatively thin semiconductor layer **22***c*. In this regard, SOI substrate **36** having a relatively thin semiconductor layer **22***c* may be fabricated using a bulk silicon wafer which is implanted and oxidized by oxygen to thereby form a relatively thin silicon dioxide layer **22***b* on a monocrystalline wafer surface **22***a*. Thereafter, another wafer (illustrated as layer **22***c*) is bonded to layer **22***b*. In this exemplary embodiment, semiconductor layer **22***c* (i.e., monocrystalline silicon) is disposed on insulation layer **22***b* (i.e. silicon dioxide), having a thickness of approximately 350 nm, which is disposed on a first substrate layer **22***a* (for example, monocrystalline silicon), having a thickness of approximately 190 nm.

[0094] Notably, all techniques for providing or fabricating SOI substrate **14***a*, whether now known or later developed, are intended to be within the scope of the present inventions.

[0095] With reference to FIGS. **4**A and **4**B, an exemplary method of fabricating or forming micromachined mechanical structure **12** according to this embodiment of the present inventions may begin with forming first cavity **24** in semiconductor layer **22***c* using well-known lithographic and etching techniques. In this way, a selected portion of semiconductor layer **22***c* (for example, 1 μm) is removed to form first cavity **24** which forms a portion of the chamber in which the mechanical structure, for example, moveable electrode **18**, resides).

[0096] With reference to FIGS. **4**C and **4**D, thereafter, moveable electrode **18** and contact area **26** are formed in semiconductor layer **22***c* and moveable electrode **18** is "released" from insulation layer **22***b*. In this regard, trenches **28***a-c* are formed in semiconductor layer **22***c* to define moveable electrode **18** and contact area **26** therefrom. (See, FIG. **4**C). The trenches **28***a-c* may be formed using well-known deposition and lithographic techniques. Notably, all techniques for forming or fabricating trenches **28***a-c*, whether now known or later developed, are intended to be within the scope of the present inventions.

[0097] After moveable electrode **18** is defined via trenches **28***b* and **28***c*, moveable electrode **18** may be "released" by etching portions of insulation layer **22***b* that are disposed under moveable electrode **18**. For example, in one embodiment, where insulation layer **22***b* is comprised of silicon dioxide, selected portions may be removed/etched using well-known wet etching techniques and buffered HF mixtures (i.e., a buffered oxide etch) or well-known vapor etching techniques using vapor HF. The trenches **28***b* and **28***c*, in addition to defining the features of moveable electrode **18**, may also permit etching and/or removal of at least selected portions of insulation layer **22***b* thereby providing a void or cavity **30** beneath moveable electrode **18**. (See, FIG. **4**D). Proper design of mechanical structures **12** (and in particular moveable electrode **18**) and control of the HF etching process parameters may permit insulation layer **22***b*

to be sufficiently removed or etched to release moveable electrode **18** and permit proper operation of micromachined mechanical structure **12** and microelectromechanical system **10**. Notably, cavities **24** and **30** form the chamber in which the mechanical structure, for example, moveable electrode **18**, resides.

[0098] With reference to FIG. **4**E, second substrate **14***b* may be fixed to the exposed portion(s) of semiconductor layer **22***c*. The second substrate **14***b* may be secured to the exposed portion(s) of semiconductor layer **22***c* using, for example, well-known bonding techniques such as fusion bonding, anodic-like bonding and/or silicon direct bonding. Other bonding technologies are suitable including soldering (for example, eutectic soldering), thermo compression bonding, thermo-sonic bonding, laser bonding and/or glass reflow, and/or combinations thereof. Indeed, all forms of bonding, whether now known or later developed, are intended to fall within the scope of the present invention.

[0099] In conjunction with securing second substrate **14***b* to the exposed portion(s) of semiconductor layer **22***c*, the atmosphere (including its characteristics) in which moveable electrode **18** operates may also be defined. In this regard, the chamber in which the moveable electrode **18** reside may be defined when second substrate **14***b* is secured and/or fixed to the exposed portion(s) of semiconductor layer **22***c* or after further processing (for example, an annealing step may be employed to adjust the pressure). Notably, all techniques of defining the atmosphere, including the pressure thereof, during the process of securing second substrate **14***b* to semiconductor layer **22***c*, whether now known or later developed, are intended to be within the scope of the present inventions.

[0100] For example, second substrate **14***b* may be secured to the exposed portion(s) of semiconductor layer **22***c* in a nitrogen, oxygen and/or inert gas environment (for example, helium). The pressure of the fluid (gas or vapor) may be selected, defined and/or controlled to provide a suitable and/or predetermined pressure of the fluid in the chamber immediately after fixing substrate **14***b* to the exposed portion (s) of semiconductor layer **22***c* (in order to avoid damaging portions of micromachined mechanical structure **12**), after one or more subsequent processing steps (for example, an annealing step) and/or after completion of micromachined mechanical structure **12** and/or microelectromechanical system **10**.

[0101] Notably, the gas(es) employed during these processes may provide predetermined reactions (for example, oxygen molecules may react with silicon to provide a silicon oxide). All such techniques are intended to fall within the scope of the present inventions.

[0102] The second substrate **14***b* may be formed from any material now known or later developed. In a preferred embodiment, second substrate **14***b* includes or is formed from, for example, materials in column IV of the periodic table, for example silicon, germanium, carbon; also combinations of these, for example silicon germanium, or silicon carbide; also of III-V compounds for example gallium phosphide, aluminum gallium phosphide, or other III-V combinations; also combinations of II, IV, V, or VI materials, for example silicon nitride, silicon oxide, aluminum carbide, or aluminum oxide; also metallic silicides, germanides, and carbides, for example nickel silicide, cobalt silicide, tungsten carbide, or platinum germanium silicide; also doped variations including phosphorus, arsenic, antimony, boron, or aluminum doped silicon or germanium, carbon, or combinations like silicon germanium; also these materials with various crystal structures, including single crystalline, polycrystalline, nanocrystalline, or amorphous; also with combinations of crystal structures, for instance with regions of single crystalline and polycrystalline structure (whether doped or undoped).

[0103] Before or after second substrate **14***b* is secured to the exposed portion(s) of semiconductor layer **22***c*, contact area **26***b* may be formed in a portion of second substrate **14***b* to be aligned with, connect to or overlie contact area **26***a* in order to provide suitable, desired and/or predetermined electrical conductivity (for example, N-type or P-type) with contact area **26***a* when second substrate **14***b* is secured to first substrate **14***a*. (See, FIG. **4**F). The contact area **26***b* may be formed in second substrate **14***b* using well-known lithographic and doping techniques. In this way, contact area **26***b* may be a highly doped region of second substrate **14***b* which provides enhanced electrical conductivity with contact area **26***a*.

[0104] Notably, contact area **26***b* may be a counter-doped region or heavily counter-doped region of second substrate **14***b* which includes a conductivity that is different from the conductivity of the other portions of second substrate **14***b*. In this way, contact areas **26***a* and **26***b* are electrically isolated from the other portions of second substrate **14***b*. Thus, in this embodiment, semiconductor layer **22***c* may be a first conductivity type (for example, an N-type conductivity which may be provided, for example, via introduction of phosphorous and/or arsenic dopant(s), among others) and second substrate **14***b* may be a second conductivity type (for example, a P-type conductivity which may be provided, for example, via introduction of boron dopant(s), among others). As such, contact area **26***b* may be a counter-doped region or heavily counter-doped N-type region which provides suitable, desired and/or predetermined electrical conductivity characteristics when second substrate **14***b* is secured to first substrate **14***a* and contact areas **26***a* and **26***b* are in physical and electrical contact.

[0105] With reference to FIG. **4**G, microelectromechanical system **10** may be completed by depositing, forming and/or growing insulation layer **32** and a contact opening may be etched to facilitate electrical contact/connection to contact area **26***b*, via conductive layer **34** (for example, a heavily doped polysilicon, metal (such as aluminum, chromium, gold, silver, molybdenum, platinum, palladium, tungsten, titanium, and/or copper), metal stacks, complex metals and/or complex metal stacks) may then be deposited (and/or formed) to provide the appropriate electrical connection to contact areas **26** (which includes, in this example, contacts areas **26***a* and **26***b*).

[0106] Notably, insulation layer **32** and/or conductive layer **34** may be formed, grown and/or deposited before or after second substrate **14***b* is secured to the exposed portion (s) of semiconductor layer **22***c*. Under these circumstances, when second substrate **14***b* is secured to first substrate **14***a*, the microelectromechanical system **10** may be completed.

[0107] The insulating layer **32** may be, for example, silicon dioxide, silicon nitride, BPSG, PSG, or SOG, or combinations thereof. It may be advantageous to employ silicon nitride because silicon nitride may be deposited in a more conformal manner than silicon oxide. Moreover, sili-

con nitride is compatible with CMOS processing, in the event that microelectromechanical system **10** includes CMOS integrated circuits.

[0108] Notably, prior to formation, deposition and/or growth of insulation layer **32** and/or conductive layer **34**, additional micromachined mechanical structures **12** and/or transistors of circuitry **16** may be formed and/or provided in second substrate **14***b* or in other substrates that may be fixed to first substrate **14***a* and/or second substrate **14***b*. In this regard, the exposed surface of second substrate **14***b* may be a suitable base upon which integrated circuits (for example, CMOS transistors) and/or micromachined mechanical structures **12** may be fabricated on or in. Such integrated circuits may be fabricated using well-known techniques and equipment. For example, with reference to FIG. **5**, in one embodiment, transistor regions **36**, which may be integrated circuits (for example, CMOS transistors) of circuitry **16**, may be provided in second substrate **14***b*. The transistor regions **36** may be formed before or after second substrate **14***b* is secured (for example, bonded) to first substrate **14***a*. In this regard, with reference to FIG. **6**A, transistor implants **38** may be formed using well-known lithographic and implant processes, after second substrate **14***b* is secured to first substrate **14***a* and concurrently with the formation of contact area **26***b*.

[0109] Thereafter, conventional transistor processing (for example, formation of gate and gate insulator **40**) may be employed to complete the transistors of circuitry **16**. (See, FIG. **6**B). The "back-end" processing of microelectromechanical system **10** (for example, formation, growth and/or deposition of insulation layer **32** and conductive layer **34**) may be performed using the same processing techniques as described above. (See, for example, FIGS. **6**C and **6**D). In this regard, insulation layer **32** may be deposited, formed and/or grown and patterned and, thereafter, conductive layer **34** (for example, a heavily doped polysilicon, metal (such as aluminum, chromium, gold, silver, molybdenum, platinum, palladium, tungsten, titanium, and/or copper), metal stacks, complex metals and/or complex metal stacks) is deposited and/or formed. In the illustrative embodiments, contact **20** is accessed directly by the transistors of circuitry **16** via conductive layer **34**. Here, conductive layer **34** may be a low resistance electrical path that is deposited and patterned to facilitate connection of micromachined mechanical structure **12** and circuitry **16**.

[0110] As noted above, the transistors of transistor region **36** may be formed prior to securing second substrate **14***b* to first substrate **14***a*. (See, for example, FIGS. **7**A and **7**B). Indeed, all of the "back-end" processing, in addition to formation of the transistors of transistor region **36**, may be completed prior to securing second substrate **14***b* to first substrate **14***a*. (See, for example, FIGS. **8**A and **8**B).

[0111] With reference to FIGS. **9**, **10**A-**10**I, **11** and **12**A-**12**J, in another embodiment of the present inventions, semiconductor layer **22***c* of SOI substrate **14***a* is the same conductivity as second substrate **14***b*. In these embodiments, micromachined mechanical structure **12** may include additional features to electrically isolate contact **20**. For example, with reference to FIG. **9**, in one embodiment, micromachined mechanical structure **12** includes isolation trenches **42***a* and **42***b* that isolates contact **20** (and contact areas **26***a* and **26***b*) from portions of second substrate **14***b*. The isolation trenches **42***a* and **42***b* may include an insulator material, for example, silicon dioxide or silicon nitride. Indeed, as illustrated, material that forms insulation layer **32** may also be deposited in isolation trenches **42***a* and **42***b*. Notably, FIGS. **10**A-**10**I illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **9**.

[0112] With reference to FIG. **11**, in another exemplary embodiment, isolation regions **44***a* and **44***b* are deposited and/or implanted into portions of semiconductor layer **22***c* of SOI substrate **14***a* in order to facilitate electrical isolation of contact **20** after second substrate **14***b* is secured or fixed (via, for example, bonding). The isolation regions **44***a* and **44***b* may be any material or structure that insulates contact **20**, for example, an insulator material and/or an oppositely doped semiconductor region. FIGS. **12**A-**12**J illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **11** wherein isolation regions **44***a* and **44***b* are oppositely doped semiconductor regions and an insulation material is disposed in isolation trenches **42***a* and **42***b*.

[0113] FIG. **13**A illustrates an exemplary microelectromechanical system **10** wherein the isolation regions **44***a* and **44***b* are oppositely doped semiconductor regions (relative to the conductivity of second substrate **14***b*) and a semiconductor, having a conductivity different from the conductivity of the semiconductor of second substrate **14***b*, is disposed (for example using epitaxial deposition techniques) in isolation trenches **42***a* and **42***b*. FIGS. **13**B and **13**C illustrate selected portions of an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **13**A.

[0114] Notably, the embodiments of FIGS. **9**, **11** and **13**A may also include circuitry **16** disposed in second substrate **14***b*. The fabrication techniques described above and illustrated in FIGS. **5**-**8**B may be employed in the embodiments of FIGS. **9** and **11**. Indeed, prior to or after formation, deposition and/or growth of insulation layer **32** and/or conductive layer **34**, additional micromachined mechanical structures **12** and/or transistors of circuitry **16** may be formed and/or provided in second substrate **14***b* or in other substrates that may be fixed to first substrate **14***a* and/or second substrate **14***b*. For the sake of brevity, those discussions, in connection with the embodiments of FIGS. **9**, **11** and **13**A, will not be repeated.

[0115] The present inventions may also employ more than two substrates to form and encapsulate micromachined mechanical structure **12**. For example, with reference to FIG. **14**, in one embodiment, microelectromechanical system **10** includes first substrate **14***a*, second substrate **14***b* and third substrate **14***c*. Briefly, by way of overview, in this embodiment, micromachined mechanical structure **12** (including moveable electrode **18** and contact **20**) is formed in second substrate **14***b* and encapsulated via third substrate **14***c*. In this regard, micromachined mechanical structure **12** is formed in a portion of substrate **14***b*. Thereafter, substrate **14***c* is secured (for example, bonded) to exposed surface of substrate **14***b* to encapsulate micromachined mechanical structure **12**. In this embodiment, the portion of substrate **14***b* in which micromachined mechanical structure **12** is formed includes a conductivity that is different from the conductivity of the semiconductor of first substrate **14***a* and third substrate **14***c*.

[0116] With reference to FIGS. **15**A and **15**B, an exemplary method of fabricating or forming micromachined mechanical structure **12** according to this embodiment of the present inventions may begin with forming first cavity **24** in

first substrate **14**_a_ using well-known lithographic and etching techniques. In one exemplary embodiment, first cavity **24** includes a depth of about 1 μm.

[0117] With reference to FIGS. **15**C and **15**D, second substrate **14**_b_ may be fixed to first substrate **14**_a_. The second substrate **14**_b_ may be secured to the exposed portion(s) of first substrate **14**_a_ using, for example, well-known bonding techniques such as fusion bonding, anodic-like bonding and/or silicon direct bonding. As mentioned above, other bonding technologies are suitable including soldering (for example, eutectic soldering), thermo compression bonding, thermo-sonic bonding, laser bonding and/or glass reflow, and/or combinations thereof. Indeed, all forms of bonding, whether now known or later developed, are intended to fall within the scope of the present invention.

[0118] Before or after securing second substrate **14**_b_ to first substrate **14**_a_, second cavity **30** may be formed in second substrate **14**_b_-again using well-known lithographic and etching techniques. In one exemplary embodiment, second cavity **30** also includes a depth of about 1 μm. Thereafter, the thickness of second substrate **14**_b_ may be adjusted to accommodate further processing. For example, second substrate **14**_b_ may be grinded and polished (using, for example, well known chemical mechanical polishing ("CMP") techniques) to a thickness of between 10 μm-30 μm. Notably, cavities **24** and **30** form the chamber in which the mechanical structure, for example, moveable electrode **18**, resides.

[0119] The second substrate **14**_b_ may be formed from any material now known or later developed. In a preferred embodiment, second substrate **14**_b_ includes or is formed from, for example, materials in column IV of the periodic table, for example silicon, germanium, carbon; also combinations of these, for example silicon germanium, or silicon carbide; also of III-V compounds for example gallium phosphide, aluminum gallium phosphide, or other III-V combinations; also combinations of III, IV, V, or VI materials, for example silicon nitride, silicon oxide, aluminum carbide, or aluminum oxide; also metallic silicides, germanides, and carbides, for example nickel silicide, cobalt silicide, tungsten carbide, or platinum germanium silicide; also doped variations including phosphorus, arsenic, antimony, boron, or aluminum doped silicon or germanium, carbon, or combinations like silicon germanium; also these materials with various crystal structures, including single crystalline, polycrystalline, nanocrystalline, or amorphous; also with combinations of crystal structures, for instance with regions of single crystalline and polycrystalline structure (whether doped or undoped).

[0120] With reference to FIG. **15**E, moveable electrode **18** and contact area **26** are defined and formed in second substrate **14**_b_. In this regard, trenches **28**_a-c_ are formed in second substrate **14**_b_ to define moveable electrode **18** and contact area **26** therefrom. (See, FIG. **15**E). The trenches **28**_a-c_ may be formed using well-known deposition and lithographic techniques. Notably, all techniques for forming or fabricating trenches **28**_a-c_, whether now known or later developed, are intended to be within the scope of the present inventions.

[0121] Thereafter, third substrate **14**_c_ may be fixed to the exposed portion(s) of second substrate **14**_b_. (See, FIG. **15**F). The third substrate **14**_c_ may also be secured to the exposed portion(s) of second substrate **14**_b_ using, for example, well-known bonding techniques such as fusion bonding, anodic-like bonding and/or silicon direct bonding. In conjunction with securing third substrate **14**_c_ to second substrate **14**_b_, the atmosphere (including its characteristics) in which moveable electrode **18** operates may also be defined—for example, as described above. Notably, all techniques of defining the atmosphere, including the pressure thereof, during the process of securing third substrate **14**_c_ to second substrate **14**_b_, whether now known or later developed, are intended to be within the scope of the present inventions.

[0122] The third substrate **14**_c_ may be formed from any material discussed above relative to second substrate **14**_b_. For the sake of brevity, such discussions will not be repeated.

[0123] Before or after third substrate **14**_c_ is secured to second substrate **14**_b_, contact area **26**_b_ may be formed in a portion of third substrate **14**_c_ to be aligned with, connect to or overlie contact area **26**_a_. The contact area **26**_b_ may be a semiconductor region that includes a doping that provides the same conductivity as contact area **26**_a_. In this way, a suitable, desired and/or predetermined electrical conductivity is provided with contact area **26**_a_ when third substrate **14**_c_ is secured to second substrate **14**_b_. (See, FIG. **15**G). Thus, contact area **26**_b_ may be a highly doped region of third substrate **14**_c_ which provides enhanced electrical conductivity with contact area **26**_a_. The contact area **26**_b_ may be formed in third substrate **14**_c_ using well-known lithographic and doping techniques.

[0124] Notably, contact area **26**_b_ may be a counter-doped region or heavily counter-doped region of third substrate **14**_c_ which includes a conductivity that is different from the conductivity of the other portions of third substrate **14**_c_. In this way, contact areas **26**_a_ and **26**_b_ are electrically isolated from the other portions of third substrate **14**_c_. Thus, in this embodiment, second substrate **14**_b_ may be a first conductivity type (for example, an N-type conductivity) and third substrate **14**_c_ may be a second conductivity type (for example, a P-type conductivity). As such, contact area **26**_b_ may be a counter-doped region or heavily counter-doped N-type region which provides suitable, desired and/or predetermined electrical conductivity characteristics when third substrate **14**_c_ is secured to second substrate **14**_b_ and contact areas **26**_a_ and **26**_b_ are in physical contact.

[0125] With reference to FIG. **15**H, microelectromechanical system **10** may be completed by depositing, forming and/or growing insulation layer **32** and a contact opening may be etched to facilitate electrical contact/connection to contact area **26**_b_. The conductive layer **34** (for example, a heavily doped polysilicon, metal (such as aluminum, chromium, gold, silver, molybdenum, platinum, palladium, tungsten, titanium, and/or copper), metal stacks, complex metals and/or complex metal stacks) may then be deposited to provide the appropriate electrical connection to contact **26**_a_ and **26**_b_.

[0126] Notably, insulation layer **32** and/or conductive layer **34** may be formed, grown and/or deposited before or after third substrate **14**_c_ is secured to second substrate **14**_b_. Under these circumstances, when third substrate **14**_c_ is secured to second substrate **14**_b_, the microelectromechanical system **10** may be completed.

[0127] The insulating layer **32** may be, for example, silicon dioxide, silicon nitride, BPSG, PSG, or SOG, or combinations thereof. It may be advantageous to employ silicon nitride because silicon nitride may be deposited in a

more conformal manner than silicon oxide. Moreover, silicon nitride is compatible with CMOS processing, in the event that microelectromechanical system **10** includes CMOS integrated circuits.

[0128] As mentioned above with respect to other embodiments of the present inventions, prior to formation, deposition and/or growth of insulation layer **32** and/or conductive layer **34**, additional micromachined mechanical structures **12** and/or transistors of circuitry **16** may be formed and/or provided in third substrate **14***c* or in other substrates that may be fixed to first substrate **14***a* and/or second substrate **14***b*. (See, for example, FIGS. **16**, **17** and **18**). In this regard, the exposed surface of third substrate **14***c* or another substrate disposed thereon may be a suitable base upon which integrated circuits (for example, CMOS transistors) (see, FIG. **16**) and/or micromachined mechanical structures **12** (see, FIGS. **17** and **18**). Such integrated circuits and micromachined mechanical structures **12** may be fabricated using the inventive techniques described herein and/or well-known fabrication techniques and equipment.

[0129] For example, with reference to FIG. **16**, in one embodiment, transistor regions **36** (which may be integrated circuits (for example, CMOS transistors) of circuitry **16**) may be provided in second substrate **14***b*. The transistor regions **36** may be formed before or after third substrate **14***c* is secured (for example, bonded) to second substrate **14***b*. The fabrication techniques described above and illustrated in FIGS. **5**-**8**B may be employed in the embodiments of FIG. **14**. Indeed, prior to or after formation, deposition and/or growth of insulation layer **32** and/or conductive layer **34**, additional micromachined mechanical structures **12** and/or transistors of circuitry **16** may be formed and/or provided in second substrate **14***b* or in other substrates that may be fixed to first substrate **14***a* and/or second substrate **14***b*. For the sake of brevity, those discussions, in connection with the embodiments of FIG. **15**, will not be repeated.

[0130] Notably, although second cavity **30** is described and illustrated in the previous embodiment as being formed in second substrate **14***b*, second cavity **30** may be formed in third substrate **14***c*, as illustrated in FIGS. **19** and **20**A-**20**H. Indeed, a portion of second cavity **30** may be formed in second substrate **14***b* and a portion of second cavity **30** may be formed in third substrate **14***c*.

[0131] Similarly, first cavity **24** may be formed in second substrate **14***b*, as illustrated in FIG. **21**. Indeed, first cavity **24** and second cavity **30** may both be formed in second substrate **14***b*. (See, for example, FIG. **22**). Moreover, a portion of first cavity **24** may be formed in first substrate **14***a* and a portion of first cavity **24** may be formed in second substrate **14***b*. Indeed, all permutations of formation of first cavity **24** and second cavity **30** are intended to fall within the scope of the present inventions.

[0132] With reference to FIGS. **23**-**30**I, in another embodiment of the present inventions, first substrate **14***a* and/or third substrate **14***c* are/is the same conductivity as second substrate **14***b*. In these embodiments, micromachined mechanical structure **12** may include additional features to electrically isolate contact **20**. For example, with reference to FIG. **23**, in one embodiment, second substrate **14***b* is a semiconductor having the same conductivity as the conductivity of third substrate **14***c*. In this embodiment, micromachined mechanical structure **12** includes isolation trenches **42***a* and **42***b* that isolates contact **20** (and contact areas **26***a* and **26***b*) from portions of third substrate **14***c*. In this exemplary embodiment, the isolation trenches are aligned with isolation regions **44***a* and **44***b* which are disposed in or on second substrate **14***b*.

[0133] The isolation trenches **42***a* and **42***b* may include a material that insulates contact **20** (and contact areas **26***a* and **26***b*) from portions of third substrate **14***c*. In the exemplary embodiment of FIG. **23**, an insulating material, for example, silicon dioxide or silicon nitride, is deposited and/or grown in isolation trenches **42***a* and **42***b*. Indeed, as illustrated, material that forms insulation layer **32** may also be deposited in isolation trenches **42***a* and **42***b*. Notably, FIGS. **24**A-**24**I illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **23**.

[0134] As mentioned above, isolation regions **44***a* and **44***b* which are disposed in or on second substrate **14***b*. The isolation regions **44***a* and **44***b* may be any material or structure that insulates contact **20**, for example, an insulator material and/or an oppositely doped semiconductor region. In the exemplary embodiment of FIG. **23**, isolation regions **44***a* and **44***b* includes oppositely doped semiconductor material.

[0135] With reference to FIG. **25**, in another exemplary embodiment, first substrate **14***a* is a semiconductor having the same conductivity as the conductivity of second substrate **14***b*. In this embodiment, micromachined mechanical structure **12** includes an isolation region **44** that isolates contact **20** (and, in particular, contact area **26***a*) from portions of first substrate **14***a*. In this exemplary embodiment, the isolation region **44** is aligned with cavity **24** and trench **28***a* in order to provide suitable contact isolation. The isolation region **44** may include any material or structure that insulates contact **20**, for example, an insulator material and/or an oppositely doped semiconductor region. In the exemplary embodiment of FIG. **25**, isolation regions **44***a* and **44***b* includes oppositely doped semiconductor material. Notably, FIGS. **26**A-**26**H illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **25**.

[0136] In another exemplary embodiment, first, second and third substrates **14***a*, **14***b* and **14***c* include semiconductor regions having the same conductivity. With reference to FIG. **27**, in this embodiment, micromachined mechanical structure **12** includes an isolation trenches **42***a* and **42***b* as well as isolation regions **44***a*, **44***b*, and **44***c*. The isolation trenches **42***a* and **42***b*, and isolation regions **44***a*, **44***b*, and **44***c*, in combination, electrically isolate contact **20** (and, in particular, contact areas **26***a* and **26***b*) from contiguous portions of first substrate **14***a* and third substrates **14***c*. In this exemplary embodiment, the isolation region **44***a* is aligned with cavity **24** and trench **28***a*, and isolation trenches **42***a* and **42***b* are aligned with isolation regions **44***b* and **44***c*. In this way, contact **20** includes suitable contact isolation.

[0137] The isolation trenches **42***a* and **42***b* may include any material that insulates contact **20** (and contact areas **26***a* and **26***b*) from portions of third substrate **14***c*. In the exemplary embodiment of FIG. **27**, an oppositely doped semiconductor is deposited and/or grown in isolation trenches **42***a* and **42***b*.

[0138] The isolation regions **44***a*, **44***b* and **44***c* may be disposed in or on first substrate **14***a* and/or second substrate **14***b*. In the exemplary embodiment of FIG. **27**, isolation regions **44***a* and **44***b* includes oppositely doped semicon-

ductor material. Notably, FIGS. **28**A-**28**I illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **23**.

[0139] As mentioned above, isolation trenches **42***a* and **42***b* may include any material or structure that insulates contact **20**, for example, an insulator material and/or an oppositely doped semiconductor region. With reference to FIGS. **29** and **30**A-**30**I, isolation trenches **42***a* and **42***b* may include an insulating material (for example, silicon dioxide or silicon nitride) which is deposited and/or grown in isolation trenches **42***a* and **42***b*. As illustrated, material that forms insulation layer **32** may also be deposited in isolation trenches **42***a* and **42***b*. In this regard, FIGS. **30**A-**30**I illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **29**.

[0140] Although not previously illustrated, the present inventions may employ grinding and polishing (using, for example, well known chemical mechanical polishing ("CMP") techniques at various stages in order to, for example, provide a desired surface and/or thickness. For example, with reference to FIGS. **31**A-**31**D, where material **46** is deposited and/or grown in isolation trenches **42***a* and **42***b*, the exposed surface may be subjected to grinding and polishing in order to remove a portion of the deposited and/or grown material from the upper surface of substrate **14***c*. With reference to FIG. **31**C, after grinding and polishing, the surface is prepared for further processing, for example, "back-end" processing (see, for example, FIG. **31**D) or incorporation of additional micromachined mechanical structures **12** and/or transistors of circuitry **16**.

[0141] Notably, it may be advantageous to employ isolation trenches **42** and isolation regions **44** in the embodiments where substrates **14***a* and **14***c* include a conductivity that is different from the conductivity of substrate **14***b*. (See, for example, FIG. **32** and FIGS. **33**A-**33**I). In this embodiment, isolation trenches **42** and isolation regions **44** provide additional electrical isolation for contact **20**. All permutations and/or combinations of such features are intended to fall within the scope of the present inventions.

[0142] The embodiments of FIGS. **23**, **25**, **27**, **29** and **32** may also include circuitry **16** disposed in third substrate **14***c*. The fabrication techniques described above and illustrated in FIGS. **5**-**8**B may be employed in the embodiments of FIGS. **23**, **25**, **27**, **29** and **32**. Indeed, prior to or after formation, deposition and/or growth of insulation layer **32** and/or conductive layer **34**, additional micromachined mechanical structures **12** and/or transistors of circuitry **16** may be formed and/or provided in third substrate **14***c* or in other substrates that may be fixed to first substrate **14***a* and/or second substrate **14***b*. For the sake of brevity, those discussions, in connection with the embodiments of FIGS. **23**, **25**, **27**, **29** and **32**, will not be repeated.

[0143] In another aspect, the present inventions may employ an insulative layer between the substrate in which the micromachined mechanical structures **12** resides and one or more opposing or juxtaposed substrates. Such a configuration may provide certain processing advantages as well as enhance the electrical isolation of the micromachined mechanical structures **12** from one or more opposing or juxtaposed substrates. For example, with reference to FIG. **34**, in this exemplary embodiment, micromachined mechanical structure **12** (including moveable electrode **18** and contact **20**) is formed in second substrate **14***b* and encapsulated via third substrate **14***c*. In this regard, micromachined mechanical structure **12** is formed in a portion of substrate **14***b*. Thereafter, substrate **14***c* is secured (for example, bonded) to exposed surface of substrate **14***b* to encapsulate micromachined mechanical structure **12**. In this embodiment, insulative layers **48***a* (having a thickness of about 1 μm) is disposed and patterned on first substrate **14***a* to provide cavity **24** when second substrate **14***b* is disposed thereon. Similarly, insulative layer **48***b* (having a thickness of about 1 μm) is disposed and patterned on second substrate **14***b* to provide cavity **30** when third substrate **14***c* is disposed thereon. Notably, substrate **14***a*, **14***b* and **14***c* may include the same or different conductivities.

[0144] The insulative layers **48***a* and **48***b* may include, for example, an insulation material (for example, a silicon dioxide, nitride, BPSG, PSG, or SOG, or combinations thereof). It may be advantageous to employ silicon nitride because silicon nitride may be deposited, formed and/or grown in a more conformal manner than silicon oxide. Moreover, silicon nitride is compatible with CMOS processing, in the event that microelectromechanical system **10** includes CMOS integrated circuits in one or more of substrates **14** thereof.

[0145] With reference to FIGS. **35**A-**35**C, an exemplary method of fabricating or forming micromachined mechanical structure **12** according to this embodiment of the present inventions may begin with depositing, forming and/or growing insulative layer **48***a* on first substrate **14***a*. Thereafter, first cavity **24** is formed in insulative layer **48***a* using well-known lithographic and etching techniques. The thickness and characteristics of insulative layer **48***a* may be adjusted to accommodate further processing. For example, insulative layer **48***a* may be polished (using, for example, well known CMP techniques) to provide a smooth planar surface for receipt of second substrate **14***b* and provide a desired depth of first cavity **24**. In one exemplary embodiment, first cavity **24** includes a depth of about 1 μm.

[0146] With reference to FIGS. **35**D-**35**G, second substrate **14***b* may be fixed to insulative layer **48***a* using, for example, well-known bonding techniques such as fusion bonding and/or anodic-like bonding. The insulative layer **48***b* may then be deposited, formed and/or grown on first substrate **14***b*. The second cavity **30** may then be formed in insulative layer **48***b*—again using well-known lithographic and etching techniques. Thereafter, the thickness and characteristics of insulative layer **48***b* may be adjusted to accommodate further processing. For example, insulative layer **48***b* may be polished (using, for example, well known CMP techniques) to provide a smooth planar surface for receipt of second substrate **14***c* and provide a desired depth of second cavity **30**. In one exemplary embodiment, second cavity **24** includes a depth of about 1 μm.

[0147] In addition to forming second cavity **24** in insulative layer **48***b*, contact trench window **50** is also formed therein. (See, FIG. **35**G). In this way, trench **28***a* may be formed concurrently with providing trenches **28***b* and **28***c* which permits definition of contact are **26***a* and moveable electrode **18** simultaneously. The trenches **28***a-c* may be formed using well-known deposition and lithographic techniques. Notably, all techniques for forming or fabricating trenches **28***a-c*, whether now known or later developed, are intended to be within the scope of the present inventions.

[0148] Notably, the first and second substrates **14***b* may be formed from any material now known or later developed. In a preferred embodiment, second substrate **14***b* includes or is

formed from, for example, materials in column IV of the periodic table, for example silicon, germanium, carbon; also combinations of these, for example silicon germanium, or silicon carbide; also of III-V compounds for example gallium phosphide, aluminum gallium phosphide, or other III-V combinations; also combinations of III, IV, V, or VI materials, for example silicon nitride, silicon oxide, aluminum carbide, or aluminum oxide; also metallic silicides, germanides, and carbides, for example nickel silicide, cobalt silicide, tungsten carbide, or platinum germanium silicide; also doped variations including phosphorus, arsenic, antimony, boron, or aluminum doped silicon or germanium, carbon, or combinations like silicon germanium; also these materials with various crystal structures, including single crystalline, polycrystalline, nanocrystalline, or amorphous; also with combinations of crystal structures, for instance with regions of single crystalline and polycrystalline structure (whether doped or undoped).

[0149] Thereafter, third substrate **14***c* may be secured to the exposed portion(s) of insulative layer **48***b*. (See, FIG. **35**H). The third substrate **14***b* may be secured using, for example, well-known bonding techniques such as fusion bonding and/or anodic-like bonding. In conjunction with securing third substrate **14***c* to second substrate **14***b*, the atmosphere (including its characteristics) in which moveable electrode **18** operates may also be defined. Notably, all techniques of defining the atmosphere, including the pressure thereof, during the process of securing third substrate **14***c* to insulative layer **48***b*, whether now known or later developed, are intended to be within the scope of the present inventions.

[0150] The third substrate **14***c* may be formed from any material discussed above relative to first substrate **14***a* and/or second substrate **14***b*. For the sake of brevity, such discussions will not be repeated.

[0151] With reference to FIGS. **35**I and **35**J, after third substrate **14***c* is secured to insulative layer **48***b*, contact area **26***b* may be formed. In this regard, contact area window **52** is formed in third substrate **14***c* and insulative layer **48***b* to expose a portion of contact area **26***a*. Such processing may be performed using well-known lithographic and etching techniques. For example, in one embodiment, where third substrate **14***c* is a semiconductor material (for example silicon), a portion of may be removed using reactive ion etching. Thereafter, a portion of insulative layer **48***b* may be removed to expose contact area **26***b*. In this regard, where insulative layer **48***b* is comprised of silicon dioxide, selected portions may be removed/etched using well-known wet etching techniques and buffered HF mixtures (i.e., a buffered oxide etch) or well-known vapor etching techniques using vapor HF.

[0152] The contact area **26***b* may be deposited, formed and/or grown in contact area window **52**. The contact area **26***b* may be an epitaxially deposited semiconductor that includes a doping that provides the same conductivity as contact area **26***a*. In this way, a suitable, desired and/or predetermined electrical conductivity is provided with contact area **26***a* when third substrate **14***c* is secured to second substrate **14***b*. (See, FIG. **35**K). Thus, contact area **26***b* may be a highly doped polysilicon region which provides enhanced electrical conductivity with contact area **26***a*.

[0153] As mentioned above, although not illustrated, the present inventions may employ grinding and polishing (using, for example, well known chemical mechanical polishing ("CMP") techniques at various stages in order to, for example, provide a desired surface and/or thickness. (See, for example, FIGS. **31**A-**31**D). The formation of contact area **26***b* will likely employ such processing in order to provide the cross-sectional view of FIG. **35**K.

[0154] With reference to FIG. **35**L, microelectromechanical system **10** may be completed by depositing, forming and/or growing insulation layer **32** and a contact opening may be etched to facilitate electrical contact/connection to contact area **26***b*. The conductive layer **34** (for example, a heavily doped polysilicon, metal (such as aluminum, chromium, gold, silver, molybdenum, platinum, palladium, tungsten, titanium, and/or copper), metal stacks, complex metals and/or complex metal stacks) may then be deposited to provide appropriate electrical connection to contact **26***a* and **26***b*.

[0155] Notably, insulation layer **32** and/or conductive layer **34** may be formed, grown and/or deposited before or after third substrate **14***c* is secured to second substrate **14***b*. Under these circumstances, when third substrate **14***c* is secured to second substrate **14***b*, the microelectromechanical system **10** may be completed.

[0156] The insulating layer **32** may be, for example, silicon dioxide, silicon nitride, BPSG, PSG, or SOG, or combinations thereof. It may be advantageous to employ silicon nitride because silicon nitride may be deposited in a more conformal manner than silicon oxide. Moreover, silicon nitride is compatible with CMOS processing, in the event that microelectromechanical system **10** includes CMOS integrated circuits.

[0157] As mentioned above with respect to other embodiments of the present inventions, prior to formation, deposition and/or growth of insulation layer **32** and/or conductive layer **34**, additional micromachined mechanical structures **12** and/or transistors of circuitry **16** may be formed and/or provided in third substrate **14***c* or in other substrates that may be fixed to first substrate **14***a* and/or second substrate **14***b*. In this regard, the exposed surface of third substrate **14***c* or another substrate disposed thereon may be a suitable base upon which integrated circuits (for example, CMOS transistors) and/or micromachined mechanical structures **12**. Such integrated circuits and micromachined mechanical structures **12** may be fabricated using the inventive techniques described herein and/or well-known fabrication techniques and equipment. For the sake of brevity, those discussions, in connection with the embodiments of FIGS. **34** and **35**A-L, will not be repeated.

[0158] With reference to FIGS. **36** and **37**A-**37**I, in another exemplary embodiment, microelectromechanical system **10** may be formed using at least three substrates **14***a-c* and insulative layer **48***a* disposed between substrates **14***a* and **14***b*. In this embodiment, the portion of substrate **14***b* in which micromachined mechanical structure **12** is formed includes a cavity (like that of previous embodiments) as well as a conductivity that is different from the conductivity of the semiconductor of third substrate **14***c*.

[0159] Briefly, with reference to FIGS. **35**A-**35**C, an exemplary method of fabricating or forming micromachined mechanical structure **12** according to this embodiment of the present inventions may begin with depositing, forming and/or growing insulative layer **48***a* on first substrate **14***a*. As mentioned above, insulative layer **48***a* may include, for

example, an insulation material (for example, a silicon dioxide, nitride, BPSG, PSG, or SOG, or combinations thereof).

[0160] Thereafter, first cavity **24** is formed in insulative layer **48***a* using well-known lithographic and etching techniques. (See, FIG. **37**C). The thickness and characteristics of insulative layer **48***a* may be adjusted to accommodate further processing. For example, insulative layer **48***a* may be polished (using, for example, well known CMP techniques) to provide a smooth planar surface for receipt of second substrate **14***b* and provide a desired depth of first cavity **24**. In one exemplary embodiment, first cavity **24** includes a depth of about 1 μm.

[0161] With reference to FIGS. **37**D and **37**E, second substrate **14***b* may be fixed to insulative layer **48***a* using, for example, well-known bonding techniques such as fusion bonding and/or anodic-like bonding. Before or after securing second substrate **14***b* to first substrate **14***a*, second cavity **30** may be formed in second substrate **14***b* using well-known lithographic and etching techniques. In one exemplary embodiment, second cavity **30** also includes a depth of about 1 μm. Thereafter, the thickness of second substrate **14***b* may be adjusted to accommodate further processing. For example, second substrate **14***b* may be grinded and polished (using, for example, well known chemical mechanical polishing ("CMP") techniques) to a thickness of between 10 μm-30 μm.

[0162] With reference to FIG. **37**F, trenches **28***a-c* may be formed to define moveable electrode **18** and contact area **26***a*. The trenches may be formed using well-known deposition and lithographic techniques. Notably, all techniques for forming or fabricating trenches **28***a-c*, whether now known or later developed, are intended to be within the scope of the present inventions.

[0163] The first and second substrates **14***a* and **14***b* may be formed from any material discussed above relative to first substrate **14***a* and/or second substrate **14***b* of other embodiments. For the sake of brevity, such discussions will not be repeated.

[0164] Thereafter, third substrate **14***c* may be secured to the exposed portion(s) of second substrate **14***b*. (See, FIG. **35**G). The third substrate **14***b* may be secured using, for example, well-known bonding techniques such as fusion bonding, anodic-like bonding and/or silicon direct bonding. In conjunction with securing third substrate **14***c* to second substrate **14***b*, the atmosphere (including its characteristics) in which moveable electrode **18** operates may also be defined. Notably, all techniques of defining the atmosphere, including the pressure thereof, during the process of securing third substrate **14***c* to second substrate **14***b*, whether now known or later developed, are intended to be within the scope of the present inventions.

[0165] Like first and second substrates **14***a* and **14***b*, third substrate **14***c* may be formed from any material discussed above relative to first, second and/or third substrates of other embodiments. For the sake of brevity, such discussions will not be repeated.

[0166] Before or after third substrate **14***c* is secured to second substrate **14***b*, contact area **26***b* may be formed in a portion of third substrate **14***c* to be aligned with, connect to or overlie contact area **26***a*. The contact area **26***b* may be a semiconductor region that includes a doping that provides the same conductivity as contact area **26***a*. In this way, a suitable, desired and/or predetermined electrical conductivity is provided with contact area **26***a* when third substrate **14***c* is secured to second substrate **14***b*. (See, FIG. **37**H). Thus, contact area **26***b* may be a highly doped region of third substrate **14***c* which provides enhanced electrical conductivity with contact area **26***a*. The contact area **26***b* may be formed in third substrate **14***c* using well-known lithographic and doping techniques.

[0167] Notably, contact area **26***b* may be a heavily counter-doped region of third substrate **14***c* which includes a conductivity that is different from the conductivity of the other portions of third substrate **14***c*. In this way, contact areas **26***a* and **26***b* are electrically isolated from the other portions of third substrate **14***c*. Thus, in this embodiment, second substrate **14***b* may be a first conductivity type (for example, an N-type conductivity) and third substrate **14***c* may be a second conductivity type (for example, a P-type conductivity). As such, contact area **26***b* may be a heavily counter-doped N-type region which provides suitable, desired and/or predetermined electrical conductivity characteristics when third substrate **14***c* is secured to second substrate **14***b* and contact areas **26***a* and **26***b* are in physical contact.

[0168] With reference to FIG. **37**I, microelectromechanical system **10** may be completed by depositing, forming and/or growing insulation layer **32** and a contact opening may be etched to facilitate electrical contact/connection to contact area **26***b*. The conductive layer **34** (for example, a heavily doped polysilicon, metal (such as aluminum, chromium, gold, silver, molybdenum, platinum, palladium, tungsten, titanium, and/or copper), metal stacks, complex metals and/or complex metal stacks) may then be deposited to provide appropriate electrical connection to contact **26***a* and **26***b*.

[0169] Notably, insulation layer **32** and/or conductive layer **34** may be formed, grown and/or deposited before or after third substrate **14***c* is secured to second substrate **14***b*. Under these circumstances, when third substrate **14***c* is secured to second substrate **14***b*, the microelectromechanical system **10** may be completed.

[0170] The insulating layer **32** may be, for example, silicon dioxide, silicon nitride, BPSG, PSG, or SOG, or combinations thereof. It may be advantageous to employ silicon nitride because silicon nitride may be deposited in a more conformal manner than silicon oxide. Moreover, silicon nitride is compatible with CMOS processing, in the event that microelectromechanical system **10** includes CMOS integrated circuits.

[0171] As mentioned above with respect to other embodiments of the present inventions, prior to formation, deposition and/or growth of insulation layer **32** and/or conductive layer **34**, additional micromachined mechanical structures **12** and/or transistors of circuitry **16** may be formed and/or provided in third substrate **14***c* or in other substrates that may be fixed to first substrate **14***a* and/or second substrate **14***b*. In this regard, the exposed surface of third substrate **14***c* or another substrate disposed thereon may be a suitable base upon which integrated circuits (for example, CMOS transistors) and/or micromachined mechanical structures **12**. Such integrated circuits and micromachined mechanical structures **12** may be fabricated using the inventive techniques described herein and/or well-known fabrication techniques and equipment. For the sake of brevity, those discussions, in connection with the embodiments of FIGS. **36** and **37**A-I, will not be repeated.

[0172] In this embodiment, the portion of substrate **14***b* in which micromachined mechanical structure **12** is formed includes a conductivity that is the same as the conductivity of the semiconductor of third substrate **14***c*. In this embodiment, micromachined mechanical structure **12** includes an isolation trenches **42***a* and **42***b* as well as isolation regions **44***a* and **44***b*. The isolation trenches **42***a* and **42***b*, and isolation regions **44***a* and **44***b*, in combination, electrically isolate contact **20** (and, in particular, contact areas **26***a* and **26***b*) from contiguous portions of third substrate **14***c*. In this exemplary embodiment, isolation region **44***a* is aligned with cavity **24** and trench **28***a*, and isolation trenches **42***a* and **42***b* are aligned with isolation regions **44***b* and **44***c*. In this way, contact **20** includes suitable contact isolation.

[0173] Briefly, with reference to FIGS. **39**A-**39**D and **39**F, an exemplary method of fabricating or forming micromachined mechanical structure **12** according to this embodiment of the present inventions may be substantially the same as with the previous embodiment. For the sake of brevity those discussions will not be repeated.

[0174] With reference to FIG. **39**E, in this embodiment, isolation regions **44***a* and **44***b* are deposited and/or implanted into portions of substrate **14***b* in order to facilitate electrical isolation of contact **20** after second substrate **14***b* is secured or fixed (via, for example, bonding). The isolation regions **44***a* and **44***b* may be any material or structure that insulates contact **20**, for example, an insulator material and/or an oppositely doped semiconductor region. In the illustrative example, isolation regions **44***a* and **44***b* are oppositely doped semiconductor region (relative to the conductivity of substrate **14***c*).

[0175] With reference to FIG. **39**F, trenches **28***a-c* may be formed to define moveable electrode **18** and contact area **26***a*. The trenches may be formed using well-known deposition and lithographic techniques. Notably, all techniques for forming or fabricating trenches **28***a-c*, whether now known or later developed, are intended to be within the scope of the present inventions.

[0176] Thereafter, third substrate **14***c* may be secured to the exposed portion(s) of second substrate **14***b*. (See, FIG. **39**G). The third substrate **14***b* may be secured using, for example, well-known bonding techniques such as fusion bonding, anodic-like bonding and/or silicon direct bonding. In conjunction with securing third substrate **14***c* to second substrate **14***b*, the atmosphere (including its characteristics) in which moveable electrode **18** operates may also be defined. Notably, all techniques of defining the atmosphere, including the pressure thereof, during the process of securing third substrate **14***c* to second substrate **14***b*, whether now known or later developed, are intended to be within the scope of the present inventions.

[0177] Thereafter, isolation trenches **42***a* and **42***b* are formed in portions of third substrate **14***c*. (See, FIG. **39**H). The isolation trenches **42***a* and **42***b* may be formed using well-known lithographic and etching techniques. In this exemplary embodiment, the isolation trenches are aligned with isolation regions **44***a* and **44***b* which are disposed in or on second substrate **14***b*.

[0178] With reference to FIG. **39**I, isolation trenches **42***a* and **42***b* may include a material that insulates contact **20** (and contact areas **26***a* and **26***b*) from portions of third substrate **14***c*. In the exemplary embodiment, an insulating material, for example, silicon dioxide or silicon nitride, is deposited and/or grown in isolation trenches **42***a* and **42***b*. Indeed, as illustrated, material that forms insulation layer **32** may also be deposited in isolation trenches **42***a* and **42***b*. Notably, isolation trenches **42***a* and **42***b* may include any material that insulates contact **20** (and contact areas **26***a* and **26***b*) from portions of third substrate **14***c*.

[0179] With reference to FIG. **39**I-**39**K, microelectromechanical system **10** may be completed by depositing, forming and/or growing insulation layer **32** and a contact opening may be etched to facilitate electrical contact/connection to contact area **26***b*. The processing may be the same or similar to that described herein with any of the other embodiments. For the sake of brevity, those discussions will not be repeated.

[0180] Moreover, as mentioned above with respect to other embodiments of the present inventions, prior to formation, deposition and/or growth of insulation layer **32** and/or conductive layer **34**, additional micromachined mechanical structures **12** and/or transistors of circuitry **16** may be formed and/or provided in third substrate **14***c* or in other substrates that may be fixed to first substrate **14***a* and/or second substrate **14***b*. In this regard, the exposed surface of third substrate **14***c* or another substrate disposed thereon may be a suitable base upon which integrated circuits (for example, CMOS transistors) and/or micromachined mechanical structures **12**. Such integrated circuits and micromachined mechanical structures **12** may be fabricated using the inventive techniques described herein and/or well-known fabrication techniques and equipment. For the sake of brevity, those discussions, in connection with the embodiments of FIGS. **38** and **39**A-K, will not be repeated.

[0181] In another embodiment, with reference to FIG. **40**, after formation of cavity **18** in first substrate **14***a*, intermediate layer **54** is deposited or grown before second substrate **148** is secured to first substrate **14***a*. In one embodiment, intermediate layer **54** may be a native oxide. In another embodiment, a thin insulating layer is deposited. In this way, first substrate **14***a* is electrically isolated from second substrate **14***b*. Thereafter, second substrate **14***b* may be fixed to intermediate layer **54** using, for example, well-known bonding techniques such as fusion bonding and/or anodic-like bonding. Before or after securing second substrate **14***b* to first substrate **14***a*, second cavity **30** may be formed in second substrate **14***b* using well-known lithographic and etching techniques. In one exemplary embodiment, second cavity **30** also includes a depth of about 1 μm. Thereafter, the thickness of second substrate **14***b* may be adjusted to accommodate further processing. For example, second substrate **14***b* may be grinded and polished (using, for example, well known chemical mechanical polishing ("CMP") techniques) to a thickness of between 10 μm-30 μm.

[0182] FIGS. **41**A-**41**H illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **23**. For the sake of brevity, the exemplary process flow will not be discussed in detail; reference however, is made to the discussions above.

[0183] The embodiment including intermediate layer **54** may be employed in conjunction with any of the embodiments described herein. (See, for example, FIGS. **42**A and **42**B, **43**A-**43**K). For the sake of brevity, the exemplary process flow will not be discussed in detail; reference however, is made to the discussions above.

[0184] There are many inventions described and illustrated herein. While certain embodiments, features, materi-

als, configurations, attributes and advantages of the inventions have been described and illustrated, it should be understood that many other, as well as different and/or similar embodiments, features, materials, configurations, attributes, structures and advantages of the present inventions that are apparent from the description, illustration and claims (are possible by one skilled in the art after consideration and/or review of this disclosure). As such, the embodiments, features, materials, configurations, attributes, structures and advantages of the inventions described and illustrated herein are not exhaustive and it should be understood that such other, similar, as well as different, embodiments, features, materials, configurations, attributes, structures and advantages of the present inventions are within the scope of the present inventions.

[0185] Each of the aspects of the present inventions, and/or embodiments thereof, may be employed alone or in combination with one or more of such aspects and/or embodiments. (See, for example, FIGS. **42**A and **42**B, **43**A-**43**K). For the sake of brevity, those permutations and combinations will not be discussed separately herein. As such, the present inventions are not limited to any single aspect or embodiment thereof nor to any combinations and/or permutations of such aspects and/or embodiments.

[0186] Notably, it may be advantageous to adjust the alignment and etch processes to enhance electrical isolation of portions of micromachined mechanical structure **12**, for example, contact **20** (including contact areas **26***a* and **26***b*). For example, with reference to FIG. **44**, trench **28***a* may be aligned to provide suitable or predetermined overlap of isolation region **44***a* and **44***b* as well as include suitable or predetermined over etch into isolation region **44***a*. Further, isolation region **44***c* may include dimensions such that when cavity **30** is formed, a portion of isolation region **44***c* is removed. (See, FIGS. **45**C and **45**D). Moreover, with reference to FIG. **46**A, isolation trenches **42***a* and **42***b* may include suitable or predetermined over etch into isolation regions **44***a* and **44***b*. Indeed, isolation trench **28***a* may be substantially larger and/or have considerably different tolerances than trenches **28***b* and **28***c* given that the dimensions of the trench are insignificant relative to trenches **28***b* and **28***c* which may largely define the mechanical structure of the system **10**. (See, FIG. **46**B). Such processing techniques may be applied to any of the embodiments described and/or illustrated herein.

[0187] Further, the processing flows described and illustrated herein are exemplary. These flows, and the order thereof, may be modified. All process flows, and orders thereof, to provide microelectromechanical system **10** and/or micromachined mechanical structure **12**, whether now known or later developed, are intended to fall within the scope of the present inventions. For example, there are many techniques to form moveable electrode **18** and contact **20** (and in particular contact area **26***a*). With reference to FIG. **47**A-**47**D, in one embodiment, mask **56***a* may be deposited and patterned. Thereafter, cavity **30** may be formed (See, FIGS. **47**A and **47**B). Thereafter, mask **56***b* may be deposited and patterned in order to form and define moveable electrode **18** and contact area **26** (See, FIGS. **47**C and **47**D).

[0188] Alternatively, with reference to FIGS. **48**A-**48**C, masks **56***a* and **56***b* may be deposited and patterned. After trenches **28***a*-**28***c* are formed, mask **56***b* may be removed and cavity **30** may be formed.

[0189] Further, substrates **14** may be processed to a predetermined and/or suitable thickness before and/or after other processing during the fabrication of microelectromechanical system **10** and/or micromachined mechanical structure **12**. For example, with reference to FIGS. **49**A-**49**G, in one embodiment, first substrate **14***a* may be a relatively thick wafer which is grinded (and polished) after substrates **14***b* and **14***c* are secured to a corresponding substrate (for example, bonded) and processed to form, for example, micromachined mechanical structure **12**. (Compare, for example, FIGS. **49**A-G and **49**H).

[0190] The processing flows described and illustrated with respect to substrate **14***c* may also be modified. For example, with reference to FIGS. **50**A-**50**G, in one embodiment, substrate **14***c* may be a relatively thick wafer which is grinded (and polished) after secured to a corresponding substrate (for example, bonded). In this exemplary embodiment, substrate **14***c* is grinded and polished after being bonded to substrate **14***b*. (Compare, for example, FIGS. **50**C and **50**D) Thereafter, contact **20** may be formed. (See, for example, FIGS. **50**E-**50**G).

[0191] Indeed, substrate **14***a* and **14***c* may be processed (for example, grinded and polished) after other processing. (See, for example, FIGS. **51**A-**51**J). Notably, all processing flows with respect to substrates **14** are intended to fall within the scope of the present invention.

[0192] Further, as mentioned above, each of the aspects of the present inventions, and/or embodiments thereof, may be employed alone or in combination with one or more of such aspects and/or embodiments. For example, with reference to FIG. **52**, microelectromechanical system **10** may include implant regions **58***a* and **58***b* in substrate **14***c* to facilitate electrically isolation of contact area **26***b* from other portions of substrate **14***c*. In this embodiment implant regions **58***a* and **58***b* may be any material or structure that insulates contact **20**, for example, an oppositely doped semiconductor region. FIGS. **53**A-**53**H illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **52** wherein implant regions **58***a* and **58***b* are oppositely doped semiconductor regions.

[0193] Notably, implant regions **58***a* and **58***b* may be employed in any of the embodiments described and illustrated herein. For example, the implant regions **58***a* and **58***b* may be employed in conjunction with or in lieu of isolation trenches **42***a* and **42***b*.

[0194] In addition, as mentioned above, isolation regions **44***a* and **44***b* may be deposited and/or implanted into portions of substrate **14***b* in order to facilitate electrical isolation of contact **20** after third substrate **14***c* (or second substrate **14***b* where an SOI substrate **14***a* is employed (see, FIG. **11**)) is secured or fixed (via, for example, bonding). The isolation regions **44***a* and **44***b* may be any material or structure that insulates contact **20**, for example, an insulation material and/or an oppositely doped semiconductor region. FIGS. **55**A-**55**K illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **54** wherein isolation regions **44***a* and **44***b* are insulation material (for example, a silicon nitride or silicon dioxide) and an insulation material is disposed in isolation trenches **42***a* and **42***b*.

[0195] Further, as an alternative to counter-doping a region in substrate **14***c* to form contact area **26***b*, with reference to FIG. **56** and FIGS. **57**A-**57**J, contact area **26***b* may be formed by providing a "window" in substrate **14***c* (for example, etching a portion of substrate **14***c* as illustrated

in FIG. **57**H) and thereafter depositing a suitable material to provide electrical conductivity with the underlying contact area **26***a*. Notably, the material (for example, a doped polysilicon) which forms contact area **26***b* may be deposited by epitaxial deposition and thereafter planarized to provide a suitable surface for contact **20** formation. (See, for example, FIGS. **57**H and **57**I).

[0196] As mentioned above, all forms of bonding, whether now known or later developed, are intended to fall within the scope of the present invention. For example, bonding techniques such as fusion bonding, anodic-like bonding, silicon direct bonding, soldering (for example, eutectic soldering), thermo compression, thermo-sonic bonding, laser bonding and/or glass reflow bonding, and/or combinations thereof.

[0197] Notably, any of the embodiments described and illustrated herein may employ a bonding material and/or a bonding facilitator material (disposed between substrates, for example, the second and third substrates) to, for example, enhance the attachment of or the "seal" between the substrates (for example, between the first and second substrates **14***a* and **14***b*, and/or the second and third substrates **14***b* and **14***c*), address/compensate for planarity considerations between substrates to be bonded (for example, compensate for differences in planarity between bonded substrates), and/or to reduce and/or minimize differences in thermal expansion (that is materials having different coefficients of thermal expansion) of the substrates and materials therebetween (if any). Such materials may be, for example, solder, metals, frit, adhesives, BPSG, PSG, or SOG, or combinations thereof.

[0198] With reference to FIG. **58**, in one exemplary embodiment, bonding material or bonding facilitator material **60** may be disposed between substrates **14***b* and **14***c*. Such a configuration may provide certain advantages. For example, in this exemplary embodiment, micromachined mechanical structure **12** (including moveable electrode **18** and contact **20**) is formed in second substrate **14***b* and encapsulated via third substrate **14***c*. In this regard, micromachined mechanical structure **12** is formed in a portion of substrate **14***b*. Thereafter, substrate **14***c* is secured (for example, bonded) to exposed surface of substrate **14***b* to encapsulate micromachined mechanical structure **12**. In this embodiment, bonding material or bonding facilitator material **60** (for example, having a thickness of about 1 μm) is disposed and patterned on second substrate **14***b* to provide cavity **30** when third substrate **14***c* is disposed thereon and bonded thereto. Notably, substrates **14***a*, **14***b* and **14***c* may include the same or different conductivities.

[0199] As mentioned above, bonding material or bonding facilitator material **60** may include, for example, solder, metals, frit, adhesives, BPSG, PSG, or SOG, or combinations thereof. It may be advantageous to employ BPSG, PSG, or SOG in order to electrically isolate contact **20** from portions of substrates **14***b* and/or **14***c*. Moreover, BPSG, PSG, or SOG is compatible with CMOS processing, in the event that microelectromechanical system **10** includes CMOS integrated circuits in one or more of substrates **14** thereof.

[0200] Notably, FIGS. **59**A-**59**J illustrate an exemplary process flow for fabricating microelectromechanical system **10** of FIG. **58**. The process flow may employ a flow which is substantially similar to the process of FIGS. **35**A-**35**L—with the exception that bonding material or bonding facilitator material **60** is employed (deposited and patterned) in addition to or in lieu of insulative layer **48***b* of FIGS. **35**E-**35**L. For the sake of brevity, the discussion will not be repeated here.

[0201] An alternative embodiment employing bonding material or bonding facilitator material **60**, and technique for fabricating such embodiment, is illustrated in FIGS. **60** and **61**A-**61**K, respectively. In this embodiment, bonding material and/or a bonding facilitator material **60** is provided prior to formation of resonator **18** and contact area **26***a* (via contact area trench **28***a* and moveable electrode trenches **28***b* and **28***c*). As mentioned above, all process flows, and orders thereof, to provide microelectromechanical system **10** and/or micromachined mechanical structure **12**, whether now known or later developed, are intended to fall within the scope of the present inventions.

[0202] The embodiments employing bonding material or bonding facilitator material **60** may be implemented in any of the embodiments described herein. For example, transistors of a transistor region may be formed prior to securing third substrate **14***c* to second substrate **14***b*. (See, for example, FIGS. **7**A and **7**B). Indeed, all of the "back-end" processing, in addition to formation of the transistors of transistor region, may be completed prior to securing third substrate **14***c* to second substrate **14***b*. (See, for example, FIGS. **8**A and **8**B).

[0203] Moreover, any of the bonding material or bonding facilitator materials **60** (may include, for example, solder, metals, frit, adhesives, BPSG, PSG, or SOG, or combinations thereof may be implemented between the first and second substrates **14***a* and **14***b*, and/or the second and third substrates **14***b* and **14***c*, and/or any other substrates that are bonded. All such permutations are intended to fall within the scope of the present inventions.

[0204] Further, with respect to any of the embodiments described herein, circuitry **16** may be integrated in or on substrate **14**, disposed in a separate substrate, and/or in one or more substrates that are connected to substrate **14** (for example, in one or more of the encapsulation wafer(s)). (See, for example, FIGS. **62**-**64**). In this regard, microelectromechanical device **10** may include micromachined mechanical structure **12** and circuitry **16** as a monolithic-like structure including mechanical structure **12** and circuitry **16** in one substrate.

[0205] The micromachined mechanical structure **12** and/or circuitry **16** may also reside on separate, discrete substrates. (See, for example, FIGS. **65** and **66**A-**66**F). In this regard, in one embodiment, such separate discrete substrate may be bonded to or on substrate **14**, before, during and/or after fabrication of micromachined mechanical structure **12** and/or circuitry **16**. (See, for example FIGS. **5**, **6**A-**6**D, **7**A-**7**C and **8**A).

[0206] For example, as mentioned above, the electronics or electrical circuitry may be clock alignment circuitry, for example, one or more phase locked loops (PLLs), delay locked loops (DLLs), digital/frequency synthesizer (for example, a direct digital synthesizer ("DDS"), frequency synthesizer, fractional synthesizer and/or numerically controlled oscillator) and/or frequency locked loops (FLLs). In this regard, the output of mechanical structure **12** (for example, an microelectromechanical oscillator or microelectromechanical resonator) is employed as a reference input signal (i.e., the reference clock). The PLL, DLL, digital/frequency synthesizer and/or FLL may provide frequency multiplication (i.e., increase the frequency of the

output signal of the microelectromechanical oscillator). The PLL, DLL, digital/frequency synthesizer and/or FLL may also provide frequency division (i.e., decrease the frequency of the output signal of the microelectromechanical oscillator). Moreover, the PLL, DLL, digital/frequency synthesizer and/or FLL may also compensate using multiplication and/or division to adjust, correct, compensate and/or control the characteristics (for example, the frequency, phase and/or jitter) of the output signal of the microelectromechanical resonator.

[0207] The multiplication or division (and/or phase adjustments) by compensation circuitry **18** may be in fine or coarse increments. For example, compensation circuitry **18** may include an integer PLL, a fractional PLL and/or a fine-fractional-N PLL to precisely select, control and/or set the output signal of compensated microelectromechanical oscillator. In this regard, the output of microelectromechanical resonator may be provided to the input of the fractional-N PLL and/or the fine-fractional-N PLL (hereinafter collectively "fractional-N PLL"), which may be pre-set, pre-programmed and/or programmable to provide an output signal having a desired, selected and/or predetermined frequency and/or phase.

[0208] Notably, in one embodiment, the parameters, references (for example, frequency and/or phase), values and/or coefficients employed by the compensation circuitry in order to generate and/or provide an adjusted, corrected and/or controlled output having, for example, a desired, selected and/or predetermined frequency and/or phase (i.e., the function of the compensation circuitry), may be externally provided to the compensation circuitry either before or during operation of compensated microelectromechanical oscillator. In this regard, a user or external circuitry/devices/systems may provide information representative of the parameters, references, values and/or coefficients to set, change, enhance and/or optimize the performance of the compensation circuitry and/or compensated microelectromechanical oscillator.

[0209] Finally, it should be further noted that while the present inventions will be described in the context of microelectromechanical systems including micromechanical structures or elements, the present inventions are not limited in this regard. Rather, the inventions described herein are applicable to other electromechanical systems including, for example, nanoelectromechanical systems. Thus, the present inventions are pertinent, as mentioned above, to electromechanical systems, for example, gyroscopes, resonators, temperatures sensors, accelerometers and/or other transducers.

[0210] The term "depositing" and other forms (i.e., deposit, deposition and deposited) in the claims, means, among other things, depositing, creating, forming and/or growing a layer of material using, for example, a reactor (for example, an epitaxial, a sputtering or a CVD-based reactor (for example, APCVD, LPCVD, or PECVD)).

[0211] Further, in the claims, the term "contact" means a conductive region, partially or wholly disposed outside the chamber, for example, the contact area and/or contact via.

[0212] It should be further noted that the term "circuit" may mean, among other things, a single component or a multiplicity of components (whether in integrated circuit form or otherwise), which are active and/or passive, and which are coupled together to provide or perform a desired function. The term "circuitry" may mean, among other things, a circuit (whether integrated or otherwise), a group of such circuits, one or more processors, one or more state machines, one or more processors implementing software, or a combination of one or more circuits (whether integrated or otherwise), one or more state machines, one or more processors, and/or one or more processors implementing software. The term "data" may mean, among other things, a current or voltage signal(s) whether in an analog or a digital form.

[0213] The embodiments of the inventions described herein may include one or more of the following advantages, among others:

- **[0214]** embodiments presenting mechanically robust encapsulation;
- **[0215]** embodiments presenting clean environment for micromachined mechanical structure **12** (and the electrodes thereof);
- **[0216]** embodiments presenting relatively less expensive fabrication in comparison to conventional techniques;
- **[0217]** embodiments presenting relatively smaller footprint in comparison to conventional techniques;
- **[0218]** embodiments presenting one or more surfaces compatible with/for CMOS circuitry/integration;
- **[0219]** embodiments presenting single crystal surfaces (where one or more substrates are single crystal);
- **[0220]** embodiments presenting diffused contacts;
- **[0221]** embodiments eliminating epitaxial depositions;
- **[0222]** embodiments eliminating SOI substrates;
- **[0223]** embodiments presenting improved CMOS compatibility;
- **[0224]** embodiments providing enhanced atmosphere/environment control and characteristics (for example, improved vacuum and lower/no chlorine;
- **[0225]** improved gap control for definition of micromachined mechanical structure;
- **[0226]** embodiments eliminating timed release of moveable electrodes (for example, timed HF (vapor) etch);
- **[0227]** embodiments eliminating oxide stress in substrates;
- **[0228]** embodiments providing enhanced stiction characteristics (for example, less vertical stiction); and
- **[0229]** embodiments eliminating vents in the resonator and the attendant shortcomings of thin film encapsulation.

[0230] The above embodiments of the present inventions are merely exemplary embodiments. They are not intended to be exhaustive or to limit the inventions to the precise forms, techniques, materials and/or configurations disclosed. Many modifications and variations are possible in light of the above teaching. It is to be understood that other embodiments may be utilized and operational changes may be made without departing from the scope of the present inventions. As such, the foregoing description of the exemplary embodiments of the inventions has been presented for the purposes of illustration and description. It is intended that the scope of the inventions not be limited to the description above.

1-30. (canceled)

31. A system comprising:

a first substrate;

a chamber;

a microelectromechanical structure, wherein the microelectromechanical structure is (i) formed from a portion of the first substrate and (ii) at least partially disposed in the chamber;
a second substrate, bonded to the first substrate, wherein a surface of the second substrate forms a wall of the chamber;
circuitry disposed in or on the second substrate; and
a contact, wherein:
a first portion of the contact is (i) formed from a portion of the first substrate and (ii) at least a portion thereof is disposed outside the chamber; and
a second portion of the contact is formed from a portion of the second substrate.

32. The system of claim **31** wherein:
the first substrate includes carbon, polycrystalline silicon, porous polycrystalline silicon, amorphous silicon, silicon carbide, silicon/germanium, germanium, and/or gallium arsenide; and
the second substrate includes carbon, polycrystalline silicon, porous polycrystalline silicon, amorphous silicon, silicon carbide, silicon/germanium, germanium, and/or gallium arsenide.

33. The system of claim **32** wherein:
the first portion of the contact is a semiconductor material having a first conductivity;
the second substrate is a semiconductor material having a second conductivity; and
the second portion of the contact is a semiconductor material having the first conductivity.

34. The system of claim **33** wherein the second portion of the contact is a semiconductor material that is counterdoped to include the first conductivity.

35. The system of claim **31** further including a trench disposed in the second substrate and around at least a portion of the second portion of the contact.

36. The system of claim **35** wherein the trench includes an insulation material disposed therein to electrically isolate the second portion of the contact from the second substrate.

37. The system of claim **31** wherein the first substrate is a semiconductor on insulator substrate.

38. The system of claim **31** wherein the first and second substrates are bonded using fusion bonding, anodic-like bonding, silicon direct bonding, soldering, thermo compression, thermo-sonic, laser bonding and/or glass reflow.

39. The system of claim **31** wherein the contact is electrically coupled to the circuitry.

40. The system of claim **39** wherein the circuitry generates clock signals from an output signal of the microelectromechanical structure.

41. The system of claim **40** wherein the circuitry adjusts, compensates, corrects and/or controls the frequency and/or phase compensation of the output signal of the microelectromechanical structure.

42. The system of claim **41** wherein the circuitry includes one or more phase locked loops, delay locked loops, digital synthesizer, frequency synthesizer, fractional synthesizer, numerically controlled oscillator, and/or frequency locked loops.

43. The system of claim **31** wherein the microelectromechanical device is a portion of an accelerometer, gyroscope, transducer, filter and/or resonator.

44. The system of claim **31** wherein the microelectromechanical structure includes more than one mechanical structure.

45. The system of claim **44** wherein at least one of the mechanical structures is a filter, resonator, accelerometer, gyroscope, pressure sensor, strain sensor, tactile sensor, magnetic sensor or temperature sensor.

46. A system comprising:
a first substrate;
a second substrate, wherein the second substrate is bonded to the first substrate;
a chamber;
a microelectromechanical structure, wherein the microelectromechanical structure is (i) formed from a portion of the second substrate and (ii) at least partially disposed in the chamber;
a third substrate, bonded to the second substrate, wherein a surface of the third substrate forms a wall of the chamber; and
circuitry disposed in or on the third substrate.

47. The system of claim **46** wherein:
the first substrate includes carbon, polycrystalline silicon, porous polycrystalline silicon, amorphous silicon, silicon carbide, silicon/germanium, germanium, and/or gallium arsenide; and
the second substrate includes carbon, polycrystalline silicon, porous polycrystalline silicon, amorphous silicon, silicon carbide, silicon/germanium, germanium, and/or gallium arsenide.

48. The system of claim **46** further including a contact having:
a first portion of the contact (i) formed from a portion of the second substrate and (ii) at least a portion thereof being disposed outside the chamber; and
a second portion of the contact formed from a portion of the third substrate;
wherein:
the first portion of the contact is a semiconductor material having a first conductivity;
the third substrate is a semiconductor material having a second conductivity; and
the second portion of the contact is a semiconductor material having the first conductivity.

49. The system of claim **48** wherein the second portion of the contact is a polycrystalline or monocrystalline silicon that is counterdoped to include the first conductivity.

50. The system of claim **46** further including:
a contact having:
a first portion of the contact (i) formed from a portion of the second substrate and (ii) at least a portion thereof being disposed outside the chamber; and
a second portion of the contact formed from a portion of the third substrate; and
a trench disposed in the third substrate and around at least a portion of the second portion of the contact.

51. The system of claim **50** wherein the trench includes an insulation material disposed therein to electrically isolate the second portion of the contact from the third substrate.

52. The system of claim **50** further including an isolation region disposed in the second substrate such that the trench is aligned with and juxtaposed to the isolation region.

53. The system of claim **52** wherein:
the first portion of the contact is a semiconductor material having a first conductivity;

the isolation region is a semiconductor material having a second conductivity; and
the second portion of the contact is a semiconductor material having the first conductivity.

54. The system of claim **46** further including:
a contact having:
a first portion of the contact (i) formed from a portion of the second substrate and (ii) at least a portion thereof being disposed outside the chamber; and
a second portion of the contact formed from a portion of the third substrate; and
an isolation region, disposed in the first substrate such that a first portion of the contact is aligned with and juxtaposed to the isolation region.

55. The system of claim **46** further including:
a contact having:
a first portion of the contact (i) formed from a portion of the second substrate and (ii) at least a portion thereof being disposed outside the chamber; and
a second portion of the contact formed from a portion of the third substrate;
a first isolation region, disposed in the first substrate such that the first portion of the contact is aligned with and juxtaposed to the first isolation region; and
a second isolation region, disposed in the second substrate such that the second portion of the contact is aligned with and juxtaposed to the second isolation region.

56. The system of claim **55** wherein:
the first and second portions of the contact are semiconductor materials having a first conductivity; and
the first and second isolation regions are semiconductor materials having the second conductivity.

57. The system of claim **56** further including a trench, disposed in the third substrate and around at least a portion of the second portion of the contact.

58. The system of claim **57** wherein the trench includes an insulation material disposed therein to electrically isolate the second portion of the contact from the third substrate.

59. The system of claim **58** wherein the trench is aligned with and juxtaposed to the second isolation region.

60. The system of claim **46** wherein the second and third substrates are bonded using fusion bonding, anodic-like bonding, silicon direct bonding, soldering, thermo compression, thermo-sonic, laser bonding and/or glass reflow.

61. The system of claim **46** wherein the contact is electrically coupled to the circuitry.

62. The system of claim **61** wherein the circuitry generates clock signals from an output signal of the microelectromechanical structure.

63. The system of claim **62** wherein the circuitry adjusts, compensates, corrects and/or controls the frequency and/or phase compensation of the output signal of the microelectromechanical structure.

64. The system of claim **63** wherein the circuitry includes one or more phase locked loops, delay locked loops, digital synthesizer, frequency synthesizer, fractional synthesizer, numerically controlled oscillator, and/or frequency locked loops.

65. The system of claim **61** wherein the microelectromechanical device is a portion of an accelerometer, gyroscope, transducer, filter and/or resonator.

66. The system of claim **46** wherein the microelectromechanical structure includes more than one mechanical structure.

67. The system of claim **66** wherein at least one of the mechanical structures is a filter, resonator, accelerometer, gyroscope, pressure sensor, strain sensor, tactile sensor, magnetic sensor or temperature sensor.

* * * * *