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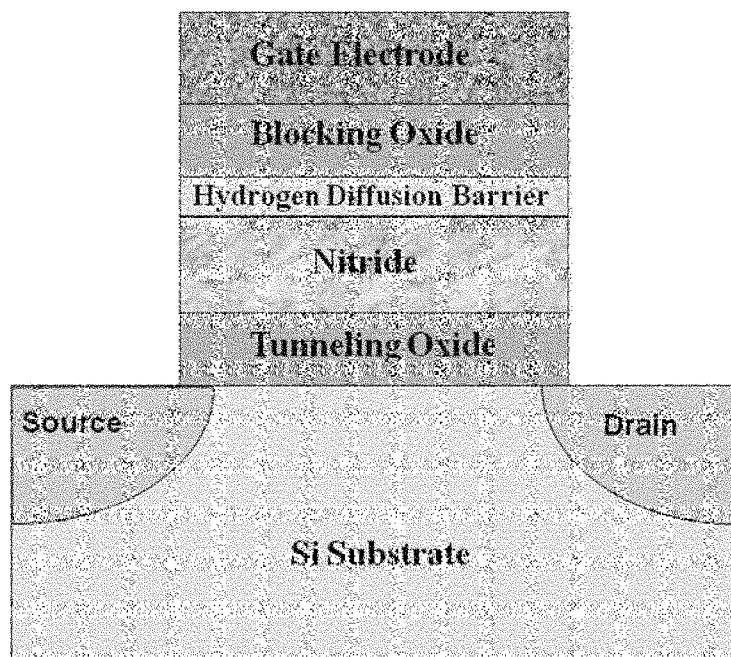
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(54) **Title:** SEMICONDUCTOR DEVICE COMPRISING A HYDROGEN DIFFUSION BARRIER AND METHOD OF FABRICATING SAME



(57) **Abstract:** A hydrogen diffusion barrier made of SiAlON is fabricated in the semiconductor device so that hydrogen diffusion may be prevented or reduced by this barrier. One method of fabricating the barrier is to heat or anneal the layers of silicon nitride and aluminum oxide to form a layer of SiAlON at the interface of these layers. Hydrogen from diffusing into layers of a semiconductor device and degrading the device by, e.g., forming a leakage path therein are prevented.



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Description

Title of Invention: SEMICONDUCTOR DEVICE COMPRISING A HYDROGEN DIFFUSION BARRIER AND METHOD OF FABRICATING SAME

Technical Field

[0001] The present invention relates to a semiconductor device such as a nonvolatile charge trapping memory device, and more particularly to a hydrogen diffusion barrier used for such a device. The invention also relates to a process for fabricating such a device.

Background Art

[0002] Nonvolatile flash memory devices based on the localized charges trap in silicon nitride layer have been attracted much attention for large data storage in recent years. A charge-trapping memory device typically consists of tunnel oxide, trap silicon nitride and block oxide layers stacked on silicon substrate, and a gate electrode on the block oxide layer also known as silicon-oxide-nitride-oxide-silicon (SONOS) [PTL 1]. Because of their simple cell structure, low power operation, and most importantly its compatibility with the conventional complementary metal-oxide-semiconductor (CMOS) and metal-oxide-field-effect-transistor (MOFET) technologies, they have been used widely in portable recording devices to store large amount of information. However, hydrogen diffusion is believed to play a role in degrading the devices performance and reliability.

[0003] For nonvolatile memory devices with SiO₂ thin films transistor, hydrogen-containing forming gas annealing (FGA) is a standard manufacturing process commonly used in industries to reduce the defects in SiO₂ films and interface states. These defects are associated with Si dangling bonds which are often found at the SiO₂/Si interface. Typically, FGA treatments are conducted in an H₂-N₂ gas mixture around 400 degrees [Celsius] to 450 degrees [Celsius] for 30 minutes. Atomic hydrogen is believed to passivate the Si-SiO₂ interface traps by forming Si-H bonds which terminate dangling bonds at the SiO₂/Si interface, fixing interface and reducing interface charge traps. However, the hydrogen bonds to Si can be broken when a device is exposed to ion radiation and/or subjected to external electrical fields [PTL 2]. In other words, the use of hydrogen to passivate electrically active interface traps in silicon based memory devices can set the stage for the subsequent formation of hydrogen defects or impurities during devices operation which can affect the generation of charge traps resulting in charge loss.

[0004] In addition, the CMOS/MOSFET manufacturing process often requires other fabrication steps that expose the device to hydrogen, often at elevated temperatures, such

as H-rich low pressure chemical vapor deposition (LPCVD) and/or Plasma-enhanced chemical vapor deposition (PECVD) for depositing gate electrodes and/or etching processes using hydrogen plasma. During these process steps that involve hydrogen, the hydrogen species in principal can diffuse through the gate electrode to underlying layers and/or interfaces. The diffusing H may react with SiO_2 network, leading to the formation of leakage path, which eventually result in breakdown. In addition, hydrogen species can also reach and stay in nitride and bottom nitride/oxide interface, where they will trap charges during the device operation resulting in data loss. By incorporating a hydrogen diffusion barrier film between blocking oxide and nitride layers, it is possible to suppress diffusion of the hydrogen atoms to the bottom oxide layer. The following technology is disclosed with regarding to the type of hydrogen diffusion barrier layer.

- [0005] Hydrogen degradation is also an issue in the field where complex metal oxides that are used in ferroelectric nonvolatile memory (FeRAM) and high-K materials in MOSFETs applications. Examples of complex metal oxides subject to hydrogen degradation in FeRAM include: BST, BSN, PZT and certain perovskites. These materials have a problem with desorption of oxygen atoms during heat treatments in a reducing ambient of the hydrogen annealing such as FGA. As a result, the electronic properties of capacitor are degraded thus they are not suitable for storing information [PTL 3]. In addition, it has been widely reported that hydrogen is a main source for the instabilities of MOSFETs such as negative-bias-temperature instability and hot carrier instability. These issues are related to the diffusion of hydrogen into SiO_2/Si interface and its ability to passivate and depassivate Si dangling bonds [NPL 1].
- [0006] Conventionally, TiN, AlN, Si_3N_4 and SiO_xN_y , have been used in the semiconductor device fabrication to prevent hydrogen diffusion. However, these hydrogen barriers are known to have several problems themselves. For example, the most popular method to produce a layer of silicon nitride and silicon oxynitride is by plasma enhanced chemical vapor deposition (PECVD), often employed with organometallic precursors, using a gas such as SiH_4 and NH_3 , which can leave residual hydrogen species in the film. In addition, both aluminum nitride and titanium nitride are conductive, they can generate large stress during heat treatment and they have limited uses due to their electrically conductive property. Therefore, these hydrogen barriers have not been completely effective in solving hydrogen diffusion problem, thus reducing yields and reliability [PTL 4].
- [0007] Recently, it has been reported that thermal stable silicon oxynitride ($\text{Si}_2\text{N}_2\text{O}$), which can be formed directly on top of nitride layer by N_2 thermal annealing can effectively block H species from diffusion to bottom oxide layers due to its dense matrix structure [NPL 2]. However, thermodynamic study has revealed that $\text{Si}_2\text{N}_2\text{O}$ phase can exist

only at elevated temperatures in a small window of oxygen and nitrogen partial pressure [NPL 3]. This obviously relates to experimental difficulty of fabricating SiON diffusion barrier layer.

[0008] Moreover, as the flash memory devices dimensions are getting smaller and smaller, the scaling down of devices is strongly limited by the thickness of SiO₂ blocking oxide layer. In order to reduce the gate leakage current during device operation, high dielectric constant blocking oxides have been proposed and investigated for improving device performance. Among high-k materials, Aluminum oxide (Al₂O₃) has been used in charge trapping structure in such a manner as TaN-Al₂O₃-Si₃N₄-SiO₂-Si (TANOS) [NPL 4]. Due to its high band gap and dielectric constant, memory device with Al₂O₃ acting as the blocking oxide layer has showed that this structure can eliminate back tunneling during erase operation resulting in higher erase speed and efficiency compared to device with SiO₂ as a blocking oxide layer. Therefore, there is a need for developing a new hydrogen diffusion barrier with similar properties as Si₂N₂O layer for charge traps memory devices that uses high k as a blocking oxide layer.

[0009] The present invention provides a solution to hydrogen diffusion problem and other problems, and offers further advantages over oxide-nitride-oxide flash memory device with a hydrogen diffusion barrier and methods of forming a hydrogen diffusion barrier.

Citation List

Patent Literature

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 [PTL 2] US Patent Pub. 2008/0096396
 [PTL 3] US Patent 6781184
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Summary of Invention

Technical Problem

[0012] In view of the above, the objective of the present invention is to provide a semiconductor device such as a charge trapping semiconductor memory device with a hydrogen diffusion barrier that has an excellent hydrogen barrier property that can prevent the diffusion of hydrogen to an underlying layer, e.g., bottom nitride and oxide layers.

Solution to Problem

[0013] According to one aspect of the present invention, there is provided a semiconductor device comprising a hydrogen diffusion barrier is provided, wherein the hydrogen diffusion barrier contains SiAlON.

The hydrogen diffusion barrier may be amorphous.

The semiconductor device may be a charge trapping nonvolatile memory device.

The hydrogen diffusion barrier may be formed in a shape of a layer.

A thickness of the layer of the hydrogen diffusion barrier may be 1-3 nm.

The layer of the hydrogen diffusion barrier may be sandwiched between a layer of aluminum oxide and a layer of silicon nitride.

A layer of silicon oxide may be provided on a surface of the layer of silicon nitride opposite to the layer of the hydrogen diffusion barrier.

The layer of silicon oxide may be a tunneling oxide layer and the layer of aluminum oxide may be a blocking oxide layer.

A gate electrode may be provided on a surface of the blocking oxide layer opposite to the hydrogen diffusion barrier, and a silicon substrate may be provided on a surface of the tunneling oxide layer opposite to the layer of nitride, the substrate comprising a source and a drain.

According to another aspect of the present invention, a method of fabricating any one of the semiconductor devices as shown above is provided, wherein the hydrogen diffusion barrier is fabricated by thermal annealing silicon nitride and aluminum oxide contacting each other.

The thermal annealing may be carried out in an atmosphere of a mixture of hydrogen and nitrogen or nitrogen.

The thermal annealing may be carried out at a temperature of 600-900 degrees [Celsius].

According to still another aspect of the present invention, a method of fabricating any one of the semiconductor devices as shown above is provided, wherein the hydrogen diffusion barrier is fabricated by physical deposition.

The physical deposition may be pulsed laser deposition or sputtering.

Advantageous Effects of Invention

[0014] With the present invention, a novel hydrogen diffusion barrier of a high performance and easier to fabricate is provided.

Brief Description of Drawings

[0015] [fig.1]Fig. 1 is a block diagram showing a cross-sectional side view of the MONOS structure of the prior art that has aluminum oxide as a blocking oxide structure without a hydrogen diffusion barrier.

[fig.2]Fig. 2 is a block diagram showing a cross section side view of a MONOS structure that have aluminum oxide as a blocking oxide structure and a hydrogen diffusion barrier according to the present invention.

[fig.3]Fig. 3(a) is a cross section TEM image of the MONOS structure without SiAlON hydrogen diffusion barrier, and Fig. 3(b) is a cross section TEM image of the MONOS structure with SiAlON hydrogen diffusion barrier.

[fig.4]Fig. 4 is a graph showing a relationship between hydrogen content and depth of the ONOS structures in the semiconductor memory devices with and without hydrogen diffusion barrier according the present invention.

[fig.5]Fig. 5 is a graph showing a relationship between hydrogen content and depth of the ONOS structure with a thicker SiAlON hydrogen diffusion barrier, which was fabricated by PLD instead of thermally annealing.

[fig.6]Fig. 6(a) is a graph showing TDS of H₂O and H₂ species of ONOS structure with hydrogen diffusion barrier, and Fig. 6(b) is a graph showing TDS of H₂O and H₂ species of ONOS structure without hydrogen diffusion barrier

[fig.7]Fig. 7(a) is a graph showing an improvement in electrical characteristics for MONOS memory device with hydrogen diffusion barrier according to the present invention as compared to memory device, and Fig. 7(b) is a graph showing an improvement in electrical characteristics for MONOS memory device without hydrogen diffusion barrier according to the present invention as compared to memory device.

Description of Embodiments

[0016] The present invention is directed hydrogen diffusion barrier and the methods for fabricating the barrier layer that have an excellent hydrogen barrier property in particularly useful for memory device, such as SONOS, MONOS and other semi-

conductor devices that require hydrogen diffusion barrier to prevent hydrogen from penetrating down to bottom layers.

[0017] In accordance with the present invention, the hydrogen diffusion barrier comprises silicon oxide, aluminum oxide, and silicon nitride (SiAlON).

[0018] It is noticed by present inventor that the structure of SiAlON is similar to that of SiON which shows to have very good hydrogen barrier property. In SiAlON, there is a substitution of Si atoms of Si_3N_4 by Al atoms with accompanied by atomic replacement of N atoms of Si_3N_4 by O atoms, to satisfy valency requirements. The chemical replacement changes some of Si-N bonds to Al-O bonds. Comparing these two bonds, the bond lengths are about the same, while the Al-O bond strength is much higher than that of Si-N. The presence of Al-O bonds of higher strength provides higher activation energy needed for the diffusion of interstitial species. The invention also provides a hydrogen diffusion barrier layer that is amorphous. When subjected to high temperature manufacturing processes, this hydrogen barrier layer does not crystallize. In addition, amorphous SiAlON hydrogen diffusion barrier can be easily formed by thermal annealing and/or by pulsed laser deposition.

[0019] For assuring the advantages of the present invention, memory device samples with hydrogen diffusion barrier were prepared as a MIS (metal-insulator-semiconductor) capacitor structure based on Metal-Oxide-Nitride-Oxide-Silicon (MONOS).

[0020] The MONOS structure includes a lower thin oxide layer or tunneling oxide layer, a silicon nitride layer, a thin hydrogen diffusion layer and a blocking oxide layer. The method of preparing this structure begins with forming a thin tunneling oxide layer (SiO_2) on the surface of silicon substrate by thermal growth. Next, the silicon nitride (SiN) layer is formed on the surface of tunneling oxide layer by pulsed laser deposition (PLD). Then, the blocking oxide layer (Al_2O_3) layer is deposited on top of silicon nitride to form oxide-nitride-oxide-silicon (ONOS) under the same oxygen partial pressure and substrate temperature as that of depositing silicon nitride layer. Finally, ONOS structure is then annealed in $\text{H}_2\text{-N}_2$ gas mixture for 60 minutes at 600 degrees [Celsius] to form SiAlON hydrogen diffusion barrier between blocking oxide layer and silicon nitride layer.

[0021] For electrical characterizations, aluminum gate electrodes with diameter of 300 nm may be deposited on the oxide-nitride-oxide-silicon structure using ion beam sputtering system with shadow mask. The FGA process is conducted thereafter at 400 degrees [Celsius] for 30 minutes in 5% H_2 -95% N_2 gas mixture.

Experiments

[0022] A MONOS structure and processes for making same according to the present invention will be now described in details based on experiments, with reference to Fig. 2 through Fig. 7.

- [0023] Fig. 2 shows schematic of a cross section side view of a memory capacitor including a hydrogen diffusion barrier according to the present invention. Referring to Fig. 2, MONOS structure includes a lower thin oxide layer or tunneling oxide layer, a silicon nitride layer, a thin hydrogen diffusion barrier layer, a blocking oxide layer and metal contact. Generally, the substrate may be any known silicon-based semiconductor and/or silicon layer formed on non-silicon based semiconductor. Preferably, the substrate is a doped silicon or undoped silicon substrate.
- [0024] The method begins with forming 4 nm to 5 nm of tunneling oxide layer (SiO_2) on the surface of silicon substrate. The tunneling oxide can be formed by thermal grown or by chemical vapor deposition (CVD). In the present experiment, the tunneling layer was formed by thermal growth at 800 degrees [Celsius] in dry O_2 ambient with O_2 flow rate of 0.4 L/min for 5 minutes and oxidation for 5 minutes at 800 degrees [Celsius]. Next, 10 nm of silicon nitride layer was formed on the surface of tunneling oxide layer. Then, 12 nm of blocking oxide layer (Al_2O_3) layer was deposited on top of silicon nitride to form oxide-nitride-oxide-silicon (ONOS) structure under the same oxygen partial pressure and substrate temperature without breaking vacuum on the deposition chamber. Generally, the nitride and blocking oxide can be formed or deposited by any suitable means including but not limited to CVD, sputtering, PLD, and atomic layer deposition (ALD). In the present experiment, the silicon nitride and blocking oxide layers were deposited by PLD. Following are the PLD conditions used for fabricating the nitride and blocking oxide layers:
- [0025] 1) Laser: KrF excimer laser with energy of 150 mJ/m²
 2) Laser Frequency: 5 Hz
 3) $\text{P}(\text{O}_2)$ partial pressure: 1×10^{-5} torr
 4) Substrate temperature: 300 degrees [Celsius]
 5) Distance between target and substrate: 50 mm
 6) Apparatus: pulsed laser deposition system [purchased from Pascal Technologies]
 7) Targets: Si_3N_4 and Al_2O_3 with diameter of 20 mm and purity of at least 99.9% manufactured by Kojundo Chemical Lab. Co., Ltd.
- [0026] SiAlON hydrogen diffusion barrier in the present experiments was formed between blocking oxide layer and silicon nitride layer by annealing ONOS structure in 95% H_2 - 5% N_2 gas mixture for 60 minutes at 600 degrees [Celsius] to about 900 degrees [Celsius] for 5 seconds, preferably at least 600 degrees [Celsius] in 95% H_2 -5% N_2 gas mixture or 100% N_2 gas.
- [0027] Figs. 3(a) and 3(b) show cross-sectional TEM images ONOS structure with and without hydrogen diffusion barrier respectively for comparison purposes. The TEM image of as-deposited sample (Fig. 3(a)) confirms the amorphous nature of aluminum oxide layer and reveal there is no presence of intermixing layer between silicon nitride

layer and blocking oxide layer. In contrast, Fig. 3(b) shows a relatively uniform and thicker interfacial layer near aluminum oxide and silicon nitride in interface after annealing with a thickness of around 1 nm. It has been reported that formation of interfacial layer during aluminum oxide formation and/or subsequent post-annealing seems to be unavoidable [NPL 5]. Possible reason for the formation of interfacial layer is due to the lack of oxygen near the aluminum oxide and silicon nitride interface and a difference of solubility between Al and Si atoms. The lack of oxygen in aluminum oxide films near the interface causes chemical incompatibility which leads to the formation of intermixed layer. In addition, because the solubility of Si in Al is larger than that of Al in Si, it will be possible for Si in silicon nitride near the interface to diffuse into aluminum oxide layer upon annealing to form an amorphous interfacial layer of SiAlON. The angle-resolved x-ray photoemission (XPS) results (not shown) further indicate that Al2p and Si2p photoelectrons emitted at the aluminum oxide and silicon nitride interface exhibit an additional peak to that of Al₂O₃ and Si₃N₄ at around 1 eV lower binding energy. This demonstrates that by annealing ONOS structure at 600 degrees [Celsius] in 5%H₂-95%N₂ gas mixture for 60 minutes, a thin SiAlON layer can be formed on top of silicon nitride film.

[0028] Fig. 4 illustrates a relationship between hydrogen content and depth of the ONOS structures with and without hydrogen diffusion barrier measured by Nuclear reaction analysis (NRA) in a vacuum chamber with based pressure of 10⁻⁶ torr, which connected to an ion beam line of the MicroAnalysis Laboratory (MALT) tandem accelerator at the University of Tokyo. Typical ¹⁵N²⁺ ions at the resonance energy of ~6.4 eV and beam currents of 100-200 nA is used to incident on the sample surface at angle of 45 degrees to the surface normal to visualizing the changes of the hydrogen concentration distribution at the surface and near aluminum oxide/silicon nitride interface of ONOS structures with and without SiAlON layer. It can be seen from Fig. 4, the spectra exhibit two peaked signals. The peak centers at ion energy of 6.385 eV for both structures correspond to the H at the aluminum oxide surfaces which may consist of any H-containing compounds such as atomic H, H₂, H₂O, OH and hydrocarbon groups. It can be seen that H are presented more near the surface of ONOS structure with SiAlON layer compared to ONOS structure without hydrogen diffusion barrier. The smaller peak at high ion beam energy (~6.43 eV) and depth of ~12 nm is attributed to Hydrogen species that present at the aluminum oxide surface, but relocate to near aluminum oxide and silicon nitride interface due to high kinetic energy of NRA's ions. The results indicate that ONOS structure with SiAlON layer can store much more H concentrations near aluminum oxide and silicon nitride interface than ONOS structure without SiAlON layer.

[0029] Fig. 5 illustrates a relationship between hydrogen content and depth profile of the

ONOS with a SiAlON hydrogen diffusion barrier fabricated by PLD. The process for forming ONOS structure with SiAlON fabricated by PLD began with forming a 4 nm tunneling oxide layer (SiO_2) on the surface of silicon substrate by thermal growth. Next, the 10 nm silicon nitride (SiN) layer was formed on the surface of tunneling oxide layer by pulsed laser deposition (PLD). Then, 3 nm of SiAlON was formed on top of silicon nitride layer by PLD using $\text{Al}_2\text{O}_3\text{:Si}_3\text{N}_4$ (1:1 mole ratio) target. Finally, 9 nm of blocking oxide (Al_2O_3) was deposited using the same PLD conditions that were mentioned above. The ONOS structure was then annealed in FGA for 1 hour at 600 degrees [Celsius]. It can be seen from Fig. 5, SiAlON grown by PLD can also store hydrogen. This result shows that the SiAlON layer that is formed by either thermal annealing or grown by PLD has an effective hydrogen barrier property. However, because of the lack of chemical identification in NRA, the stable and unstable hydrogen cannot be easy to be distinguished. Therefore, the thermal behavior of hydrogen in the ONOS structure with and without hydrogen diffusion barrier is examined by thermal desorption spectroscopy (TDS).

[0030] Figs. 6(a) and 6(b) show TDS of H_2O and H_2 species of ONOS structure with and without SiAlON layer. The TDS data reveal that H dominantly desorbs below 600 degrees [Celsius] for both structures. The H_2O and H peaks at 130 degrees [Celsius] to 150 degrees [Celsius] (alpha peak) attribute to hydrogen desorption from surface of aluminum oxide. The H_2O and H peaks at around 500 degrees [Celsius] (beta peak) attribute to hydrogen desorption from silanol (SiO-H_2). It can be seen that the ONOS structure with SiAlON layer shows less hydrogen desorption behavior at around 500 degrees [Celsius]. This can explain that during formation of SiAlON layer which requires the ONOS structure to be annealed at 600 degrees [Celsius], majority of Si-H bonds from the dangling bonds existing at the SiO_2/Si interface are desorbed to the vacuum. Interestingly, Fig. 6(b) shows an additional gamma peak appears at 900 degrees [Celsius] for ONOS with SiAlON layer, but not on ONOS structure without SiAlON layer. This indicates the ability of SiAlON to capture thermally stable H species. It is known that H bonds in conventional Si-H, N-H, Al-H and O-H units cannot stand in such high temperature. These results suggest that the stability of these H species is attributed to the high thermal stability of SiAlON network, rather than to the bonding strength of hydrogen.

[0031] Figs. 7(a) and 7(b) illustrate graphs showing an improvement in electrical characteristics for the MONOS memory device with SiAlON hydrogen diffusion barrier according to the present invention as compared to the memory device without SiAlON hydrogen diffusion barrier. Fig. 7a shows a relationship between capacitance and applied voltage (C-V). In this measurement, the C-V window indicates how well the structure store charge. It can be seen from Fig. 7(a), the C-V window for ONOS

structure without the hydrogen diffusion barrier is smaller than that for ONOS structure with the hydrogen diffusion barrier. This indicates that the memory device with the hydrogen diffusion barrier offers comparable or better charge trapping ability compared to the conventional memory devices that do not have the hydrogen diffusion barrier. Fig. 7(b) shows a relationship between leakage current and applied voltage (I-V). From this figure, it can be seen that ONOS structure with the SiAlON hydrogen diffusion barrier is lower in leakage current than that of ONOS structure without the SiAlON hydrogen diffusion barrier. This fact confirms that by incorporating SiAlON hydrogen diffusion barrier in ONOS structure, not only it can effectively store hydrogen but also improve the electrical characteristics of charge-trapping memory devices.

[0032] The SiAlON hydrogen barrier that is formed by thermal annealing or by PLD of the present invention shows very good barrier property for SONOS or MONOS non-volatile charge trapping memory devices. The present invention is not limited to charge trapping nonvolatile memory devices and FeRAM memory devices. Therefore, various modifications of the methods can be made by those skilled in the art without departing from the present invention as defined by the claims.

[0033] Though the present invention was explained in detail by reference to a specific device structure, i.e., a nonvolatile charge trapping memory device, it should be noted that the invention is not limited to such a particular type of a semiconductor devices but can be applied to any semiconductor devices in which the hydrogen diffusion barrier is beneficial to be incorporated.

Claims

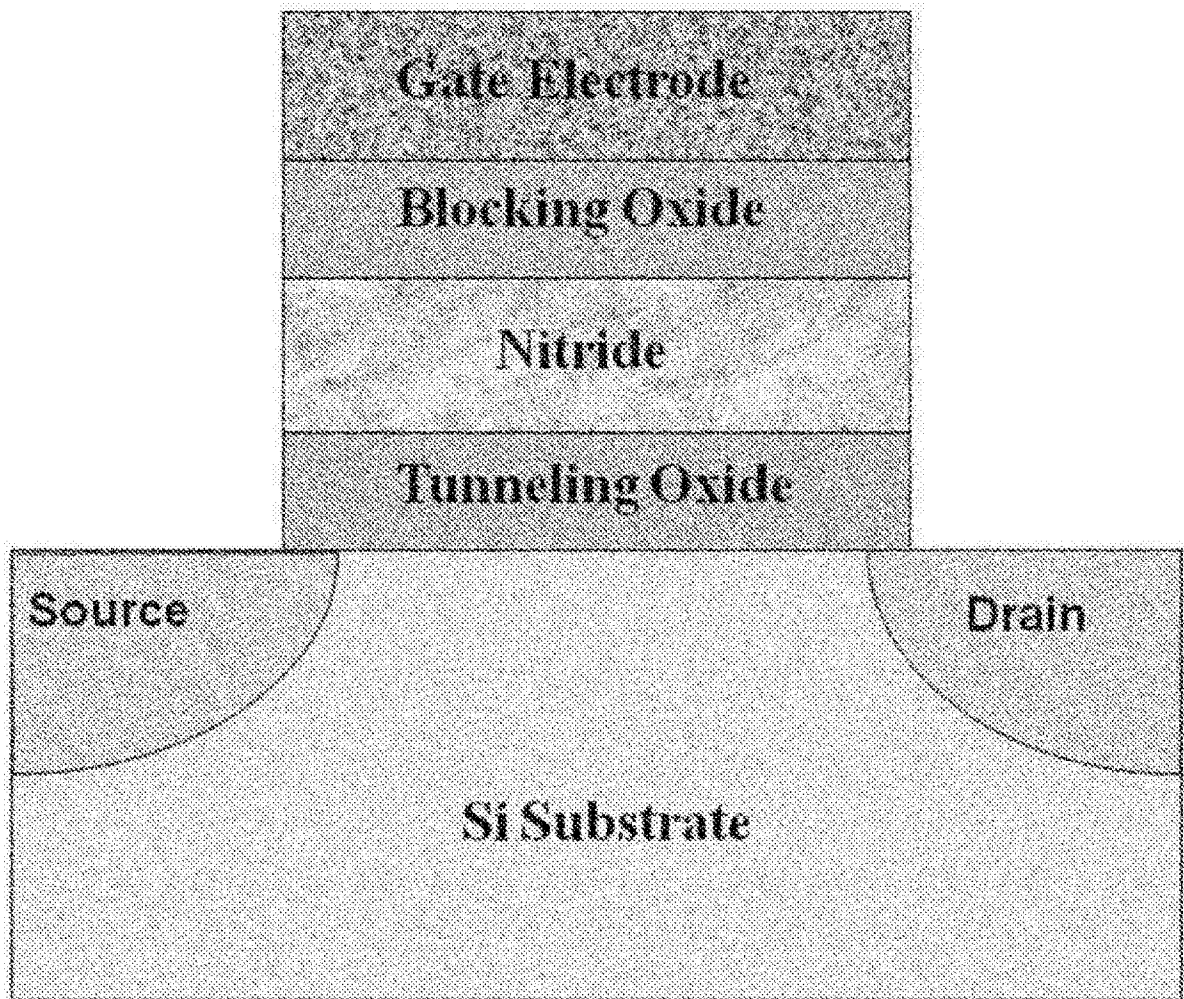
- [Claim 1] A semiconductor device comprising a hydrogen diffusion barrier, wherein the hydrogen diffusion barrier contains SiAlON.
- [Claim 2] The semiconductor device as set forth in claim 1, wherein the hydrogen diffusion barrier is amorphous.
- [Claim 3] The semiconductor device as set forth in claim 1 or 2, wherein the semiconductor device is a charge trapping nonvolatile memory device.
- [Claim 4] The semiconductor device as set forth in any one of claims 1-3, wherein the hydrogen diffusion barrier is formed in a shape of a layer.
- [Claim 5] The semiconductor device as set forth in claim 4, wherein a thickness of the layer of the hydrogen diffusion barrier is 1-3 nm.
- [Claim 6] The semiconductor device as set forth in claim 4 or 5, wherein the layer of the hydrogen diffusion barrier is sandwiched between a layer of aluminum oxide and a layer of silicon nitride.
- [Claim 7] The semiconductor device as set forth in claim 6, wherein a layer of silicon oxide is provided on a surface of the layer of silicon nitride opposite to layer of the hydrogen diffusion barrier.
- [Claim 8] The semiconductor device as set forth in claim 7, wherein the layer of silicon oxide is a tunneling oxide layer and the layer of aluminum oxide is a blocking oxide layer.
- [Claim 9] The semiconductor device as set forth in claim 8, wherein a gate electrode is provided on a surface of the blocking oxide layer opposite to the hydrogen diffusion barrier, and wherein a silicon substrate is provided on a surface of the tunneling oxide layer opposite to the layer of nitride, the substrate comprising a source and a drain.
- [Claim 10] A method of fabricating the semiconductor device as set forth in any one of claims 1-9, wherein the hydrogen diffusion barrier is fabricated by thermal annealing silicon nitride and aluminum oxide contacting each other.
- [Claim 11] The method of fabricating the semiconductor device as set forth in claim 10, wherein the thermal annealing is carried out in an atmosphere of a mixture of hydrogen and nitrogen or nitrogen.
- [Claim 12] The method of fabricating the semiconductor device as set forth in claim 10 or 11, wherein the thermal annealing is carried out at a temperature of 600-900 degrees [Celsius].
- [Claim 13] A method of fabricating the semiconductor device as set forth in any one of claims 1-9, wherein the hydrogen diffusion barrier is fabricated

by physical deposition.

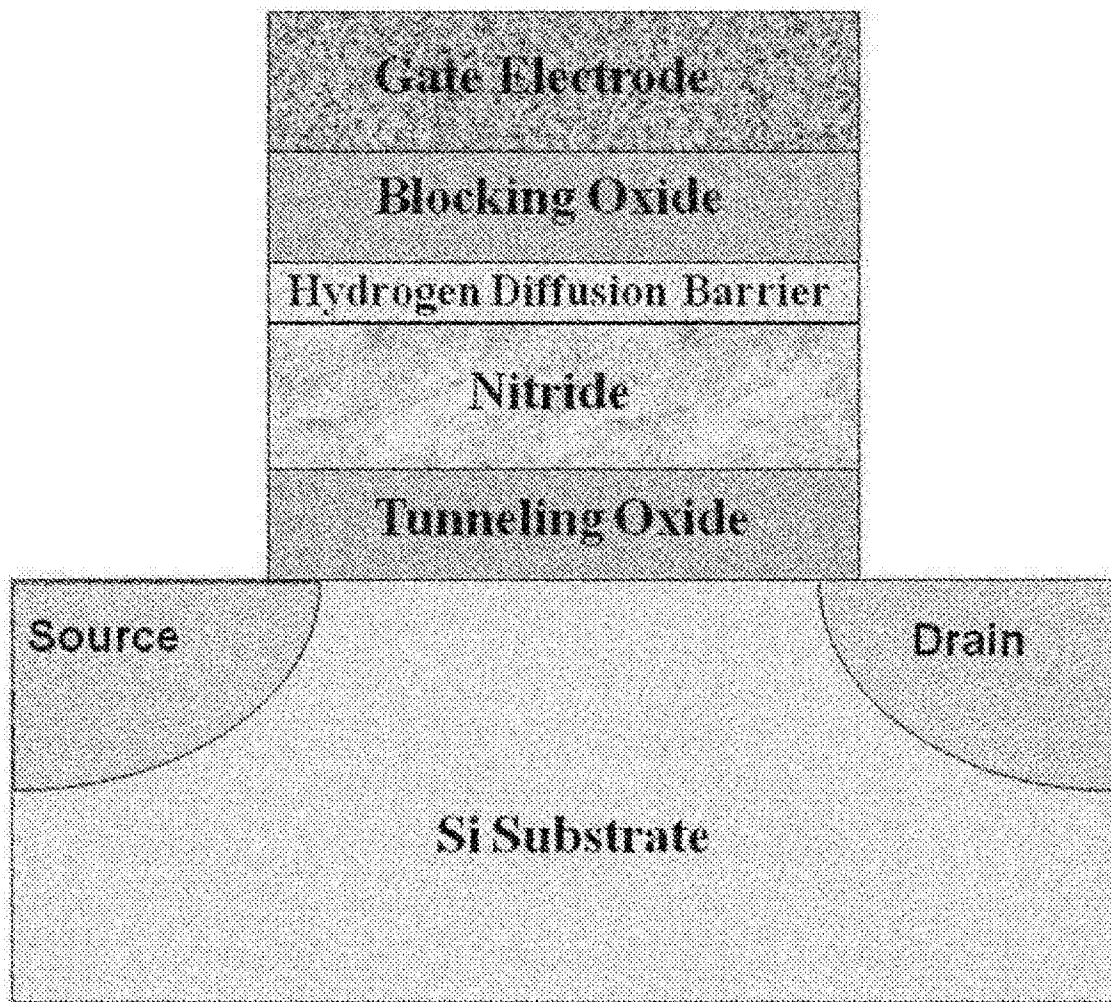
[Claim 14]

The method of fabricating the semiconductor device as set forth in claim 13, wherein the physical deposition is pulsed laser deposition or sputtering.

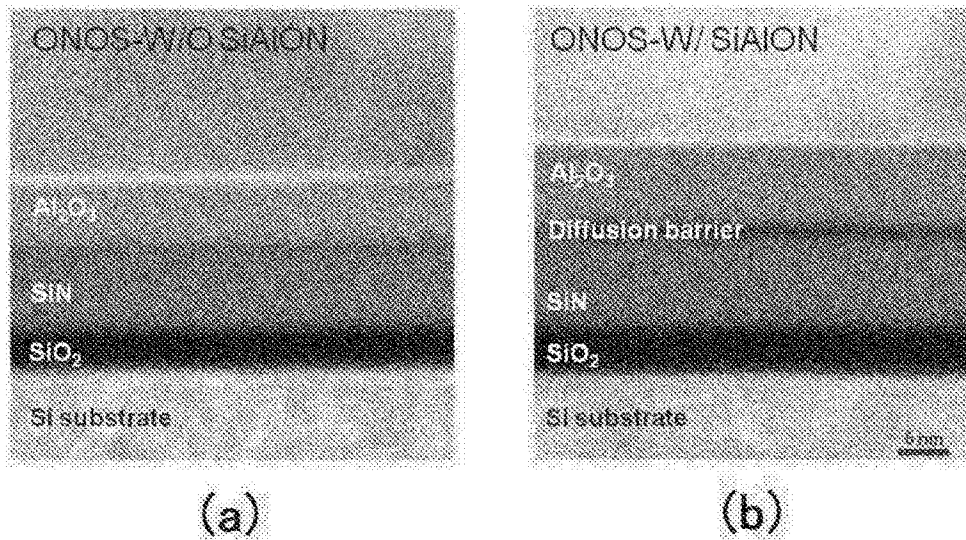
[Fig. 1]



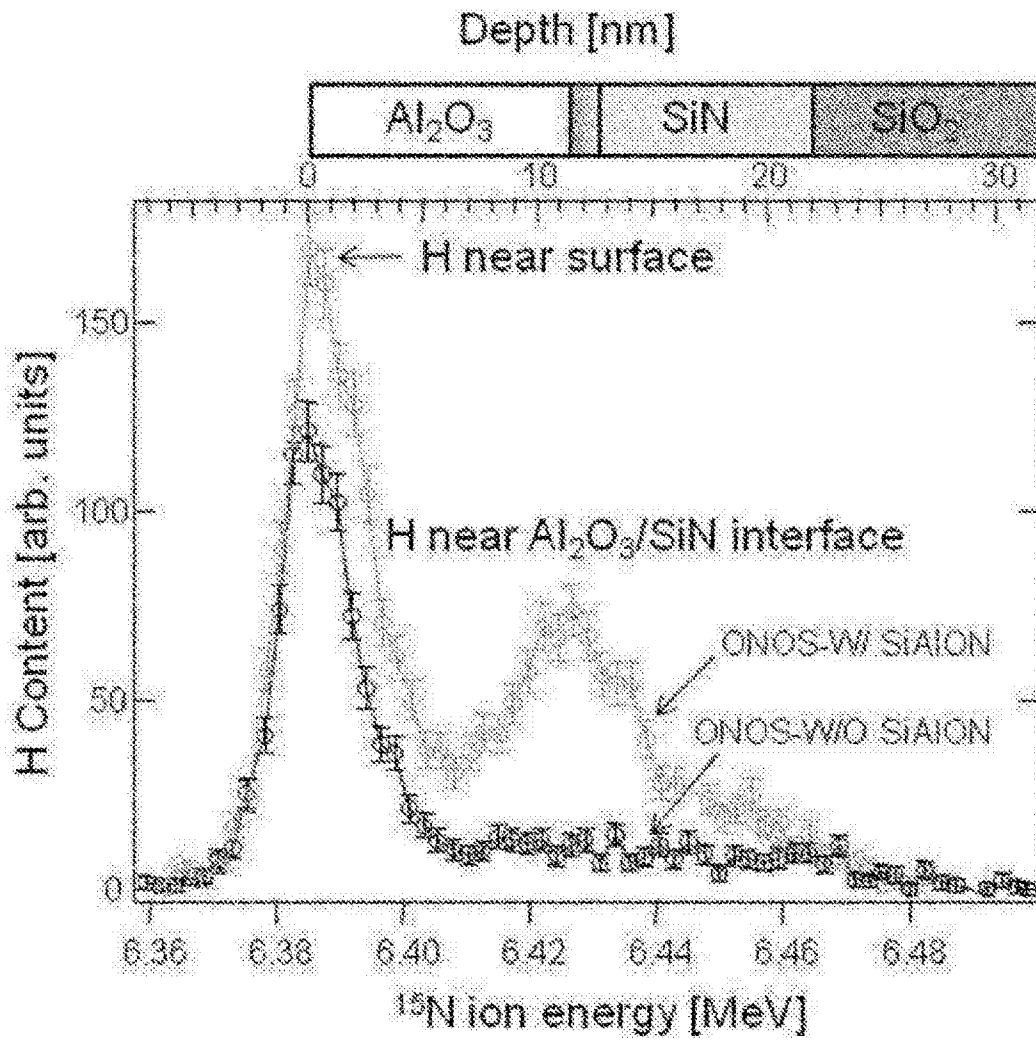
[Fig. 2]



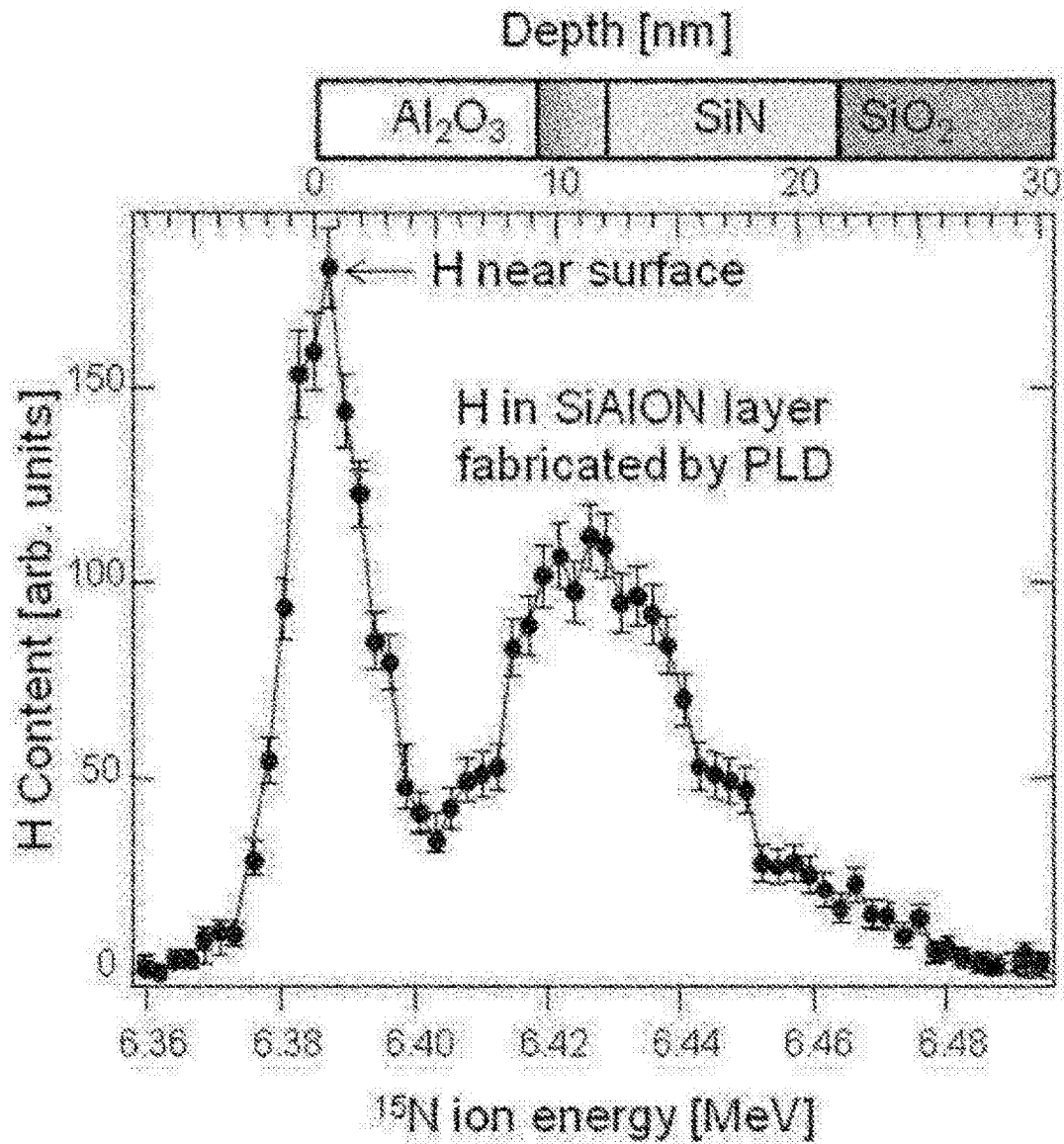
[Fig. 3]



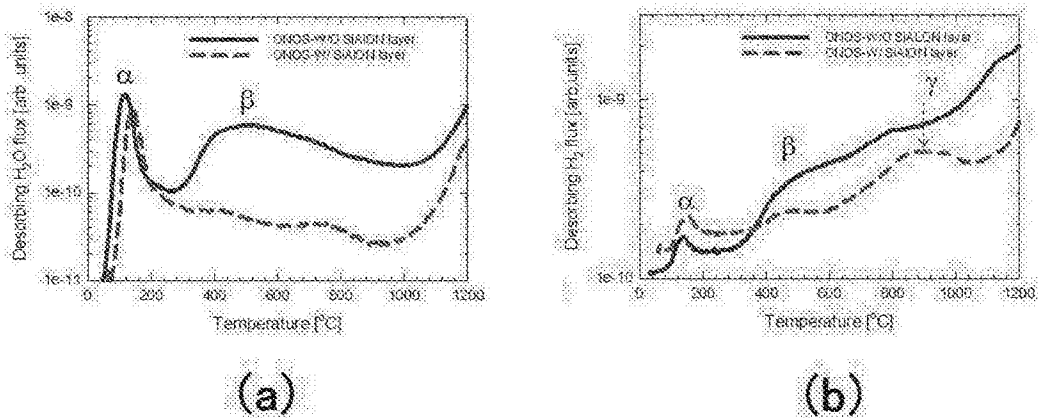
[Fig. 4]



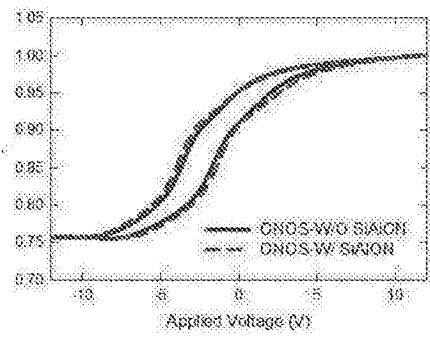
[Fig. 5]



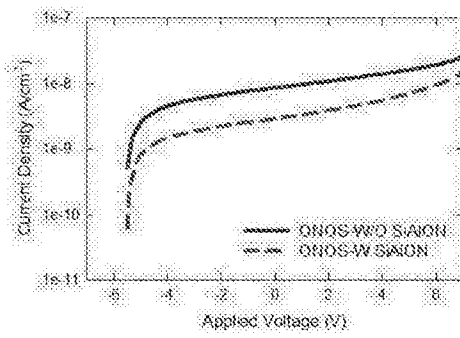
[Fig. 6]



[Fig. 7]



(a)



(b)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2015/001013

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. H01L21/336(2006.01)i, H01L27/105(2006.01)i, H01L29/78(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L21/336, H01L27/105, H01L29/78

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
 Published unexamined utility model applications of Japan 1971-2015
 Registered utility model specifications of Japan 1996-2015
 Published registered utility model applications of Japan 1994-2015

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2008-130743 A (KABUSHIKI KAISHA TOSHIBA) 2008.06.05, [0021], [0028], [0029] & US 2008/0116507 A1 & KR 10-2008-0045646 A	1-14
X A	JP 2010-541296 A (MICRON TECHNOLOGY, INC) 2010.12.24, [0068] & US 2009/0097320 A1 & WO 2009/051944 A2 & EP 2198457 A2 & KR 10-2010-0071101 A & CN 101821849 A & TW 200935606 A	1-5, 13, 14 6-12
Y A	JP 2014-502783 A (TEXAS INSTRUMENTS INCORPORATED) 2014.02.03, claim12 & WO 2012/078162 A1 & CN 103250251 A	1-5, 13, 14 6-12



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

28.04.2015

Date of mailing of the international search report

19.05.2015

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2015/001013

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2013-43963 A (KONICA MINOLTA ADVANCED LAYERS, INC.) 2013.03.04, [0161]-[0163] (No Family)	1-5, 13, 14
Y	JP 2009-267366 A (NEC ELECTRONICS CORPORATION) 2009.11.12, [0023] & US 2009/0194809 A1	3-5