ORIGINAL

SYSTEM-IN PACKAGES

ABSTRACT

System-in packages, or multichip modules, are described which can include multi-layer chips and multi-layer dummy substrates over a carrier, multiple through vias blindly or completely through the multi-layer chips and completely through the multi-layer dummy substrates, multiple metal plugs in the through vias, and multiple metal interconnects, connected to the metal plugs, between the multi-layer chips. The multi-layer chips can be connected to each other or to an external circuit or structure, such as mother board, ball grid array (BGA) substrate, printed circuit board, metal substrate, glass substrate, or ceramic substrate, through the metal plugs and the metal interconnects.

We Claim :-

1. A system-in package comprising:

a carrier (11);

a first chip (68) over said carrier (11), wherein said first chip (68) comprises a first semiconductor substrate (58), a first metal layer (34 or 26) under a bottom surface of said first semiconductor substrate (58), and a first dielectric layer (48) under said bottom surface of said first semiconductor substrate (58) and over said first metal layer (34 or 26);

a second chip (68) over said carrier (11), wherein said second chip (68) comprises a second semiconductor substrate (58) having a top surface (58s) substantially coplanar with a top surface (58s) of said first semiconductor substrate (58), wherein said second chip (68) is separated from said first chip (68);

a gap filling material (64) in a gap between said first chip (68) and said second chip (68);

a first metal plug (5p) in said first chip (68), wherein said first metal plug (5p) passes vertically through said first semiconductor substrate (58) and said first dielectric layer (48) and contacts said first metal layer (34 or 26);

a first insulating material (50 or 500a) enclosing said first metal plug (5p), wherein said first insulating material (50 or 500a) is enclosed by said first semiconductor substrate (58);

a first dielectric structure (60 or 66) over said top surface (58s) of said first semiconductor substrate (58), over said top surface (58s) of said second semiconductor substrate (58), and over said gap filling material (64);

a first metal interconnect (1) in said first dielectric structure (60 or 66) and over said first chip (68), wherein said first metal interconnect (1) is connected to said first metal plug (5p);

a third chip (72) over said first dielectric structure (60 or 66) and over said first metal interconnect (1);

a second metal plug (6p) in said third chip (72), wherein said second metal plug (6p) passes vertically through a third semiconductor substrate (96) of said third chip (72) and contacts said first metal interconnect (1);

a second insulating material (90 or 500a) enclosing said second metal plug (6p), wherein said second insulating material (90 or 500a) is enclosed by said third semiconductor substrate (96);

a second dielectric structure (88 or 120) over a top surface (96s) of said third semiconductor substrate (96); and

a second metal interconnect (2) in said second dielectric structure (88 or 120) and over said third chip (72), wherein said second metal interconnect (2) is connected to said second metal plug (6p).

2. The system-in package of claim 1, wherein said carrier (11) comprises a silicon substrate, a glass substrate, a ceramic substrate, a metal substrate or an organic polymer substrate.

3. The system-in package of claim 1, wherein said first chip (68) comprises a central-processing-unit (CPU) chip, a graphics-processing-unit (GPU) chip, a digital-signal-processing (DSP) chip, a flash memory chip, a dynamic-random-access-memory (DRAM) chip, a static-random-access-memory (SRAM) chip, a wireless local area network (WLAN) chip, a baseband chip, a logic chip, an analog chip, a power device, a regulator, a power management device, a global-positioning-system (GPS) chip, a Bluetooth chip, or a system-on chip (SOC) comprising one or more of a central-processing-unit (CPU) circuit block, a graphics-processing-unit (GPU) circuit block, a digital-signal-processing (DSP) circuit block, a memory circuit block, a baseband circuit block, a Bluetooth circuit block, a global-positioning-system (GPS) circuit block, a wireless local area network (WLAN) circuit block and a modem circuit block.

4. The system-in package of claim 1, wherein said first semiconductor substrate (58) has a thickness between 2 and 20 micrometers.

5. The system-in package of claim 1, wherein said second metal plug (6p) further contacts a second metal layer (106 or 114) of said third chip (72), wherein said second metal layer (106 or 114) is under said third semiconductor substrate (96).

6. The system-in package of claim 1 further comprising a third metal plug (5p) in said second chip (68), wherein said third metal plug (5p) passes vertically through said second semiconductor substrate (58) and contacts a second metal layer (34 or 26) of said second chip (68), wherein said second metal layer (34 or 26) is under a bottom surface of said second semiconductor substrate (58), wherein said first metal interconnect (1) is further over said second chip (68) and connected to said third metal plug (5p).

7. The system-in package of claim 1, wherein said first metal plug (5p) contacts a contact point (18) of said carrier (11).

8. The system-in package of claim 1 further comprising a third metal plug (5p) in said first chip (68), a fourth metal plug (5p) in said second chip (68), and a third metal interconnect (1) in said first dielectric structure (60 or 66) and over said first and second chips (68), wherein said third metal plug (5p) passes vertically through said first semiconductor substrate (58) and contacts a second metal layer (34 or 26) of said first chip (68), wherein said second metal layer (34 or 26) is under said bottom surface of said first semiconductor substrate (58), wherein said fourth metal plug (5p) passes vertically through said second semiconductor substrate (58) and contacts a third metal layer (34 or 26) of said second chip (68), wherein said third metal layer (34 or 26) is under a bottom surface of said second semiconductor substrate (58), wherein said third metal interconnect (1) connects said third metal plug (5p) and said fourth metal plug (5p).

9. The system-in package of claim 1, wherein said first chip (68) has a different circuit design from a circuit design of said second chip (68).

10. The system-in package of claim 1 further comprising a dummy substrate (62) over said carrier (11) and in said gap, wherein said dummy substrate (62) has a top surface (62s) substantially coplanar with said top surface (58s) of said first semiconductor substrate (58), wherein said first dielectric structure (60 or 66) is further over said top surface (62s) of said dummy substrate (62).

11. The system-in package of claim 1 further comprising a metal bump (126 or 666) connected to said second metal interconnect, wherein said metal bump comprises tin, copper, nickel or gold.

12. The system-in package of claim 1, wherein said first metal interconnect (1) comprises a signal trace, a power trace or a ground trace.

13. The system-in package of claim 1, wherein said first insulating material (50 or 500a) comprises a second dielectric layer (50) on a sidewall of said first metal plug (5p) and in contact with a top surface of said first metal layer (34 or 26), wherein said first metal plug (5p) is enclosed by said second dielectric layer (50).

14. The system-in package of claim 1, wherein said second insulating material (90 or 500a) comprises an insulating ring (500a) in said third semiconductor substrate, wherein said second metal plug (6p) passes vertically through and is enclosed by said insulating ring (500a).

15. The system-in package of claim 1, wherein said second metal plug (6p) comprises electroplated copper (86) in said second insulating material (90 or 500a) and a titanium-containing or tantalum-containing layer (92) at a border of said second metal plug (6p).

16. The system-in package of claim 1, wherein said first metal interconnect (1) comprises an electroplated copper layer (56) and a titanium-containing or tantalum-containing layer (52) at a sidewall and bottom of said electroplated copper layer (56).

17. The system-in package of claim 1, wherein said first metal interconnect (1) comprises a titanium-containing or tantalum-containing layer (52) and an electroplated copper layer (56) over said titanium-containing or tantalum-containing layer (52), wherein said electroplated copper layer (56) has a sidewall not covered by said titanium-containing or tantalum-containing layer (52).

18. The system-in package of claim 1 further comprising a third metal plug (6p) in said third chip (72), wherein said third metal plug (6p) passes vertically through said third semiconductor substrate (96) and contacts a second metal layer (106 or 114) of said third chip (6p), wherein said second metal layer (106 or 114) is under a bottom surface of said third semiconductor substrate (96), wherein said second metal interconnect (2) is further connected to said third metal plug (6p).

19. The system-in package of claim 18, wherein a total number of bit lines in parallel data communication between said first and third chips (68 and 72) is more than 128, and one of said bit lines is provided by said first, second and third metal plugs (5p and 6p) and said first and second metal interconnects (1 and 2).

20. The system-in package of claim 1, wherein said first metal interconnect (1) has a top surface substantially coplanar with a top surface of said first dielectric structure (60).

21. The system-in package of claim 1, wherein said first semiconductor substrate (58) has a thickness between 1 and 50 micrometers.

22. The system-in package of claim 1, wherein said third semiconductor substrate (96) has a thickness between 1 and 50 micrometers.

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